HARMONIC-FREE UTILITY/DC POWER CONDITIONING INTERFACES

by

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(EE 1977, ME 1977)

S.M., Massachusetts Institute of Technology
(1980)

E.E., Massachusetts Institute of Technology
(1980)

SUBMITTED TO THE DEPARTMENT OF
ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

SEPTEMBER, 1982

Signature of Author Signature redacted
EECS Department, 7 September, 1982

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Submitted to the Department of Electrical Engineering and Computer Science on 7 September, 1982 in partial fulfillment of the requirements for the degree of Doctor of Science.

ABSTRACT

The typical design of a power circuit now used to interface a dc system to the electric utility is such that a heavily distorted current is drawn from the utility. The harmonic currents generated in this manner create harmonic voltages as they flow through the impedances of the utility's network. If the distortion of the utility's waveforms becomes great enough, it is possible that components of both the utility and the load will be adversely affected. Although such detrimental effects are not yet prevalent, there is concern that the rapidly growing number of power circuits connected to the utility will eventually cause intolerable levels of distortion to be reached. At some point, corrective measures will be needed.

This thesis proposes and develops one possible corrective measure: a utility/dc power conditioning interface that draws very little harmonic current from the utility system. Active waveshaping techniques are used to achieve this effect. The appropriateness and the applicability of this approach to the harmonic distortion problem of the future are first argued. The design and control of such an interface is then discussed. Finally, the power circuit's feasibility in the medium-power range is demonstrated with a 6 kW, harmonic-free rectifier.

Compared to the interfaces it is intended to replace, the harmonic-free utility/dc power conditioning interface presented in this work has a more complicated power circuit and control system. The added cost of this complexity is offset by several additional advantages that the harmonic-free interface offers, however. These advantages include 1)unity power factor operation at all power levels without compensating capacitors; 2)the reduction, by a factor of ten or more in some cases, of the peak energy storage required in the power circuit; and 3)a corresponding increase in the rate at which the power level can be changed.

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I believe in the mentor/protégé relationship. Knowledge is an essential part of a person's being, and its transfer is therefore a very personal experience. True teachers exist to give a part of themselves to their pupils, and true pupils, in the search for growth, open themselves to their teachers. Both need the attention of the other; both profit from the exchange that takes place. It is, however, only through a close and lasting interaction between a teacher and a pupil that the two can fully realize the product of their efforts. Those fortunate enough to take part in such an interaction provide, to each other, a continual reminder of where they started, how they got where they are, and why it was important to do so. Of all that is to be taught and learned, none is as valuable as the perspective this reminder offers.

I have two mentors. One, my father, has taught me to aspire, to be productive, and to be discerning in my life. The other, Professor John Kassakian, has done the same for my view of my professional career. To both I owe a gratitude that can not be measured.

A true pupil, in turn, becomes a true teacher. I look forward to this role, and I hope that, as a mentor, I might begin to repay, in a somewhat indirect but very appropriate way, the debt I owe to those who have given me so much.

ACKNOWLEDGEMENTS

The members of my committee, Prof R.D. Thornton, Dr. A. Kusko, and Prof. G. Verghese, have provided knowledge, experience, support, and guidance throughout my years as a doctoral student. To them I owe a special appreciation for the contributions they have made. Prof. Verghese, in particular, has, due to his availability and his skill in fields for which I am only moderately trained, played an important role in the development and presentation of this work.

This research effort was sponsored, in part, by the Electric Energy Systems Division of the Department of Energy under the supervision of Mr. D.J. Roesler, Program Manager (Contract No. EX-76-A-01-2295 T.O. 47H).

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CHAPTER I

INTRODUCTION

The electric utility system is designed to provide a fundamental sinusoidal voltage waveform to linear loads that will, when so driven, draw fundamental sinusoidal currents. Under these conditions, the quality of the system's service can be controlled quite well. Not all of the system's loads are linear, however; some, when driven by a single frequency voltage, draw a current that is distorted. The harmonic currents created in this manner flow through the branches of the system's network and distort the voltage waveform that the utility delivers to its customers. This distortion degrades the performance of both the system and its load. Excessive dissipation, interference with communication and control signals, and overstressing of components are examples of the detrimental effects that can occur.

Motors and transformers are the original sources of harmonic distortion. Compared to their fundamental component, however, the percentage of harmonic currents these loads draw from the utility is small, and they have therefore seldomly caused serious distortion related problems. Installations of electronic power conditioning circuits, on the other hand, present a much more nonlinear load to the utility. The process by which these circuits change the utility's sinusoidal waveforms into those special waveforms required by their loads can also cause the current drawn from the utility to be substantially distorted.

Although power circuits are now only a small fraction of the

system's total load, there is great potential for their number and total power rating to grow. As this growth proceeds, the level of distortion in the utility will increase, and there is great concern that intolerable harm will result.

The analogy between the distortion of the utility and the pollution of an environmental system is often made. It is not completely correct. The purpose of the electric utility is to provide power, not pure fundamental waveforms. Its ability to do so is impaired by many of its loads. Some require a widely varying level of power, some are highly reactive, and now, with the advent of power conditioning, some draw substantial harmonic currents. All such loads degrade the operation of the system. Each must be accommodated, but none should be considered foreign.

The reference to pollution does have some proper connotations, however. We are in the beginning stages of what must be projected as a rapid growth of conditioned load. Although distortion related problems are relatively minor now, experience has shown that such growth will ultimately cause serious problems if no corrective actions are taken. The best time to investigate and propose solutions is certainly now, but much of what must be known to do so is elusive. As with other pollution problems, the interactions are complex, the important parameters are continually changing, and the situation of the future is difficult to predict. The questions grow more rapidly than the answers, and every corrective action found to be optimal in some respect is also found to have unlimited exceptions to its use.

The search for a solution must be more focused. The intangibles

must be set aside and the dilemmas must be resolved as well as is possible with our current understanding. As efforts are then devoted to more well defined goals, the knowledge and skills that can be brought to bear will be much more likely to reach a satisfactory solution to the harmonic distortion problem of the future.

This thesis proposes, and begins the effort of reaching, one possible goal: the development of a utility/dc power conditioning interface that draws very little harmonic current from the utility system. Active waveshaping techniques are used to achieve this effect.

The organization of this work is as follows. The first two chapters develop the goal. The salient issues of the harmonic distortion problem are discussed and the appropriateness of a specific solution, an ideal power conditioning interface, is argued. The second two chapters present the design of such an interface. One covers the circuit's topological aspects, the other discusses the issues of control. These are then followed by a chapter that presents the design and actual performance of a 6 kW ideal interface.

Nowhere in this work are all the details of all the aspects of the harmonic distortion issue discussed. If such an understanding is desired, a study of the literature will have to be made. To facilitate such a study, an extensive list of the papers published on the subject over the last several decades has been provided.

CHAPTER II

THE HARMONIC DISTORTION PROBLEM

Harmonic distortion threatens the quality of our electric utility service. This is not to say that distorted waveforms in the system are a recent development: motors and transformers have been present from the beginning and the first power conditioned loads were attached to the utility over fifty years ago. Nor does it mean that a distortion-free service would be sufficient: there are many other anomalies within the system and its load that make the utility's performance less than ideal. The threat is not even that distortion is the system's most undesirable problem, but rather that it is a growing one. Many of the difficulties faced by the utility will continue to be the same as they have always been. They can be handled with well understood and well practiced methods. Both the magnitude and character of the harmonic distortion problem are undergoing a significant change, however. The potential for harm due to this change is great.

The technical community is aware that a solution is needed and has begun the search. Many papers have been published in the last ten years. Some provide detailed analytical work or empirical results that improve our understanding of the magnitude of the problem. Most offer educational overviews that attempt to define and specify various aspects of the harmonic distortion issue. Technical organizations have set up committees to investigate the problem and suggest solutions. Government agencies have supported studies by industrial and academic institutions. Utility companies are developing the tools and awareness needed to

assess the present status of the problem. The work has only begun, however; there are still many uncertainties. A clearly defined policy has yet to be developed.

It is both the rapid growth and the changing character of the sources of harmonic current that impede the development of a clear and workable solution. Our present ability to solve distortion problems is based on features that will eventually be less prevalent. For example, the ability to relate a source of harmonic currents to its corresponding detrimental effects will diminish. The control over an installation of conditioned load will decrease. The development of a specific solution for a specific situation will be harder to achieve.

Unfortunately, while the features of the utility's future conditioned load make the straightforward corrective procedures of the past unusable, they do not readily indicate what should be done instead. To find solutions that are well suited to the coming situation, it is first necessary to know where our efforts should be directed. This, in turn, requires that we understand the nature of the change that is taking place.

The following sections of this chapter will help develop this understanding. The first will present the harmonic distortion problem as it now exists and the second will describe how conditioned load is changing. These will then be followed by a discussion of the difficulties caused by the change and a review of the technical community's reaction to these difficulties.

II.a The Harmonic Distortion Problem Up To Now

Even though the number of power conditioned loads has steadily grown over the last several decades, the salient features of the harmonic distortion problem have changed very little. The difficulties we now experience and the solutions we impose are therefore much the same as they have always been. There are simply more occurrences.

Perhaps the most important feature of the harmonic issue today is the negligible level of distortion in most of the power system. We have not had to face a situation where harmonic problems occur throughout the system, from the lowest sector of the load to the generators. The total amount of conditioned load is not yet great enough to cause such an affect. Instead, the problems that do arise are isolated instances. Not every power circuit creates an intolerable situation, and those that do can be dealt with individually.

The problems we currently experience are caused by power circuits that condition high levels of power for heavy industrial loads.[19,20] Because the level of distortion created by these circuits decreases with distance through the network, the extent of the affected area is usually limited. Most harmonic currents are shunted at the first regulation capacitor; only the lowest frequency components continue to flow deeper into the network. Since much of the impedance seen by the power circuit is the result of nearby feeders and transformers, the extent of the voltage distortion is also limited to the locality. There are, in essence, islands of distortion within a network that is free of distortion.[18,106,111]

Because the distorted areas are limited in size, when harmonic problems are recognized, the offending sources are easy to locate. First, there are normally several complaints that help define the problem area. Second, due to the industrial nature of high-power conditioned load, there are only certain types, and usually small numbers, of facilities where the power circuit could be. Finally, once the potential offenders are located, it is often possible to turn each power circuit off to determine its contribution to the detrimental effects observed.

Once a harmonic related problem is recognized and the source of the distortion has been found, certain well defined steps can be taken. One is to use either phase-multiplication techniques or passive filters to limit the amount of injected harmonic current to acceptable levels. Another is to connect the power circuit directly to a higher power level, and therefore lower impedance, branch of the network to reduce the voltage distortion produced by the harmonic currents. Yet a third is to use either separate electric services or intervening filters to isolate the sensitive load from the distorted waveforms.

Each of these solutions has been applied in many high-power situations; each is well analyzed and documented.[8,16,17] There are difficulties and disadvantages associated with their implementation, but they are all capable of reaching the desired goal. The problem is really only a matter of deciding to what extent the corrective measures should be taken. To either over- or under-correct can waste material and effort.

A major portion of the research done to this day is directed

towards facilitating decisions about corrective measures. Modeling and analysis tools have been developed to predict the levels of distortion that will occur in a given situation.[4,194,196,197] Some are more sophisticated than others, but they all can determine the consequence of a small number of conditioned loads in a limited section of the system's network. Experiments have been conducted to relate the level of harm experienced by many typical loads to the magnitude and frequency spectrum of the distortion to which they are subjected.[68,79,92,99] Measurement tools have been developed to determine what levels of distortion already exist.[159,164] Whenever all these sources of information fail to be adequate, the existing wealth of experience in similar situations can often give a very good indication of what should be done.

Fortunately, the very nature of high-power conditioned load lends itself, in several ways, to the control of harmonic distortion. First, the cost and importance of the power circuit are great enough to cover the expense of a special engineering effort devoted to each particular case. Second, both the designer and the purchaser of the power circuit are very aware of the consequences of the installation. They know that the distortion can cause problems and that the greatest detrimental effects are likely to be experienced by the load within the same facility. They are anxious to avoid these problems and are willing to incorporate corrective measures from the beginning. Finally, whenever the problems are not handled by those who own the power circuit, the utility often has the ability, due to the industrial nature of the load, to exercise considerable control. The situation is quite different,

however, for low- and medium-power loads, as will be discussed next.

II.b How Conditioned Load Is Changing

There are several rapidly growing technologies that will increase the number, variety, and total power rating of conditioned load connected to the utility. One is the electronic industry. The number of electronic circuits we need and can afford is undergoing a tremendous growth. Although it is usually a secondary issue to both the designer and the user, each of these circuits will require a power conditioning interface with the utility. Other technologies that depend on power conditioning in a more direct way are also developing. Solar-photovoltaic installations will need utility interfaced converters for load balancing. Electric vehicles will need battery chargers. Automated assembly lines will need controllable and efficient motor drives.

The power electronic technology is keeping pace with these advancing technologies. A growing group of power electronic engineers is developing more sophisticated circuit topologies and control techniques. Better semiconductor devices continue to become more readily available at lower prices, and passive energy storage components have been improved. New fabrication techniques that make the production of power circuits easier are also available. The results of these developments are that a power circuit is now cheaper, lighter, smaller, more efficient, and more reliable than had previously been possible. These improvements are so substantial that they are, themselves, largely

responsible for the feasibility, and therefore rapid growth, of conditioned load.

The combined technological advancements are doing more than increasing the system's conditioned load, however; they are changing its character. Low-power loads that could once be neglected will become so numerous that they will begin to have an important combined effect. An emerging group of conditioned loads in the medium-power range will also be a new source of considerable concern. High-power loads will always retain their significant impact, simply because their power ratings are so substantial, but the time when all other loads could be completely ignored will come to an end.

Low- and medium-power conditioned loads have features that are distinctly different than those of high-power loads. It is, in fact, these differences, rather than the actual level of power flow, that distinguish the three classifications. These differences, described below, are the reason it is so difficult to know how to handle the harmonic distortion problems that can be expected in the future.

High-power conditioned loads are typified by the three-phase converters used for industrial processes, motor drives, and HVDC links. They are few in number but represent dominant fractions of the load in their locality. As discussed in the last section, they are individually designed and installed at specific sites. The percentage of distortion in the current they draw from the utility is small relative to that of low-power conditioned loads, but the impact that a single power circuit can have on the system and the local load is more significant. The extent of the harmonic related problems may vary from one situation to

the next, but each implementation of high-power conditioned load has the potential to produce major detrimental effects.

Low-power conditioned loads are exemplified by small computers, laboratory instruments, communication equipment, and home appliances. In contrast to high-power loads, they are connected to a single phase of the utility. The amount of distortion in their ac current waveform is very high; total harmonic distortion levels of 70% or more are common. They are mass-produced and widely distributed throughout the system. No single low-power conditioned load distorts the system to an appreciable level; they demand attention only as a collective group.

Medium-power conditioned loads require power in the 1 to 100 kW range, a level previously reserved for circuits designed along the lines of the high-power installations. Examples of such loads include motor drives, battery chargers, uninterruptable power supplies, and line-interfaced inverters. The technological advancements described above have created a need for, and the ability to provide, power circuits that can handle this level of power and still retain many of the attributes of low-power load. They are mass-produced and have the potential to be very numerous. They will be widely distributed throughout the residential, commercial, and light-industrial sectors of the system and will often operate from a single-phase service. Unlike low-power loads, however, each medium-power conditioned load has the capability of creating substantial levels of distortion on its own. As a group, they have great potential to cause harm.

II.c The Difficulties Caused By This Change

If the amount of conditioned load were simply growing, the level of concern would not be as great as it is. Even as more high-power conditioned loads were installed, the corrective procedures that have always been used would be able to handle the problems that arose. The increased experience would even improve the skill with which the problems were solved. But the growth is bringing about a shift toward the low- and medium-power conditioned loads. These loads, by their distinct nature, present difficulties that are not well suited to the established methods of solution.

The mass-produced feature of the new conditioned loads will eliminate the close relationship between the designer and the user of a power circuit. The designer will know nothing about the installation site and will have no details about the topology and the impedance of the local network, or about the number and kind of sensitive loads that will be affected by the power circuit. Without this information, designers can not modify their circuits for each particular application. Designs must work satisfactorily in all situations, no matter where they are connected to the utility, no matter how many other power circuits are in the locality, and no matter how sensitive the local load is.

The users of the mass-produced conditioned loads are similarly distant from the details of the interfaces that are being installed. Customers no longer play an active role in specifying the power circuit's performance, but simply buy what is available. Their concerns are primarily with the requirements of the load and they may even be unaware of the problems that distortion can cause. Because they will

not normally have the expertise necessary to make decisions about what is installed, they can not be expected to play a role in the control of the electric system's distortion level.

The widely distributed nature of the new conditioned loads causes its own difficulties. One is that it will no longer be easy to locate, or even define, the significant sources of harmonic distortion. There will be too many of them, connected to every sector of the system's network, to allow any one power circuit's contribution to be separated from the others. All will be responsible for the detrimental effects to one degree or another. Corrective procedures cannot be brought to bear on any individual power circuit; they must be applied to the entire class of conditioned load instead.

A related consequence of the dispersed nature of the installation sites is the utility's inability to know where, and how many, power conditioned loads are connected to the network. The typical owners of low- and medium-power loads do not consume power at a level that allows the utility to justify close monitoring. But without such monitoring, the utility will not be able to exert control over the harmonic current sources once they have been installed.

The reduction from three-phase to single-phase operation is a third, and important, feature of the new conditioned loads. With only one phase to work from, phase multiplication techniques that can substantially reduce the harmonic content of the ac current are no longer possible. Harmonic reduction must be achieved in more complicated and expensive ways. For those power circuits that provide an interface to a dc system, single-phase operation also requires larger

dc side filter elements than would be needed in a three-phase power circuit. The added expense of these larger components consumes resources that might otherwise be applied toward the shaping of the ac current waveform.

II.d The Reaction to the Changing Situation

The response to the evolving harmonic distortion issue is occurring on two levels. The first is the growing awareness that distortion is a problem and the development of more conservative attitudes toward the pollution of the utility system. The second is the direct effort to deal with exactly those difficulties that the changing character of conditioned load is introducing.

Harmonic distortion has become a much more familiar phenomenon than it used to be. Both the user and the manufacturer of sensitive loads such as computers and communication equipment are now aware of the harm that a distorted utility can cause. The customer is concerned when a conditioned load is installed nearby; the manufacturer realizes that efforts must be made to reduce the sensitivity of a product.

The manufacturers of conditioned loads are also beginning to understand that corrective efforts on their part are advantageous. Those who produce power circuits to control lights, heating, and electric motors are already installing filters in their products to remove the most damaging harmonic components from the ac current. This action is in direct response to the desires of the market place and is otherwise voluntary.

The change in attitude by all concerned does not solve the harmonic

distortion problem of the future, but it does affect the type of solutions that can be feasibly implemented. The more the problem is recognized and the more a solution is felt to be needed, the easier it is to propose corrective measures that require substantial cooperation.

There is not yet a direct answer to what those measures should be, however. Several concepts related to the character of the future harmonic distortion problem have been introduced by the technical community. Ideas such a stochastic cancellation of harmonic currents, centralized filters, and active harmonic filters are examples of what is being discussed.[122,154,155,156] These ideas have prompted interesting work, but they have not led to the formulation of a policy.

Instead, the most direct and prominent response to the emergence of low- and medium-power conditioned loads is the proposal of a limit for the level of distortion that will be allowed to exist in the utility's voltage waveform. The power system's voltage must already meet certain amplitude and frequency requirements; the addition of a harmonic distortion level regulation seems consistent and is widely discussed.[8,113,116] Such a standard does not always represent the optimal way to solve the distortion problem, but it does provide a specific goal toward which both the designer of the power circuit and the manufacturer of a sensitive component can work. With this goal, they should be able to come to well defined decisions about how their products must be designed.

The European governments proposed standards nearly ten years ago. Their major concern was for the unrestricted trade of household appliances from one country to another. They wanted to provide

manufacturers the guarantee that their products would be accepted by other countries as long as they met the standards proposed. The allowable levels of distortion set in the regulation were low (5% THD of the voltage waveform) and subject to future change.[114]

These formal standards are most significant for the precedents they have set. The ideas that there should be regulation, that the standards should be based on the total harmonic distortion of the voltage waveform, and that the allowable level should be around 5% are often suggested.

The United States government has approached the harmonic distortion issue in a different manner. Regulation, although discussed, has not yet been seriously proposed. Instead, over the past five years the government has been heavily involved in the development of the new technologies most relevant to the growth of medium-power load: photovoltaic and wind powered energy generation, fuel cells for load balancing, and electric vehicles. Since the development of the required power circuits was an integral part of each program, the government has been able to direct research efforts into the harmonic distortion area. Several studies have been sponsored to determine what level of distortion is acceptable, what levels exist, and what levels can be expected as their programs reach the implementation stage. This is not to say that regulations have been ruled out in the United States. There is just a realization that time and resources are available to become more sure about what those regulations should be.

Whether or not regulation is the best, or even an appropriate, approach to the harmonic distortion problem of the future is still

unknown, however. Although it seems to provide a well defined solution, it also raises many questions that have not yet been answered. Some of these questions will be discussed in the next chapter.

CHAPTER III

THE IDEAL UTILITY/DC INTERFACE: A VIABLE APPROACH FOR THE FUTURE

The specification of a standard for the harmonic content in the utility's voltage waveform is not intended as a solution to the future distortion problem. It is simply a declaration of what distortion level is tolerable. Unlike the management of the voltage's fundamental amplitude or frequency, however, the utility has very little means to control the distortion that exists in its waveform. If a single conditioned load were responsible for the intolerable level of voltage distortion, it might be possible for the utility to implement corrective procedures. But when the excessive level of distortion is reached only through the combined contributions of many conditioned loads, there is very little the utility can feasibly do.

For this reason, when harmonic standards are either contemplated or proposed, they are usually meant as restrictions on conditioned load rather than as requirements for the utility industry to meet. Presumably, only those loads that satisfy the requirements of the standards would be allowed to connect to the utility.

The standards proposed by the European agencies allow any single conditioned load to distort the system's voltage up to the limits specified.[114] The conditioned load under test is to be connected to a standard network consisting of a stiff voltage source and a representative impedance. As long as the harmonic components in the voltage at the terminals of the load remain within the regulated levels, the appliance is approved.

The problem with this approach is that it treats each source of harmonic current separately, with no regard for the contribution of the others. For the distortion problems of the past, where isolated high-power conditioned loads were the only concern, this policy would have been valid. But for the problems of the future, where many low- and medium-power conditioned loads combine to create harmful levels of distortion, the approach is inappropriate. For example, if the first electric vehicle battery charger in a residential area were allowed to create the maximum harmonic voltage levels, subsequent installations of the same power circuit would cause the levels to be exceeded. A regulation policy where individual power circuits are each allowed to cause the maximum tolerable voltage distortion can not escape this problem.

An alternate policy might be to restrict the amount of harmonic current each conditioned load could draw from the utility, regardless of the voltage that this level of current would cause. The point of this approach would be to anticipate the combined contributions of many conditioned loads and to control each such that voltage distortion they created as a group would remain within the levels that were acceptable. Such an approach would require not only that an acceptable level of voltage distortion be determined, but also that the total amount of harmonic current that would, for a typical network, give rise to this level be calculated. It would then be necessary to assign a limit, perhaps based on a per unit rating, to the harmonic currents each load could contribute.

While this approach might avoid the problems faced by the control-

of-harmonic-voltage approach, it does require a great deal of knowledge about the situation of the future. The question of how low the current limits must be set to guarantee that the acceptable level of voltage distortion will never be exceeded is difficult to answer. Too much depends on how many conditioned loads there are. Even if the growth of power conditioning installations could be reasonably predicted, situations where conditioned loads are much more concentrated than the average would suggest will always occur.

The true problem with both regulation policies is that, in declaring what threshold of distortion is tolerable, they suggest that it is not necessary to do still better. If, in response to such standards, the currently used power circuits that draw very distorted currents are to be replaced with circuits designed to draw less harmonic currents, a considerable effort will be required to do so. The emphasis of this effort should be more than the attainment of specified levels; the work should be devoted to reducing the harmonic currents as much as possible.

Rather than meeting unavoidably arbitrary standards, the goal should be to make the power circuit an ideal interface, a two port element that would condition power without allowing either the character of the power circuit or the nature of the system at one port to be imposed upon the system at the other. Such an interface, if feasible for the low- and medium-power conditioned loads, would be well suited to exactly those difficulties that the loads in these power ranges have introduced.

In the next section of this chapter, the arguments for and against

the ideal interface as a solution to the harmonic distortion problem of the future are discussed. These are then followed by a presentation of some basic issues on how the interface might be designed.

III.a Arguments For and Against the Ideal Interface

The ideal interface is an appropriate way to deal with the widely distributed and diverse nature of the future conditioned load. All other approaches, whether they emphasize regulation of the harmonic current sources, alteration of the network impedance, or isolation of sensitive components, depend strongly on the number, power rating, and location of the conditioned load. These features of the load are hard to discern and are constantly changing. To be effective, the alternative approaches must either foresee all possible situations or be continually updated. Both tasks are difficult to accomplish. The ideal interface, in comparison, is a solution that does not depend on factors that are uncontrollable. Instead, it is a solution that always works, no matter where and how much conditioned load there might be.

The ideal interface also deals effectively with the problems caused by the mass-produced nature of low- and medium-power conditioned load. Because the power circuit's performance is not dependent on the character of the system's network, the designer does not need to know the details of the installation site. The purchaser is similarly free from concern, and does not need to be aware of potential problems, or to recognize actual detrimental effects, or to understand the details of corrective measures. Sensitive components located near the power circuit will not be adversely affected, no matter how many or what type

they are.

In essence, the ideal interface avoids all those problems that made the low- and medium-power conditioned load difficult to handle. There are no questions about what level of distortion is tolerable, what effect the distribution system will have, how and when corrective measures should be implemented, or how long the solution will remain satisfactory. These intangible aspects of the future harmonic distortion problem could never be adequately addressed. The ideal interface approach bypasses them and forces efforts to be focused on a fixed point: the power circuit. The problem and the goal therefore become well specified. This feature is, in itself, an important virtue of the ideal interface approach.

That the ideal interface is a permanent solution is also important. The power circuit, once developed, will benefit from the lack of need to change. Components intended specifically for the ideal interface can be produced. The design and the manufacturing process can be finely tuned. The market will require large numbers of identical units. As all these features help reduce the cost of the ideal interface, its feasibility will become much greater than the initial costs would suggest.

The cost of the ideal interface may be further offset by additional beneficial features that its design provides. As the next two chapters will show, the ideal interface is capable of presenting a unity power factor load to the utility; no compensation capacitors are needed. The ideal interface also requires far less energy storage within the power circuit than is possible with today's typical circuit designs. Besides reducing size, weight, and cost, this lower energy requirement allows a

much faster control of the power that is delivered to the load. All these features are useful and help to reduce the overall cost of the power circuit. The marginal cost that must be associated with the reduction of harmonic currents is therefore not as great as it would otherwise be.

Finally, it is appropriate that the ideal interface approach is a solution that requires the cause of the distortion to bear the cost of its correction. The designers of power circuits have long considered it necessary to provide their load with clean waveforms; their view of the utility system should adopt this same consideration.

There are shortcomings and limitations to the ideal interface approach. The following paragraphs discuss some of these points.

One argument against the ideal interface is that it is an extreme solution. It may be much more of an effort than is required. The rate at which conditioned load will grow is not certain. Many power circuits installed at any time in the near future may not remain in service long enough to take part in a combined contribution of significant harmonic distortion. There will always be situations where the extreme efforts required to obtain negligible harmonic distortion levels are not needed. But if the use of an ideal interface is left to choice, much of the value of the approach will be lost.

The ideal interface approach also forces a conservative, rather than an optimal, solution. No advantage is taken of natural cancellation between conditioned loads. Centralized solutions that exhibit economies of scale are not followed. There is no selective reduction of harmonic components based on the actual detrimental effects

observed. Corrective measures are always taken at the power level; a solution at the signal level, as might be possible in communication equipment for example, is no longer considered. The cost associated with the loss of an optimal solution can never be determined, but it should be recognized.

Finally, there is a technological limit to the ideal interface. The level of power that can be reached while maintaining an acceptably low level of distortion has an upper limit. This limit will improve with technological advancements, but it will never be possible to provide an ideal interface for all conditioned loads.

III.b How to Obtain an Ideal Interface

Most applications of power conditioning circuits involve the transfer of energy between the utility and a dc load or source. Even when the load requires alternating waveforms, a dc link is often provided to separate the utility interface function from the inversion function. For this reason, the ideal interfaces developed in this and the following chapters will be dedicated to utility/dc power conversion.

The power circuits currently used to provide an interface between the utility and a dc system are able to meet the requirements of their dc systems quite well. It is the shaping of the ac current waveform into a fundamental sinusoid that is needed to make the power circuit an ideal interface.

One way to achieve the sinusoidal current waveform is to use passive waveshaping techniques. In this approach, the semiconductor devices of the power circuit perform only very basic functions: they

provide rectification and control of power level. Passive filters are then used to remove the unwanted components from the waveforms of both the ac and dc systems.

To remove the harmonic components from the ac current waveform, a collection of tuned shunt filters is commonly used for the lower frequencies. A damped low-pass filter is then provided to take care of the remaining components. Finally, to increase the impedance against which the tuned filters can work, an inductor is usually placed in series with the utility. For a given filter, the larger this series inductor, the more effective the tuned filters will be. No passive filter is completely effective, however. The better job of waveshaping the filter must do, the larger, more complicated, and expensive it will be.

The other way to shape the ac current waveform is to use active waveshaping techniques. In this approach, the number of switch transitions per cycle is increased above the minimum level required. This increase can be accomplished by either the use of a few switches operated at a high frequency or the use of many switches, each of which is operated at a correspondingly lower frequency. By properly placing the switch transistions throughout the cycle, certain harmonic components can be removed from the ac current waveform. The more switch transitions there are, the more harmonic components that can be eliminated. Whatever components are left in the ac current waveform will be at high frequencies and can be easily removed with a simple and small low-pass filter.

The two approaches can be combined to any degree desired. The more

one approach accomplishes, the less the other must do.

III.c Active vs. Passive Waveshaping

Each waveshaping technique has its advantanges and disadvantages. The passive approach is the one that has been traditionally used, simply because the available semiconductor devices have not been suitable for any active waveshaping technique beyond phase multiplication. This condition no longer exists for the low- and medium-power conditioned loads, however. As devices capable of high frequency operation become more readily available in these power ranges, the feasibility of the active waveshaping approach is improving. Compared to the fixed limitations of the passive waveshaping technique, the active technique is steadily becoming more desirable.

The following paragraphs outline the difficulties of the passive approach and discuss the ways in which the active waveshaping technique overcomes them.

A passive filter has certain design limitations that cannot be circumvented. The Q of each tuned, series shunt filter can not be made arbitrarily high; the filter would be too difficult to tune initially and would not remain tuned as temperature and age affected the component values. Low values of Q (20 or less) are needed, particularly if the product is to be mass-produced.

The low Q has disadvantanges, however. For a given characteristic impedance of the filter, the lower the Q, the higher the filter's series resistance. As this resistance is increased, the dissipation caused by both the filtered harmonic current and the fundamental current needed to

fulfill the reactive requirement of the capacitor becomes greater. More series resistance also means that the filter will have a higher impedance at its tuned frequency. To achieve the same level of filtering with this increased resistance, the inductor placed in series with the utility will have to be made correspondingly larger.

A passive filter with many tuned series branches is also complicated to design. Between each frequency at which the filter presents a low impedance to the power circuit there is a parallel resonance that gives a very high impedance. If the power circuit injects currents at any of these alternate frequencies, the filter will resonate. The harmonic voltage seen by the power circuit and the harmonic current injected into the utility under that condition could become very large. At these same parallel resonant frequencies, the filter appears as a low impedance from the utility side. Currents injected by other conditioned loads at these frequencies may therefore flow into the filter and over-stress its components.

It is important to make sure the parallel resonant frequencies are positioned such that these detrimental effects are not substantial. To do so is difficult, particularly as the number of filter branches is increased.

A passive filter provides reactive power flow correction as well as the removal of harmonic components. Since the correction is usually needed by the circuit, this is a beneficial feature that helps offset the cost of the filter. The level of reactive power drawn by the filter is fixed, however; it can not respond to changes in the operation of the power circuit. A nominal value of correction must be chosen instead.

Unless special disconnect switches are provided, the filter continues to draw this reactive power even when the power circuit is not operating. The losses produced by this power flow can significantly reduce the overall efficiency of the power circuit.

The active waveshaping technique, by it nature, avoids the problems faced by the passive approach. One advantage of an active waveshaping power circuit is its much simpler interaction with the utility. Only a high frequency, low-pass filter is needed between the circuit's switches and the line. The design of such a filter is straightforward. No tuning is required and there is no important dependence on the system's impedance.

Another advantage of the active approach is that power compensation capacitors are not needed. An active waveshaping power circuit has the ability to draw a unity power factor current from the utility at all times. As will be shown later, it is actually easier to make an ideal interface that operates at unity power factor than it is to make one that can work at an arbitrary power factor.

The design and implementation of an active ideal ac-dc interface are not free from complexity, however. The topology of the power circuit must be chosen to meet the requirements placed on the interface and the correct positions of the switch transitions must be determined. The issues and details concerning these two problems will be discussed in the following two chapters of this work.

CHAPTER IV

TOPOLOGICAL FEATURES OF AN ACTIVE UTILITY/DC INTERFACE

This chapter presents the salient topological features of an active ideal utility-to-dc system interface. It begins with the development of the circuit's basic element: a lossless waveform transformer that can couple a dc system to an ac system. The various topologies this transformer can assume as its requirements range from the most general to the very simple will be outlined and compared. In addition to the waveform transformer, the ideal interface also requires passive elements for load balancing energy storage and switch frequency filtering. Those factors that affect the optimal design of these parts of the interface will be identified. Although much of the discussion in this chapter will deal with single-phase interfaces, the extension to three-phase systems, presented in the final section, is straightforward and, in some ways, easier to implement.

The voltage present at the ac terminals of the ideal interface has a sinusoidal waveform whose magnitude and phase are a function of the impedance of the utility system and the current drawn by the interface. Because the general operation of the interface does not depend on the parameters of the voltage presented to it, the utility will be modeled as a perfect voltage source throughout this chapter. It is only in the design of the switch frequency filters that the actual impedance of the utility plays an important role. When these filters are discussed, this influence will be considered.

The dc system may be either a source, sink, or passive load.

IVa. The Basic Element: A Lossless Waveform Transformer

The heart of the ideal ac-dc interface is a power circuit composed only of semiconductor devices. It has two ports, stores no energy, and, in the ideal sense, has no dissipation. The power entering one port is always equal to the power leaving the other. However, even though the products of the respective voltages and currents must be equal at all times, the ratios of each port's variables can assume any value desired.

The simplest application of such a power circuit is a dc-dc converter. This type of converter is typically used to change a dc waveform, either voltage or current, from one level to another. The power circuit can be thought of as a waveform transformer that couples the two systems. For time periods long compared to a switch period, the ratio between the currents or voltages at the two ports is a function of how the semiconductor devices are switched. This ratio will be called the waveform transformation factor.

For dc-dc conversion, the waveform transformation factor is usually constant. It is adjusted only in response to changing load or source characteristics. It is possible, however, to purposefully alter the factor over time to generate a time-varying waveform from a dc waveform. If the transformer is capable of both positive and negative transformation factors, it is even possible to produce an ac waveform with freely controlled parameters.

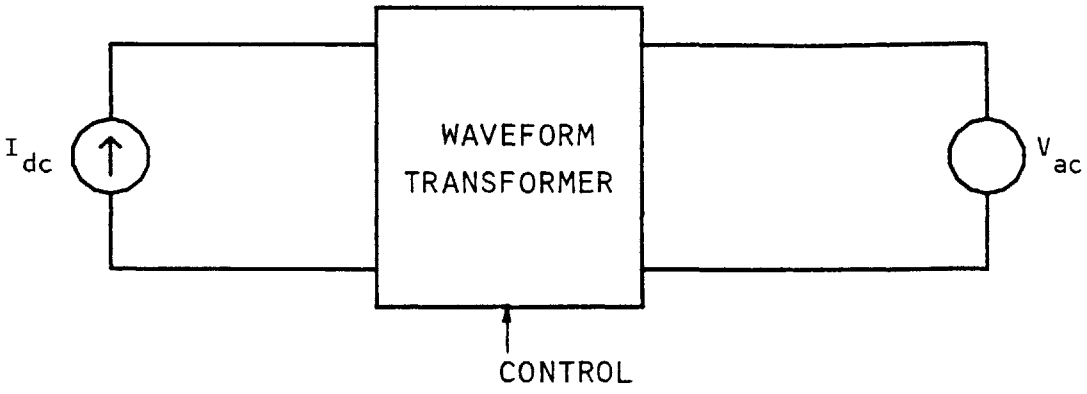
There are two ways such a lossless waveform transformer could be used to make an ideal ac-dc interface. One approach assumes the dc system is a current source; the other assumes it is a voltage source. It does not matter whether the dc system is actually an active source or

sink, or whether it is simply a passive load. It is only important to distinguish between those systems that have either current or voltage source characteristics.

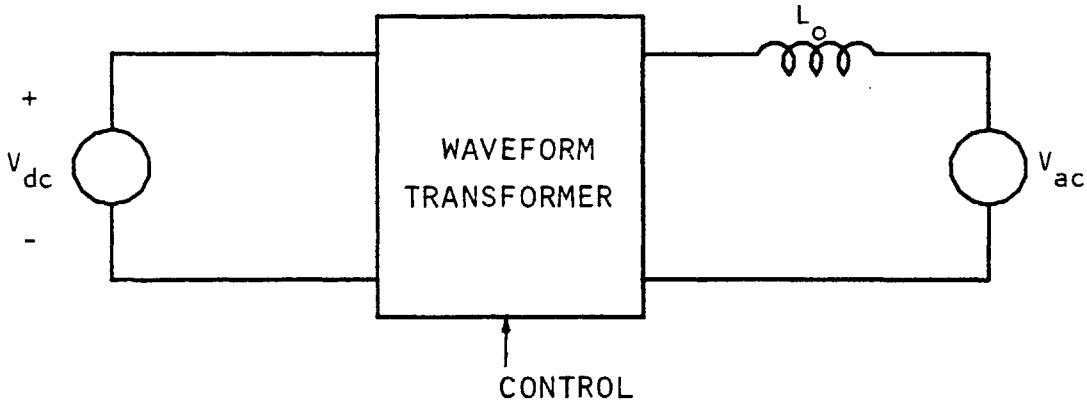
In the following discussion, that variable, current or voltage, which describes the dc system will be called the characteristic variable, the other will be called the companion variable. How a passive load assumes the characteristic of a current or voltage source will be discussed in the section on load balancing filter elements.

If the dc system is a current source, the waveform transformer is connected directly between the utility's ac voltage source and the dc system, as shown in Figure 4-1a. The switching pattern of the semiconducter devices is controlled to change the dc current waveform into a fundamental ac current waveform with whatever amplitude and phase are wanted. This implementation is the simplest form of the ideal ac-dc interface.

If the dc system has the characteristics of a voltage source, the waveform transformer will generate an ac voltage waveform, rather than current, at its output. Two ac voltage sources result: one, the utility, has features that are specified; the other, the output of the transformer, has features that are totally adjustable. An interconnecting inductor is placed between these two voltage sources as shown in Figure 4-1b. The amplitude and phase of the ac current flowing through this inductor and into the utility can then be controlled by adjusting the output waveform of the transformer. The more accurately and quickly this voltage waveform can be adjusted, the smaller the inductor may be.



a) For a Current Source DC System



b) For a Voltage Source DC System

Fig. 4-1: The Ideal Interface.

In many applications, the magnitude of the dc variable changes over time. For simplicity, this variation will be considered either as very slow compared to the fundamental ac period or as transient steps that are separated by long periods of steady-state operation.

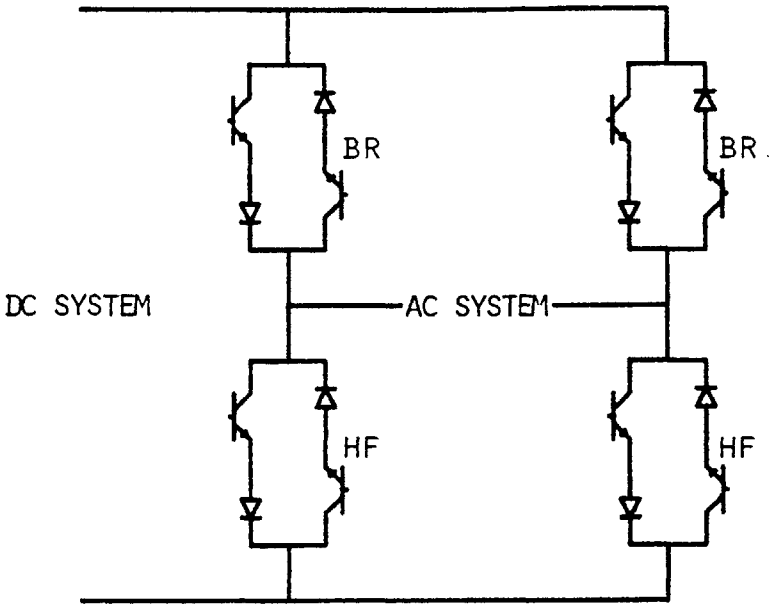
IV.b Semiconductor Requirements of the Waveform Transformer

Although a waveform transformer can be made to work from any non-zero characteristic dc variable, the discussion of this section will initially assume that the transformation factor can vary only between plus and minus one. The characteristic dc variable must therefore be greater than the peak of the corresponding ac variable. How the power circuit can be modified to remove this restriction will be discussed at the end of this section.

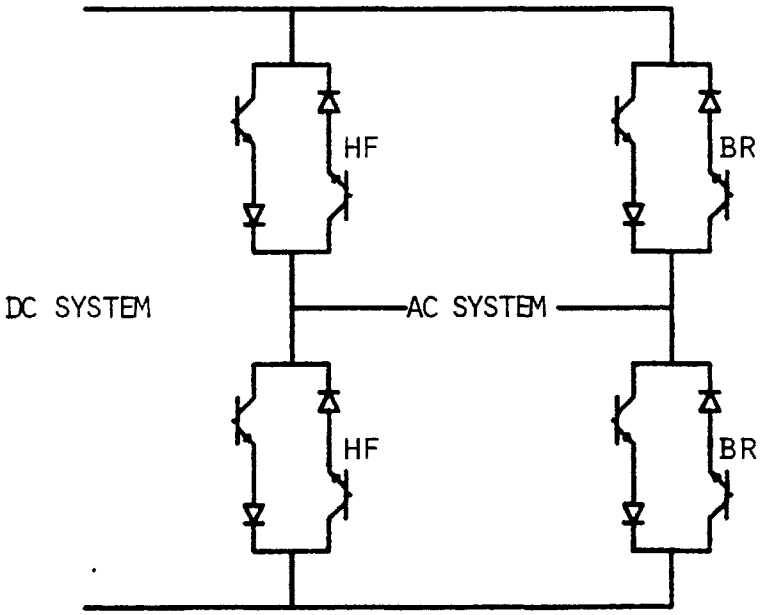
The General Waveform Transformer

Figures 4-2a and 4-2b show actual implementations of a general waveform transformer. To allow four quadrant operation on both the ac and dc sides, the transformer needs four switches, each of which must carry a bipolar current and support a bipolar voltage. Each switch must withstand the larger of the transformer's input and output voltage and carry the larger of the input and output current. For a given power level, therefore, the closer the characteristic dc variable is to the peak of the corresponding ac waveform, the lower the requirements placed on the switches.

Two of the four switches, marked with the letters "HF" in the figures of this chapter, are turned on and off at high frequencies to



a) For a Current Source DC System



b) For a Voltage Source DC System

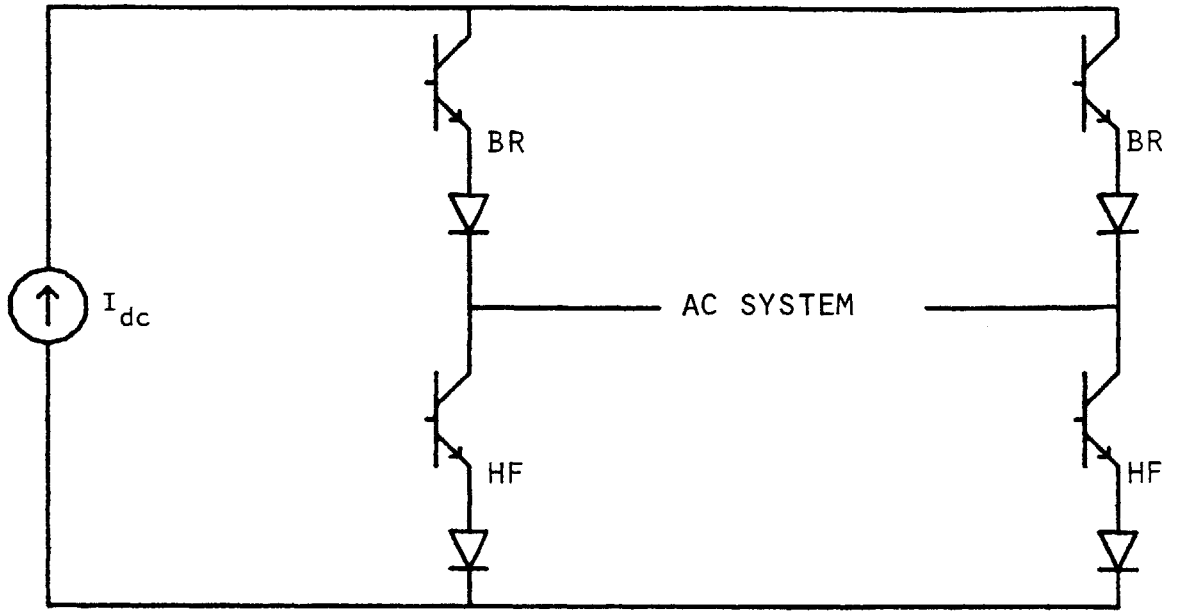
Fig. 4-2: The General Waveform Transformer.

provide the active waveshaping. The relative percentage of time during which each of these two switches conducts determines the transformation factor at that instant. The other two switches do not operate at high frequencies; they change state only when one of the four input and output variables changes polarity. Since they perform a low frequency bridge function, they are labeled with the letters "BR".

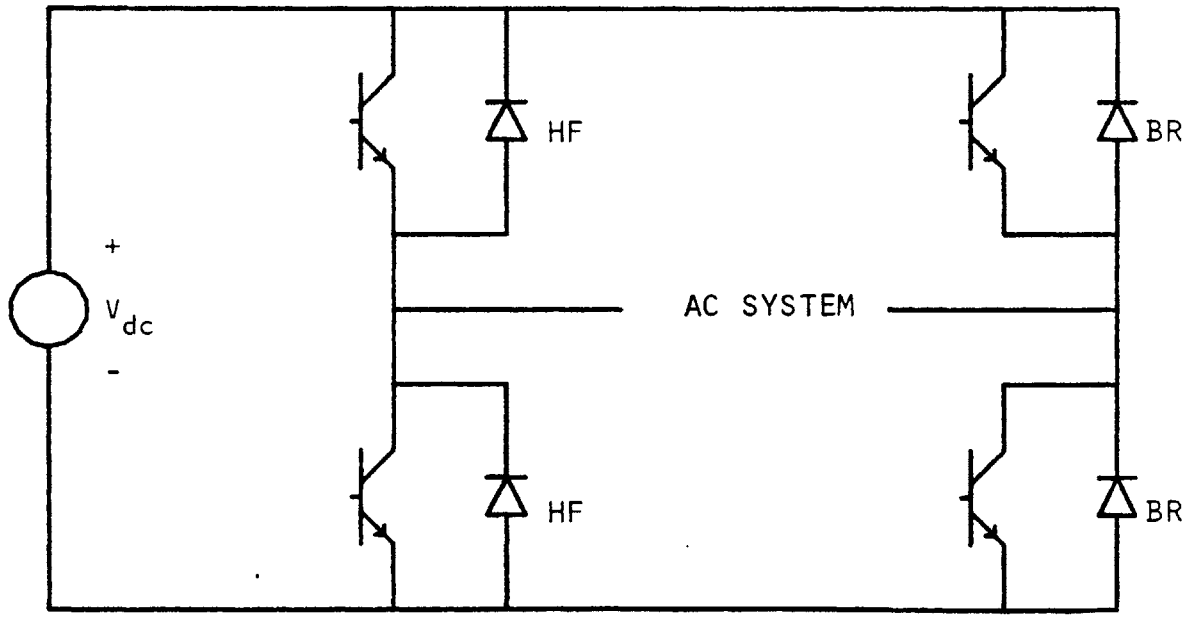
As can be seen from Figure 4-2, the position of the two types of switches depends on the characteristic of the dc system. The bridge switches in the current source case are responsible for changing the direction in which the current passes through the ac system. They are therefore placed on opposite branches of the topology. In the voltage source case, the bridge switches are used to change the polarity of the voltage presented to the ac system. To do this, they must be located on the same branch of the topology. In either case, the high frequency switches occupying the remaining two positions are able to control the average time during which the characteristic dc variable is presented to the ac system.

Waveform Transformer for a Two Quadrant DC System

The double bipolar requirement of the four switches in the waveform transformer can be removed if four quadrant operation is not needed for the dc system. In many useful applications, the dc system operates in only two quadrants. The characteristic variable (voltage or current) remains unipolar while the companion variable changes polarity to give bidirectional power flow. For these situations, the four switches of the waveform transformer have bipolar requirements on only



a) For a Current Source DC System



b) For a Voltage Source DC System

Fig. 4-3: The Waveform Transformer for a Two Quadrant DC System.

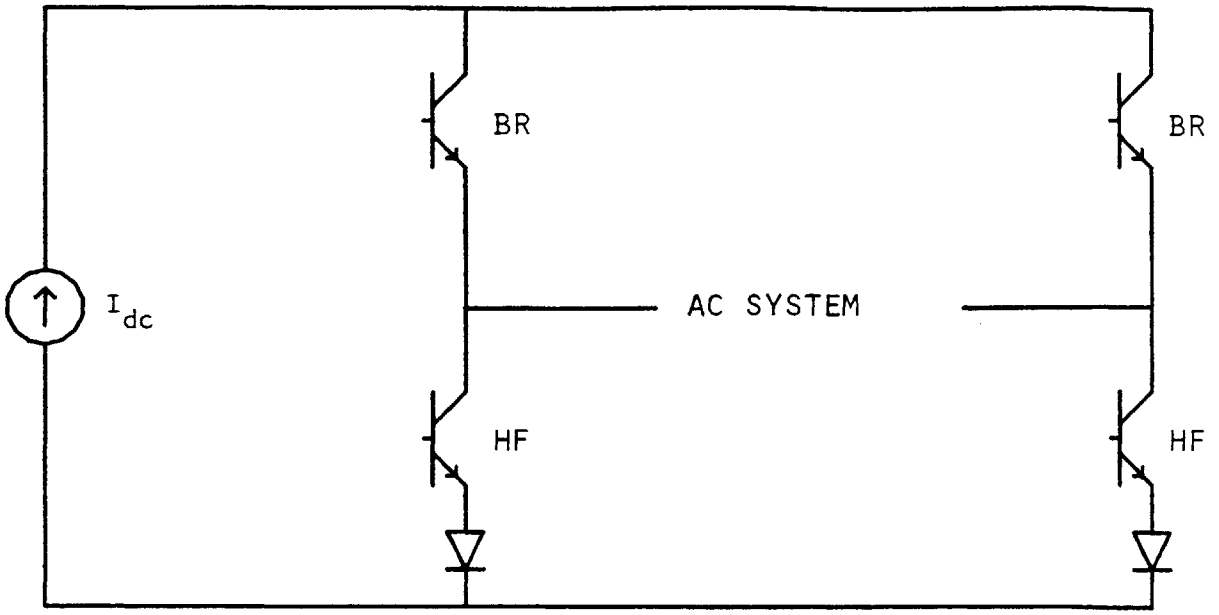
one of their variables. In the current source case, the switches must withstand bipolar voltages when not conducting; in the voltage source case, the switches must carry bipolar currents.

Implementations for these two cases are shown in Figures 4-3a and 4-3b. The total number of semiconductor devices is half that needed for the more general waveform transformer. For the voltage source case, the number of devices in the conductive path at any one time, and therefore the amount of conduction losses, is also halved.

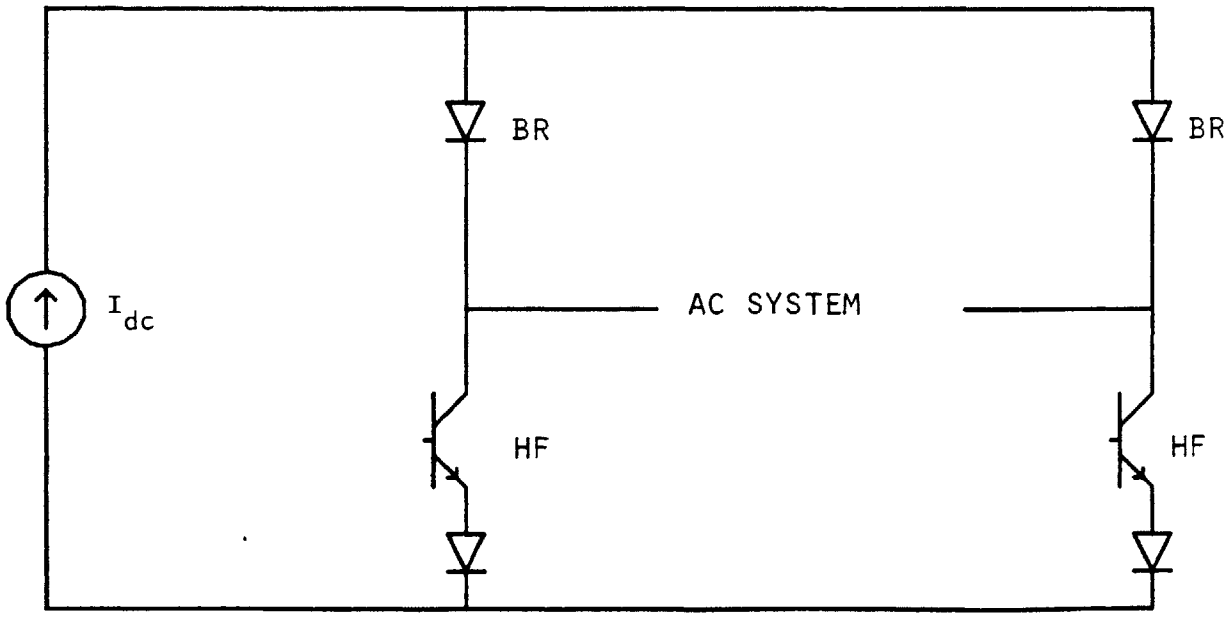
Waveform Transformer for a One Quadrant DC System

A great number of dc systems have power flow in only one direction. For those applications, the waveform transformer operates in only one quadrant on its dc side and two quadrants on the utility side. Since there is no provision to change the direction of power flow, the ac current waveform must have zero phase shift with respect to the voltage waveform at the transformer's output. In the current source case, this restriction implies unity power factor operation. In the voltage source case, there must be a slight phase shift between the utility's voltage and current to supply the reactive needs of the interconnecting inductor. The inductor is usually very small, however; the deviation from unity power factor is negligible.

The implementation of the waveform transformer when the power flow is unidirectional is shown in Figures 4-4 and 4-5. The first figure corresponds to the dc current source case; the second to the dc voltage source case. The two high frequency switches in each topology are identical to the previous topologies; they have one bipolar and one

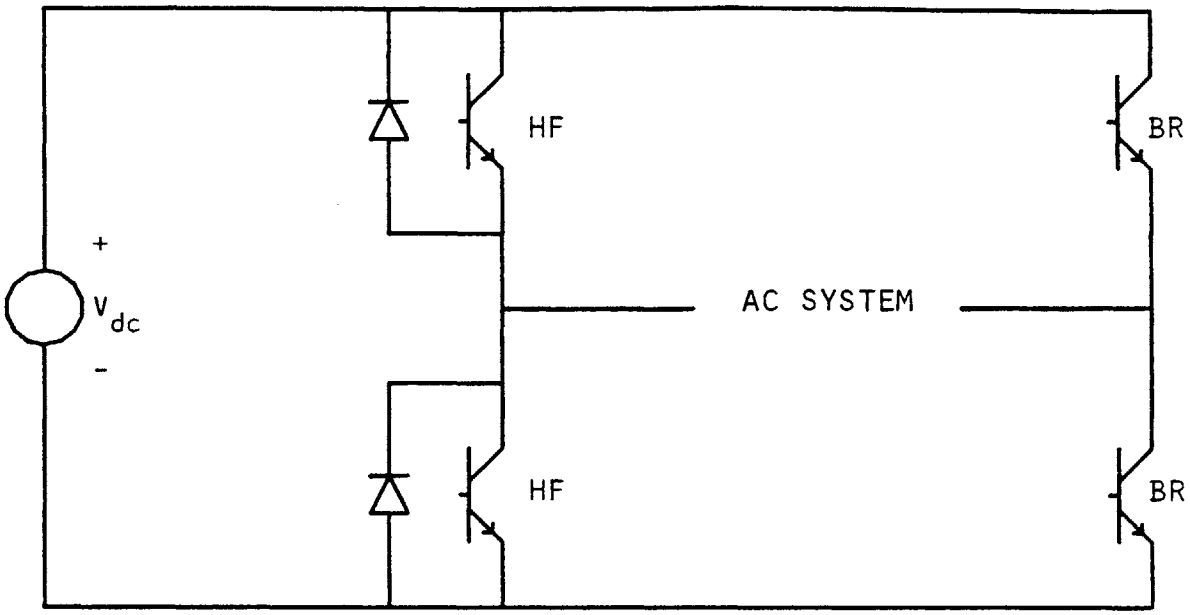


a) Power Flow from DC System to Utility

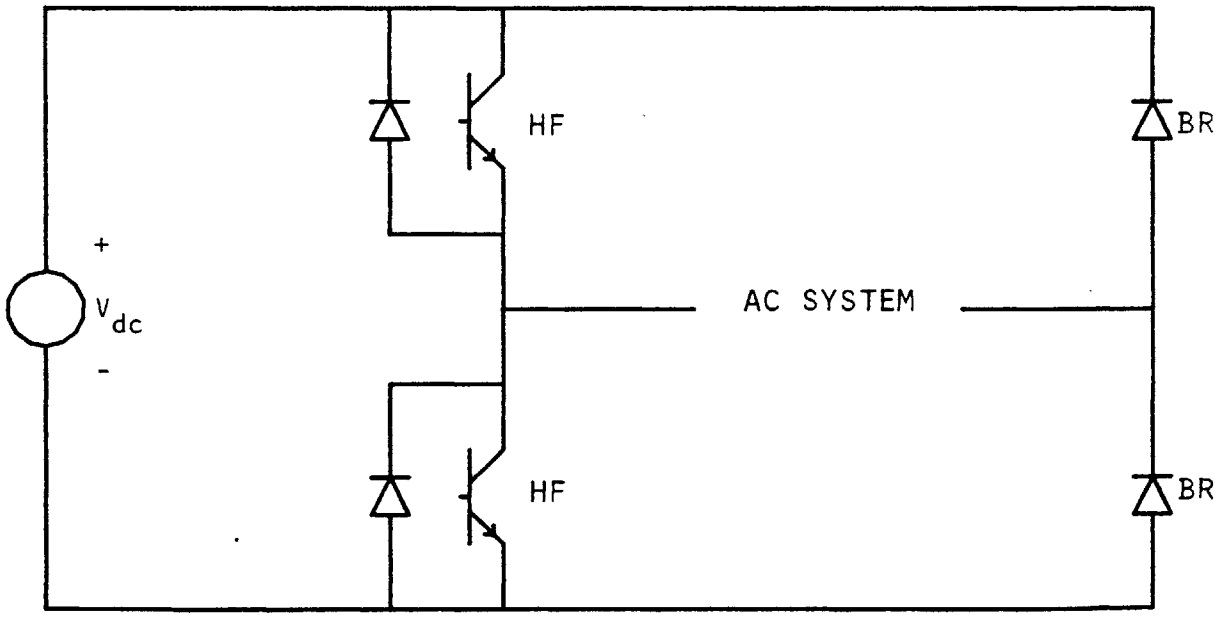


b) Power Flow from Utility to DC System

Fig. 4-4: Waveform Transformer for a One Quadrant DC Current Source.



a) Power Flow from DC System to Utility



b) Power Flow from Utility to DC System

Fig. 4-5: Waveform Transformer for a One Quadrant DC Voltage Source.

unipolar variable. The two bridge switches have reduced requirements, however; each can now be implemented with a single semiconductor device. As can be seen from these topologies, an ideal interface designed to operate at unity power factor is actually simpler than one that can operate at an arbitrary power factor.

The nature of the bridge switches is determined by the direction of power flow. When power flows into the dc system, the switches are naturally turned off; diodes can be used. When power flows from the dc system into the utility, the switches must be actively turned off; transistors or other controlled semiconductor devices are needed. This feature of the bridge switch is easily verified for these unidirectional power flow cases. It also points out the mode of operation for the bridge switches in the bipolar power flow cases previously discussed.

A Separated Waveform Transformer

The high frequency waveshaping and the bridge functions can be separated into two sections of the power circuit. This separation requires twice as many bridge switches, but, for the unidirectional power flow case, the number of high frequency switches is halved. Since the high frequency switches are both more expensive and have higher losses than the bridge switches, the separation is typically well justified. Figures 4-6 and 4-7 show how a separated waveform transformer can be implemented.

The bridge switches in a separated waveform transformer have lowered power ratings. The peak voltage and current they must withstand are no longer determined by the larger of the transformer's input and

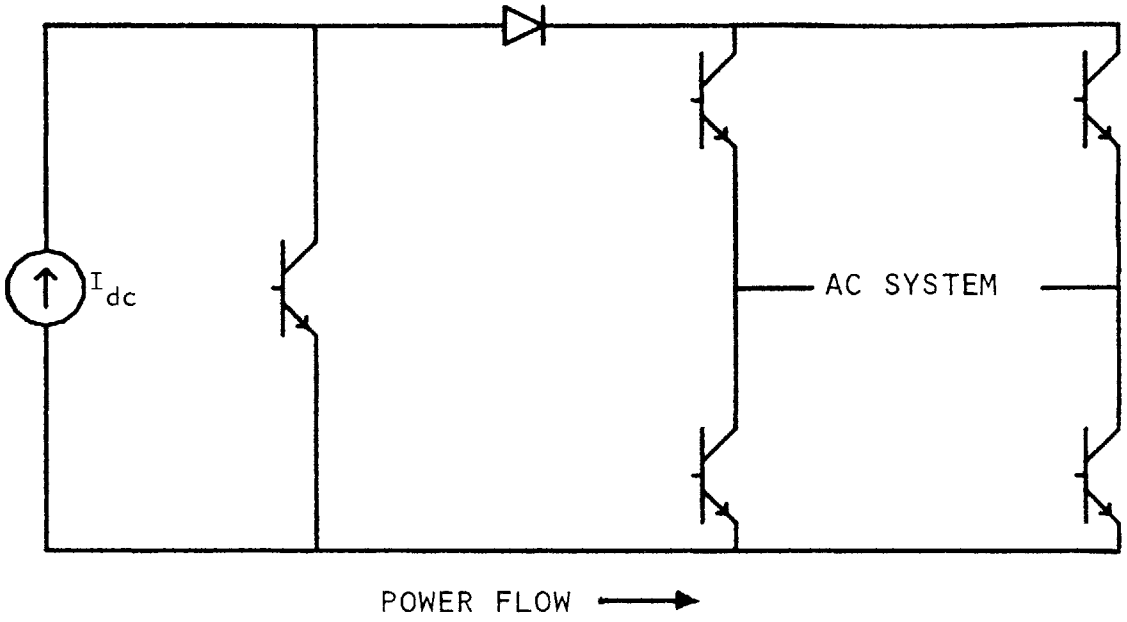


Fig. 4-6: A Separated Waveform Transformer for a DC Current Source.

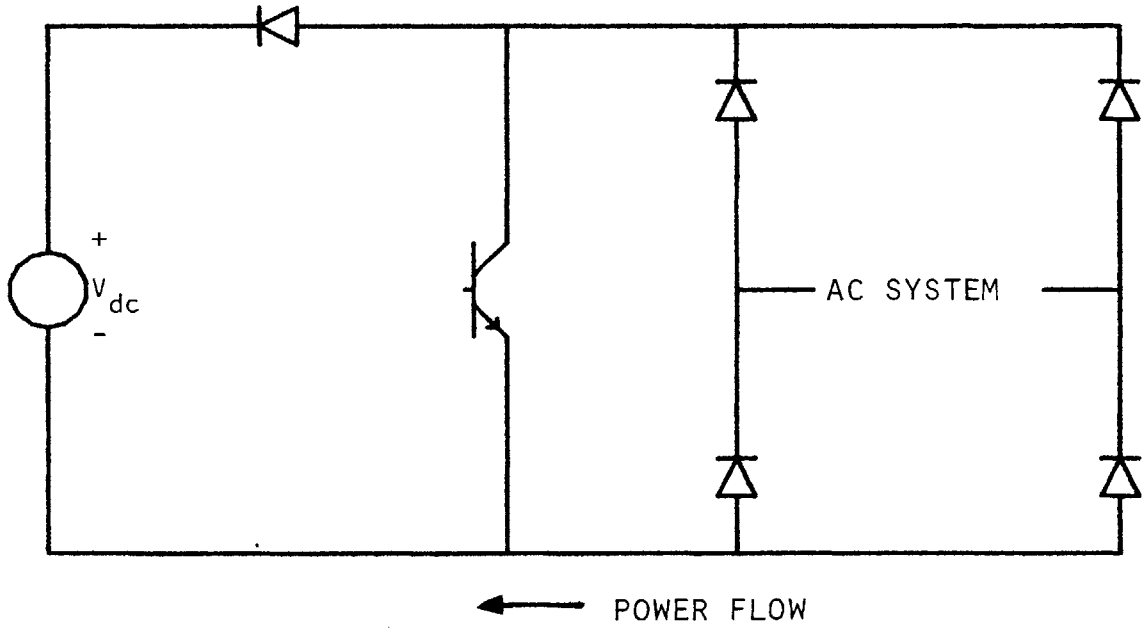


Fig. 4-7: A Separated Waveform Transformer for a DC Voltage Source.

output variables; they are simply dependent on the peak ac waveform values. When the characteristic dc variable is such that the transformation factor is always substantially less than unity, the reduction in power ratings can be significant.

Transformation Factors Greater Than Unity

For all the topologies presented so far, the waveform transformer has only been able to produce an ac variable that is lower than the characteristic dc variable. It is possible to add a small energy storage element to the high frequency switches so that the transformer can reach factors far greater than unity. Figure 4-8 shows the alteration that must be made to the unidirectional and separated power circuit given in Figure 4-7. The topology of the high frequency switches and the energy storage element is that of an up/down, or buck/boost, dc-dc converter.

When the power flow is bidirectional, the implementation of the up/down converter with only two bridge switches is difficult. It requires either four high frequency switches and an inductor or three high frequency switches and two inductors. For these applications it is better to separate the bridge and waveshaping functions, as shown in Figure 4-9. Although the number of bridge switches is again double that of the normal topologies, the separated power circuit requires only two high frequency switches and one inductor.

The ability to have transformation factors greater than unity does not come free; the semiconductor device ratings are substantially increased over those of the previous topologies. The high frequency

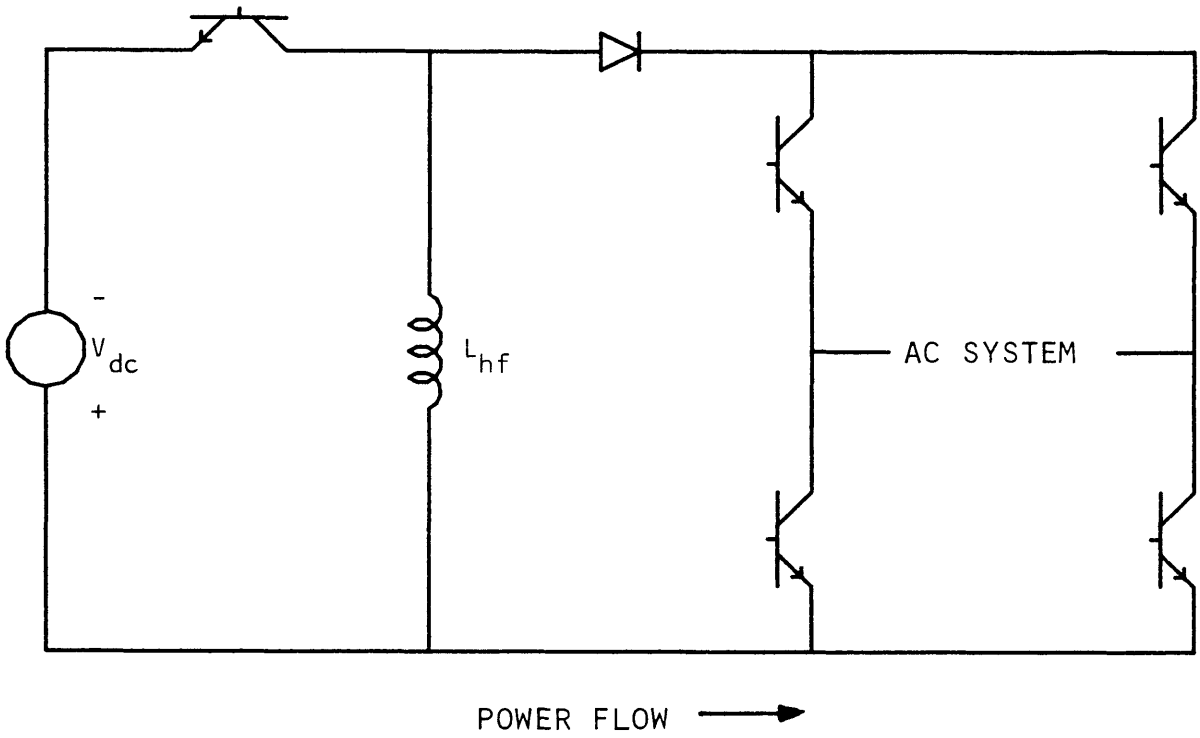


Fig. 4-8: A One Quadrant Waveform Transformer Capable of a Transformation Factor Greater Than Unity.

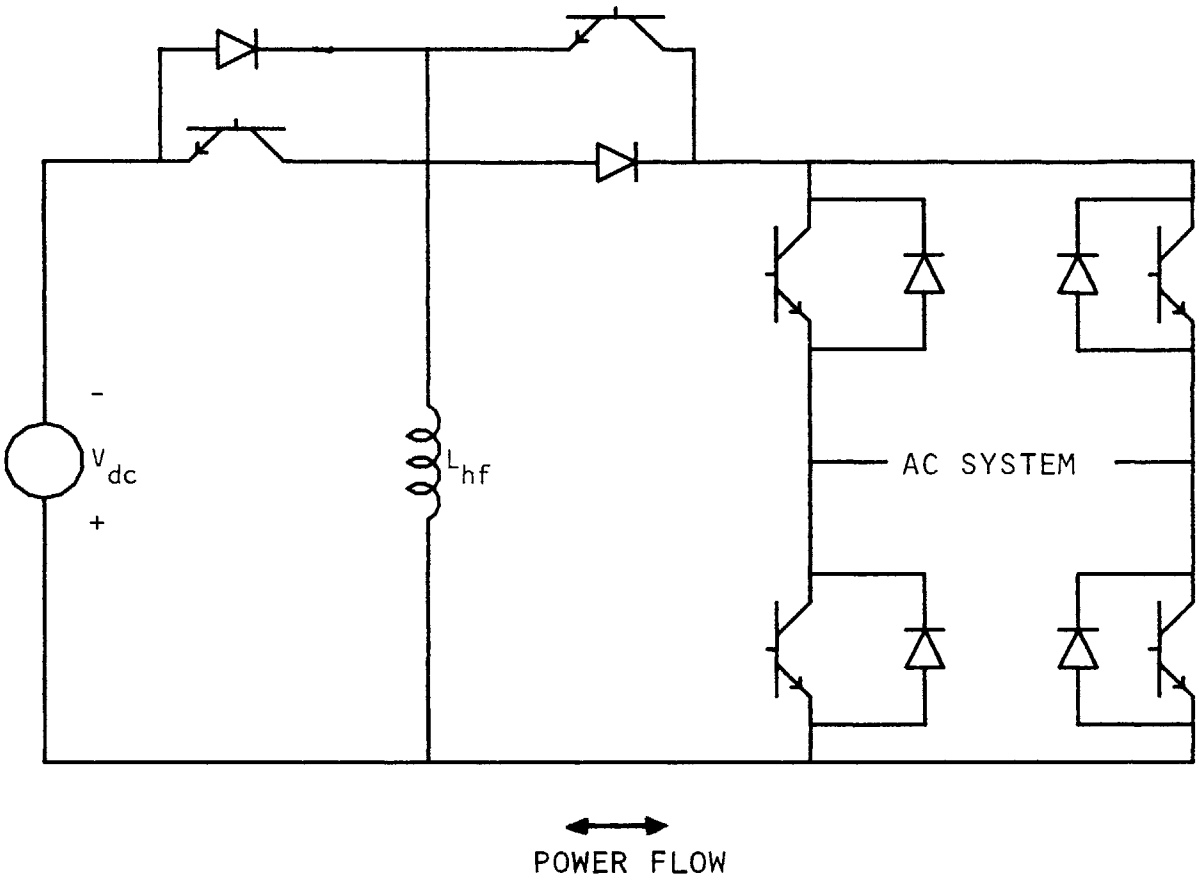


Fig. 4-9: A Two Quadrant Waveform Transformer Capable of a Transformation Factor Greater Than Unity.

switches must now withstand a voltage and carry a current whose values are the sum, instead of the larger, of the corresponding input and output variables. This penalty is so severe that the up/down converter topology should not be used unless it is actually needed.

Electrical Isolation Between the AC and DC Systems

Very often the ideal interface is required to provide electrical isolation between the utility and the dc system. The simplest way to accomplish this isolation is to place a 60 Hz transformer at the utility connection. When the power flow is unidirectional and the functions of the waveform transformer have been separated, it is possible to maintain the original number of bridge switches by using a center-tapped isolation transformer. Figure 4-10 shows how this is done. The center-tapped transformer is less efficient in its use of copper, but the economy, efficiency, and reliability of fewer bridge switches can offset this disadvantage. The center-tapped approach is particularly advantageous when the direction of power flow requires actively controlled bridge switches since it reduces the number of drive systems needed.

It is also possible to achieve electrical isolation with a high frequency transformer. Various topologies can be used; many examples of high frequency links can be found in commercially available switching power supplies. Figure 4-11 shows one approach that incorporates a flyback converter. Because the volt-seconds applied to the isolation transformer in these topologies is much less than that of the 60 Hz utility waveform, the transformer is lighter and cheaper. Its flux

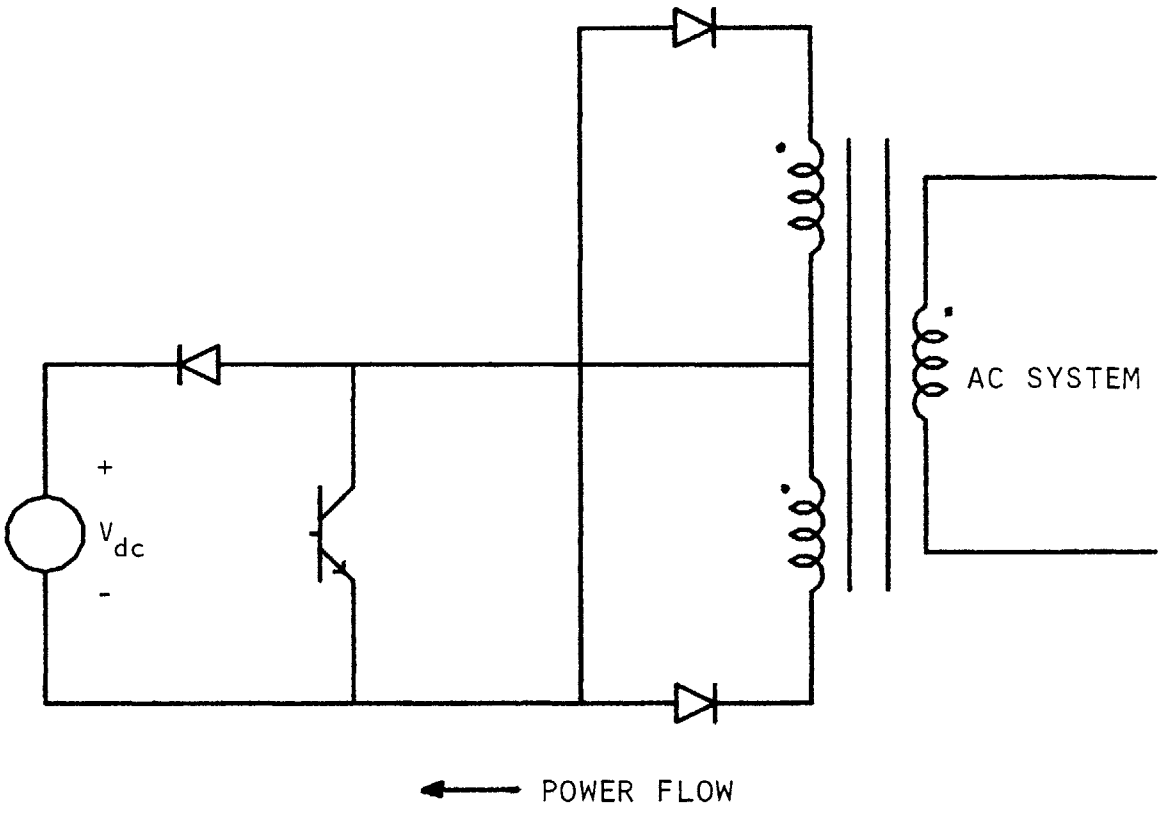


Fig. 4-10: A Separated Waveform Transformer with a 60 Hz Isolation Transformer in the Bridge.

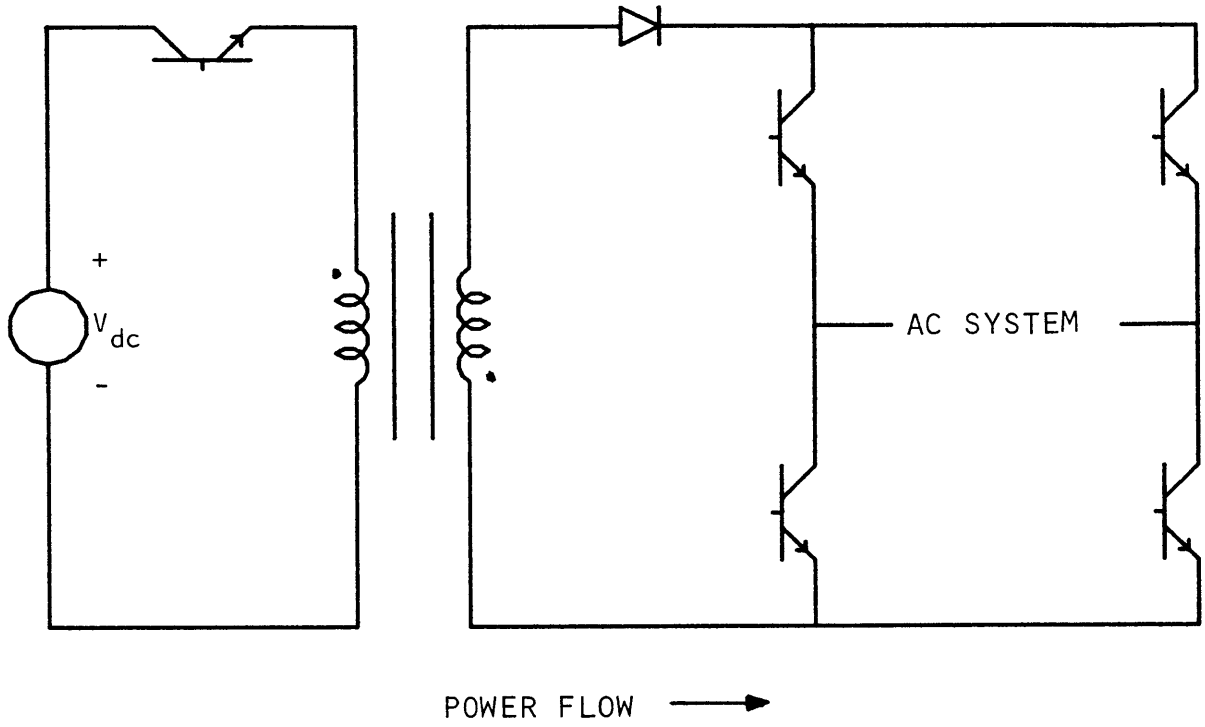


Fig. 4-11: A Waveform Transformer with a High Frequency Isolation Transformer.

varies widely at the switching frequency, however; a laminated iron core cannot be used.

The high frequency isolation transformer's parasitic elements do cause problems with the transitions of the waveshaping switches. The leakage inductance affects the transition at turn-off; the coupling capacitance affects it at turn-on. Transformer designs that reduce one parasitic element cause the other to increase. Turn-on and turn-off snubbers will protect the semiconductor devices, but they are difficult to design because the switch's voltage and current levels vary so greatly. Snubbers that give adequate protection at the peak of the ac waveforms take a very long time to operate near the zero-crossings because the charging voltage and current levels are very small. Efforts must be made to keep the transformer's parasitic elements as small as possible to minimize this problem.

IV.c Load Balancing Filter Elements

The ideal utility/dc interface should deliver distortion free waveforms to both the utility and the dc system. The previous two sections have discussed how this requirement can be met on the ac side, but they have not addressed the waveforms that result on the dc side. The purpose of this section is to do so.

The waveform transformer insures that the utility current will have a fundamental sinusoid shape. The power flowing through the ac port of the interface therefore has a profile composed of two parts: a dc component and a 120 Hz sinusoidal component. Since the waveform transformer does not provide energy storage, the power flowing through

its dc port will have the same profile.

With the characteristic variable contrained to be constant by the dc system, the companion variable at the dc port must therefore have both a dc and a 120 Hz sinusoidal component. If the interface is operating at unity power factor, the magnitude of the 120 Hz component is equal to that of the dc component; if reactive power flows, the 120 Hz component is larger.

A Single Element Filter

To remove the alternating component from the companion variable before it reaches the dc system, a passive filter is needed. If the dc system has the characteristics of a current source, an inductor placed in series with the source could absorb the 120 Hz voltage component. If the dc system is a voltage source, a parallel capacitor could shunt the 120 Hz current component.

If the dc system were actually a perfect current or voltage source, the filter element would not work. The series inductor needs a less than infinite current source impedance and the parallel capacitor must have a greater than zero voltage source impedance. Without these, the passive elements would have nothing to work against and the 120 Hz components would be presented to the dc system. In actual applications this requirement is often met, particularly when the dc system is a passive load. When it is not, such as in the case of a low impedance battery, and the dc system can not handle the large alternating component of the companion variable, the impedance of the source can be adjusted with additional reactive elements.

In most applications of the ideal interface, it is actually the passive filter element that gives the dc system its voltage or current characteristic. Figure 4-12 shows how this happens for a simple resistive load. A series inductor, if large enough, would hold the load's current constant; a parallel capacitor, if large enough, would constrain the voltage. Actually, the characteristic variable of the dc system would only be constant if the element value were infinite. A less than infinite value allows some 120 Hz ripple to occur.

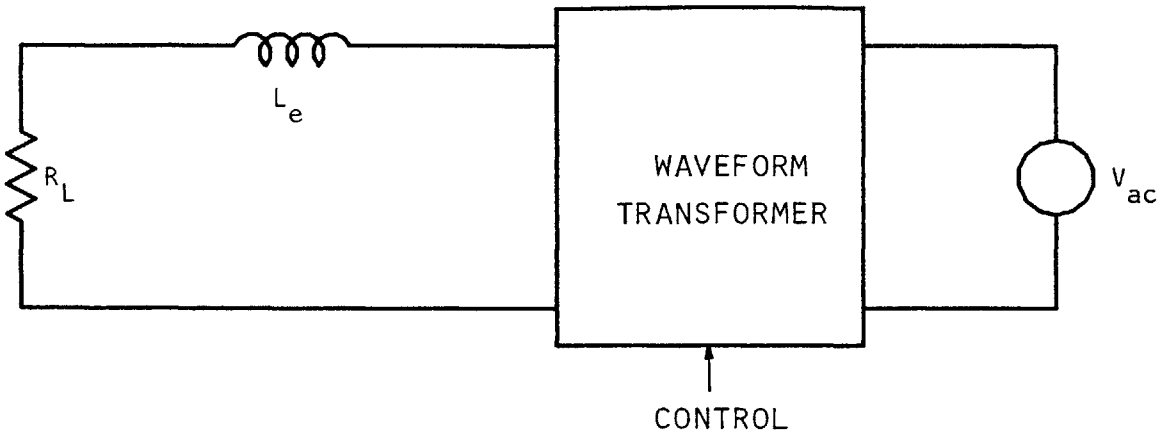
With the filter element in place and designed to make the ripple of the dc system's characteristic and companion variables negligible, there is a mismatch in power flow between the dc and ac systems. This mismatch has a 120 Hz sinusoidal profile and requires a corresponding change in the energy stored within the interface. It is the dc side filter element that supplies this load balancing energy storage.

If load balancing were the only reason for the passive filter element, it would need to store a peak energy no greater than

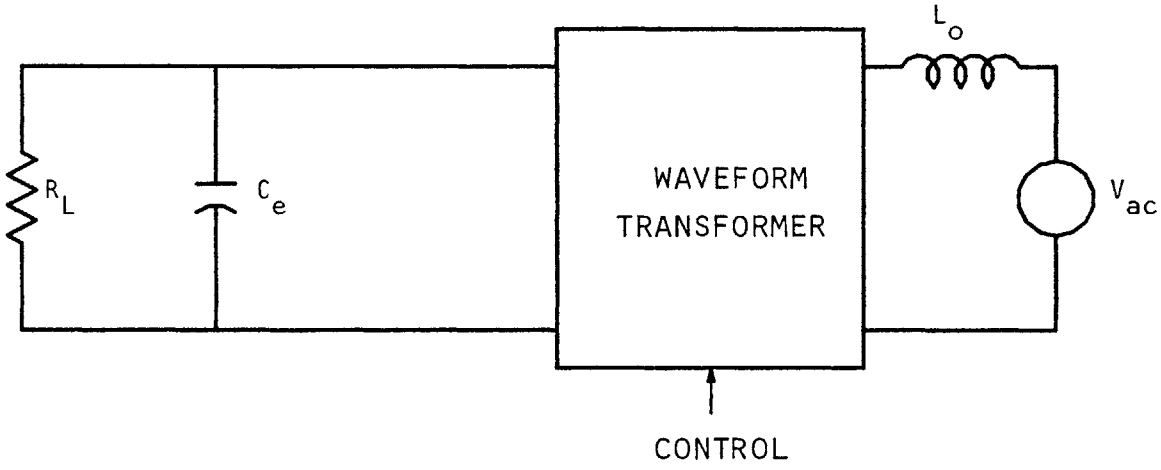
$$E_{P_{max}} = \int_{o}^{\pi/2\omega_o} \frac{P_{dc}}{\cos\phi} \sin 2\omega_o t \, dt = \frac{P_{dc}}{\omega_o \cos\phi} \qquad (4\text{-}1)$$

where ω_o = 377 rad/sec and $\cos\phi$ equals the power factor at the utility interface.

Because the value of the passive element must be chosen to provide the filtering needed, however, the peak energy stored in the passive element is much greater that which would be necessary for load balancing. For example, in the voltage source case, the parallel



a) Current Source



b) Voltage Source

Fig. 4-12: Load Balancing Element Specifies DC Load Characteristic.

capacitor must carry a current of

$$I_C = \frac{I_{dc}}{\cos\phi} \sin 2\omega_o t \tag{4-2}$$

while allowing a peak ripple in its voltage of only V_r. If the ratio between V_r and the dc voltage is defined as $R = V_r/V_{dc}$, the value of the capacitor is

$$C = \frac{I_{dc}}{2\omega_o V_r \cos\phi} = \frac{I_{dc}}{2\omega_o R V_{dc} \cos\phi} \tag{4-3}$$

The peak energy stored by the capacitor is then

$$E_C = \frac{1}{2} C V_P^2 = \frac{1}{2} \left(\frac{I_{dc}}{2\omega_o V_{dc} \cos\phi}\right) V_{dc}^2 [1+R]^2 = \left(\frac{1}{4R}\right)\left(\frac{P_{dc}}{\omega_o \cos\phi}\right)[1+R]^2 \tag{4-4}$$

Similiarly, the peak energy stored by the inductor in the current source case is

$$E_L = \frac{1}{2} \left(\frac{V_{dc}}{2\omega_o I_{dc} \cos\phi}\right) I_{dc}^2 [1+R]^2 = \left(\frac{1}{4R}\right)\left(\frac{P_{dc}}{\omega_o \cos\phi}\right)[1+R]^2 \tag{4-5}$$

The ripple ratio, R, is usually much less than one. The amount of energy storage required in the capacitor or inductor, compared to the minimum needed for power balance, is therefore approximately

$$\frac{E_{actual}}{E_{minimum}} \simeq \frac{1}{4R} \tag{4-6}$$

With a ripple ratio of $R = 2.5\%$, a typical value, the peak energy storage requirement in the passive element is ten times that needed for

load balancing. This high overhead is very costly.

A Resonant Filter Tuned to 120 Hz

The extremely high peak energy storage occurs because the passive element must meet certain impedance needs at 120 Hz and also handle a large dc component in its state variable. The first requirement forces the component value to be large; the second makes the peak of the state variable large, even though the magnitude of its ripple is quite small. Fortunately, the ac waveform that must be filtered contains only one frequency component. The single passive element can be replaced with a resonant circuit that will provide the needed impedance at 120 Hz with a much smaller element value.

Figure 4-13 shows how this is done for the two cases. That element which would be needed if the load balancing filter were not a resonant circuit will be called the primary element. The other component of the resonant filter will be called the secondary element.

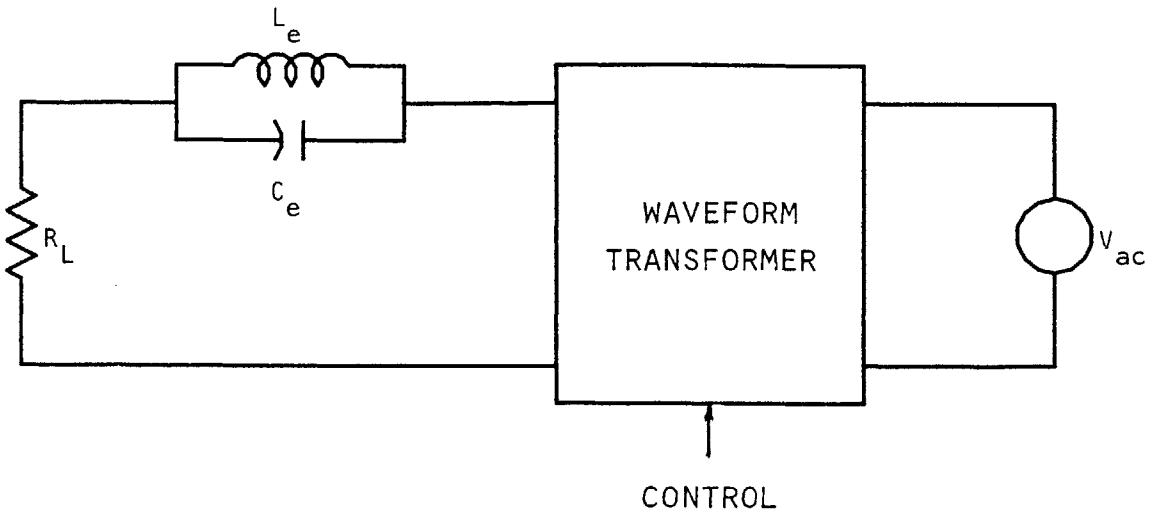
For the voltage source case, the impedance, at the tuned frequency, of a series resonant filter with a given Q is

$$Z = \sqrt{\frac{L}{C}} / Q = \frac{1}{2\omega_o CQ} \tag{4-7}$$

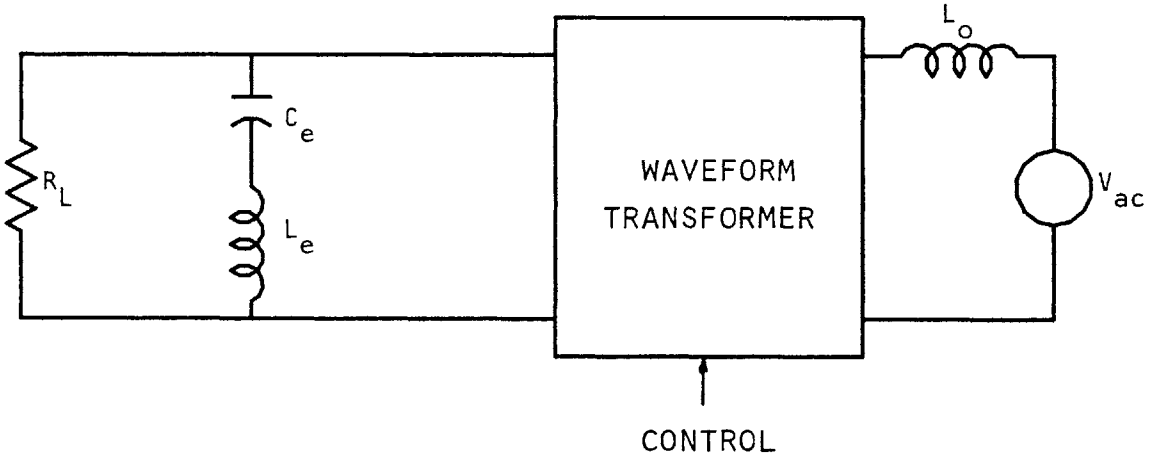
To obtain the desired ripple ratio, this impedance must be

$$Z = \frac{RV_{dc}\cos\phi}{I_{dc}} \tag{4-8}$$

This requires a capacitor value of



a) Current Source Case



b) Voltage Source Case

Fig. 4-13: Load Balancing with a 120 Hz Tuned Filter.

$$C = \frac{I_{dc}}{2\omega_o (QR) V_{dc} \cos\phi} \tag{4-9}$$

and a peak energy storage in the capacitor of

$$E_{C_{peak}} = \frac{1}{2} C \left[V_{dc} + \frac{I_{dc}}{2\omega_o C \cos\phi} \right]^2 = \left(\frac{1}{4QR} \right) \left(\frac{P_{dc}}{\omega_o \cos\phi} \right) [1+QR]^2 \tag{4-10}$$

The peak energy stored in the secondary element, the series inductor, is

$$E_{L_{peak}} = \frac{1}{2} \left(\frac{1}{4\omega_o^2 C} \right) \left(\frac{I_{dc}}{\cos\phi} \right)^2 = \left(\frac{QR}{4} \right) \left(\frac{P_{dc}}{\omega_o \cos\phi} \right) \tag{4-11}$$

For the current source case, the energy storage requirements of the inductor and capacitor are reversed.

For both cases, the ratio between the peak energy stored in the primary element and the energy required just for load balancing is now

$$\frac{E_{actual}}{E_{minimum}} = \frac{[1+QR]^2}{4QR} \tag{4-12}$$

This function is graphed in Figure 4-14.

The ripple in the primary element of the resonant circuit is Q times larger than what appears to the dc system. Therefore, when the (QR) product is equal to one, the energy stored in the element just reaches zero at its lowest point. Under this condition, the peak energy storage is exactly the minimum level required for load balancing. As the graph shows, when Q is increased towards this optimum value, the incremental returns diminish. Even when a (QR) product of one can not

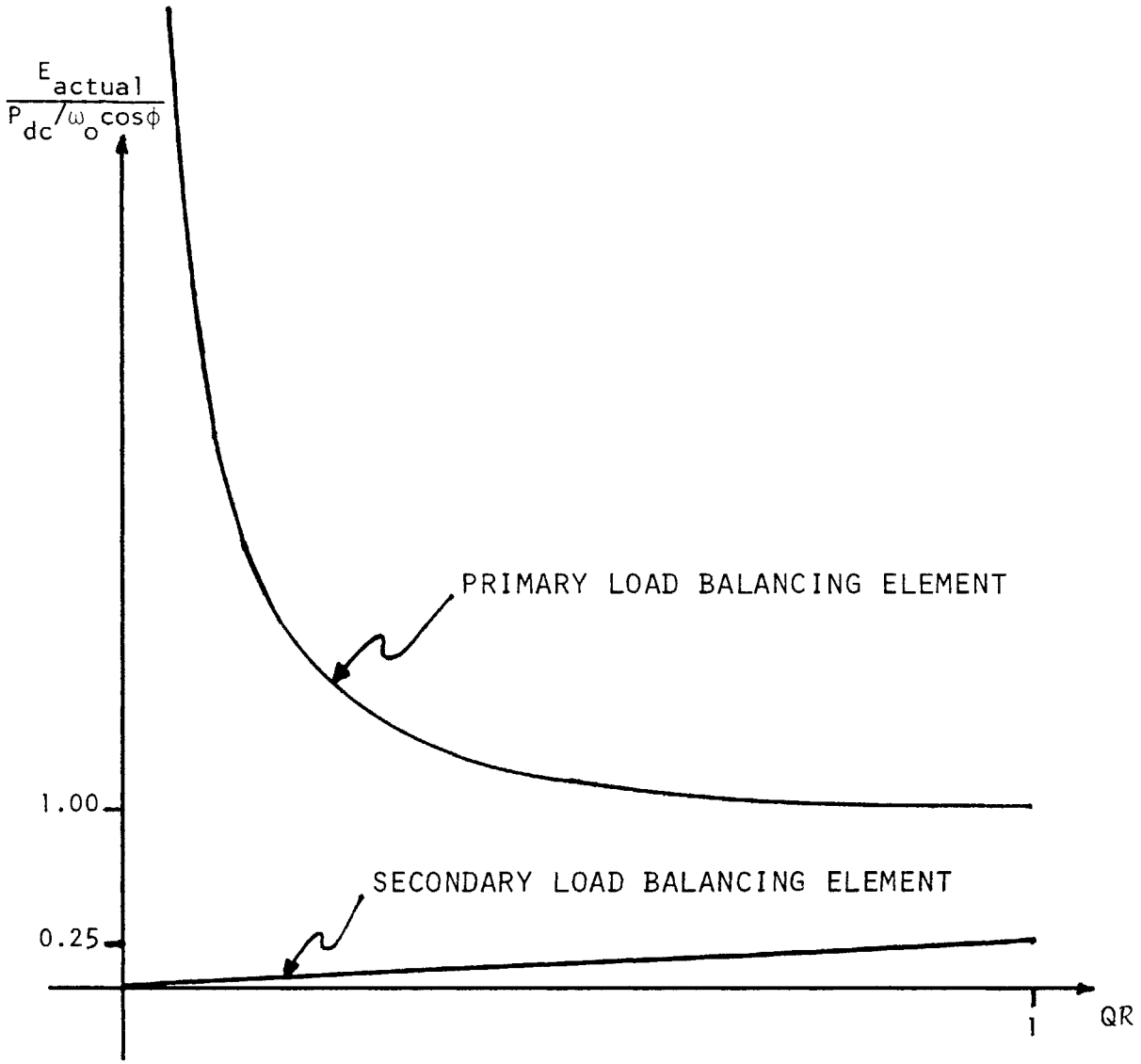


Fig. 4-14: Peak Energy Storage Requirements of the Load Balancing Elements.

be obtained because the Q would be too high, much of the benefits can still be realized with a more modest value.

Equation 4-12 does not account for all the energy storage of the tuned filter; the secondary storage element must also be considered. Its peak energy storage requirements, as a fraction of that required for load balancing, is also graphed in Figure 4-14. The storage requirement of this element is very small compared to the primary element, although it does get larger as the (QR) product increases. In no way does it counteract the benefits of using a resonant filter, but it may affect how large a (QR) product is beneficial.

If the sum of the peak energy requirements for the two elements is to be minimized, the optimum value for (QR) is

$$QR = 1/\sqrt{2} = 0.707 \qquad (4\text{-}13)$$

All ac-dc interface power circuits contain filters to reduce the ripple in the dc system. All could benefit from the use of resonant filters. But only by providing ideal waveforms to both the ac and dc systems will the filter be required to work at a single frequency. A power circuit that injects a distorted current into the utility would require a resonant filter at each harmonic of 120 Hz. The design and tuning of such a multiple resonant filter is so complicated that it is not normally used. The simplification provided by the ideal interface is a great advantage; the resonant filter is much more feasible. The reduced size, cost, and weight of the passive elements can significantly compensate for the cost of the high frequency semiconductor devices.

IV.d Waveshaping Filter Elements

The waveform transformer produces stepped waveforms on both its ac and dc sides. For the voltage source case, the dc side current and the ac side voltage are discontinuous; for the current source case, the dc side voltage and the ac side current are discontinuous. These switching frequency components must be filtered from the waveforms.

AC-Side Switch Frequency Filters

For the voltage source case, the high frequency voltage at the output of the waveform transformer can be effectively filtered by the interconnecting inductor. The size of this inductor must only be made large enough to keep the resulting current ripple below a tolerable level. Any inductive impedance present in the utility system at the switching frequency helps to further reduce the ripple.

If the utility system has an impedance comparable to that of the interconnecting inductor, however, then a significant fraction of the waveform transformer's high frequency voltage will appear at the utility's terminals. Customers connected to these same terminals may experience detrimental effects due to this substantial voltage distortion. The problem can be avoided by placing a shunt capacitor across the utility. This capacitor provides a shunt path for the switch frequency ripple currents so they do not have to flow through the impedance of the utility. Such a design for the high frequency filter, because it is second order, also allows a much smaller interconnecting inductor than would otherwise be needed to reduce the ripple to the desired level.

The discontinuous current on the ac side of the waveform transformer in the current source case can not be tolerated; the high frequency distortion is too great. Instead, a capacitor must be installed across the output of the waveform transformer to shunt this current. The capacitor will only be effective if the impedance looking toward the utility is great enough, however. If the inherent impedance of the system does not suffice, an additional series inductor must be added.

When the waveform transformer for the current source case is implemented with separate waveshaping and bridge functions, at least the capacitor of the ac side filter must be installed between the high frequency switches and the bridge. The inductor may be left on either side. If this design were not used, the bridge switches would be required to carry discontinuous currents and low frequency semiconductor devices could not be used. The purpose of the separation would therefore be defeated.

Even for the voltage source case there are advantages to the placement of the filter elements on the dc side of the bridge. The first is that the interconnecting inductor, whose current must be sensed, and the actively controlled high frequency switch, whose third terminal must be driven, would have a common electrical connection. This common node can simplify the design of the control circuit. The second is that the capacitor, if used, will only be subjected to a single polarity voltage.

Unfortunately, the placement of filter components on the dc side of the bridge causes a problem. The 60 Hz reactive requirements of the

filter elements must be supplied through either the bridge or the high frequency switches, but both are only capable of unidirectional power flow. Since the reactive requirements are usually small compared to the level of power flowing through the interface, there is no problem for most of the cycle. The needs of the filter can be supplied by an imbalance between the power flowing through the bridge and through the high frequency switches. Near the zero-crossings, this imbalance will eventually require that the power flowing through either the bridge or the high frequency switches reverse, however. Since neither is possible, a disturbance results. The ac current can not be perfectly shaped at these points in the cycle.

DC-Side Switch Frequency Filters

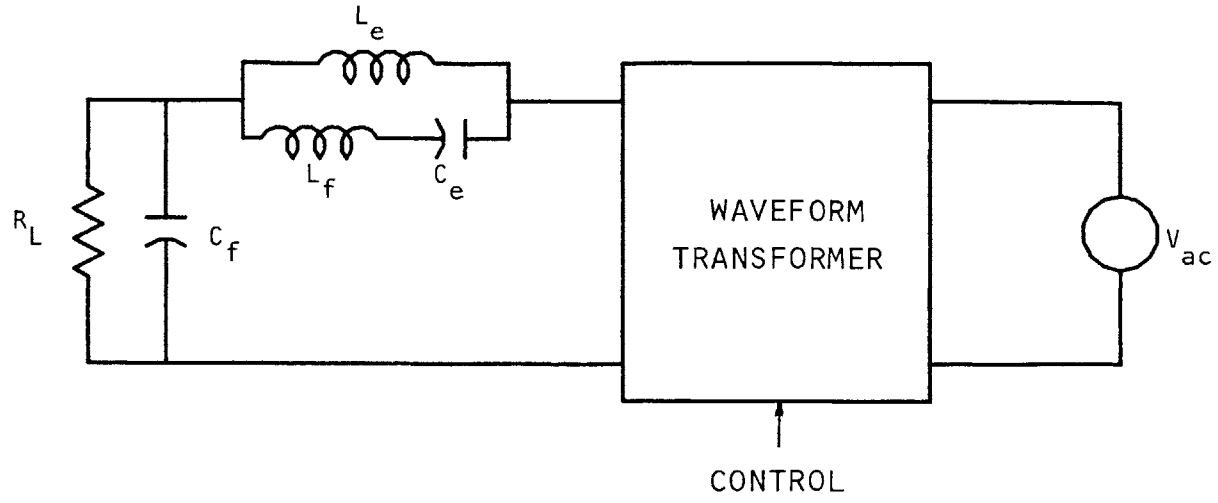
When a single passive element is used for load balancing filter, this element will also provide the high frequency filtering on the dc side of the waveform transformer. The series inductor of the current source case will withstand the high frequency voltage components and the parallel capacitor of the voltage source case will carry the high frequency currents. The value of the filter element is more than large enough to provide the high frequency filtering required.

Care must be taken to insure the load balancing filter inductor or capacitor can handle the high frequency components, however. Even though the switch frequency components of its voltage are large, the filter inductor of the current source case is usually able to handle them. The resulting changes in its flux level are too small to cause significant losses. The capacitor of the voltage source case, on the

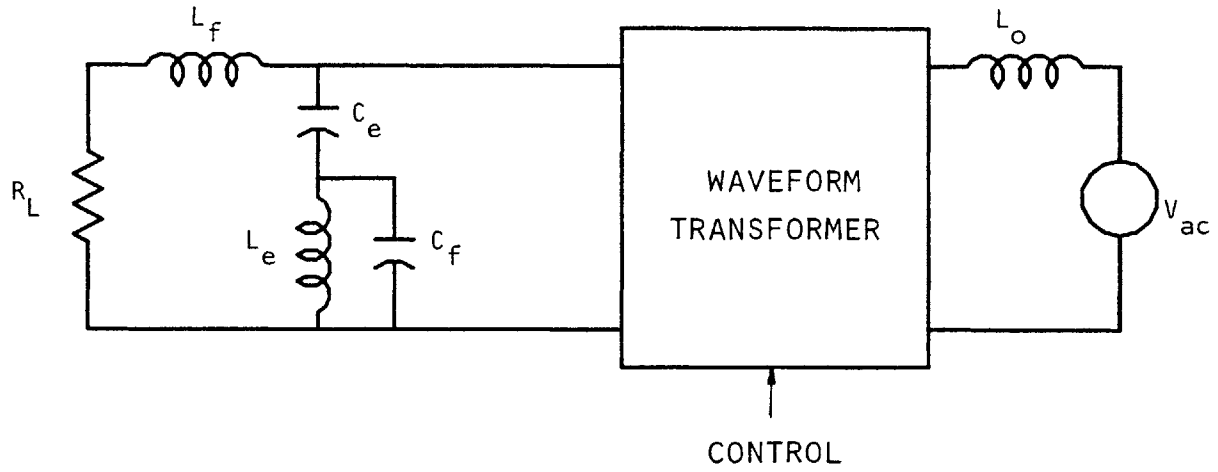
other hand, will have problems if it is not specifically designed to carry the large high frequency currents.

If a resonant filter is used for load balancing energy storage, it will not provide filtering at the switch frequency. The capacitor forms a short circuit around the inductor in the current source case and the inductor forms an infinite impedance in series with the capacitor in the voltage source case. The load balancing filter elements can no longer provide filtering at the switch frequency. Additional filter elements must therefore be added. A single filter element may be used if the impedance of the dc system will contribute to the filtering effect. If it does not, a second order filter will be needed. Either way, a second order filter will require smaller components.

Figure 4-15 shows how the dc side filter should be implemented. Notice that one element is placed in the load balancing resonant filter. There are two reasons for this placement. First, the element is not subjected to the dc variable; the peak value of its state variable is determined solely by the level of ripple in the resonant circuit. As long as the $(Q\,R)$ product is less than one, the peak energy requirement for an element placed in this position is therefore less than it would otherwise be. Second, the addition of the high frequency filter element in the resonant circuit reduces the value of the secondary load balancing filter element. The two elements combine to give an effectively larger secondary load balancing element than is actually used; its size and cost are therefore reduced.



a) Current Source Case



b) Voltage Source Case

Fig. 4-15: High Frequency Filter for the DC System.

IVe. Three-Phase Implementation

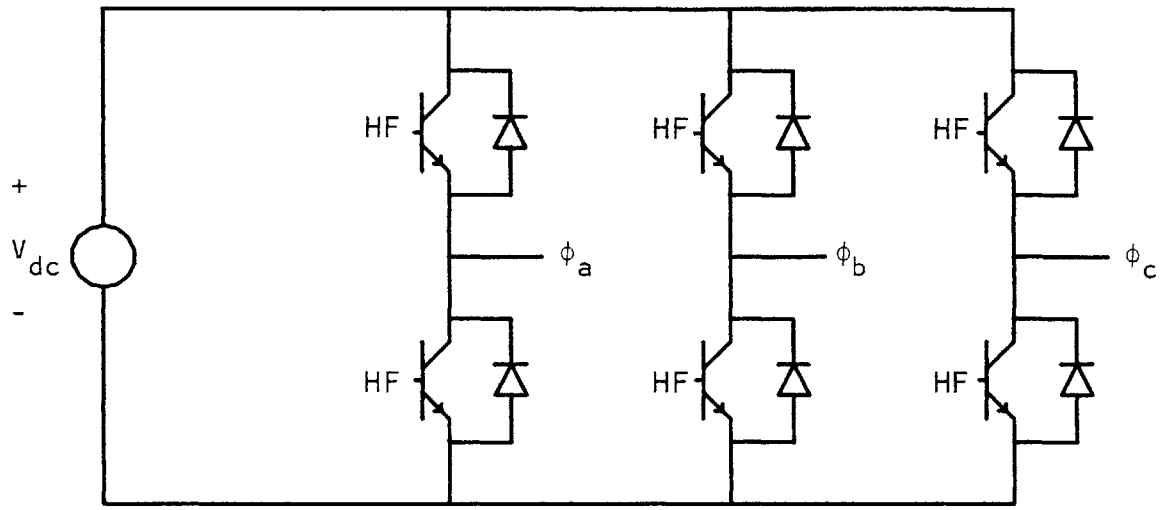
Many conditioned loads in the medum-power range have three-phase service available. The design of an active ideal interface for these applications can be simpler and cheaper per unit power than it is for the single-phase case.

Figure 4-16 shows how a three-phase waveform transformer with bidirectional power flow would be implemented for both the current source and voltage source case. Only high frequency switches are needed; the bridge function for each phase is provided by the switches of the other two phases. The power capability of the transformer is three times as great as a single-phase unit using the same semiconductor devices, but its cost is not similarly increased.

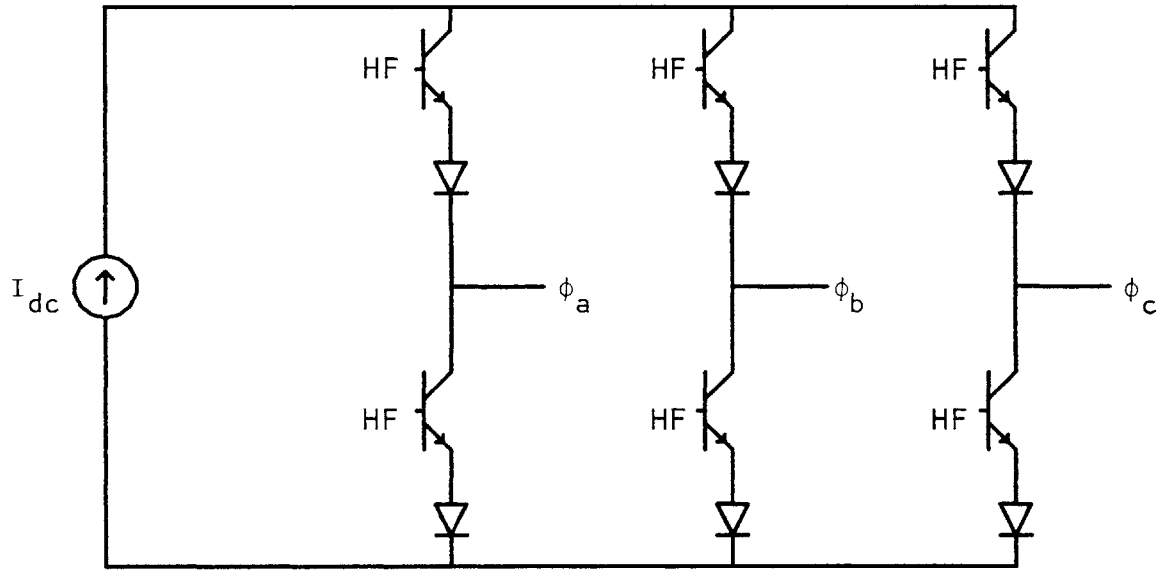
When the power flow is unidirectional, the separation approach can again be followed to halve the number of high frequency switches, but the benefits of doing so are not as great as they are for the single-phase case. Each phase could no longer share its bridge function with the other phases. Instead, four bridge switches would be needed for each phase. The implementations, as shown in Figure 4-17, require three single-phase waveform transformers connected either in series or in parallel, depending on the characteristic of the dc system.

A very important advantage of three-phase operation is that the instantaneous power flowing from the utility is always constant. There is no imbalance between power delivered and power consumed; load balancing energy storage is therefore not required.

If load balancing filter elements are not used but there are imbalances among the utility's three voltages, it is important to make

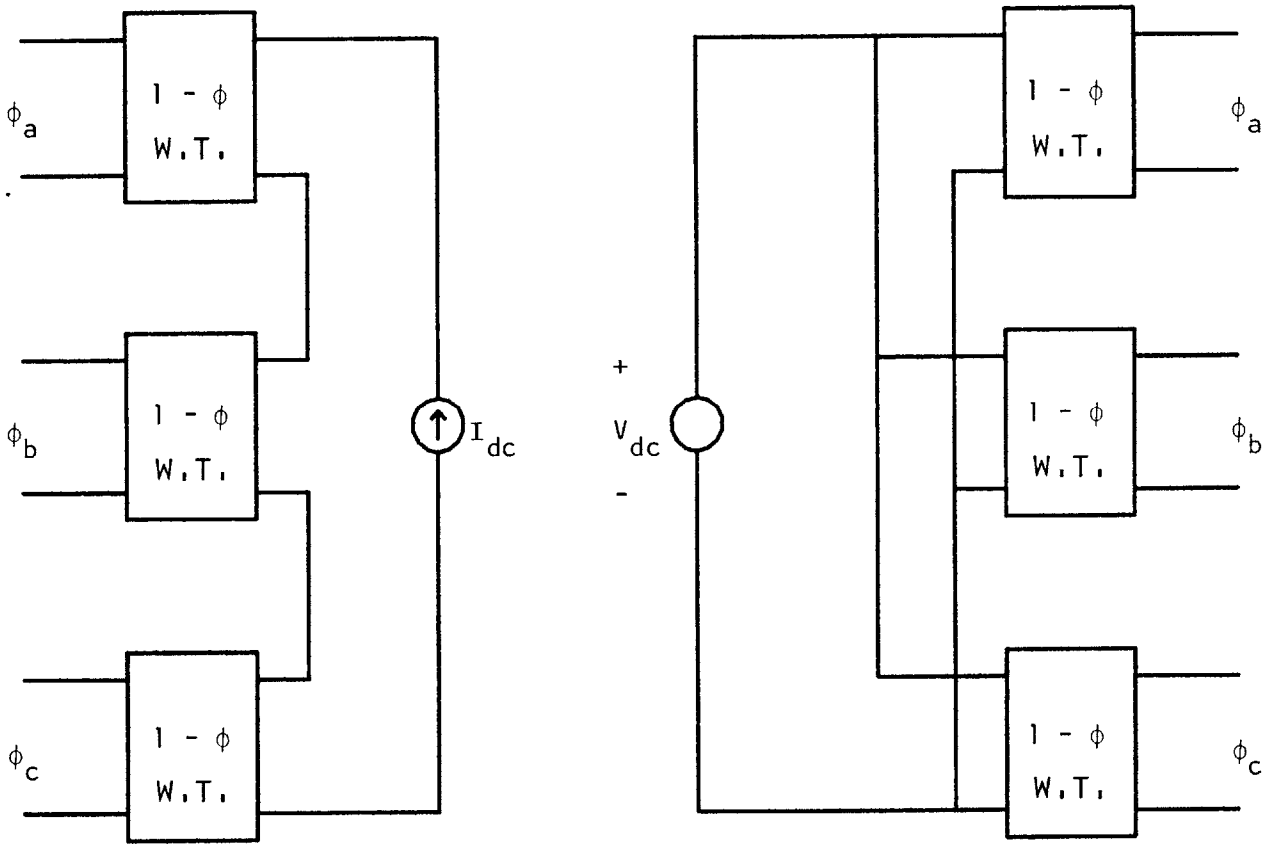


a) Voltage Source Case



b) Current Source Case

Fig. 4-16: Waveform Transformer for Three-Phase Bidirectional Power Flow.



a) Current Source Case

b) Voltage Source Case

Fig. 4-17: Ideal Interface for Three-Phase Unidirectional Power Flow.

sure the individual phase currents are adjusted to make the power for each phase the same. If this power balance can not be maintained exactly, a small amount of load balancing energy storage may be required.

The lack of a load balancing energy storage element leaves the characteristics of many dc systems undefined. A resistive load could be used in either a voltage source or current source topology. In either case, it is the design of the waveform transformer and the dc side switch frequency filter that actually provide the definition. Since the switch frequency filter elements are very small, they will not be able to hold the characteristic variable of the dc system constant for long if the three phases are not perfectly balanced. The control circuit must therefore counteract any imbalances that occur. The slower the response of the control circuit, the larger the passive elements will have to be.

CHAPTER V

CONTROL OF AN ACTIVE UTILITY/DC INTERFACE

The ideal interface described in the last chapter needs a control system to determine the correct instants at which the switch transitions should take place. This control system is responsible for both the sinusoidal shape of the ac current waveform and the level of power flow. There are several approaches to its implementation, although certain features are dictated by the topology of the power circuit. Some options result in a very simple control circuit; others are more complicated. Each approach has its advantages.

The following sections of this chapter discuss the various aspects of the control system for an ideal interface. The shaping of the ac current waveform is considered first. The domains of applicability of open-loop control and of closed-loop control are examined. For each approach, various control techniques are presented, developed, and compared. Examples and simulation results are included.

The production of the sinusoidal reference waveform and the control of the interface's power level will then be discussed. Although control of power is intimately tied to the waveshaping function, its distinct dynamic response has important implications.

Finally, the interaction among multiple control systems, a potential problem in three-phase applications or where power circuits have been paralleled, will be reviewed.

V.a Open-Loop Control of the AC Current Waveform

When the dc system has the characteristics of a current source, the ac current waveform can be shaped with an open-loop control system. The percentage of time during which each of the waveform transformer's high frequency switches carries the dc current directly determines the current on the ac side. To achieve the ac waveform desired, the relative conduction periods (or, in other words, the "instantaneous" duty cycle) should simply follow a 60 Hz, sinusoidal function of time.

Figure 5-1 shows how easily this control scheme can be implemented. A reference sinusoid with a frequency of 60 Hz is generated to indicate the desired magnitude of the ac current at any given instant. This waveform is compared with a triangle waveform at the switch frequency. The digital output of the comparator represents the percentage of time, or duty cycle, during which the dc current source should be connected to the ac system. Given a certain dc current level, the peak value of the ac current is determined by the relative amplitudes of the reference and triangle waveforms. The polarity of the reference waveform governs which bridge switches should be conducting during each half cycle.

Waveform Imperfection Due to Switch Transition Delays

For this control scheme to work correctly, the transition times of the high frequency switches must not alter the actual duty cycle from that determined by the control circuit. Delays in the drive circuit, the removal of stored charge in the semiconductor device, and commutation periods can all have an appreciable effect on the actual conduction period obtained, however. When these occur, the ac current

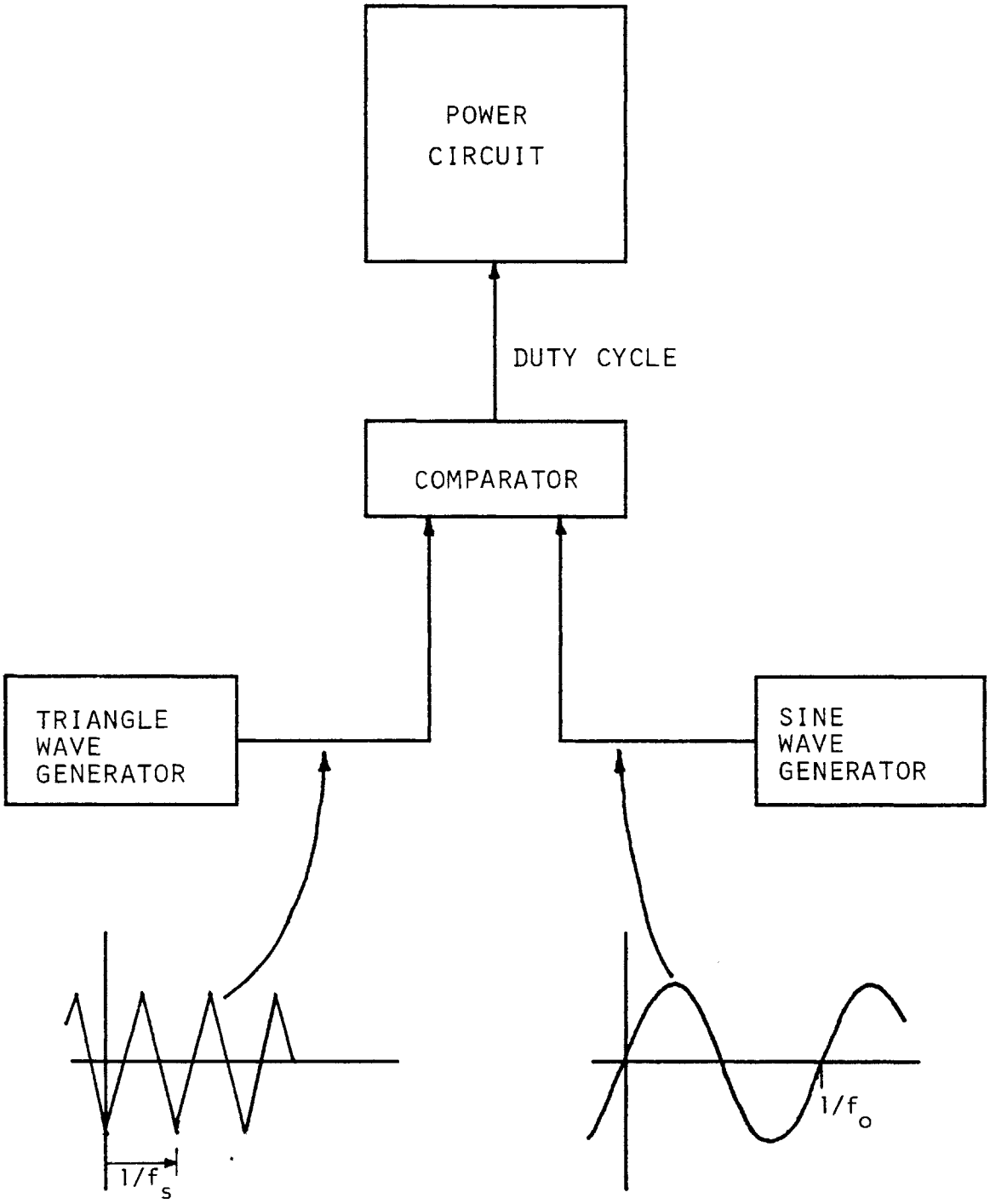


Fig. 5-1: Simple Control Circuit for Open-Loop Control Scheme.

waveform will not be perfectly shaped.

It is possible to compensate for the discrepancy between the duty cycle desired and the duty cycle actually obtained. The waveform of the control signal can be lengthened or shortened to reflect the unsymmetrical delays of the turn-on and turn-off transitions. Duty cycles less than the minimum or greater than the maximum obtainable at the nominal switch frequency can be achieved by lowering the frequency. These corrective measures require a more sophisticated control circuit than the one presented in Figure 5-1, but a microprocessor based system can accomplish the task with little difficulty.

Waveform Imperfection Due to DC Current Ripple

With a corrected duty cycle applied to the waveform transformer, the ac current is again the product of a 60 Hz sinusoid and the current flowing through the dc system. If the dc system's current is purely dc, the ac current waveform should have no distortion other than a small amount of switch frequency ripple that gets through the high frequency filter. There is usually some 120 Hz ripple in the dc current, however. The multiplication of this ripple by a fundamental sinusoid adds two components to the ac current waveform: one at the fundamental and the other at the third harmonic. Both have a magnitude equal to one half the peak of the 120 Hz ripple. Since these components supple reactive, rather that real, energy to the load balancing filter and the dc system, the additional 60 Hz current always has a 90 degree phase shift with respect to the utility voltage.

Waveform Imperfection Due to the AC-Side FIlter

The ac side of the waveform transformer in the current source case requires an L-C low-pass filter to remove the high frequency components from the ac current waveform. As explained in the last chapter, for those waveform transformers that have separate waveshaping and bridge functions, the reactive requirements of the L-C filter can not be supplied near the zero-crossings. Instead, disturbances occur.

These disturbances distort the ac current in two ways. The first is cross-over distortion; the ac current will have a zero value for a prolonged period. The second is oscillation currents; the L-C filter will respond to the disturbance by ringing for some part of the 60 Hz cycle.

There is very little dissipation to dampen the oscillation of the ac side filter. Because the utility is essentially a stiff voltage source, it does not provide the necessary losses. Neither do the impedances on the dc side of the waveform transformer. Although these impedances are reflected to the ac side, their values are first multiplied by a ratio equal to the square of the inverse of the waveform transformation factor. Since this transformation factor is near zero at the location of the disturbance, the impedance placed in parallel with the filter capacitor is too large to provide substantial damping. Only the semiconductor switches and the resistance in the filter elements provide losses for damping the oscillations.

With an open-loop control system, it is not possible to dampen the filter oscillations with feedback techniques; the energy in the oscillations must be dissipated. As shown in Figure 5-2, there are four

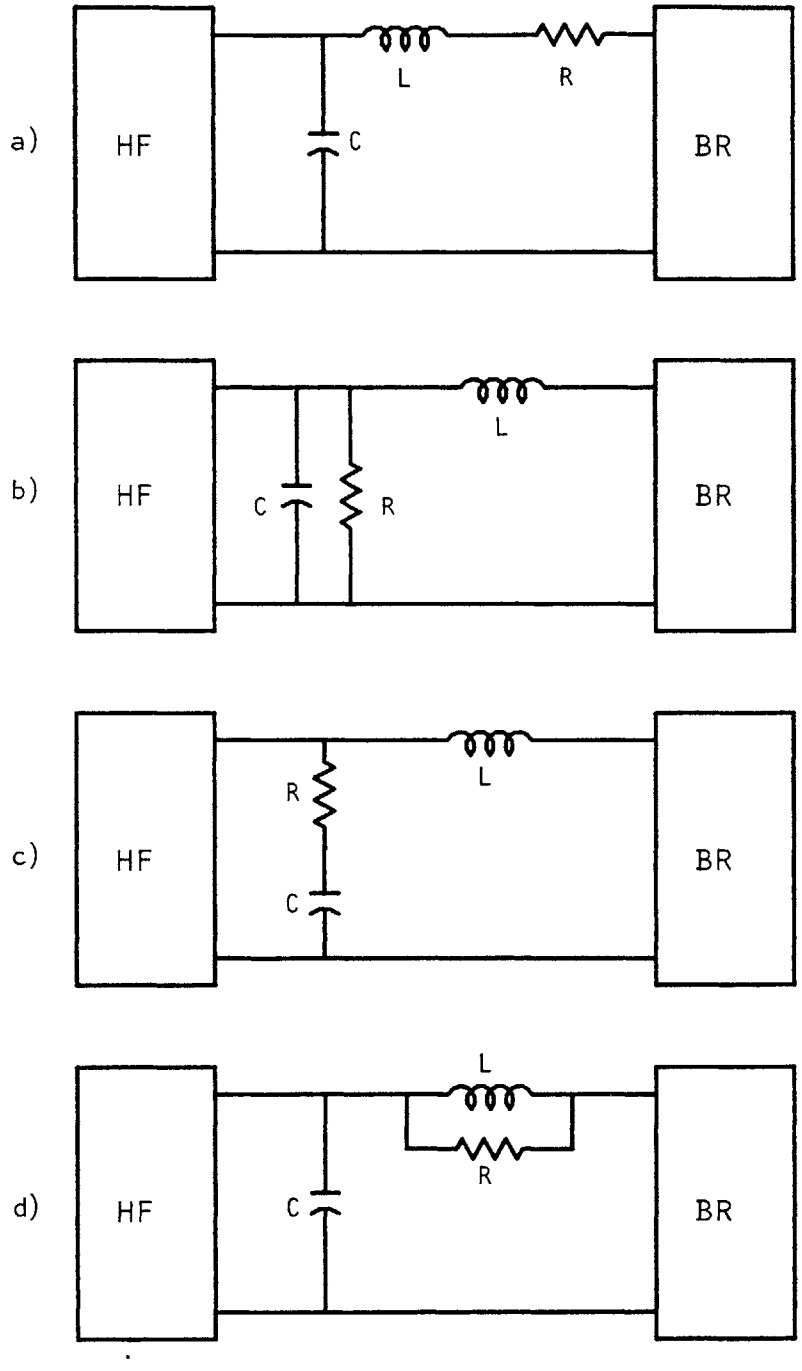


Fig. 5-2: Possible Positions for the Damping Resistor.

possible positions for a damping resistor. Two positions: in series with the inductor and in parallel with the capacitor, cannot be used. The 60 Hz waveforms cause intolerable levels of power dissipation. A resistor in series with the capacitor is also not desirable since it must carry the high frequency currents. These currents will cause the resistor to dissipate a great deal of energy and increase the voltage stress placed on the semiconductor devices. For these reasons, the best place to put the damping resistor is in parallel with the inductor. Although the resistor will reduce the effectiveness of the filter, the component values can be chosen to overcome this effect.

Figure 5-2d shows the recommended topology for the L-R-C filter. The damping ratio and the effectiveness of this filter are closely related. The damping ratio is

$$\xi = \frac{1}{2}\frac{1}{R}\sqrt{\frac{L}{C}} = \frac{1}{2\omega_f RC} \tag{5-1}$$

where ω_f is the frequency at which the filter is tuned. With a useful level of damping, the ratio of the filter's input to output current at the switching frequency is

$$\left|\frac{I_{out}}{I_{in}}\right| = \left|\frac{S\,L/R + 1}{S^2 LC + S\,L/R + 1}\right| \simeq \frac{1}{\omega_s RC} \tag{5-2}$$

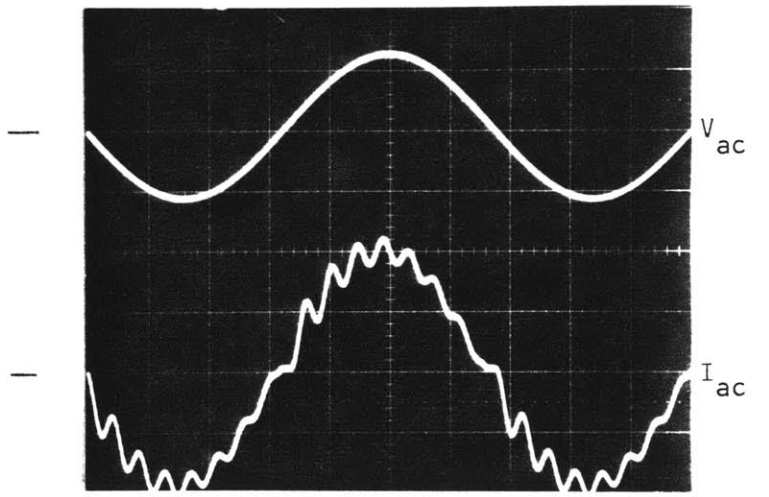
where ω_s is the switching frequency. As can be seen, for a given filter performance, the damping can only be increased by lowering the filter's tuned frequency. The relative values of the inductor and the capacitor do not have an effect on the damping achieved.

Figures 5-3a and 5-3b show simulation results of a typical filter inductor's current for two different values of damping ratios. The damping in the first figure is very small; the oscillations are present for a substantial part of the cycle. This waveform indicates the type of problem that will result if the filter is not damped. In the second figure, the damping is more substantial. With a damping ratio of 0.2 and the same natural frequency of the previous example, the oscillations are now gone within one millisecond.

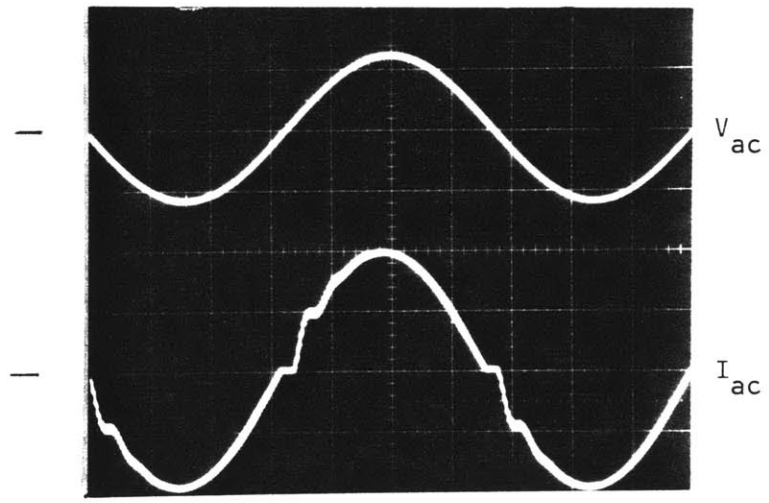
As the characteristic impedance of the filter is increased, the magnitude of the disturbance in the ac current is decreased. For a given damping ratio and tuned frequency, it is therefore desirable to make the filter inductor as large as possible and the capacitor as small as possible. Figure 5-4 shows how the filter inductor's current differs for two nominal values of characteristic filter impedance. The resonant frequency and the damping ratio are the same in both cases.

The inductor cannot be made arbitrarily large, however. As its value is increased, its reactive requirements become larger and the cross-over distortion increases. A larger inductor is also more expensive and has greater losses.

The oscillations in the ac current waveform can be controlled, but only by making tradeoffs. Either the effectiveness of the filter must be sacrificed, or larger, more expensive elements must be used. Although it is important to make sure the oscillations are not too large, it is not necessary to eliminate them entirely. The oscillations shown in Figure 5-4 present more of an aesthetic problem than a distortion problem. The magnitudes of the harmonic components in the

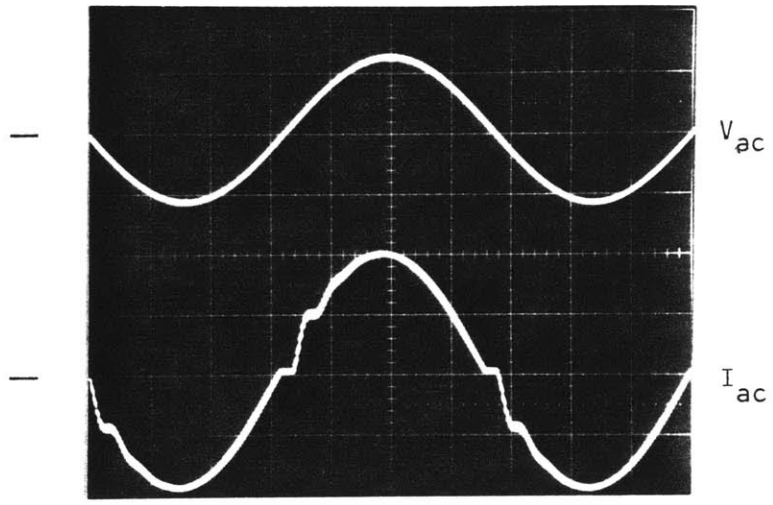


a) No Damping ($\xi = 0.02$; $\sqrt{L/C} = 0.55$ pu; $\frac{1}{2\pi\sqrt{LC}} = 1$ kHz)

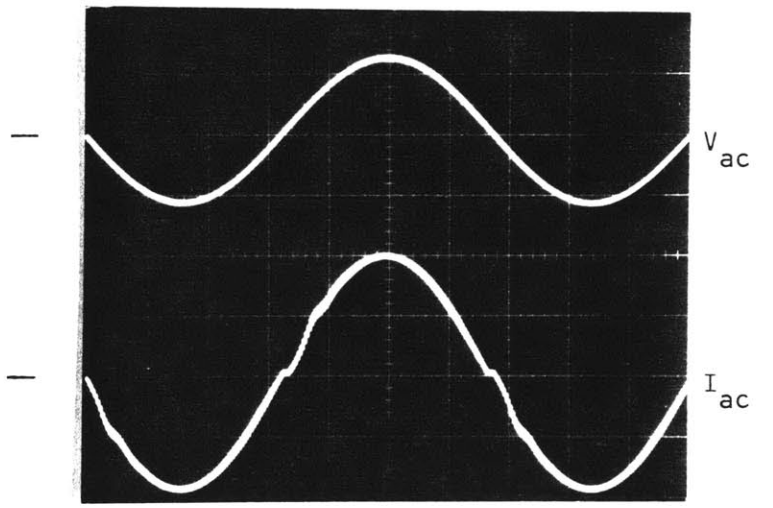


b) Moderate Damping ($\xi = 0.2$; $\sqrt{L/C} = 0.55$ pu; $\frac{1}{2\pi\sqrt{LC}} = 1$ kHz)

Fig. 5-3: Oscillations Caused by the AC Filter: Change of Damping.



a) Low Impedance ($\sqrt{L/C} = 0.55$ pu; $\xi = 0.2$; $\frac{1}{2\pi\sqrt{LC}} = 1$ kHz)



b) Moderate Impedance ($\sqrt{L/C} = 2.2$ pu; $\xi = 0.2$; $\frac{1}{2\pi\sqrt{LC}} = 1$ kHz)

Fig. 5-4: Oscillations Caused by the AC Filter: Change of Characteristic Impedance.

vicinity of the ringing frequency are only about one percent. It is important not to become too concerned with removing all of the oscillation; the cost of doing so is not worth the benefits gained.

V.b Closed-Loop Control of the AC Current Waveform

When the dc system has the characteristic of a voltage source, the ac current waveform is shaped by controlling the voltage across the interconnecting inductor. The more accurately this voltage can be controlled, the smaller the inductor can be. The waveform transformers described in the last chapter can control this voltage with sufficient bandwidth and resolution for the inductor to be no bigger than that required for the high frequency filtering. When the inductor is this small, the power circuit cannot be controlled in an open-loop manner. Feedback must be used to give the correct ac current waveform.

Closed-loop control has both advantages and disadvantages over open-loop control. The primary advantage is the ability, in some schemes, to eliminate the filter oscillations without the side-effects of a dissipation resistor. The disadvantage is that sensors are required for the feedback variables. These sensors can be complicated and costly, particularly if electrical isolation is required.

There are several closed-loop schemes that can be employed. This section will present and discuss some of these.

Synchronous Control

The first control scheme, shown in Figure 5-5, is similiar to that

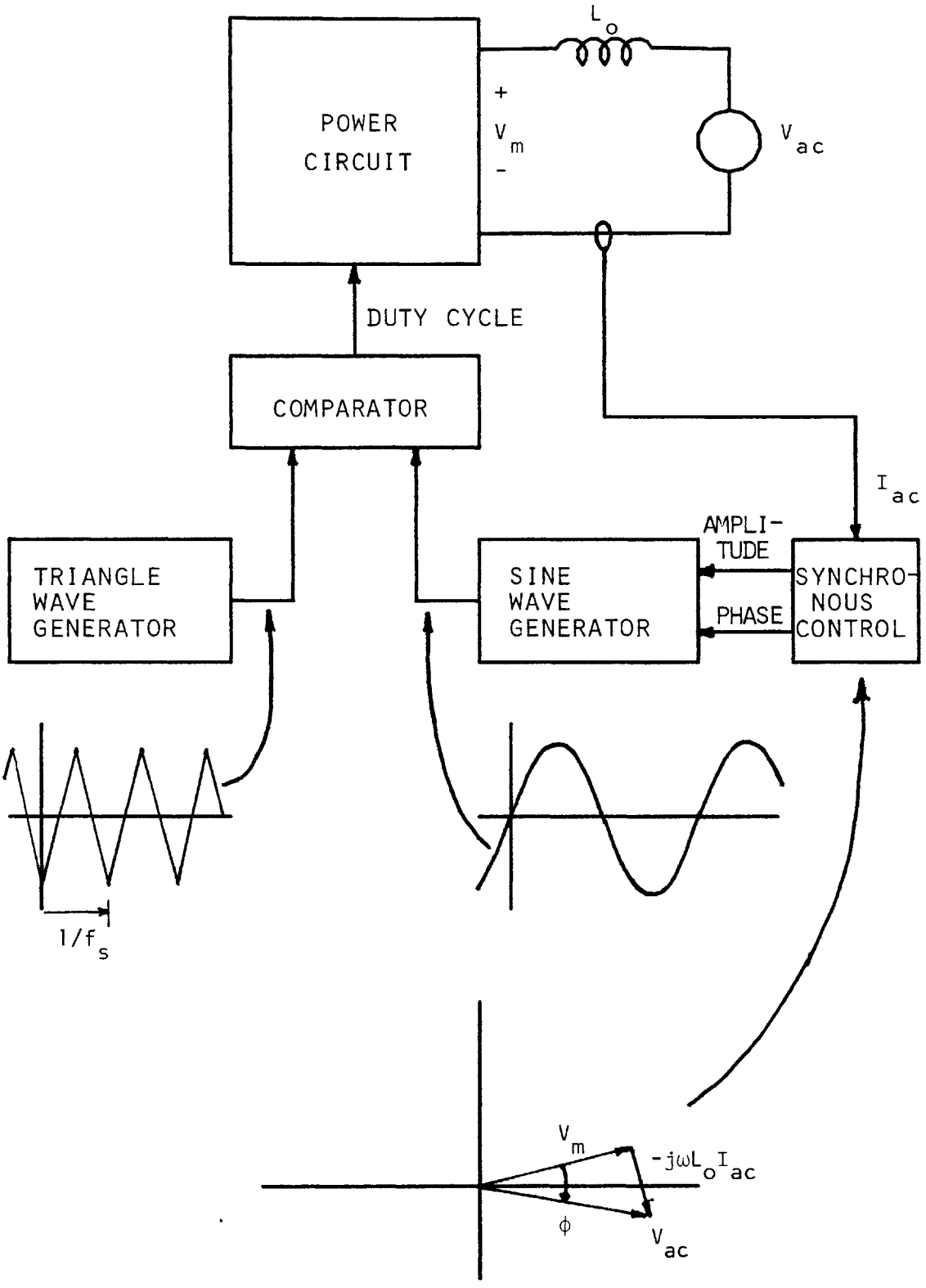


Fig. 5-5: Synchronous Control Scheme.

used by a synchronous generator. The control circuit is designed to provide a duty cycle that follows a sinusoidal reference waveform, just as was done for the current source case described above. The waveform transformer's output is now a controlled voltage source, however. Efforts must again be made to ensure that this ac voltage waveform will be an accurate replica of the reference. The reference waveform can then be adjusted in a closed-loop manner to give the ac current flowing through the interconnecting inductor the magnitude and phase desired.

This control scheme is a very familiar one and there is a great deal of experience on which to base its implementation. There are two important differences between an ideal interface and a synchronous generator, however. First, the ideal interface does not have the mechanical interaction found in a generator. This is both good and bad. On the positive side, the second-order response described by the swing-equation of the rotor is not present in the ideal interface; the control is simplified by the fewer number of system poles. On the negative side, the automatic phase adjustment that a generator provides when conditions change does not occur in the ideal interface; the control system must provide the response.

The second difference is the size of the interconnecting inductor. A synchronous generator will normally see an impedance between .5 and 1.0 per unit between its back-emf and the infinite bus. If the ideal interface's inductor were sized as small as the control schemes described below will allow, it would have a 60 Hz impedance of only .05 to .10 per unit.

With such a small inductor, only very small errors in the output voltage waveform of the waveform transformer can be tolerated. A two percent change in the amplitude or a five degree change in the phase of this waveform can give a 100 percent change in the ac current. The control system must have resolution that corresponds to this sensitivity.

The control system must also be able to react quickly to disturbances in the utility voltage or the dc system, no matter where in the cycle they occur. The interconnecting inductor is too small to withstand an imbalance for an appreciable part of the cycle. But a scheme that, by nature, uses information about the peaks and the zero-crossings of waveforms to determine its control signals does not lend itself to the necessary speed of response. For this reason, a much larger interconnecting inductor is normally used.

At least one commercially available ideal interface uses the synchronous control scheme*. The impedance of the inductor at 60 Hz is 0.50 per unit.

The synchronous control scheme cannot dampen the oscillation of the waveform transformer's filters. The control functions will not observe this oscillation and the response of the system will be too slow to have an effect at the ringing frequency. A power dissipating resistor, like the one used in the current source case, is needed instead.

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* Abbacus "SUNVERTER" (6kW), model 763-4-200; Abbacus, P.O. Box 893, Somerville, N.J.

Natural Oscillator Control

It is more fruitful to directly control the ac current everywhere in the cycle. Whenever the current is either larger or smaller (by some tolerance) than it is supposed to be, the transformation factor should be adjusted to correct the discrepancy. The prime objective would be to control the instantaeous current directly; no effort need be made to produce a sinusoidal voltage waveform at the output of the waveform transformer. During steady-state operation, the transformer's output is essentially a sinusoid, simply because it is the waveform that will give the correct ac current. Whenever there is a transient, however, the waveform transformer's output voltage will immediately change to maintain control of the ac current.

Figure 5-6 shows one approach that could be followed. This control system is designed to create a natural oscillator out of the waveform transformer and the interconnection inductor. The operation is as follows. One high frequency switch of the transformer is turned on, the difference between the ac and dc voltage is placed across the inductor, and the ac current changes linearly in one direction. When this current reaches the limit of a predetermined band around the desired sinusoidal waveform, the state of the high frequency switches is changed. During this new state, the polarity of the voltage across the inductor is the the negative of that in the first state: the ac current therefore ramps linearly in the opposite direction. Once the ac current reaches the limit on the other side of the band, the process is repeated.

If the width of the band around the reference waveform is constant, the switching frequency of the waveform transformer varies throughout

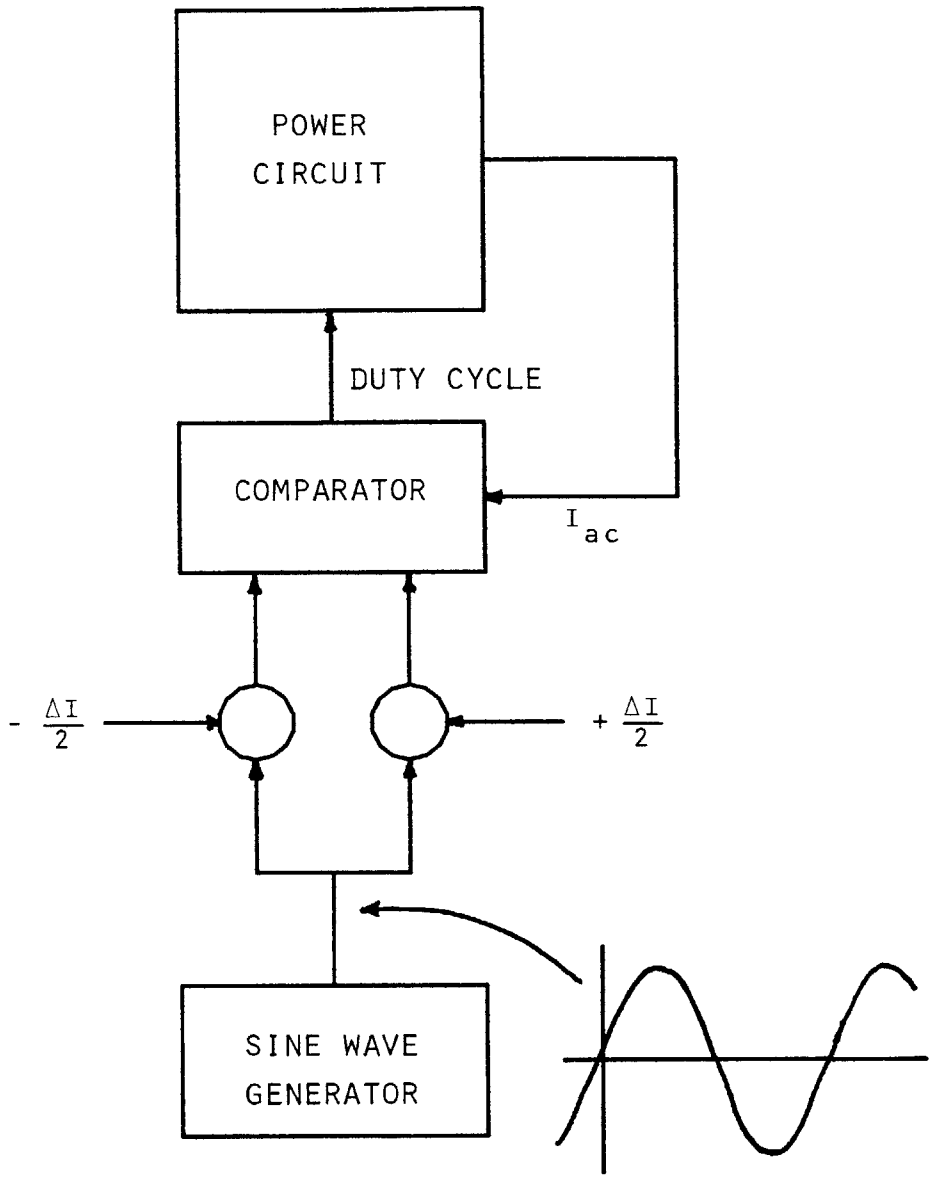

Fig. 5-6: Natural Oscillator Control Scheme.

the cycle. If this variance is considered in a quasi-static manner, the switch frequency at any operating point can be calculated. Given a width ΔI, the instantaneous frequency is

$$f_s = \frac{V_{ac}}{L \Delta I} \left(1 - \frac{V_{ac}}{V_{dc}}\right) \tag{5-3}$$

The maximum switch frequency occurs when

$$V_{ac} = V_{dc}/2 \tag{5-4}$$

and the minimum frequency, zero, occurs at the zero-crossings of the utility voltage waveform. Of course, because of the variance, no single frequency is actually obtained. Equation 5-3 is more correctly interpreted as the inverse of the switching period throughout the cycle.

The wide fluctuation in switch frequency may not be desirable. The detection and mitigation of EMI problems is more difficult when the noise spectrum is broad. The ripple in the ac current is also not always as small as it could be, given the maximum frequency capabilities of the semiconductor devices.

Both these problems can be corrected by varying the width of the band. Figure 5-7 shows how this approach works. The band is reduced where the frequency would otherwise be low and increased where it would be high. With enough sophistication in the control circuit, it is even possible to keep the switch frequency constant. Rearranging Equation 5-3 shows that for a constant frequency f_k, the width of the band should be set to

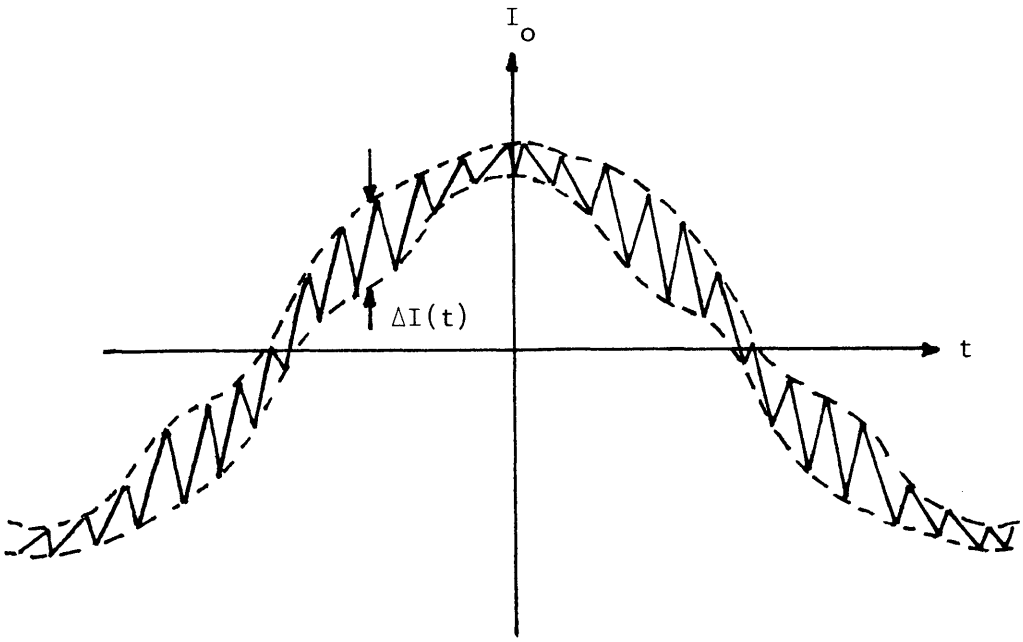

Fig. 5-7: Varied Width of Band gives Constant Switch Frequency.

$$\Delta I = \frac{V_{ac}}{L f_K}\left(1 - \frac{V_{ac}}{V_{dc}}\right) \qquad (5\text{-}5)$$

Although the natural oscillator scheme is a closed-loop control strategy, only the waveform transformer and the interconnecting inductor are part of the system. Impedances on either side of this controlled current source can modify the total system response in a way that cannot be affected by compensation techniques. Once again, with the natural oscillator approach, any oscillations that do occur in the switch frequency filters must be dampened through actual energy loss.

Linear Control

A second approach to the direct current control scheme is shown in Figure 5-8. In this control system, the devices of the waveform transformer are switched at a fixed frequency and the output voltage level is controlled by adjusting the duty cycle. The instantaneous duty cycle is given a nominal value that will produce a voltage waveform exactly equal to the instantaneous utility voltage. The ac current waveform is sensed, and the error between it and the desired waveform is multiplied by a feedback gain and used to alter the duty cycle. This incremental change in the duty cycle is in a direction that will cause the error to be reduced. How small the error will become is determined by the gain of the closed-loop system.

The linear control strategy has certain advantages. The most important is that it is a very powerful approach. The analytical tools necessary to understand exactly how the system should be compensated and

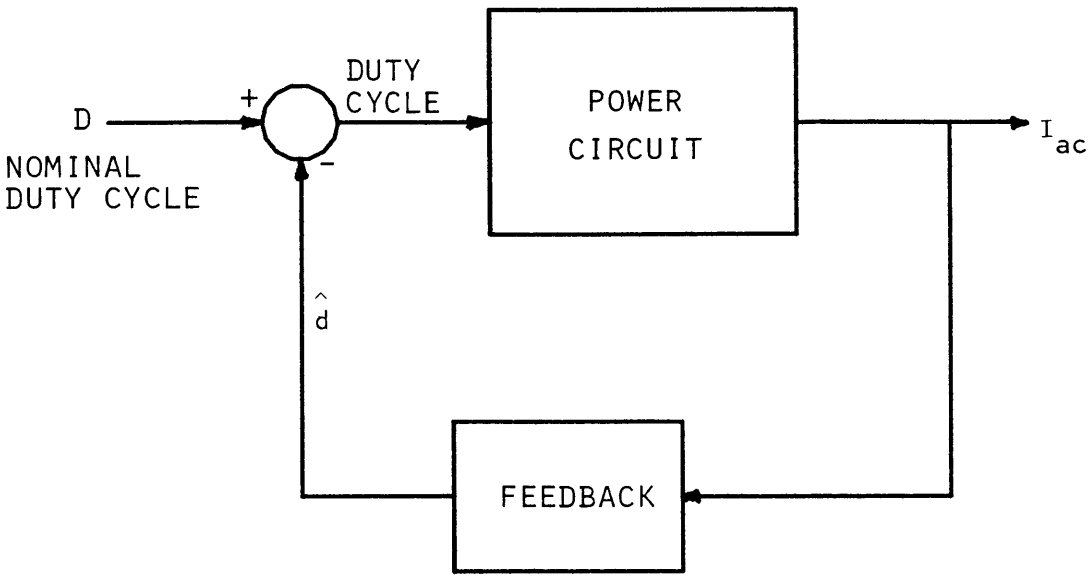

Fig. 5-8: Linear Control Scheme.

how it will respond to disturbances are well developed. Feedback compensators can be designed to give whatever response is desired under any operating condition. With proper compensation, even the oscillations in the waveform transformer's filters can be controlled.

Because the waveform transformer is a non-linear system, the standard linear mathematical representations can not be directly applied to the ideal interface. Fortunately, analysis techniques have been developed to provide a linear model of the power circuit's incremental dynamic response for frequencies lower than the switch frequency. Since the bandwidth of the closed-loop system will not normally exceed the range over which this model is valid, the problem of a non-linear system is avoided. There are, however, several implications of the non-linear nature of the power circuit on the design of the control system. The following three sections will develop these issues.

V.c Incremental Dynamics of the Ideal Interface

As discussed in the last chapter, the active ideal interface is essentially a dc-dc converter whose output is varied at a rate much lower than the switch frequency. An analysis technique, called state-space averaging* has been developed to determine the incremental dynamics of a dc-dc converter at any given operating point. The results of this analysis depend both on the topology of the circuit and on the conditions of the operating point. As long as the variation of the operating point is slow compared to the bandwidth of the closed-loop

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* R.D. Middlebrook, S. Cuk, "A general unified approach to modelling switching-converter power stages," in PESC Record, 1976, pp. 312-324.

control system, it is possible to consider the dynamics of the power circuit in a quasi-static manner. Conditions for stability anywhere in the cycle can be determined solely from the dynamics at the relevant operating point.

State-space averaging combines the state equations that describe the power circuit when one high frequency switch is closed with the equations that apply when the other switch is conducting. The two sets of state equations, weighted by the percentage of time they each apply, are added together. The resulting state equations are an accurate representation of the power circuit as long as the state variables change essentially linearly during each conduction period. This condition is usually satisfied in the ideal interface. The energy storage elements are there to provide filtering; their design is such that they limit the switch frequency fluctuations of voltages and currents to small, and therefore highly linear, waveforms.

Linear Control Example 1

An example will show how state-space averaging is applied. Consider the ideal interface with unidirectional power flow that is shown in Figure 5-9. The switching period, T, is divided into two intervals. One, denoted by DT, is the interval during which the transistor is conducting. The other, denoted (1-D)T, is the interval during which the diode is conducting. For the interval DT, the state equation that describes the power circuit is

$$\frac{d}{dt} i_o = [0] i_o + \begin{bmatrix} 0 & 1/L_o \end{bmatrix} \begin{bmatrix} V_{dc} \\ |V_{ac}| \end{bmatrix} \qquad (5\text{-}6)$$

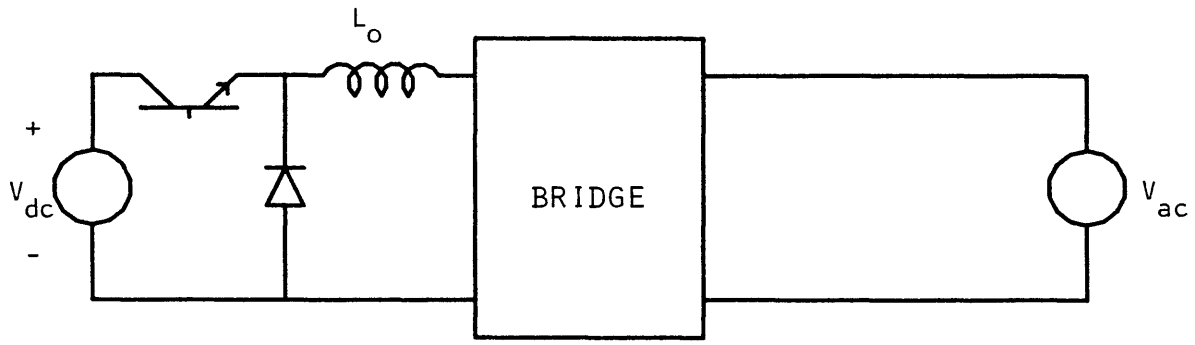


Fig. 5-9: Ideal Interface for One Quadrant DC Voltage Source.

For the interval (1-D)T, the relevant state equation is

$$\frac{d}{dt} i_o = [0] i_o + \begin{bmatrix} -1/L_o & 1/L_o \end{bmatrix} \begin{bmatrix} V_{dc} \\ |V_{ac}| \end{bmatrix} \tag{5-7}$$

The two equations averaged together give

$$\frac{d}{dt} i_o = [0] i_o + \begin{bmatrix} \frac{-(1-D)}{L_o} & \frac{1}{L_o} \end{bmatrix} \begin{bmatrix} V_{dc} \\ |V_{ac}| \end{bmatrix} \tag{5-8}$$

If I_o, V_{dc}, V_{ac}, and D are considered the variables of the operating point around which there is a perturbation, the incremental dynamics become

$$\frac{d}{dt} \hat{i}_o = [0] \hat{i}_o + \begin{bmatrix} \frac{1}{L_o} & 0 \end{bmatrix} \begin{bmatrix} V_{ac} \\ |V_{ac}| \end{bmatrix} \hat{d} \tag{5-9}$$

where the $\hat{}$ symbol denotes perturbation from the nominal value.

Taking the Laplace transforms and rearranging this equation gives

$$\frac{\hat{i}_o}{\hat{d}} = \frac{V_{dc}}{SL_o} \tag{5-10}$$

This result is not suprising; the dynamics of the power circuit are very simple.

Now that the gain and the dynamics of the power circuit are known, the control circuit can be designed. Since the power circuit is just an integrator, the compensation is easy to accomplish.

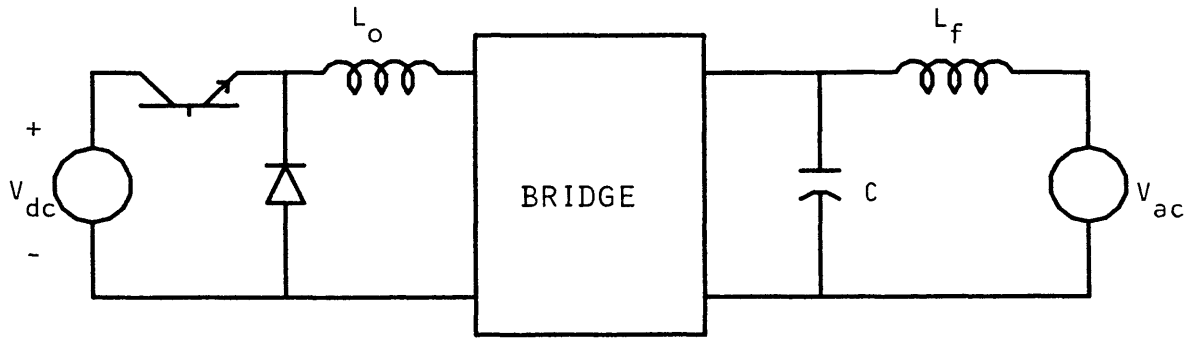


Fig. 5-10: Ideal Interface with Third-Order AC Filter.

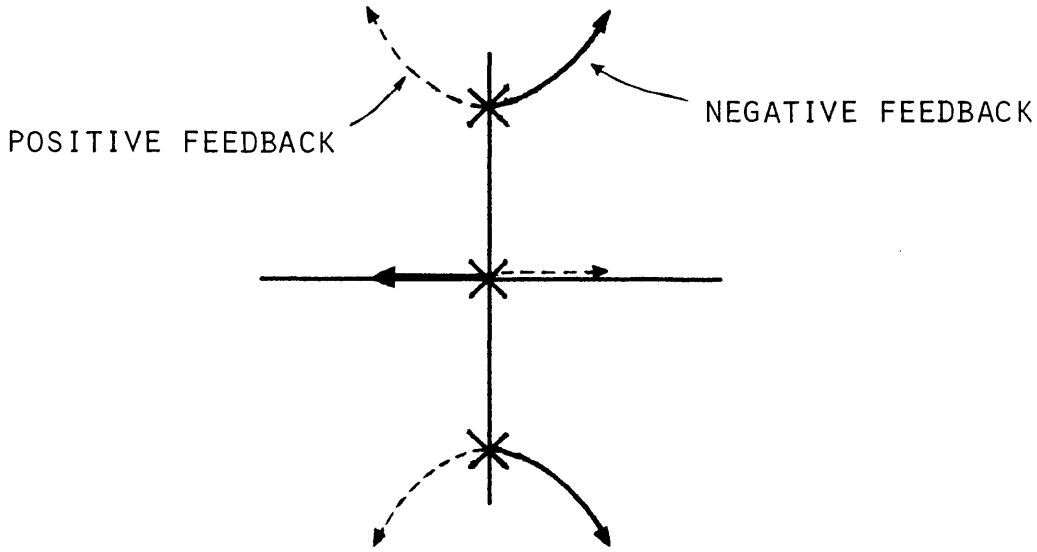
Linear Control Example 2

Another ideal interface is shown in Figure 5-10. In this example, a more complex filter has been included on the ac side of the waveform transformer to achieve the same filtering with smaller components. The inductor between the capacitor and the utility could be due to the utility's network impedance or it could be intentionally added.

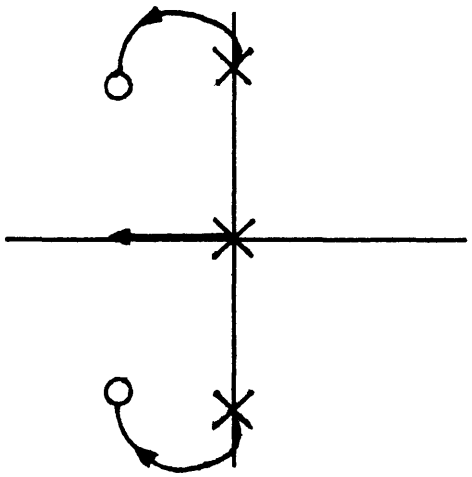
There are now three state variables. Their incremental response to a small change in the duty cycle is

$$\frac{\begin{bmatrix} \hat{i}_o \\ \hat{i}_f \\ \hat{V}_c \end{bmatrix}}{\hat{d}} = \frac{\frac{V_{dc}}{L_o}\begin{bmatrix} s^2 + \frac{1}{L_f C} \\ \frac{1}{L_f C} \\ -s/C \end{bmatrix}}{s\left[s^2 + \frac{1}{C}\left(\frac{1}{L_o} + \frac{1}{L_f}\right)\right]} \qquad (5\text{-}11)$$

This system is more difficult to compensate than the last. The ac current, $\hat{i}_f$, has three poles to its incremental response. A simple linear feedback of $\hat{i}_f$ will cause either the two complex poles or the pole at the origin to move into the right-half plane, depending on the sign of the feedback. Figure 5-11a shows the two possible root loci. Stable closed-loop operation could be achieved by providing two complex zeros in the feedback path. Figure 5-11b shows how these zeros keep the closed-loop poles in the left-hand plane. If this compensation scheme is chosen, however, two poles, farther out in the left-half plane, will have to accompany the complex zeros to limit the control circuit's high frequency gain.



a) Linear Feedback of $\hat{i}_o$



b) Two Zeros in Feedback of $\hat{i}_o$

Fig. 5-11: Root Locus of Closed-Loop System Poles.

Linear Control Example 3

Figure 5-12 shows an ideal interface that can transform both up and down. The topology of this circuit undergoes a more drastic change between the two switch states than the two previous topologies did. The incremental dynamics for this circuit are therefore more complicated, although there are still only three state variables.

The result of applying state-space averaging to this circuit gives

$$\frac{\begin{bmatrix} \hat{i}_{hf} \\ \hat{i}_o \\ \hat{V}_c \end{bmatrix}}{\hat{d}} = \frac{\begin{bmatrix} \frac{1}{L_o C}\left(\frac{V_c + V_{dc}}{L_{hf}}\right)\left[S^2 L_o C + S\left(\frac{L_o I_o}{V_c + V_{dc}}\right) + 1\right] \\ \frac{1}{L_o C}(I_{hf})\left[-S + \left(\frac{V_c + V_{dc}}{I_o}\right)\frac{(1-D)^2}{L_{hf}}\right] \\ \left(\frac{I_{hf}}{C}\right) S\left[-S + \left(\frac{V_c + V_{dc}}{I_o}\right)\frac{(1-D)^2}{L_{hf}}\right] \end{bmatrix}}{S\left[S^2 + \frac{1}{C}\left(\frac{(1-D)^2}{L_{hf}} + \frac{1}{L_o}\right)\right]} \qquad (5\text{-}12)$$

The incremental response of the ac current, $\hat{i}_o$, again has three poles, but the position of the complex pair now depends on the operating point. More importantly, this response also has a right-half plane zero. If a simple, linear feedback loop using only this state variable was closed around the power circuit, either the complex poles or the pole at the origin would move into the right-half plane, depending on the sign of the feedback. Both root loci are shown in Figure 5-13a. The zero will always attract the system poles; no left-half plane singularities in the

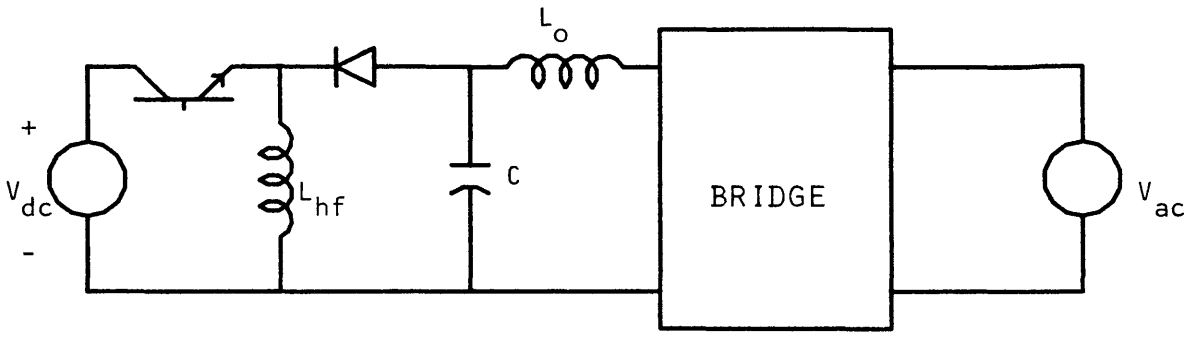
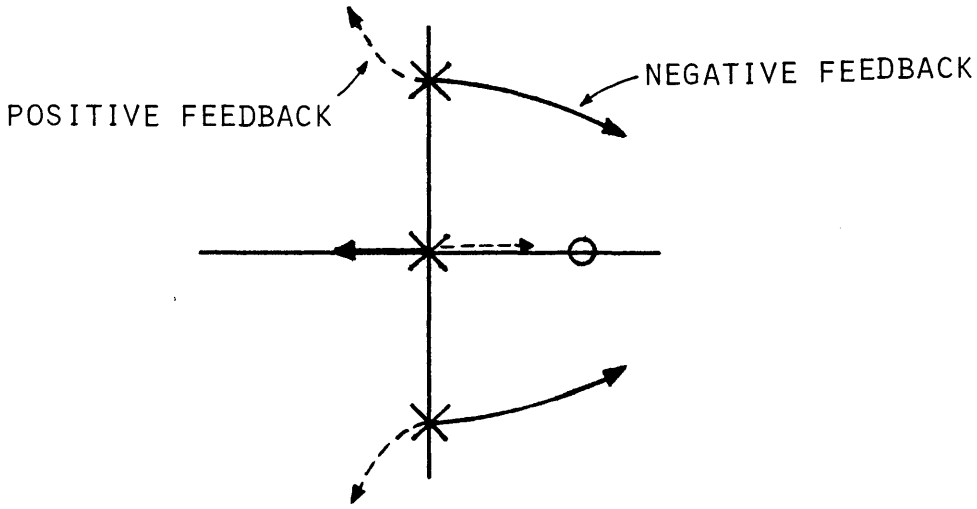
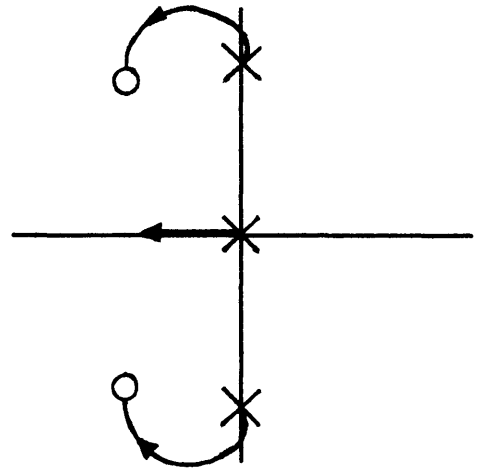


Fig. 5-12: Ideal Interface Capable of Transformation Factors Greater than Unity.



a) Linear Feedback of $\hat{i}_o$



b) Linear Feedback of $\hat{i}_{hf}$

Fig. 5-13: Root Locus of Closed-Loop System Poles.

feedback loop can keep this from happening.

It is possible to achieve a stable system by closing two feedback loops around the power circuit. The purpose of the first, or minor, loop is to move the circuit's poles into the left-half plane. When the second, or major, loop is then closed to control the shape of the ac current, the open-loop poles will no longer be positioned on the imaginary axis; the minor loop will have stabilized the power circuit.

The state variable $\hat{i}_{hf}$ does not have a right-half plane zero in its dynamic response; there are two left-half plane complex zeros instead. It is this variable that must be used for the stabilizing minor loop. Figure 5-13b shows how all three of the power circuit's poles move into the left-hand plane when this feedback loop is closed.

The incremental dynamics of the power circuit for the major feedback loop still include the right-half plane zero. Although this zero will eventually cause the closed-loop poles to move into the right-half plane, there is now more flexibility to achieve a stable system because the poles start from positions well into the left-half plane.

The three previous linear control examples cover the practical ideal interfaces whose dc systems are stiff voltage sources. The analytical results also apply to those situations where the dc system has a large parallel capacitor as a load balancing filter. Since the dynamics of the power circuit are governed by filter elements that are much smaller than this capacitor, it is quite accurate to consider the capacitor as a voltage source with zero incremental impedance.

When the load balancing filtering is provided by a resonant circuit, there is no longer an incremental ground across the dc system,

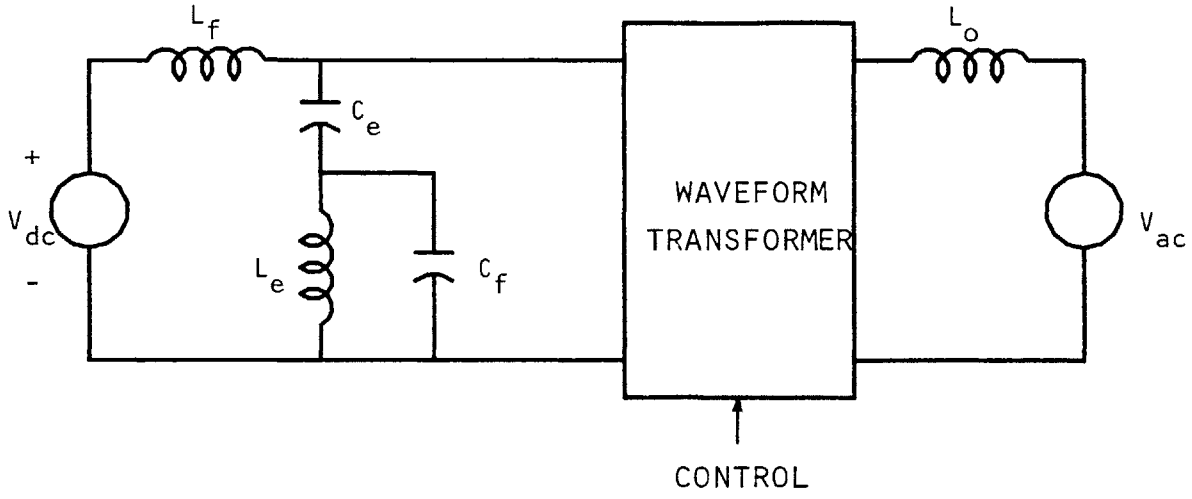
however. Instead, at high frequencies, the inductor of the series tuned circuit dominates the impedance of the resonant filter. For these cases, the impedance of the dc system will have to be considered in the incremental model.

As stated in the last chapter, a tuned load balancing filter does not provide filtering at the switching frequency. For this reason, a high frequency, L-C filter may be included in the power circuit, as shown in 5-14a. It is possible to simplify this four element filter for the incremental dynamic analysis. The load balancing capacitor can be considered a short circuit and the load balancing inductor can be considered an open circuit. This simplification is justified by the large disparity between the size of the switching frequency filter elements and the 120 Hz filter elements. Figure 5-14b shows the reduced model. This model also represents those circuits where load balancing elements are not provided.

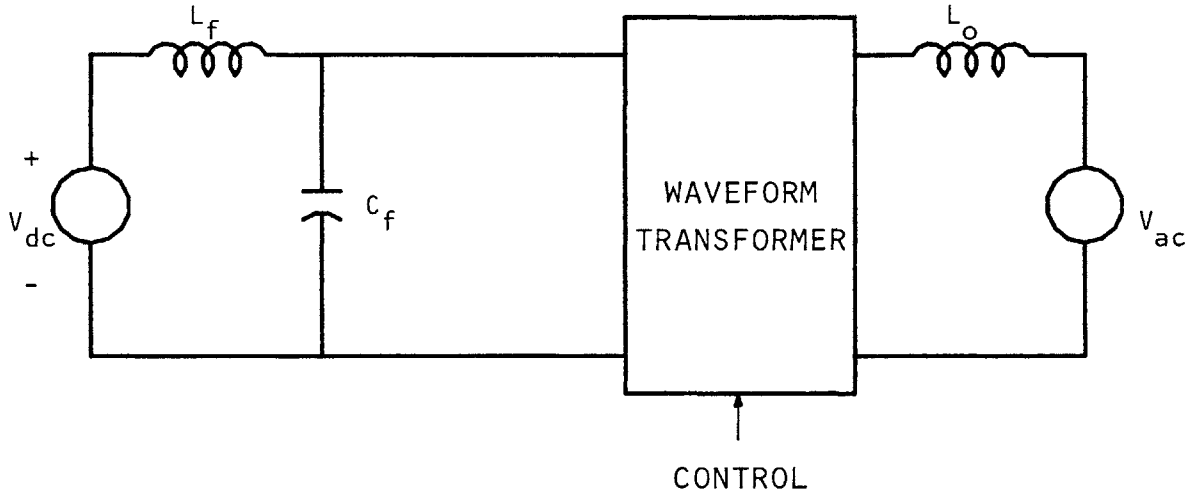
The nature of the dc system is now a factor in the power circuit's dynamics; there is no longer a large capacitor to turn a resistive load into an incremental ground. The dc side switching filter also plays an important role in the circuit's response. The analysis of ideal interfaces with tuned load balancing filters must take these issues into account.

Linear Control Example 4

The power circuit in Figure 5-15 is the simple interface of Figure 5-9 (example 1) with a switching frequency filter between the dc voltage source and the waveform transformer. The application of state-space



a) Complete Topology



b) Simplified Topology for Analysis

Fig. 5-14: High Frequency Filter on DC Side of Waveform Transformer.

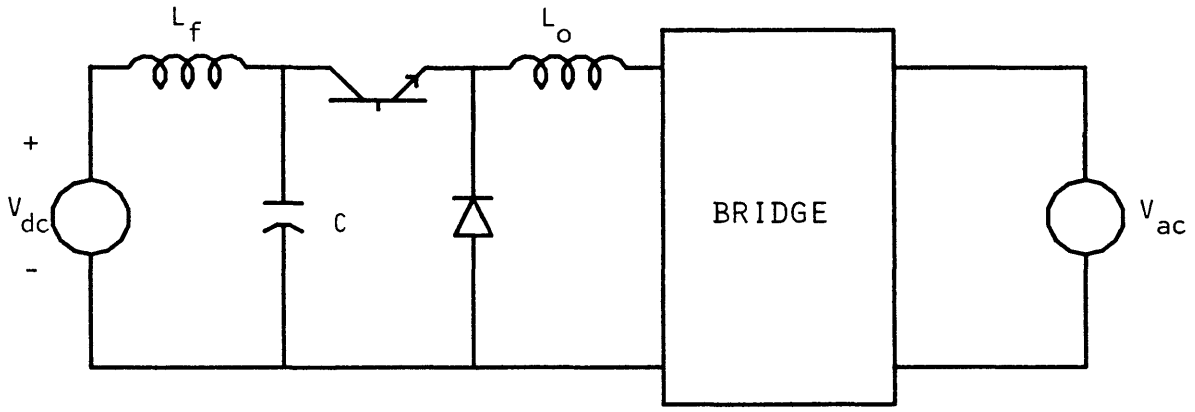


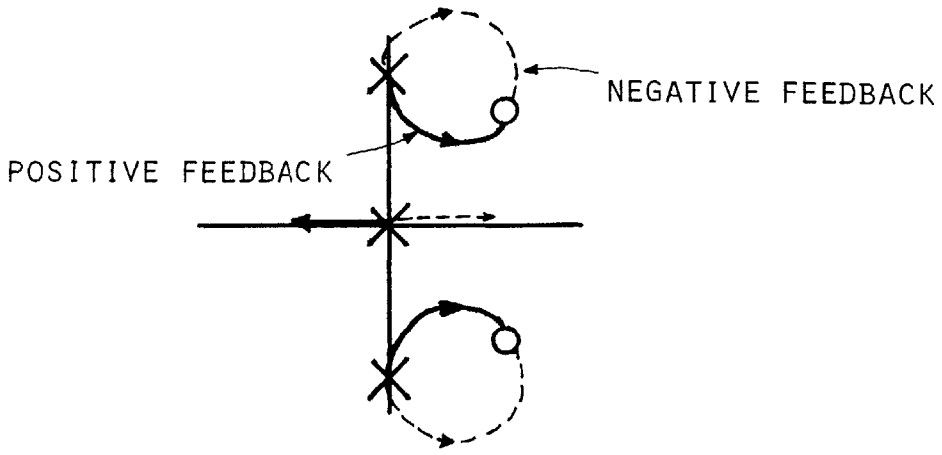
Fig. 5-15: Ideal Interface with DC Side High Frequency Filter.

averaging to this circuit gives the following incremental dynamics:

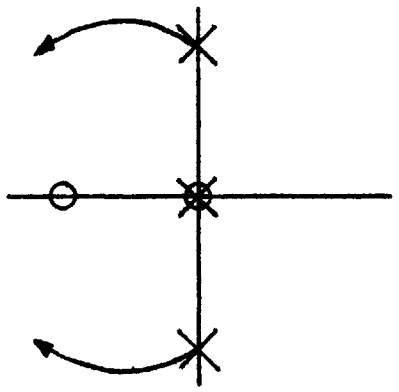
$$\frac{\begin{bmatrix} \hat{i}_f \\ \hat{i}_o \\ \hat{V}_c \end{bmatrix}}{\hat{d}} = \frac{\begin{bmatrix} \frac{1}{L_f C}\left(\frac{V_c D}{L_o}\right)\left[S\left(\frac{I_o L_o}{V_c D}\right)+1\right] \\ \frac{1}{L_f C}\left(\frac{V_c}{L_o}\right)\left[S^2 L_f C - S\left(\frac{I_o L_f D}{V_c}\right)+1\right] \\ -\frac{1}{C}\left(\frac{V_c D}{L_o}\right) S\left[S\left(\frac{I_o L_o}{V_c D}\right)+1\right] \end{bmatrix}}{S\left[S^2+\frac{1}{C}\left(\frac{1}{L_f}+\frac{D^2}{L_o}\right)\right]} \qquad (5\text{-}13)$$

where V_c, I_o, and D are the values of the state variables and the duty cycle for the operating point at which the equations apply.

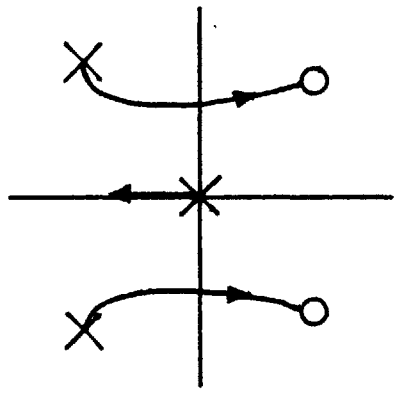
Here, as in the up/down converter case, a control system using only the ac current will not give a stable system. As Figure 5-16a shows, the closed-loop poles will move into the right-half plane. The minor-loop/major-loop approach must be followed. Of the two other state variables, the capacitor voltage is the one that should be used for the minor loop. Since the incremental gain of the power circuit for this state variable is negative, the feedback gain should also be negative. The root locus of Figure 5-16b shows how the power circuit's complex poles are moved into the left-hand plane when this minor-loop is closed. The poles and zeros of the stabilized power circuit for the major-loop are shown in Figure 5-16c. The complex zeros in the right-hand plane will still attract the complex poles, but the system will not become



a) Linear Feedback of $\hat{i}_o$



b) Linear Positive Feedback of $\hat{V}_c$



c) Linear Feedback of $\hat{i}_o$ once Power Circuit is Stabilized

Fig. 5-16: Root Locus of Closed-Loop System Poles.

unstable unless the gain is set too high.

Linear Control Example 5

Many applications of the ideal interface have dc systems that are resistors. In such situations, the resistor supplies a great deal of damping to the system's incremental dynamics. The following equations show the effect of the load resistor in the interface of Figure 5-17.

$$\frac{\begin{bmatrix} \hat{i}_f \\ \hat{i}_o \\ \hat{V}_c \end{bmatrix}}{\hat{d}} = \frac{\begin{bmatrix} \frac{1}{L_f C}\left(\frac{V_c D}{L_o}\right)\left[S\left(\frac{I_o L_o}{V_c D}\right)+1\right] \\ \frac{1}{L_f C}\left(\frac{V_c}{L_o}\right)\left[S^2 L_f C + S\left(RC - \frac{I_o L_f D}{V_c}\right)+\left(1-\frac{I_o R D}{V_c}\right)\right] \\ -\frac{1}{C}\left(\frac{V_c D}{L_o}\right)\left[S^2\left(\frac{I_o L_o}{V_c D}\right)+S\left(1+\frac{I_o R L_o}{V_c D L_f}\right)+\frac{R}{L_f}\right] \end{bmatrix}}{\left[S^3 + S^2\left(\frac{R}{L_f}\right)+S\frac{1}{C}\left(\frac{1}{L_f}+\frac{D^2}{L_o}\right)+\frac{D^2 R}{L_o C L_f}\right]} \qquad (5\text{-}14)$$

The power circuit's two complex poles are now in the left-half plane. The larger the load resistor, the closer these poles are to the real axis. If the load resistor provides sufficient damping, the interface can be controlled with a simple feedback on the ac current. If it does not, the power circuit will have to be stabilized with a minor-loop feedback.

Although the above examples cover most situations, it is possible to have other circuit topologies. Complex filters could be used on both

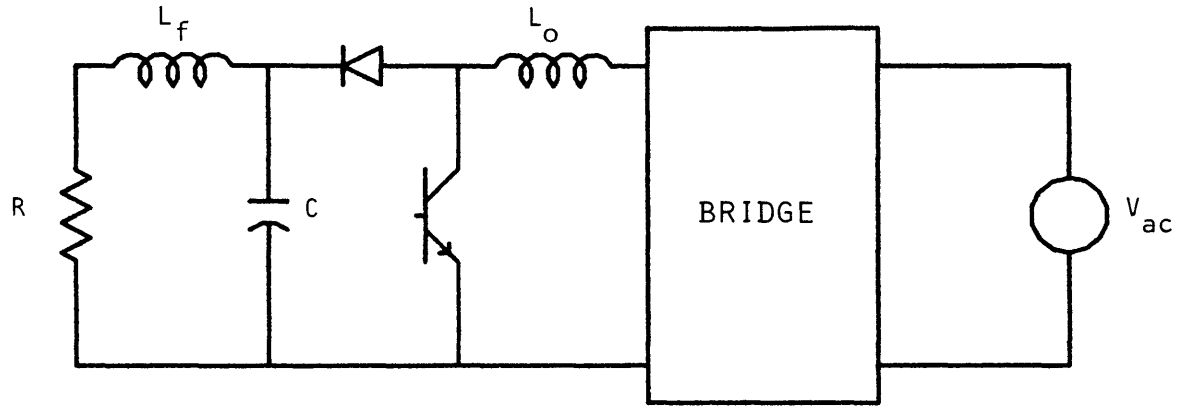


Fig. 5-17: Ideal Interface with Resistive Load for DC System.

the ac and dc sides of the power multiplier. The utility and the dc system may contribute impedances of their own. These extended power circuits can be analyzed with the same procedure used for the simpler examples, but their larger number of state variables makes the results more difficult to obtain and interpret.

V.d Time-Varying Nature of the Incremental Dynamics

The examples given in the last section show that the incremental dynamics of an ideal interface depend on the operating point at which they apply. For the first two circuits the dependence is simple; the gain of the power circuit is directly proportional to the dc voltage. For the second two cases, the dependence is more complicated. Both the gain and the pole and zero locations of the circuit are functions of the nominal duty cycle and the operating point values of the state variables. Since these variables undergo a wide variation throughout a fundamental cycle of the utility voltage, the incremental response of these last two power circuits is a strong function of time.

It should be noted that there are limited mathematical tools available in control theory that can be applied to time-varying systems. However, if the system is periodically varying, as is the case here, the situation is much better than for non-periodic systems*. This chapter will treat the time variance in a quasi-static manner. It will assume that if the system is stable at every operating point, it is stable throughout the cycle. There are results in system theory that guarantee

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* U. Mukherji, "Control synthesis for periodic plants with an application to power conditioning," Master's Thesis submitted to the EECS Department of MIT on 28 January, 1982.

this approach is valid if the variation of the system parameters is 'sufficiently slow'. More importantly, empirical evidence gained from simulations and actual test circuits has been completely consistent with this assumption. This approach therefore appears to be valid for the ideal interface.

The time variation of the power circuit's dynamic response makes it difficult to achieve the closed-loop system performance wanted. At a specified operating point it is straightforward to calculate the feedback gains necessary to place the closed-loop poles wherever they are desired. But for any fixed set of gains, the resulting pole positions will change with the operating point. In those cases where the circuit dynamics are only affected by a dc voltage whose level does not significantly change, the movement of the poles will be slight and easy to predict. However, when the incremental dynamics depend on variables that range from zero to peak values as they follow the 60 Hz sinusoidal waveforms, the closed-loop pole movements can be drastic.

One way to compensate a time dependent power circuit is to choose feedback gains that will give satisfactory performance no matter where the closed-loop poles move. This approach requires knowledge of the extreme conditions to which the converter will be subjected so that the limits of the pole movement can be determined. Tradeoffs between the system's performance at each extreme of the movement must be made; more stability at one limit is usually gained through less speed of response at the other. Although adequate feedback gains can be determined, the time-varying system will seldom be optimally compensated.

Linear Control Example 6

An example will point out the difficulties that can be encountered when the system response changes throughout the cycle. The analysis of the up/down converter presented in the last section (example 3) suggested a minor-loop feedback to move the imaginary axis poles into the left-half plane and stabilize the circuit. Even if the feedback gain was high enough to move the complex poles all the way to the complex zeros, stability would not be ensured, however. When the ac variables reach zero, the complex zeros are located on the imaginary axis. A simple linear feedback for the major-loop might be satisfactory near the peaks of the ac waveforms, but it would not work near the zero-crossings. No matter how small a gain was used, the system would always begin to go unstable during this portion of the cycle, although it would, in general, recover shortly after the zero-crossing.

The minor-loop also moves the real-axis pole to the left, but its final position, although it changes, never returns to the origin. If a pole at the origin is included in the major-loop feedback path, as shown in the control system of Figure 5-18, it is not the complex poles, but rather the two real-axis poles, that eventually approach the right plane zero. The complex poles move to the left, as shown in the root locus diagram of Figure 5-19a. If the major-loop feedback gain is not too large, the system compensated in this manner will remain stable throughout the cycle.

The response of this closed-loop system still varies during the cycle. Near the zero-crossings, the dynamics are dominated by two complex poles, as shown in Figure 5-19b. Near the peaks, the dynamics

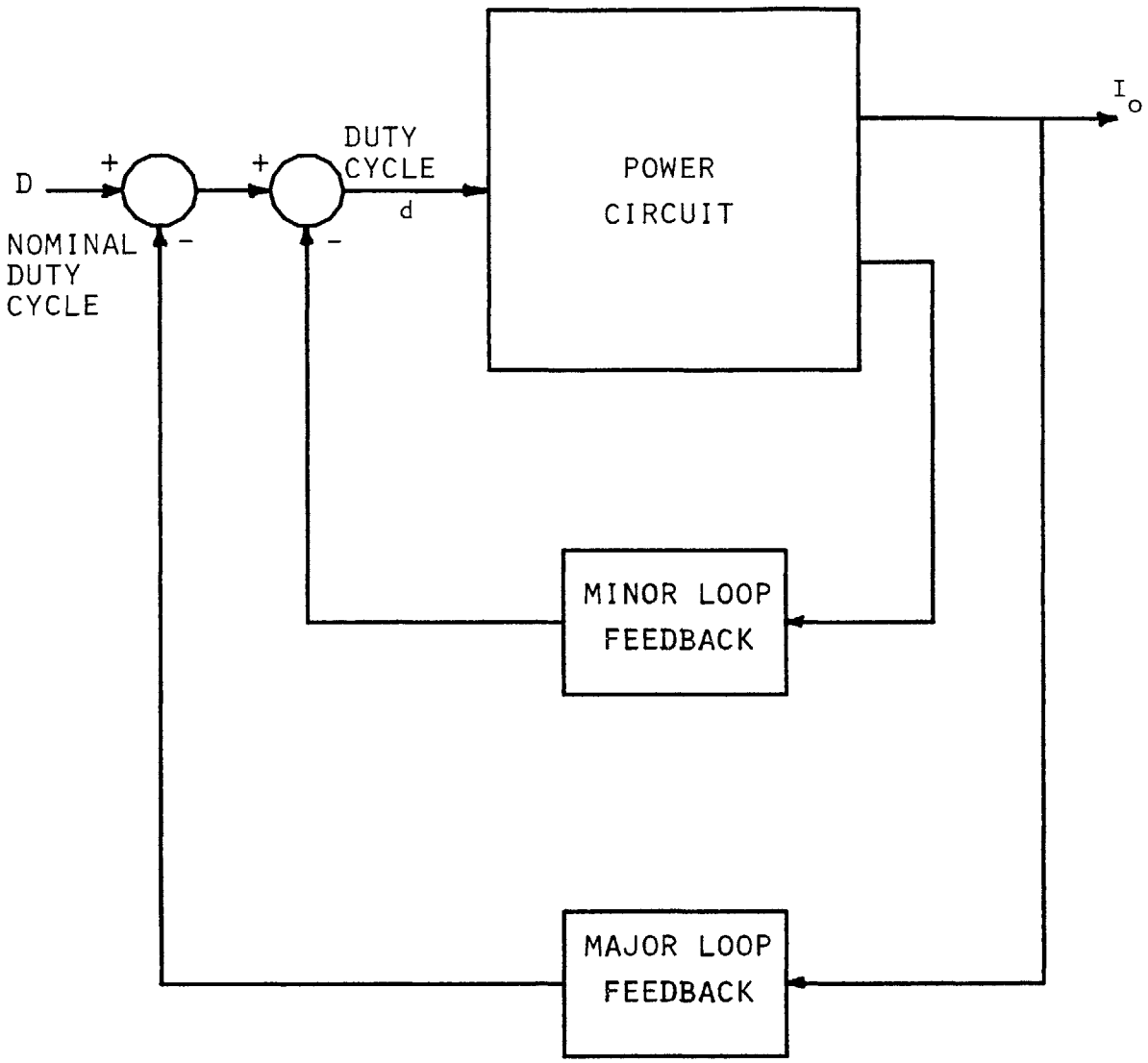
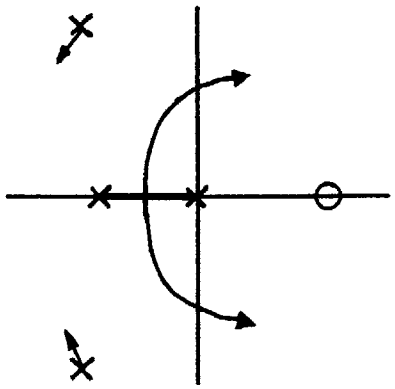
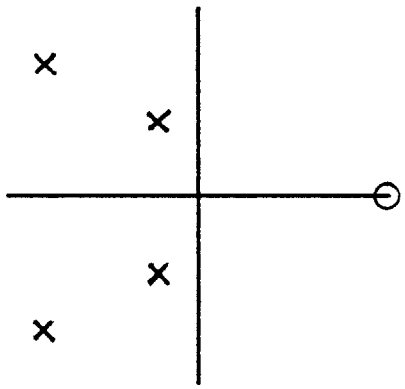


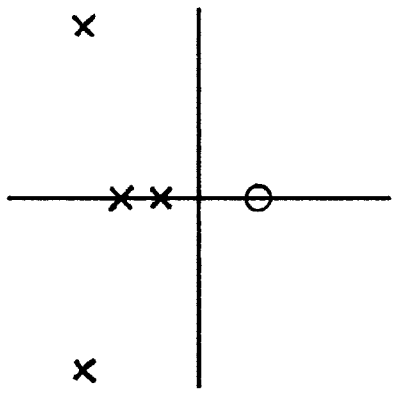
Fig. 5-18: Control System for Minor-Loop/Major-Loop Feedback.



a) Minor-Loop Feedback on $\hat{i}_{hf}$, Major-Loop Feedback on $\hat{i}_o$



b) Position of Singularities near Zero-Crossing



c) Position of Singularities near Peak

Fig. 5-19: Root Locus of Minor-Loop/Major-Loop Control System.

are dominated by real axis poles, as shown in Figure 5-19c. A decreased feedback gain improves the damping of the former situation but reduces the speed of response of the latter. A compromise must be made.

Unfortunately, the system of Figure 5-18 is least stable at the point in the cycle where the ac side filter is disturbed. The results of a simulation, given in Figure 5-20, show the oscillations that occur due to this disturbance. The minor- and major-loop feedback gains were chosen to give the best ac current waveform possible. The oscillations in the state variables eventually decay, but not because of losses in the power circuit. Instead, they disappear as the ac waveforms move away from their zero values and the closed-loop system becomes more damped. Although the oscillations shown in the figure do not cause a significant problem, they do show how susceptible to disturbances a system can be when its poles are allowed to move over a large region of the complex plane.

V.e Adaptive Feedback Gains

The difficulty of controlling the time-varying systems in the above examples is due more to the inflexibility of fixed feedback gains than to the variance of the power circuit's dynamics. For any given operating point it is possible to place the system's closed-loop poles wherever they are desired. It is simply a matter of choosing appropriate feedback gains for each of the state variables. Rather than limiting the feedback gains to fixed values, however, the gains should instead be made to change in response to the changing incremental dynamics. If this variance of the feedback gains is done correctly, the

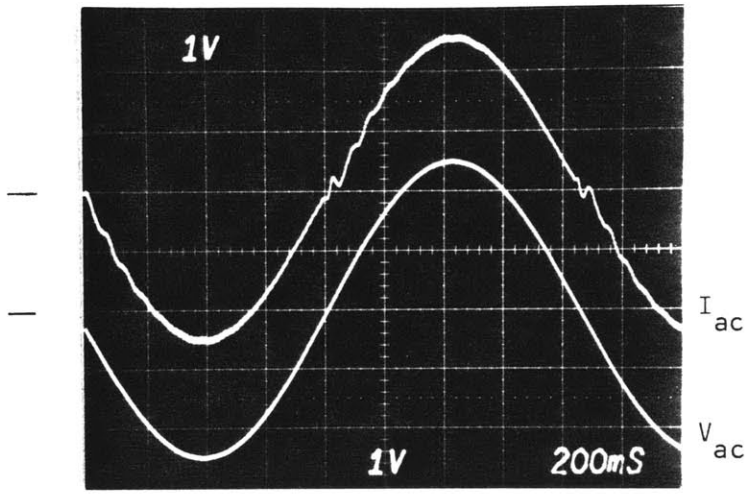


Fig. 5-20: Simulation Results Showing Oscillations in the AC Current.

closed-loop poles can be made to remain in a chosen position regardless of the power circuit's changing operating point. In essence, the feedback gains continually adapt to the power circuit's nonlinear operation.

To calculate the correct values of the feedback gains as a function of the operating point, we start with the state equations that describe the power circuit's incremental dynamics:

$$\frac{d}{dt}\hat{x} = A(t)\hat{x} + B(t)\hat{d} \qquad \text{(Eq. 5-15)}$$

If the incremental duty cycle is determined by a linear combination of the state variables, the state equations can be rewritten as

$$\frac{d}{dt}\hat{x} = [A(t) - B(t)K]\hat{x} \qquad \text{(Eq. 5-16)}$$

where K is the linear feedback gain matrix. The system's closed loop poles are now given by the determinant

$$|SI - [A(t) - B(t)K]| \qquad \text{(Eq. 5-17)}$$

The coefficients of this characteristic equation specify the location of each system pole. They are functions of both the feedback gains and the operating point variables. Once these functions are known, it is possible to specify how each feedback gain should vary with the operating point to keep the coefficients constant.

Dynamics Dependent Only on V_{dc}

For those power circuits whose dynamics are only dependent on the dc voltage, the adaptive feedback gains are simple functions of the operating point: they are inversely proportional to the dc voltage level. Figure 5-21 shows how this function can be easily implemented. The transformation of the analog signal that indicates the duty cycle into an actual digital signal for the base drive is usually accomplished by comparing the signal to a triangle wave. If the amplitude of this triangle wave is made proportional to the dc voltage, the effect will be the same as if the gains had been divided by the same variable. This modification of the normal control circuit is very simple.

Dynamics Dependent on the AC Variables

For those power circuits whose dynamics are more complicated functions of the operating point, the implementation of adaptive feedback gains is more difficult. For the up/down converter example shown in Figure 5-12 (example 3), the closed-loop system has a third-order characteristic equation:

$$S^3 + a_2S^2 + a_1S + a_o = 0 \qquad \text{(Eq. 5-18)}$$

The feedback gains, as a function of operating point and closed-loop pole positions, are

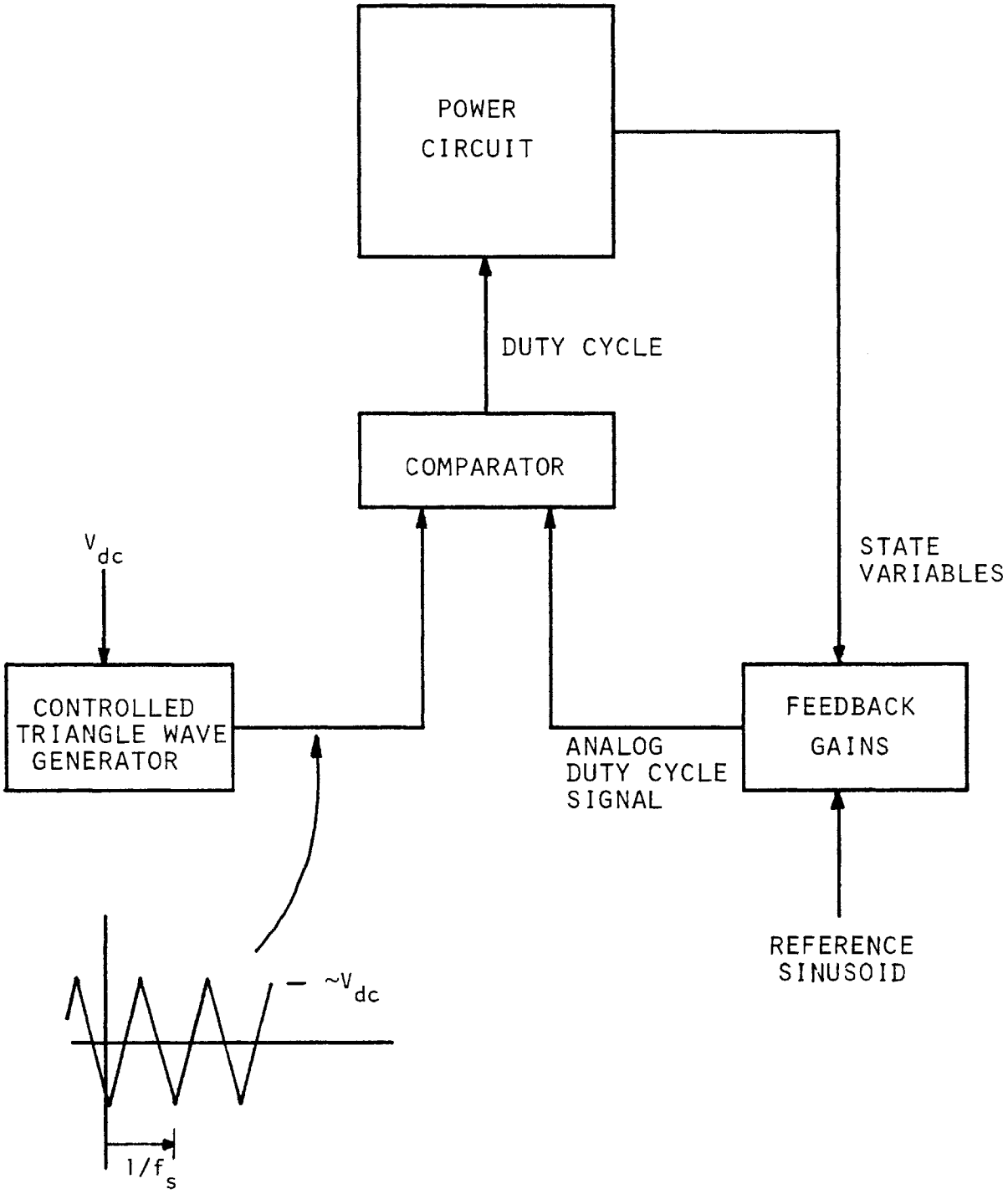


Fig. 5-21: Feedback Gains Inversely Proportional to V_{dc}.

$$K_c = \frac{\frac{I_o}{V_{dc}(1-d)}\left(\frac{1}{C}\right)\left[a_o L_{hf} C - a_2\left(\frac{L_{hf}}{L_o} + (1-D)^2\right)\right] - \frac{1}{L_{hf}C}\left(\frac{L_{hf}}{L_o} + (1-D)^2\right) + a_1}{\frac{V_{dc}}{L_{hf}C} + \frac{[I_o/(1-D)]^2}{V_{dc}\,C^2}\left(\frac{L_{hf}}{L_o} + (1-D)^2\right)}$$

$$K_o = \frac{L_{hf}}{V_{dc}}\left[a_o L_o C - a_2 - \frac{K_c I_o}{C(1-D)}\right]$$

(5-19)

$$K_{hf} = \frac{L_{hf}(1-D)}{V_{dc}}\left[a_2 + \frac{K_c I_o}{C(1-D)}\right]$$

These functions are complicated, but they can be implemented in real time. The equations can be solved with either a microprocessor or analog circuitry. The microprocessor approach is more flexible, but has a slower response to changing conditions; the analog approach is much quicker, but requires gain and offset trimming. The digital approach is desirable if it can be made to operate at sufficient speeds.

One way to implement a microprocessor based control circuit is to construct a table that holds the values of the feedback gains throughout the cycle. Since the gains depend only on the peak ac voltage, the peak ac current, and the dc voltage, it is possible for a microprocessor to precalculate this table once these three values are known. At the appropriate time, each entry of the table can then be sent to a digitally controlled amplifier of the feedback loop. With this scheme the microprocessor does not have to solve the feedback equation in real time. It is only required to construct new tables at the rate at which

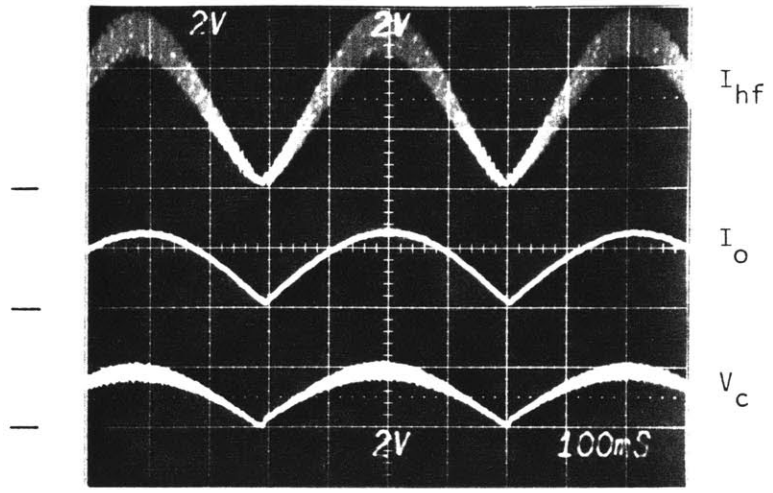
the ac and dc voltage and current levels change. This variance is usually slow enough for the microprocessor to accomplish its task in time.

Figure 5-22 shows the performance of the up/down ideal interface given in Figure 5-12 (example 3) when the control is implemented with adaptive feedback gains. The closed-loop poles of this simulation were positioned to give a dominant second-order response with a .707 damping ratio. As the ac current waveform shows, the cusps of the $\hat{i}_o$ current are not perfect due to the limited bandwidth of the power circuit. The action of the bridge switches therefore disturbs the system. The response to this disturbance is very well controlled compared to that shown in Figure 5-20, however; the oscillations are immediately damped. The system remains optimally compensated, no matter where it is in the cycle.

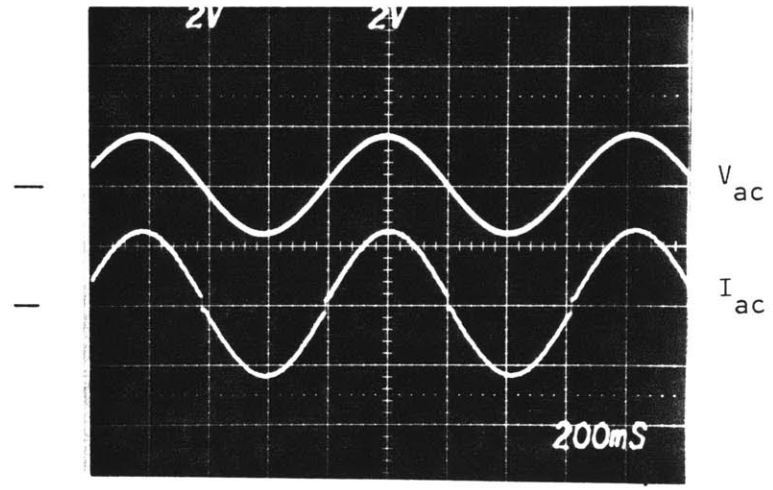
V.f The Reference Waveform

Every ideal interface control system, whether open- or closed-loop, requires a sinusoidal reference waveform. For those cases where the ac current must always have zero phase with respect to the ac voltage, a very simple way to obtain the sinusoidal shape is to use the ac voltage waveform. The control circuit must only adjust the amplitude to alter the level of power flow.

This approach is convenient, but it does present problems. The ideal interface becomes, in effect, a resistor whose value is usually changed slowly compared to a 60 Hz cycle. Any distortion in the utility voltage, within the bandwidth of the system, is duplicated in the



a) State Variables



b) Utility Variables

Fig. 5-22: Simulation Results Showing Performance of Time-Varying Feedback System.

current waveform. More important, when the power flow is from the dc system to the utility, the power circuit becomes a negative resistor. Interaction with the utility's impedance could cause instabilities.

It is possible to filter the unwanted harmonic components from the reference waveform. Doing so should also lessen the instabilities caused by the negative resistance. It is difficult to extract the fundamental component without getting a phase shift, however. Circuits designed for unidirectional power flow can not accommodate the reactive power flow that would result from this phase shift.

The sinusoidal reference waveform can be generated through digital techniques instead. This approach avoids the interaction with the utility and turns the converter into a current source. The reference waveform must still be synchronized with the ac voltage waveform, however. A standard phase-lock loop can accomplish this task, although it presents its own stability problems. As an alternate approach, a microprocessor based control circuit could achieve the synchronization in a much more flexible manner.

V.g Control of the Power Level

The dynamic response of the waveform transformer and its high frequency filters is very fast compared to 60 Hz. A change in the amplitude of the ac current waveform can therefore be made quickly. This abrupt change in the ac power level does not result in a similar change at the dc system, however. Instead, the load balancing filter limits the rate at which the dc power level can be changed.

The response of the dc power level to a step change in the ac power

is easily determined. For a resistive load R_L with a large parallel capacitor C, the response is

$$\frac{V_{dc}}{Control} = \frac{R_L}{SR_L C + 1} = \frac{R_L}{(S/2\omega_o R + 1)} \tag{5-20}$$

where R is the percent ripple in the capacitor voltage and $\omega_o = 377$ rad/sec. For an inductor in series with the back-emf of a motor, the response is that of an integrator. In either case, because the load balancing filter element is designed to isolate the dc system from large 120 Hz variations in power flow, the rate at which the average level of power can be changed is very slow compared to the fundamental period.

When the load balancing is accomplished with a tuned filter, however, the dc power level response is much improved. For the same reduction of ripple, the main energy storage element of a tuned circuit is smaller by a factor of Q than it would otherwise have to be. The greatly reduced energy storage that results allows the dc system to reach its new operating point correspondingly faster. This feature of the ideal interface is an advantage that, if needed in the particular application, can help to offset the cost of the high frequency switches.

The tuned filter does introduce a second-order characteristic to the response of the dc power level. The poles and zeros of this response are straightforward to calculate. When the dc system is a resistor R_L in parallel with a tuned shunt filter, the response to a change in power is

$$\frac{V_{dc}}{Control} = \frac{R_L[S^2/(2\omega_o)^2 + 1]}{S^2/(2\omega_o)^2 + \frac{S\,\xi}{2(2\omega_o)} + 1} \tag{5-21}$$

where $\xi = (Q R)$. This response is usually well damped by the load resistor and very fast. The new operating point can typically be reached with one quarter of a 60 Hz cycle.

If the dc system is a source or sink, rather than a resistive load, very little damping of the load balancing filter's response will take place. The control of power in such cases requires a properly compensated feedback loop. When a tuned filter is used, the compensation is more complicated, but good stability can be achieved without much sacrifice of the power circuit's inherent speed of response.

V.h Interaction Among Multiple Control Systems

When several ideal interfaces are placed in parallel for a single-phase application, or when they are combined for three phase operation, it is possible for the individual control systems to interact. If the dc system or the utility has an impedance that all interfaces share, each control system will be able to affect the operation of the other. This common impedance could be inherent to the ac or dc system, or it could be a high frequency filter intentionally shared by all the waveform transformers. In either case, it is important for the incremental analysis of each interface to include the influence of the others.

Figure 5-23 shows an example of one such system: a three phase, unidirectional power flow interface where a single L-C filter is placed between the dc voltage source and the high frequency switches of each multiplier. Each individual interface is identical to the one shown in Figure 5-15 and described by Equation 5-13 (example 4). This three-

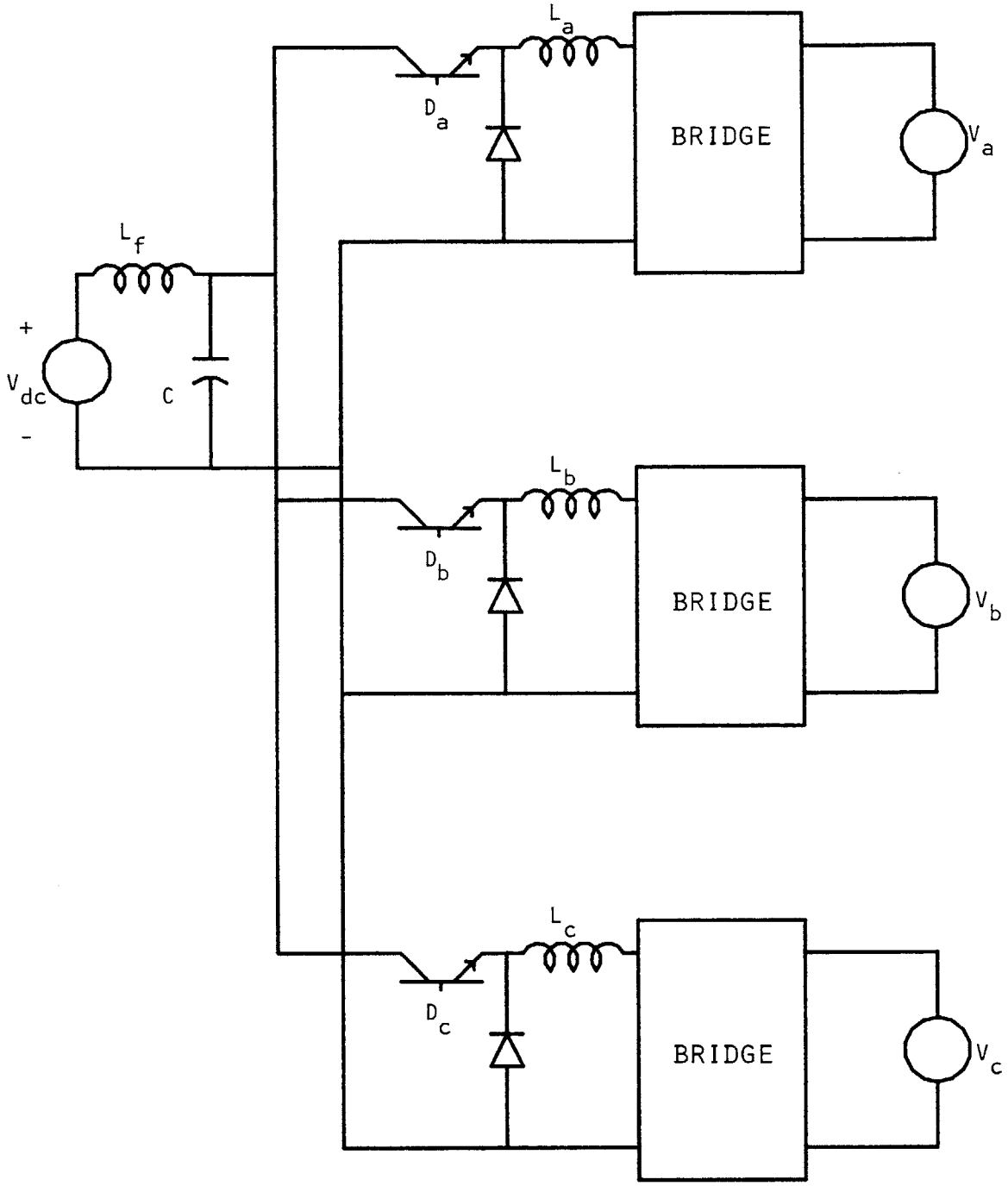


Fig. 5-23: A Three-Phase Ideal Interface.

phase system has five state variables and three controllable duty cycles.

Although the standard procedure for state-space averaging could be directly applied here, it is easier to simply extend the results found when the single-phase interface was analyzed. The state equations for the three-phase case will have the following form:

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_a \\ \hat{i}_b \\ \hat{i}_c \\ \hat{i}_f \\ \hat{V}_c \end{bmatrix} = \begin{bmatrix} A \end{bmatrix}\begin{bmatrix} \hat{i}_a \\ \hat{i}_b \\ \hat{i}_c \\ \hat{x}_f \\ \hat{V}_c \end{bmatrix} + \begin{bmatrix} B \end{bmatrix}\begin{bmatrix} \hat{d}_a \\ \hat{d}_b \\ \hat{d}_c \end{bmatrix} \qquad (5\text{-}22)$$

The A matrix represents the natural response of the system. It can be determined from the equivalent circuit shown in Figure 5-24, where the effective impedance of the three output inductors has been modified by the action of the respective waveform transformers. The A matrix that results from this topology is

$$\begin{bmatrix} A \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & D_a/L_a \\ 0 & 0 & 0 & 0 & D_b/L_b \\ 0 & 0 & 0 & 0 & D_c/L_c \\ 0 & 0 & 0 & 0 & -1/L_f \\ -\frac{D_a}{C} & -\frac{D_b}{C} & -\frac{D_c}{C} & \frac{1}{C} & 0 \end{bmatrix} \qquad (5\text{-}23)$$

The B matrix represents the driving term. For the single-phase

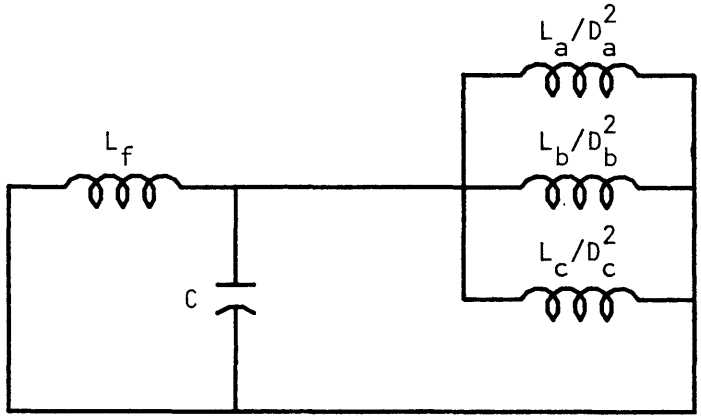


Fig. 5-24: Equivalent Circuit to Determine the A Matrix.

interface shown in Figure 5-15, an incremental change in duty cycle provides two drives. One is a charging current for the filter capacitor; the other is a charging voltage for the output inductor. The charging current is equal to the product of the change in duty cycle and the operating point current in the output inductor. The charging voltage is the product of the incremental duty cycle and the operating point voltage across the capacitor. Once this relationship is realized, it is easy to extend the principles to the three-phase interface. The B matrix that results is

$$\left[B \right] = \begin{bmatrix} V_c/L_a & 0 & 0 \\ 0 & V_c/L_b & 0 \\ 0 & 0 & V_c/L_c \\ 0 & 0 & 0 \\ -I_a/C & -I_b/C & -I_c/C \end{bmatrix} \tag{5-24}$$

With the A and B matrices determined, the power circuit's incremental dynamics can now be found. Manipulation of the state equations gives

$$[\hat{x}] = [SI - A]^{-1} \begin{bmatrix} V_c\hat{d}_a/L_a \\ V_c\hat{d}_b/L_b \\ V_c\hat{d}_c/L_c \\ 0 \\ -\frac{1}{C}\left[\hat{d}_a I_a + \hat{d}_b I_b + \hat{d}_c I_c\right] \end{bmatrix} \tag{5-25}$$

If the three control systems are separate, the dynamic response for each system can be found by setting the incremental duty cycle of the other two to zero. When this is done for the the A-phase interface, the result is

$$\left.\frac{\begin{bmatrix}\hat{i}_a\\ \hat{i}_b\\ \hat{i}_c\\ \hat{i}_f\\ \hat{V}_c\end{bmatrix}}{\hat{d}_a}\right|_{\hat{d}_b,\hat{d}_c=0} = \frac{\begin{bmatrix}\left(V_c/L_a\right)\left[S^2 - S\left(\frac{D_a I_a}{V_c C}\right) + \frac{1}{C}\left(\frac{D_b^2}{L_b} + \frac{D_c^2}{L_c} + \frac{1}{L_f}\right)\right]\\ -\left(\frac{D_b I_a}{L_b C}\right)\left[S + \frac{V_c D_a}{I_a L_a}\right]\\ -\left(\frac{D_c I_a}{L_c C}\right)\left[S + \frac{V_c D_a}{I_a L_a}\right]\\ -\left(I_a/L_f C\right)\left[S + \frac{V_c D_a}{I_a L_a}\right]\\ -\left(I_a/C\right) S\left[S + \frac{V_c D_a}{I_a L_a}\right]\end{bmatrix}}{S\left[S^2 + \frac{1}{C}\left(\frac{D_a^2}{L_a} + \frac{D_b^2}{L_b} + \frac{D_c^2}{L_c} + \frac{1}{L_f}\right)\right]} \qquad (5\text{-}26)$$

The compensation of this system can be achieved along the same lines used for single interface systems.

CHAPTER VI

A 6kW SINGLE-PHASE ACTIVE UTILITY/DC INTERFACE

This chapter describes an active ideal utility/dc interface that, when connected to a 208V single-phase utility service, can deliver a peak power of 6 kW to a dc load. Since the flow of power is unidirectional, the current drawn from the utility has a power factor of one. The load balancing filter elements of the interface are designed to give the load the characteristic of a current source. Control of the power level and the ac current's waveshape are both provided by a microprocessor circuit in an open-loop manner. A picture of the interface is shown in Figure 6-1.

The following sections of this chapter give the details of the interface's design and performance. Although the load for the ideal interface can be any single-quadrant dc system, the results presented here are based on a purely resistive load.

VI.a The Power Circuit

The schematic and the component values of the power circuit are given in Figure 6-2. As can be seen, the bridge and waveshaping functions have been separated to minimize the number of high frequency switches required. Because the flow of power is towards the dc system, the bridge consists of four diodes. The controllable high frequency switch is a GTO that is operated at 9.6 kHz.

Inductor L_e and capacitor C_e form the parallel resonant circuit that both limits the 120 Hz ripple in the load current and provides the

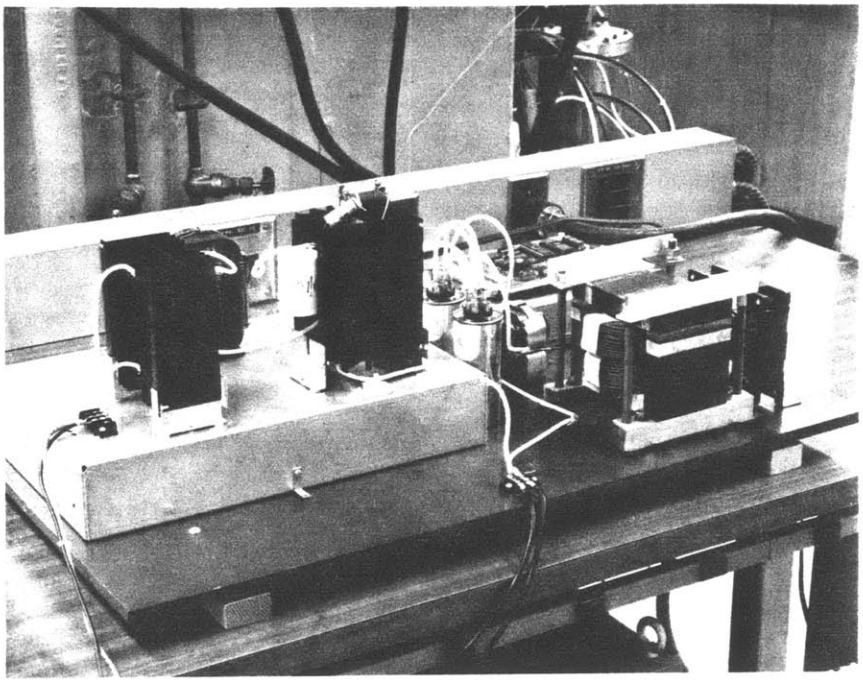


Fig. 6-1: A 6 kW Ideal Utility/DC Interface.

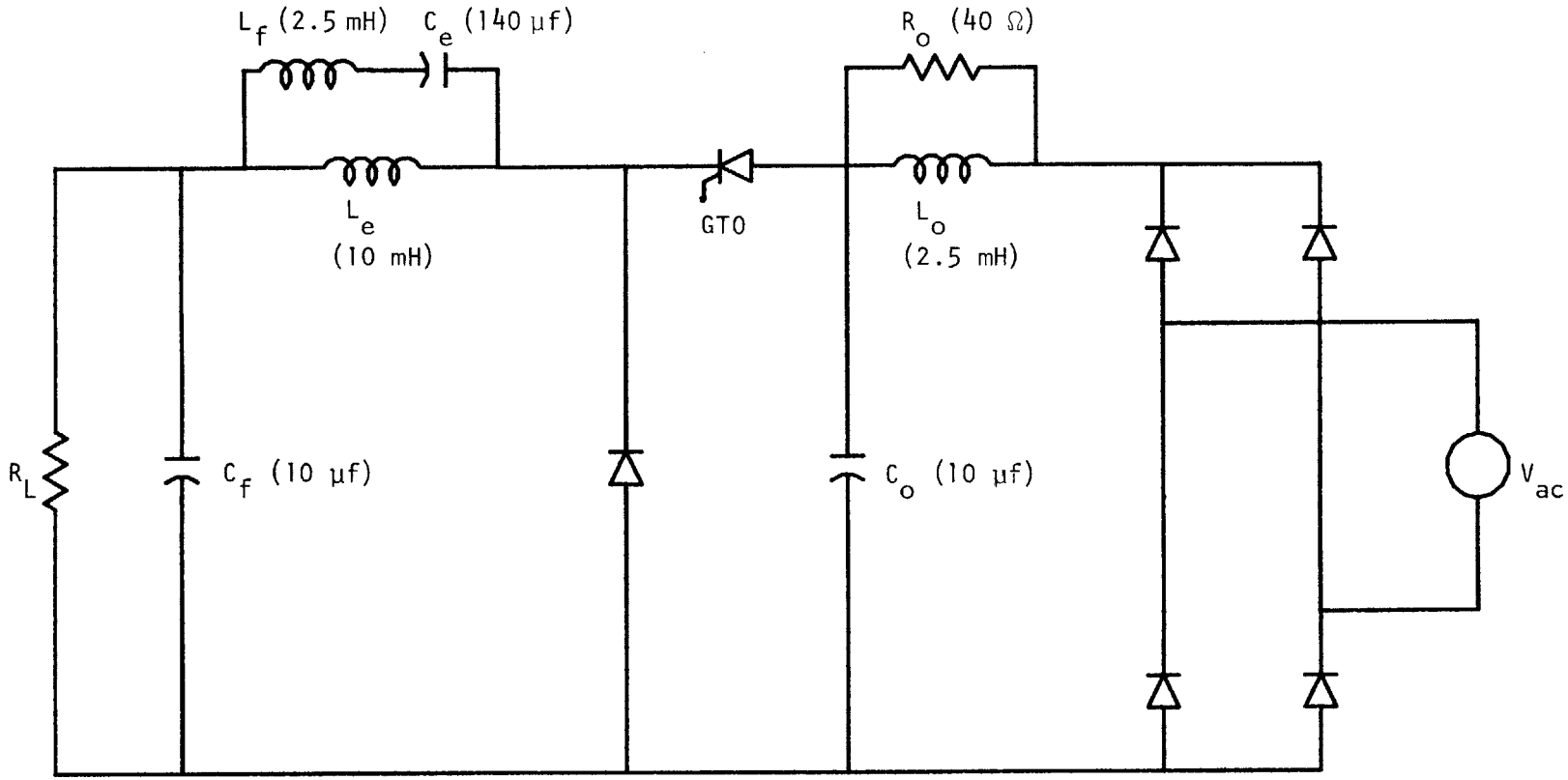


Fig. 6-2: The Power Circuit.

necessary energy storage for load balancing. Inductor L_f and capacitor C_f form a second-order low-pass filter that keeps the load voltage free of switch frequency components. Inductor L_o, capacitor C_o, and resistor R_o form a damped low-pass filter that removes the switch frequency components from the ac current waveform.

Power Level Limits

The power circuit is designed to operate from a 208V utility service. The peak of this ac voltage is 300V; the highest possible dc voltage is therefore 150V. Since all semiconductor devices in the power circuit are capable of withstanding 600V, the interface could have been designed for nearly twice the power rating, but an appropriate service was not available. If the interface is to be used in a higher ac voltage application, however, the natural impedances of the circuit's filters will have to be changed correspondingly.

The gate turn-off thyristor is the semiconductor device that limits the current level in this power circuit. The GTO (part no. GFF90A6 from Hitachi) has a peak controllable current of 90A but an rms rating of only 42A. Since, during full power operation, the GTO's duty cycle remains near unity for several milliseconds around the peak of the ac waveform, the load current must be limited to this rms rating. No attempt should be made to obtain a higher current level, even if the GTO could handle it, because doing so will saturate the inductors of the power circuit.

With a maximum dc voltage of 150V and a maximum dc current of 40A, the power that can be delivered to the load is 6kW. To achieve this

level of power, the load resistor must be equal to 3.75 ohms. If a smaller resistor is used, the dc voltage must remain sufficiently below 150V to keep the GTO's rms current within its rating.

Filter Design

The resonant load balancing filter was designed to give a peak 120 Hz ripple in the load current of 1A. This level corresponds to 2.5% of the dc component when the load resistor is 3.75 ohms. To obtain this performance, the resonant filter must have a 120 Hz impedance of 150 ohms. The impedance of inductor L_e should therefore be 150 ohms divided by the Q of the filter.

As discussed in Chapter IV, a (Q R) product of unity would give the smallest possible load balancing inductor. With R equal to 2.5%, the Q of the filter should therefore be set equal to 40. Because such a filter is difficult to both build and keep tuned, a filter with a Q of 20 was used instead. This reduction of Q is not costly; the size of L_e is only 12.5% larger than its minimum value.

With the impedance and the Q of the resonant filter known, the value of the energy storage inductor can be directly determined.

$$L_e = \frac{Z}{2\omega_o Q} = \frac{150}{2(377)(20)} = 10 \text{ mH} \qquad (6\text{-}1)$$

Because there is only a dc and a 120 Hz component in the flux of this inductor, it can be constructed from a laminated iron core. The copper will carry an rms current of 42.4A at full power.

The high frequency filter on the dc side of the power circuit was

designed with a resonant frequency of 1 kHz. The approximate factor of ten between this frequency and the switch frequency attenuates the 9.6 kHz components present in the voltage across the high frequency diode by 40 dB. The actual values of the inductor and capacitor were chosen to limit the high frequency current in the inductor to 1A. The variation of the flux in L_f that results from this high frequency current is very small; a laminated iron core can again be used. The high frequency current requirements of the capacitor are also quite easy to achieve with an inexpensive device.

Once the values of L_e and L_f have been determined, the value of the resonant filter's capacitor, C_e, can be calculated.

$$C_e = \frac{1}{(2\omega_o)^2 (L_e + L_f)} = 140\ \mu f \qquad (6\text{-}2)$$

As discussed in Chapter V, the design of the ac-side filter for a separated waveform transformer involves many tradeoffs. The results of simulations were used to determine component values that would provide a suitable compromise among the various conflicting issues. The ac filter design finally chosen is identical to the one used in the example of Figure 5-4b. The resonant frequency of the filter is 1 kHz, the damping ratio is 0.2, and the attenuation at 9.6 kHz is 28 dB, or 4%.

Protection of the Semiconductor Devices

The schematic of Figure 6-2 is not complete; it lacks several components that are required to protect the semiconductor devices. Some of these additional components, the GTO's turn-on and turn-off snubbers,

are shown in Figure 6-3. The element values in these snubbers were chosen to give more than adequate protection. They could, if desired, be made smaller to increase the power circuit's efficiency.

Besides snubbers, varistors are also included in the power circuit to provide protection. These devices are needed because it is possible, at any point in the 60 Hz cycle, that the GTO will be turned off and kept off. This sudden departure from normal operation could be the result of the control circuit deciding that the power circuit should be turned off, or it could be the result of a gate drive failure. Whatever the cause, however, the energy stored in the ac side filter inductor L_o will have to flow into the capacitor C_o. It is possible, if the interruption occurs at full power and near the peak of the ac waveforms, for the capacitor voltage to exceed 1000V under this condition.

Since this voltage level is far greater than that which the GTO can withstand, a varistor has been placed across capacitor C_o to limit it. This varistor begins to clip the voltage at 475V and will allow the voltage to rise to only 600V when it is carrying 40A. It is capable of absorbing all the energy that the worst case would demand of it. Other varistors have also been placed in parallel with each inductor to make sure that, no matter what fails, the currents in the inductors will have paths through which to flow.

VI.b The Gate Drive Circuit

Figure 6-4 shows the schematic of the gate drive circuit. There are three parts to the circuit: an opto-isolator input, a pulse shaping section, and a power section. A +/-12V power supply is also included.

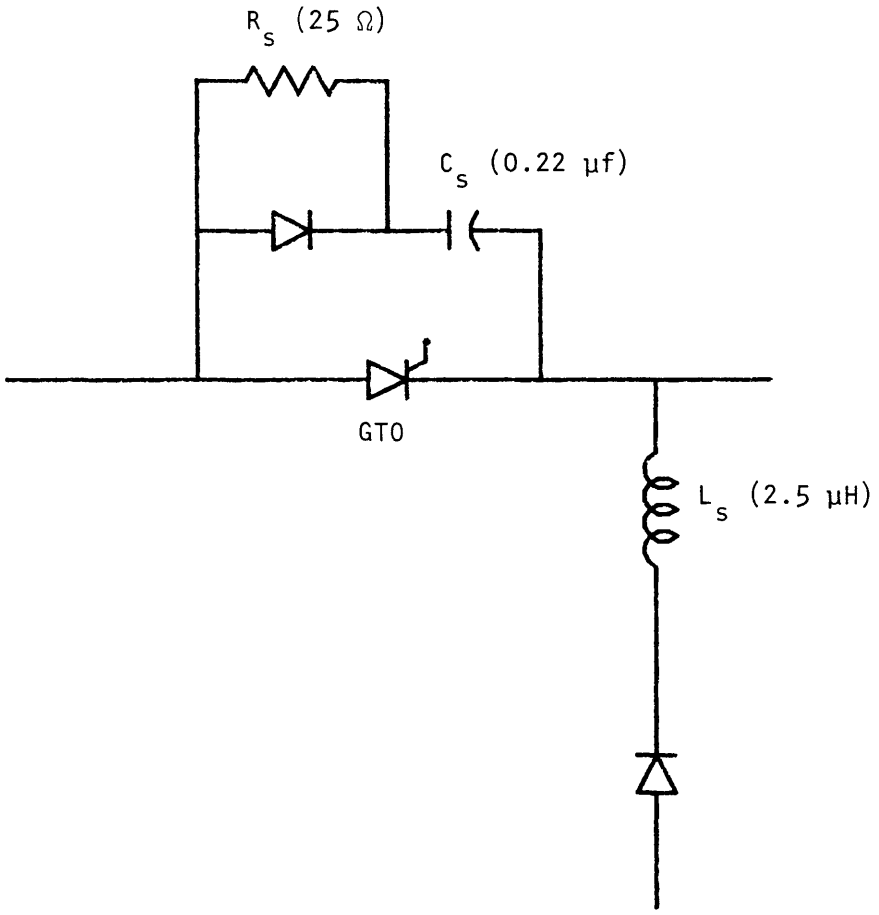


Fig. 6-3: The Turn-On and Turn Off Snubbers.

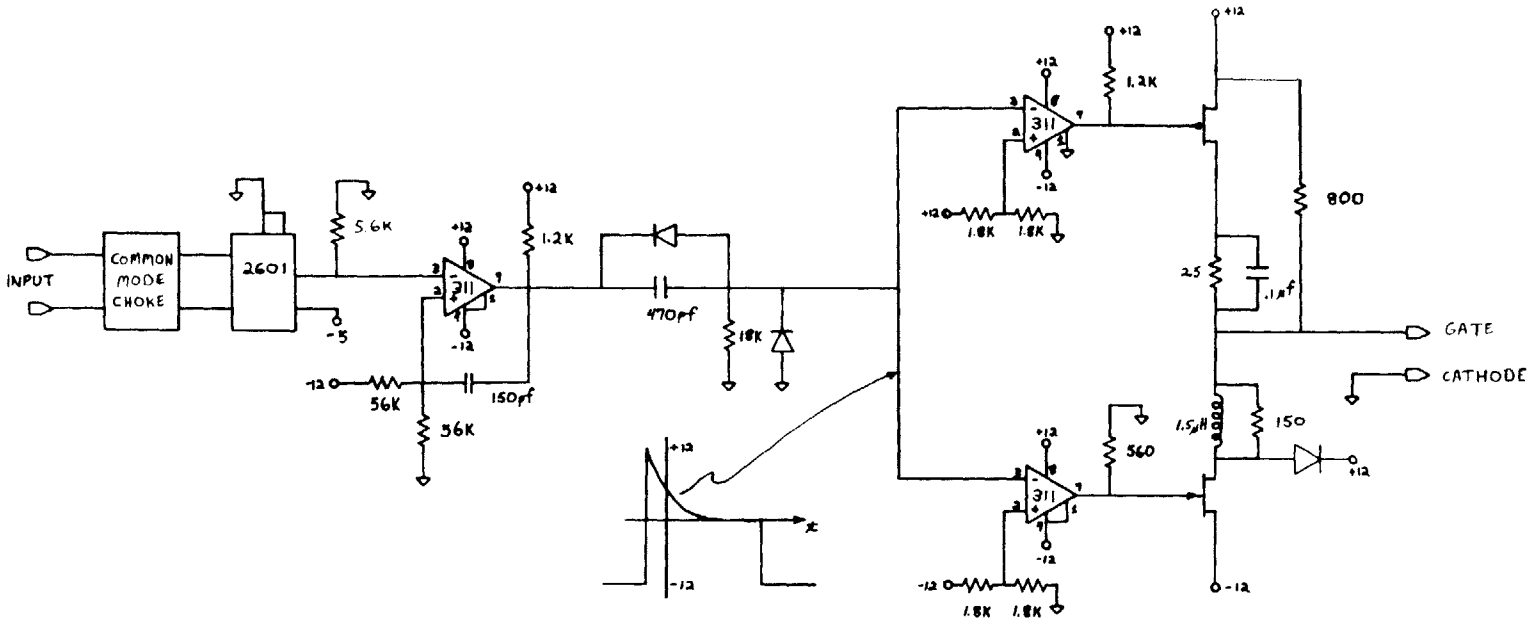


Fig. 6-4: The Gate Drive Circuit.

The circuit can easily provide the needs of the GTO's gate at 9.6 kHz and at full power.

The Isolated Input

The voltage potential between the control circuit and gate drive circuit undergoes a large step change every time the GTO turns on or off. The resulting current that flows through the coupling capacitance of the opto-isolator during these transitions is great enough to cause its output transistor to misfire. Three steps have been taken to eliminate this problem. First, an opto-isolator with a shield between its diode and transistor is used. Second, a common-mode choke is placed on the input leads of the opto-isolator to provide an impedance that will limit the flow of current. Finally, the output of the opto-isolator is passed through a comparator with ac hysteresis that will block further signals for approximately 1 μsec. after an initial transition is received.

The Power Section

The power section of the gate drive circuit uses MOS transistors because of their simple drive requirements, their fast switching times, and their large surge current ratings. When the control signal makes a transition from low to high, the top transistor of the power section pulls the GTO gate up to +12V through a 2.5 ohm resistor. This resistor has a parallel capacitor that gives an initial overshoot of gate current to help the GTO turn on faster. The capacitor also improves the gate current's initial rate of rise by compensating the parasitic

inductance of the wires leading to the GTO. After 6 μsec., the pulse shaping circuitry turns the pull-up transistor off and the GTO gate is left connected to the +12V supply through a 800 ohm resistor. This design keeps the average current requirement of the +12V power supply and the average power of the GTO gate input low.

Whenever the control signal returns low, the bottom transistor of the power section is turned on and the top transistor, if still on, is turned off. In this state, the gate of the GTO is pulled down to -12V through a 2.5 μH inductor. This inductor limits the rate of rise of the negative gate current to avoid catastrophic crowding of the anode/cathode current in the GTO. Its component value is twice that which is recommended by the GTO manufacturer.

The Pulse-Shaping Section

The pulse-shaping section of the gate drive circuit is a simple R-C-diode network and two comparators. The schmatic shows the waveform seen at the inputs of the comparators. When the control signal is set high, this waveform immediately steps up to +12V and then decays with a 9 usec time constant. From the initial rise until the waveform reaches +6V, the top comparator will turn the pull-up transistor on. When the control signal returns low, the waveform immediately drops to -12V and stays there. In this condition, the bottom comparator turns the pull-down transistor on. The output impedance of both comparators is small enough to turn the MOS transistors on and off within 50 nsecs.

Waveforms of the gate current at both turn-on and turn-off are given in the last section of this chapter.

VI.c The Control Circuit

Since the power circuit design allows open-loop control of the ac current waveform, the pattern of the gate drive signal is a rectified 60 Hz sinusoid that can be predetermined. The pattern need only be synchronized to the ac voltage waveform. With a resistive load, the power level can also be controlled in an open-loop manner. The dc voltage will be directly proportional to the peak instantaneous duty cycle of the pattern sent to the GTO. Power flow can be controlled by changing this magnitude.

The delay between the control signal and the transition of the GTO is a function of the load current and the ac voltage. To compensate for it, the duty cycle patterns are stored digitally, in table form. Each entry of each table is adjusted from its ideal value by the correct amount to get the actual duty cycle desired. Whenever the duty cycle is beyond the maximum or minimum obtainable, consecutive table entries are set such that the average duty cycle over several switching periods is correct.

Figure 6-5 show the schematic of the control circuit. There are two microprocessors in this circuit. One, the pattern processor, stores twelve tables of switch patterns, one for each of twelve different dc voltage levels. Together with a counter, this processor provides the duty cycle signal to the gate drive circuit. The other microprocessor, called the control processor, provides the synchronization with the utility, the control of the dc voltage level, and the start-up and turn-off functions. The software programs for both microprocessors are presented in the Appendix.

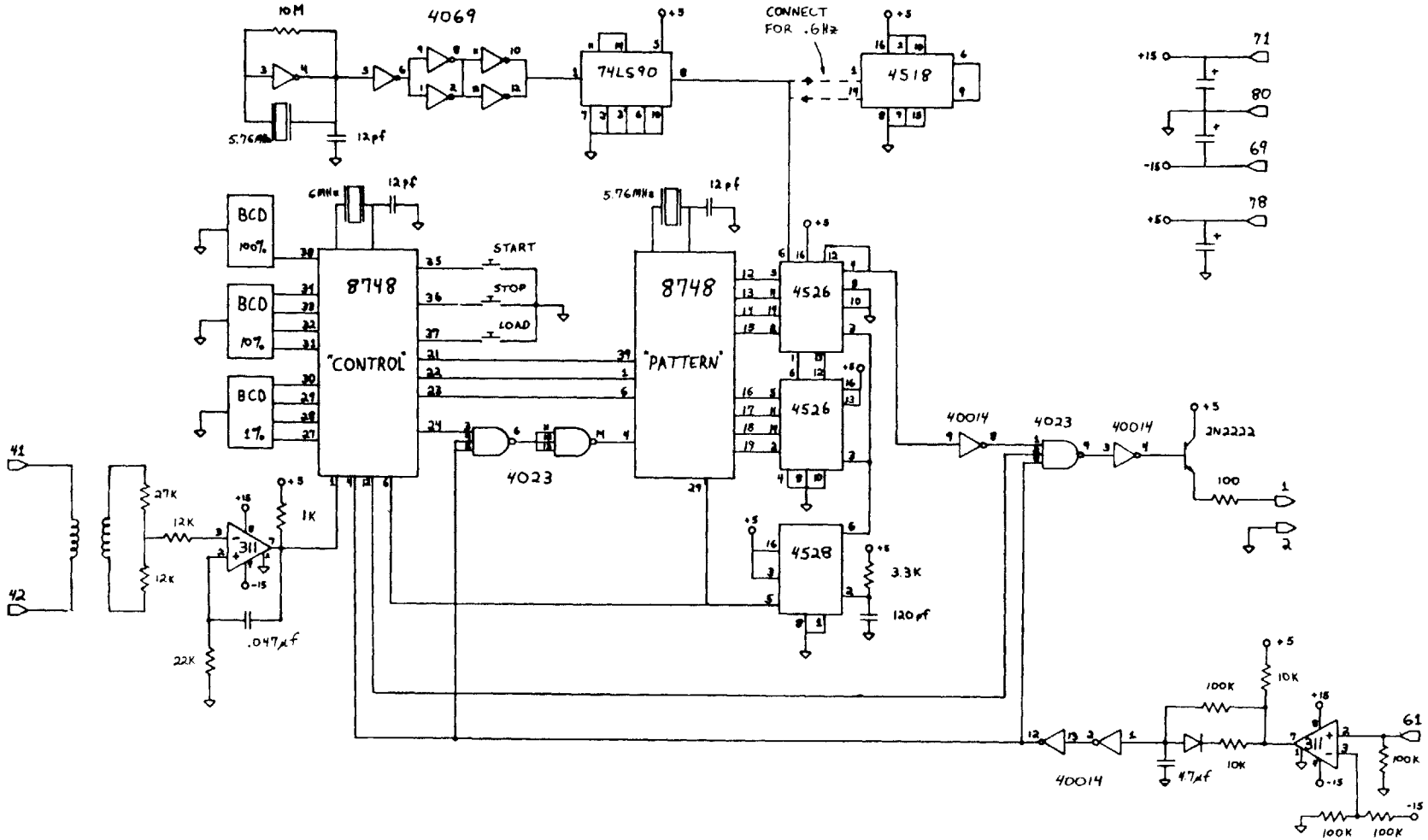


Fig. 6-5: The Control Circuit.

The Pattern Processor

With a 9.6 kHz switching frequency, there are exactly 160 switch periods during one 60 Hz cycle. To limit the size of the duty cycle pattern tables, each table contains entries for only one quarter of the fundamental cycle. A table is alternately read forward and backward to get the full pattern waveform desired.

Each switch period is 104 μsecs long. The pattern processor is not, by itself, fast enough to provide a reasonably resolved duty cycle signal for this short a period. Instead, at the beginning of each period, the processor fetches the appropriate entry from the tables in its memory and loads it into an external down-counter. From the beginning of the period until this counter reaches zero, the duty cycle signal sent to the gate drive circuit is high. Once the counter reaches zero, the signal returns low and stays there until the start of the next period. For reasons that involve the timing of the pattern processor, there are 120 counts per switch period. This number of counts gives an adequate resolution to the duty cycle signal.

Four control signals are sent to the pattern processor from the control processor. One indicates the location of the ac voltage's negative to positive zero-crossing. Whenever this signal is received, the pattern processor adjusts its table pointer to the starting address of the current table. The other three inputs control which of the twelve tables will be read. One input, when activated, forces the first, or lowest dc voltage, table to be used. The other two inputs are signals for the pattern processor to change to either the next higher or next lower table. A change from one table to another can occur at any

time in the cycle. The entry read from the new table corresponds to the present position in the 60 Hz cycle; synchronization with the utility is not lost.

The Control Processor

A major function of the control processor is to provide synchronization with the utility. To accomplish this task, the processor has two inputs. One is a digital signal that indicates the polarity of the ac voltage waveform. The other is a signal from the pattern processor that indicates the beginning of each switch period. When the polarity signal undergoes a low to high transition, the control processor sends the synchronization signal to the pattern processor and clears a switch period counter. Each time a pulse is received at the end of a switch period, this counter is incremented.

The switch period counter should be equal to 160 at the next negative to positive zero-crossing of the ac voltage waveform. If the zero-crossing occurs outside a window of plus or minus four counts from 160, the control processor decides that synchronization has been lost. At this point, the control processor inhibits the duty cycle signal sent to the gate drive circuit and forces the pattern processor to read its lowest table. Once synchronization has been lost, there must be sixteen consecutive cycles during which the zero-crossing occurs within the window before the control processor will allow normal operation to resume.

When the control circuit's power is first turned on, the control processor forces the pattern processor to read its lowest table. Since

tables are changed only under its commands, the control processor will always know which table is currently being used. The desired table can be chosen by setting the three BCD switches on the circuit board. The three digits indicate the resulting dc voltage as a percent of its maximum value. Table 6-1 (located at the end of this chapter) shows which twelve of the entries correspond to the present tables. The control processor reads the BCD switches only when the "LOAD" button is depressed.

When the dc voltage level is changed, the control processor limits the rate at which this change can be made. At present, only one table change can take place every switch period, or 104 μsecs. A change from the lowest to the highest table will therefore take 1.04 msecs. This time is moderately short compared to the dynamic response of the load balancing filter.

"START" and "STOP" buttons are provided to enable and inhibit the signal sent to the gate drive circuit.

Power-up and Power-down Protection

As the ac power for the control circuit makes its transition during power-up and power-down, the processors are not guaranteed to operate correctly. To avoid false, and possibly damaging, gate control signals, a special inhibit circuit is provided. This circuit observes the ac waveform and detects its presence or absence within one quarter cycle. When power is lost, the gate drive signal is immediately inhibited and the two processors are reset. At power-up, the inhibit and reset signals remain active for 100 msecs. This time is long enough to ensure

the supply voltage will reach its operating value before the signals are removed.

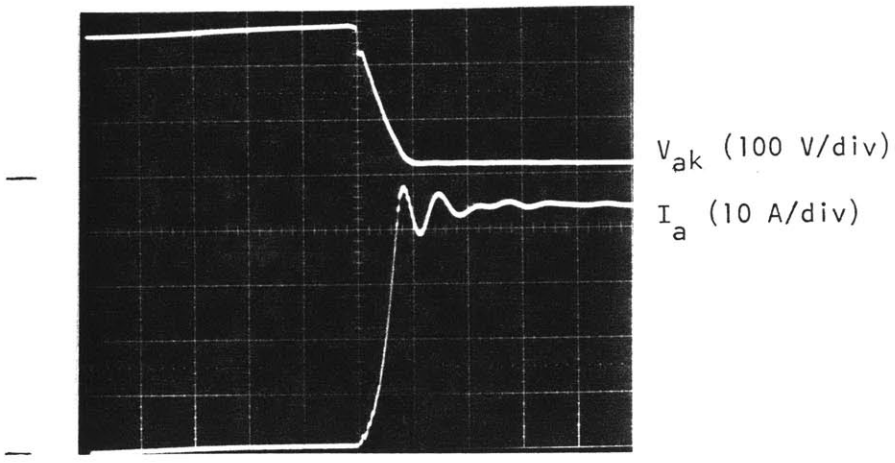
VI.d GTO Switch Transitions

The high frequency operation of the GTO is shown in Figures 6-6 and 6-7. For these figures, the GTO and high frequency diode were used as a dc-dc converter at 250V and 40A. These levels correspond to an operating point near the peak of the ac waveforms at full power. Figure 6-6 shows the details of the turn-on transition; Figure 6-7 shows the details of the turn-off transition. In both figures, the gate current and voltage are also shown.

VI.e Interface Performance

Figure 6-8 shows waveforms of the ideal interface when it is operating at full power. The ac current waveform has approximately 4.5% total harmonic distortion. Table 6-2 lists the magnitude of the individual harmonic components. As can be seen, the third and the fifth harmonics dominate the others and the switch frequency components are very small. The oscillation of the ac filter is responsible for the components around the 17^{th} harmonic. The dc voltage and current at full power have a peak 120 Hz ripple of approximately 3.5% and a peak switch frequency ripple near 1%.

The utility voltage waveform shown in Figure 6-8 is distorted. This distortion (mostly composed of 2.5% fifth harmonic) is not caused by the operation of the ideal interface, however; it is present in the waveform even when the interface is not operating. Figure 6-9 compares



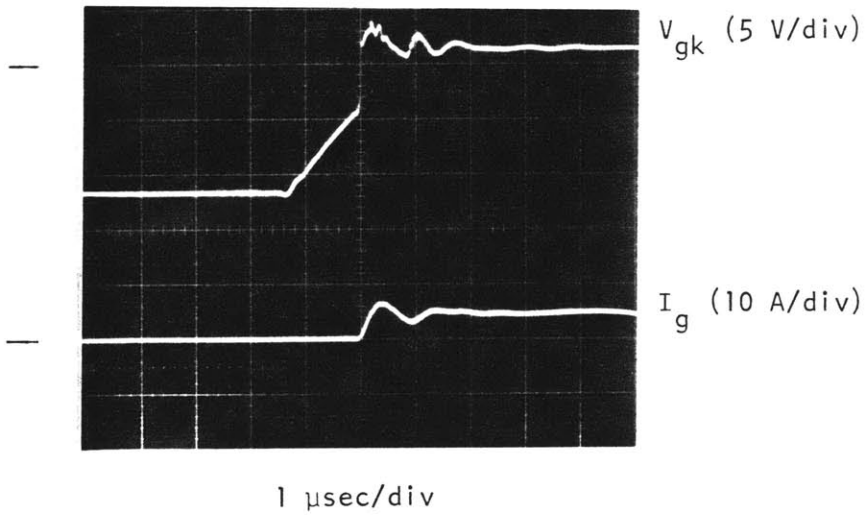
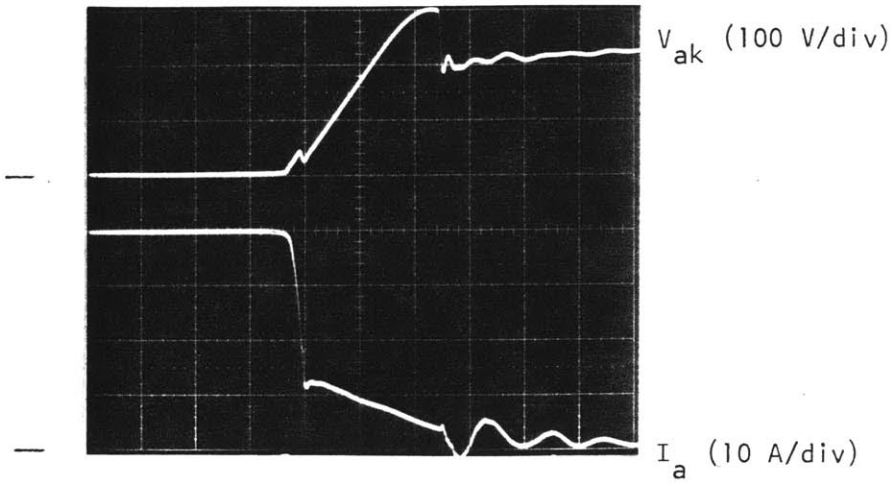


Fig. 6-6: GTO Turn-On Transition.



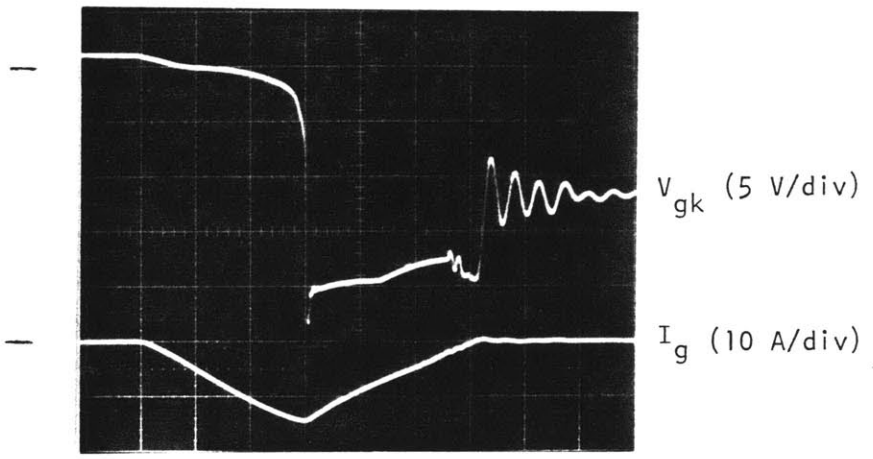
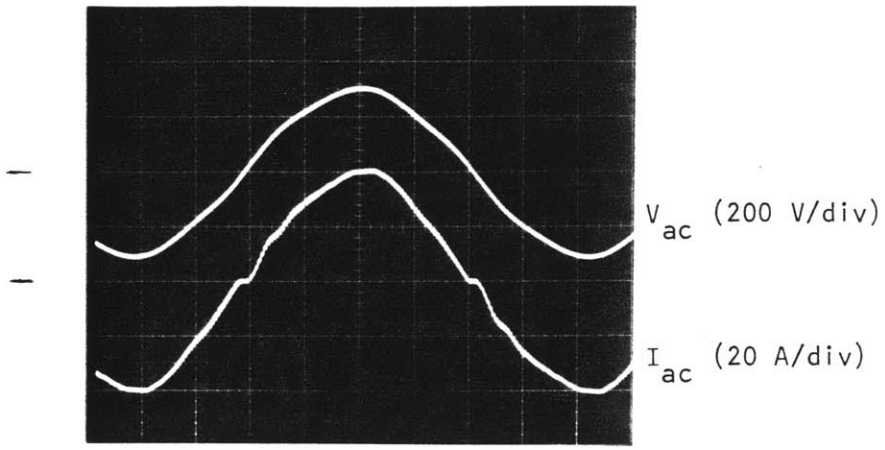


Fig. 6-7: GTO Turn-Off Transition.



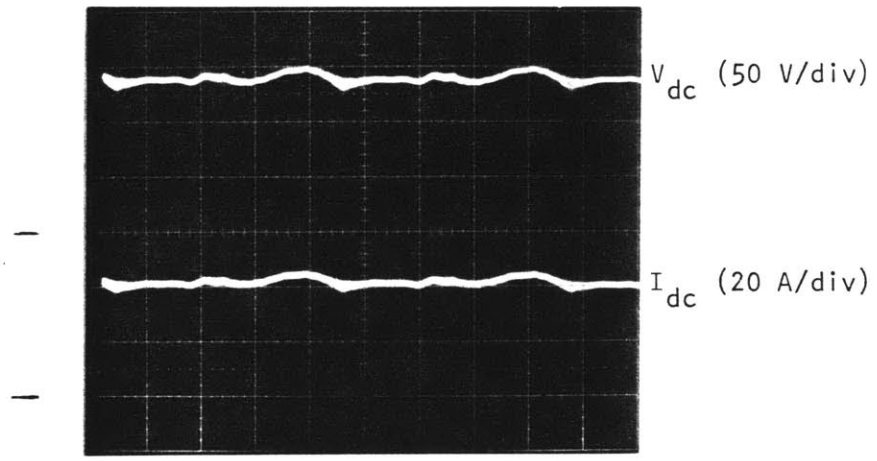
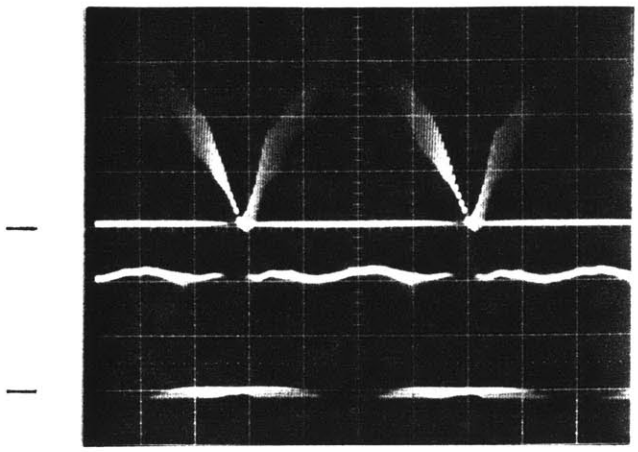


Fig. 6-8: Waveforms showing Full Power Operation



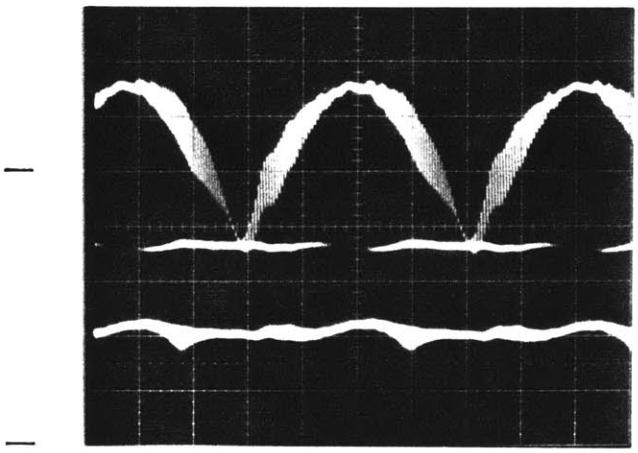


Fig. 6-8 (cont'd): Waveforms showing Full Power Operation.

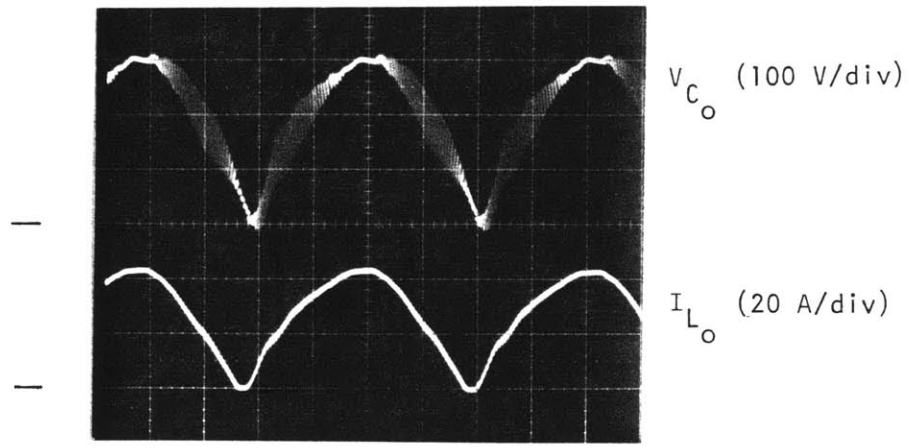


Fig. 6-8 (cont'd): Waveforms showing Full Power Operation.

the utility voltage waveform when the interface is turned off and when the interface is at full power. The waveforms appear identical and the measured increase in distortion levels was negligible.

The waveforms presented in Figure 6-10 compare the interface's operation at various power levels. Table 6-3 lists the total harmonic distortion of the ac current and Table 6-4 lists the peak ripple in the dc current for each of these power levels. These tables relate the level of distortion to the fundamental and dc currents at both the respective power level and at full power.

As Table 6-3 shows, when power is reduced from the maximum level, the ac current becomes more distorted. There are two reasons for this. First, the reactive requirements of the ac filter become greater in proportion to the level of power flow; the cross-over distortion and the oscillation that results have a greater impact on the ac current waveform. Second, because the duty cycle throughout the waveform is smaller for the lower power levels, the relative resolution with which the duty cycle can be set is correspondingly larger.

The efficiency of the interface at full power is approximately 90%. 3.5% is lost in L_e and 3% is dissipated in the high frequency switches and the snubbers. The rest is dissipated in the bridge diodes (1%) and the filter elements (2%). Table 6-5 gives the measured efficiencies for each of several power levels. These efficiencies are only approximate.

Figures 6-11a and 6-11b show how the interface responds to a large step change in power level. The ac current waveform changes immediately; the dc current response is affected by the tuned load balancing filter. If the affect of L_f and C_f are ignored, the response

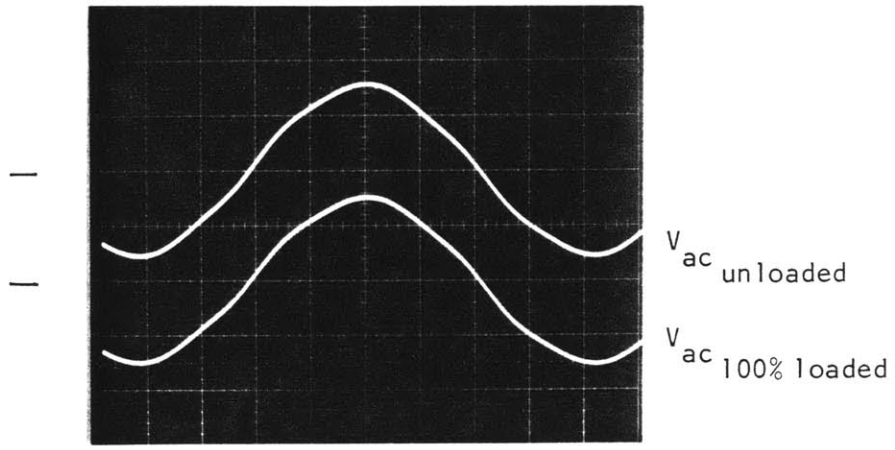
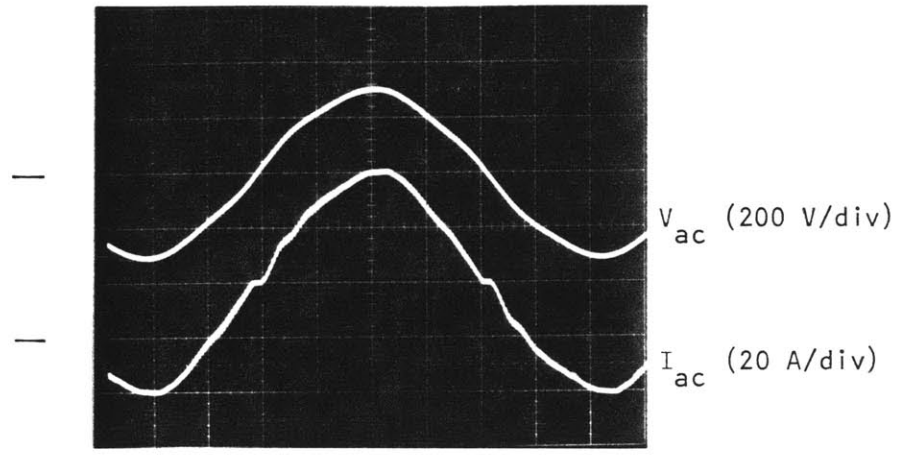
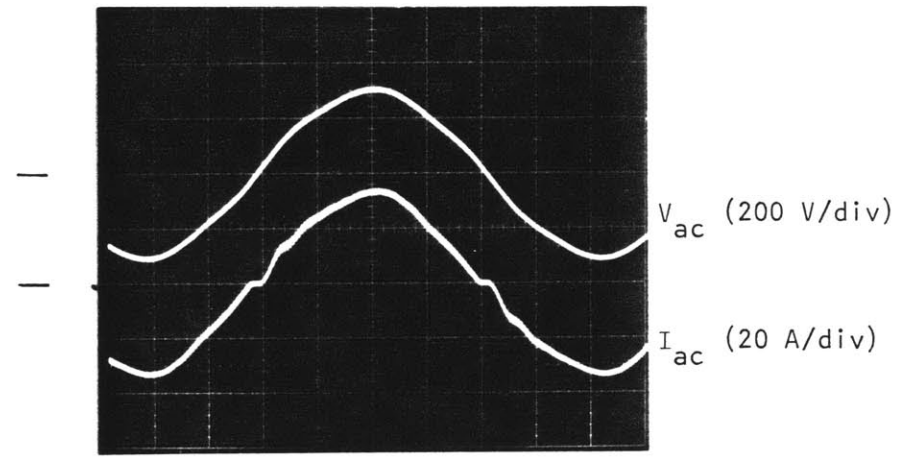


Fig. 6-9: Effect on Utility Voltage Waveform.

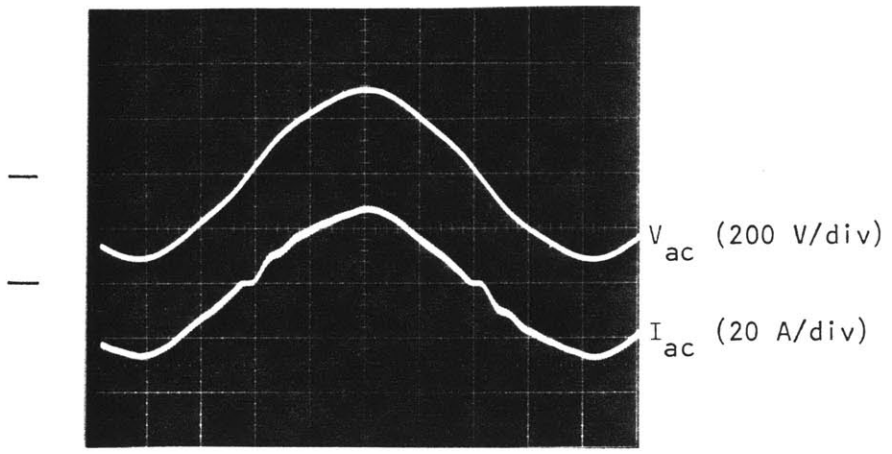


100% Power

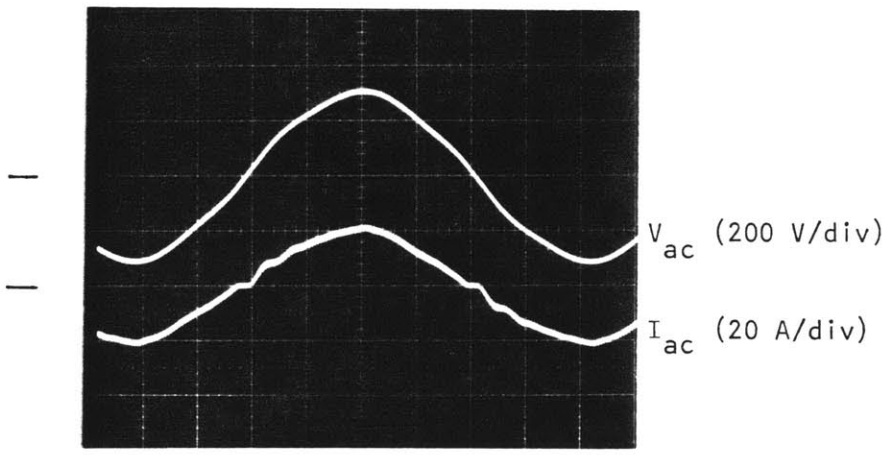


80% Power

Fig. 6-10: Waveforms Comparing Operation at Different Power Levels.

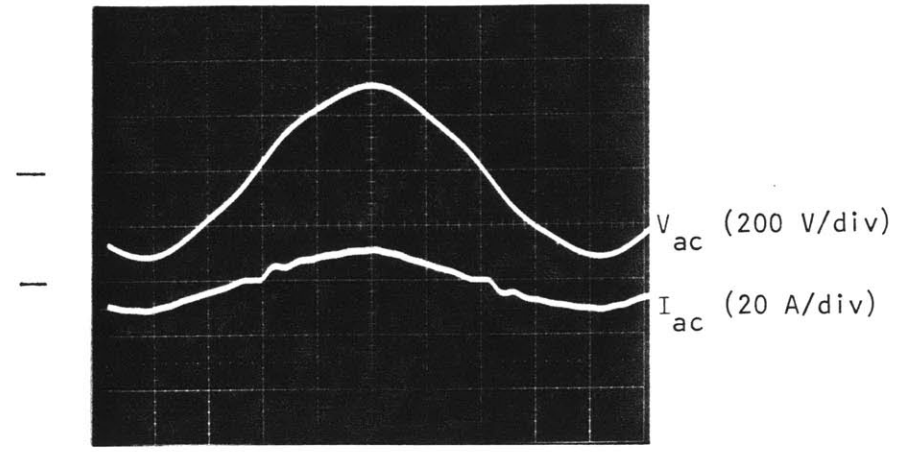


65% Power

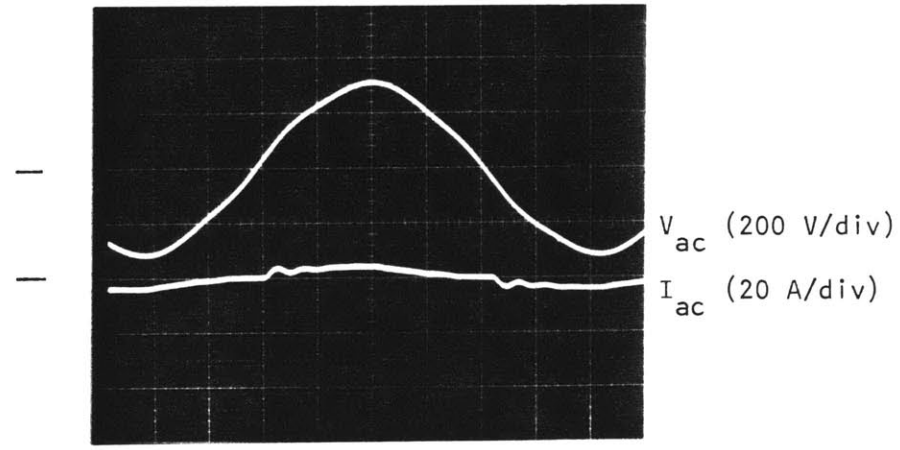


50% Power

Fig. 6-10 (cont'd): Waveforms Comparing Operation at Different Power Levels.



25% Power



10% Power

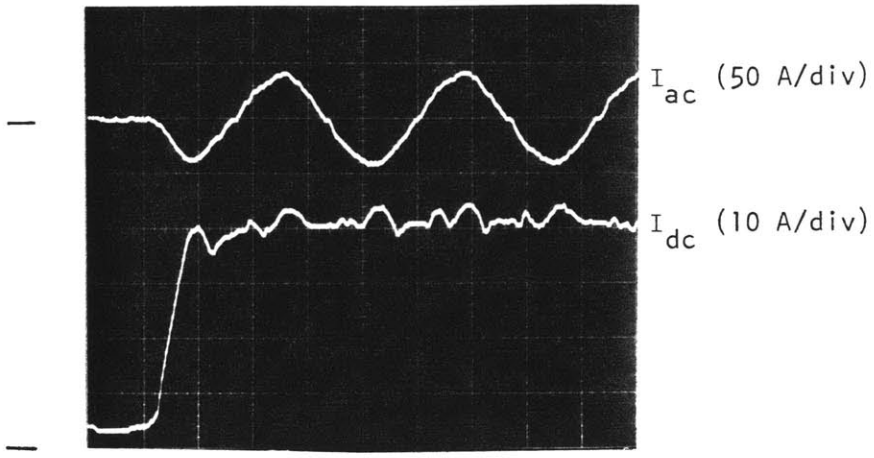
Fig. 6-10 (cont'd): Waveforms Comparing Operation at Different Power Levels.

of the load current is governed by the following equation

$$\frac{I_{dc}}{Control} = \left(\frac{1}{R_L}\right) \frac{(S/\omega_n)^2 + 1}{(S/\omega_n)^2 + 2\xi(S/\omega_n) + 1} \qquad (6\text{-}3)$$

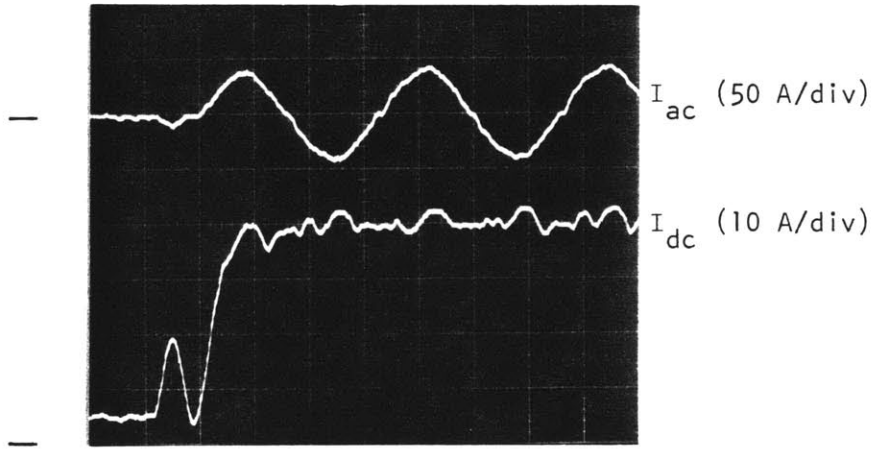
where $\omega_n = \sqrt{1/\ L_e C_e} = 2(377)$ rad/sec and $\xi = \sqrt{L_e/C_e}\ /2R_L = 1.13$.

The zeros of this response are the cause of the dc current's initial misdirection. If the step change occurs near the zero-crossing of the ac current, the misdirection is very small because there is no immediate change in the power flow presented to the load balancing filter. If, on the other hand, the step change takes place near the peak of the ac current waveform, the initial misdirection is much larger. Examples of the two different responses can be compared in Figure 6-11.



5 msec/div

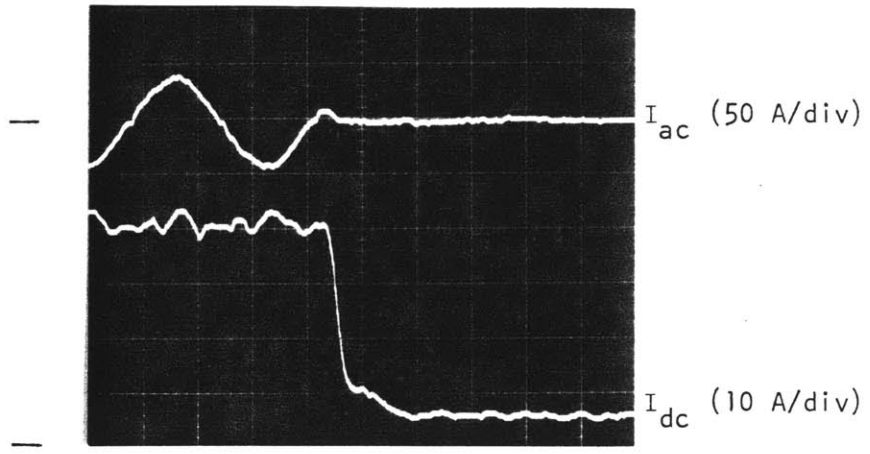
From 1% to 100% power at the zero-crossing



5 msec/div

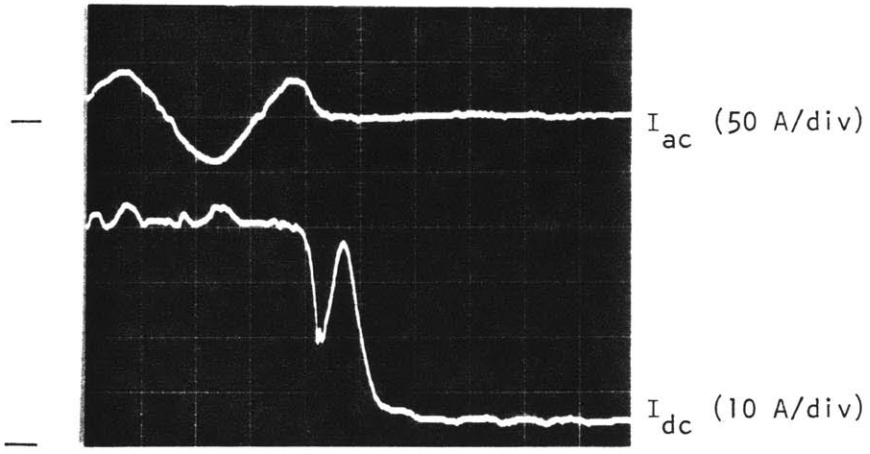
From 1% to 100% power at the peak

Fig. 6-11a: Response to a Large Step Change in Power Level.



5 msec/div

From 100% to 1% power at the zero-crossing



5 msec/div

From 100% to 1% power at the peak

Fig. 6-11b: Response to a Large Step Change in Power Level.

Table 6-1

The Twelve Table Entries in the Pattern Processor

Table Number	DC Voltage (% of 150V)
1	10%
2	20%
3	30%
4	40%
5	50%
6	60%
7	70%
8	80%
9	85%
10	90%
11	95%
12	100%

Table 6-2

The Harmonic Content of the AC Current

Harmonic	Content
3	3.0%
5	2.5%
7	1.0%
9	1.0%
11	1.0%
13	1.0%
15	1.0%
9.6 kHz	.5%

Table 6-3

AC Current Distortion for Various Power Levels

Power Level (% of full power)	THD (relative to fundamental)	THD (relative to full power)
100%	4.5%	4.5%
80%	4.5%	3.6%
65%	5.3%	3.5%
50%	6.2%	3.1%
25%	8.6%	2.2%
10%	20.7%	2.1%

Table 6-4

DC Current Ripple for Various Power Levels

Power Level (% of full power)	THD (relative to dc current)	THD (relative to full power)
100%	3.5%	3.5%
80%	3.7%	3.0%
65%	4.0%	2.6%
50%	4.1%	2.0%
25%	4.6%	1.2%
10%	5.0%	.5%

Table 6-5

Power Circuit Efficiency at Various Power Levels

Power Level (% of full power)	Efficiency
100%	90%
80%	89%
65%	89%
50%	87%
25%	84%
10%	76%

CHAPTER VII

CONCLUSIONS

The distortion of the electric utility system has caused widespread concern, not because the present level is unacceptably high, but because the dominant sources of the harmonic components, power conditioned loads, are rapidly increasing in number and total power rating. Although it is impossible to predict the complete effect of this increase, the potential for significant degradation of the system's service is great. At some point, corrective measures will be required.

The purpose of this thesis has been to propose one possible corrective measure: the use of power conditioning interfaces designed to draw ac currents with very low distortion levels. This approach to the harmonic distortion problem of the future has several virtues. First, it avoids those complex and intangible aspects of the distortion issue that make other corrective measures impossible to implement. Instead, it focuses efforts onto a single and well defined goal, that of making an ideal interface. Second, it addresses exactly that portion of the distortion problem that is the fastest growing and the most difficult to control: the emergence of mass-produced and widely distributed conditioned loads in the low- and medium-power ranges. Finally, no matter how many conditioned loads are installed as time goes on, the use of an ideal interface is a complete solution that requires no further modification to keep the utility's distortion level under control.

Once the task of developing an ideal utility/dc interface is embraced, certain issues about its design and its beneficial features

become clear: 1)Active waveshaping is a much more flexible and workable approach than passive waveshaping; 2)Unity power factor operation is actually easier to achieve than operation at any other power factor; 3)The tuning of the load balancing filter results in much smaller storage elements and a much faster rate at which the power level can be changed; 4)The interface's control system may be either open- or closed-loop, depending on the characteristic of the dc system; and 5)For a closed-loop system, the time-varying nature of the power circuit presents difficulties that can be overcome by using time-varying feedback gains. These issues are briefly outlined below.

One way to achieve an ideal interface is to use passive waveshaping techniques. In this approach, a filter composed of several series-resonant shunt filters is used to remove the harmonic components from the ac current waveform. But because the performance of this filter is easily affected by the impedance of the utility, it is not possible to come up with a single design that will work well at all installation sites. Instead, it is necessary to devote engineering effort to the design of each power circuit installed. Since this is not feasible for the large number of low- and medium-power conditioned loads, the use of passive waveshaping in these applications must be accompanied with a willingness to accept whatever level of performance results from a fixed power circuit design.

Ideal interfaces designed with active waveshaping techniques, by contrast, are very tolerant of conditions at the location of installation. The extent to which the utility can exert influence on the operation of such a circuit is negligible, and it is therefore easy

to ensure the quality of the ac current waveform no matter where the interface is installed. This feature makes the active waveshaping technique an approach well suited to the special requirements of low- and medium-power conditioned loads.

The passive waveshaping approach does offer the correction of reactive power flow, a feature which helps offset the cost of the filter. It does so with very little flexibility, however; the level of reactive power supplied by the filter can not be altered, even though the needs of the power circuit change with power level. Fortunately, the active waveshaping approach does not have this limitation; it inherently offers control of power factor at all times, no matter what the operating condition. In fact, for single-phase operation, an active interface that operates only at unity power factor is actually simpler and less expensive than one that can deliver or absorb reactive power.

An active waveshaping design also offers much more than the control of reactive power. One very important additional benefit is the ability to use a simple resonant circuit for the dc side load balancing filter. Such a design reduces, by a factor of ten or more, the peak energy this filter must store compared to that which would be needed by a filter that was not tuned. Besides the significant reduction in the filter's size, weight, and cost that results, the smaller storage elements also allow the interface's power level to be changed at a correspondingly faster rate. Step changes from zero power to full power can be completed in one quarter of a 60 Hz cycle rather than the five or ten cycles needed for a circuit that does not use a tuned filter. These beneficial features will, themselves, partially justify the cost of the

high frequency, waveshaping switches. The cost of the low distortion in the ac current waveform will therefore not be as great as it might otherwise be.

The active ideal interface requires a control system to determine the correct instants for the high frequency switch transitions. If the dc system is a current source, this control system can use an open-loop scheme. If the dc system is a voltage source, however, then the control system will have to use a closed-loop scheme. The closed-loop control of an ideal interface is difficult because the power circuit's incremental dynamics are dependent on the operating point and are therefore time-varying. Fortunately, this difficulty can be overcome by using feedback gains that adapt to the changing dynamics.

With the semiconductor devices currently available, it is technically feasible to apply active waveshaping techniques to conditioned loads in the low- and medium-power ranges (up to about 100 kW in a three-phase system). This thesis has presented a 6 kW, single-phase converter that uses a semiconductor device technology (GTO) well suited for much higher power levels. Whether or not the active ideal interface is economically feasible is yet to be proven, however. Although it is reasonable to expect the cost of harmonic-free power conditioning circuits to be high at first, the size of the market to which they will be sold, once they are regarded as necessary, is so great that the price will not remain exorbitant. We will pay extra for power circuits that treat the utility system as well as they treat the load, but the additional cost will not be unduly high and the freedom from harmonic distortion problems is a valuable asset to be obtained.

APPENDIX

SOFTWARE PROGRAMS FOR CONTROL CIRCUIT MICROPROCESSORS

```
;
;
;
;              *** SOFTWARE FOR THE PATTERN PROCESSOR  ***
;
;
;
;This program can work with a fundamental of 60 Hz for
;normal operation or with a fundamental of .6 Hz for
;simulation studies.  Each of the three START routines must
;be modified to switch between the two modes.  Two lines must
;be deleted and one line must be added to get .6 Hz operation.
;These lines are marked in the program.
;
        ORG 00H
;
;
;
RESET:  dis i                   ;disable the interrupt
        jmp INIT                ;jump to the initialization routine
;
;
;
        ORG 03H
;
;Part 1 of table-group 0 routine
;
START0: movp a,@a               ;get on-time from table entry
        outl BUS,a              ;send entry to counter
        anl P1, #00000000b      ;load counter
        movp3 a,@a              ;take out for .6 Hz
        orl P1, #00000100b      ;
        movp3 a,@a              ;take out for .6 Hz
;       call WAIT               ;put in for .6 Hz
        jf0 LBL10               ;if 0-90 degrees, jump
        inc r0                  ;increment table pointer
        jni LBL300              ;if sync signal is high, jump
        jt0 LBL400              ;if power increment signal is high, jump
        jt1 LBL50               ;if power decrement signal is high, jump
        jmp LBL70               ;otherwise, jump to LBL70
;
;
;
        ORG 16H
;
;Table for on-time at 10% current level
```

```
;
        DB      1
        DB      4
        DB      1
        DB      4
        DB      1
        DB      4
        DB      1
        DB      3
        DB      1
        DB      3
        DB      1
        DB      3
        DB      1
        DB      4
        DB      1
        DB      3
        DB      1
        DB      3
        DB      1
        DB      3
        DB      1
        DB      2
        DB      1
        DB      2
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
;
;
;
        ORG 40H
;
;Part 2 of table-group 0 routine
;
LBL10:  dec r0                  ;decrement table pointer
        jni LBL300              ;if sync signal is high, jump
```

```
        jt0 LBL400              ;if power increment signal is high, jump
        jt1 LBL50               ;if power decrement signal is high, jump
        nop                     ;
        nop                     ;
LBL70:  nop                     ;
        nop                     ;
        mov a,r0                ;get table pointer
        jmp THIS0               ;jump to THIS0
;
;
;
        ORG 56H
;
;Table for on-time at 20% current level
;
        DB      14
        DB      14
        DB      14
        DB      14
        DB      14
        DB      13
        DB      13
        DB      13
        DB      13
        DB      13
        DB      13
        DB      12
        DB      12
        DB      12
        DB      12
        DB      12
        DB      11
        DB      11
        DB      10
        DB      10
        DB      10
        DB       9
        DB       8
        DB       8
        DB       8
        DB       7
        DB       7
        DB       6
        DB       6
        DB       5
        DB       5
        DB       4
        DB       4
        DB       3
        DB       2
        DB       2
        DB       2
```

```
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
;
;
;
        ORG 80H
;
;Part 3 of table-group 0 routine
;
LBL50:  mov a,r0                ;get the table pointer
        add a, r7               ;subtract one from the table indicator
        mov r0,a                ;put new value back in r0
        jc THIS00               ;if result is not negative, jump
        jmp INIT                ;jump to INIT
;
;
THIS0:  jb5 TOP0                ;if near top of the table, jump to TOP
BOTTM0: anl a,r2                ;mask off table number bits
        xrl a,r3                ;compare rest with 22
        jnz BEGIN0              ;if not equal, jump to BEGIN0
        mov a,r0                ;get the table pointer
        orl a, r6               ;set pointer to loc 23 of correct table
        mov r0,a                ;put new pointer value back in R0
        clr f0                  ;clear the f0 flag
        jmp START0              ;jump to START0
;
;
;
        ORG 96H
;
;Table for on-time at 30% current level
;
        DB      30
        DB      30
        DB      29
        DB      29
        DB      29
        DB      28
        DB      28
        DB      28
        DB      27
        DB      27
        DB      27
        DB      26
        DB      26
        DB      25
        DB      25
        DB      24
        DB      23
```

```
        DB      23
        DB      21
        DB      21
        DB      20
        DB      19
        DB      19
        DB      18
        DB      16
        DB      16
        DB      15
        DB      14
        DB      13
        DB      11
        DB      10
        DB       9
        DB       9
        DB       7
        DB       5
        DB       5
        DB       4
        DB       2
        DB       1
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 0C0H
;
;Part 4 of table-group 0 routine
;
THIS00: jmp THIS0
LBL300: jmp LBL30
LBL400: jmp LBL40
;
;
;
TOP0:   anl a,r2                ;mask off table bits
        xrl a, r2               ;compare counter with 63
        jnz BEGIN0              ;if not equal, jump to BEGIN0
        mov a,r0                ;otherwise, get the table pointer
        anl a, r4               ;set the counter to 61
        mov r0,a                ;put new value back in r0
        cpl f0                  ;set the F0 flag to one
        jmp START0              ;jump to START0
;
;
;
BEGIN0: nop                     ;
        nop                     ;
        nop                     ;
```

```
        mov a,r0                ;get table pointer
        jmp START0              ;jump to START0
;
;
;
        ORG 0D6H
;
;Table for on-time at 40% current level
;
        DB      43
        DB      43
        DB      43
        DB      42
        DB      42
        DB      42
        DB      41
        DB      41
        DB      41
        DB      39
        DB      39
        DB      39
        DB      38
        DB      37
        DB      36
        DB      35
        DB      34
        DB      33
        DB      32
        DB      31
        DB      30
        DB      29
        DB      27
        DB      26
        DB      24
        DB      23
        DB      21
        DB      20
        DB      18
        DB      17
        DB      15
        DB      14
        DB      12
        DB      10
        DB       9
        DB       8
        DB       5
        DB       4
        DB       1
        DB       1
        DB       1
        DB       1
;
```

```
;
;
        ORG 100H
;
;
;
        jmp RESET               ;jump to RESET
        nop                     ;
;
;
;
        ORG 103H
;
;Part 1 of table-group 1 routine
;
START1: movp a,@a               ;get on-time from table entry
        outl BUS, a             ;send entry to counter
        anl P1, #00000000b      ;load counter
        movp3 a,@a              ;take out for .6 Hz
        orl P1, #00000100b      ;
        movp3 a,@a              ;take out for .6 Hz
;       call WAIT               ;put in for .6 Hz
        jf0 LBL11               ;if 0-90 degrees, jump
        inc r0                  ;increment table pointer
        jni LBL311              ;if sync signal is high, jump
        jt0 LBL411              ;if power increment signal is high, jump
        jt1 LBL51               ;if power decrement signal is high, jump
        jmp LBL71               ;otherwise, jump to LBL71
;
;
;
        ORG 116H
;
;Table for on-time at 50% current level
;
        DB      57
        DB      56
        DB      55
        DB      55
        DB      55
        DB      54
        DB      54
        DB      53
        DB      53
        DB      52
        DB      51
        DB      50
        DB      49
        DB      47
        DB      47
        DB      46
        DB      44
```

```
        DB      43
        DB      42
        DB      40
        DB      39
        DB      37
        DB      35
        DB      33
        DB      32
        DB      30
        DB      27
        DB      26
        DB      25
        DB      22
        DB      20
        DB      17
        DB      16
        DB      13
        DB      11
        DB       9
        DB       7
        DB       5
        DB       2
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 140H
;
;Part 2 of table-group 1 routine
;
LBL11:  dec r0                  ;decrement table pointer
        jni LBL311              ;if sync signal is high, jump
        jt0 LBL411              ;if power increment signal is high, jump
        jt1 LBL51               ;if power decrement signal is high, jump
        nop                     ;
        nop                     ;
LBL71:  nop                     ;
        nop                     ;
        mov a,r0                ;get table pointer
        jmp THIS1               ;jump to THIS1
;
;
;
        ORG 156H
;
;Table for on-time at 60% current level
;
        DB      69
        DB      69
        DB      68
```

```
        DB      67
        DB      67
        DB      66
        DB      66
        DB      65
        DB      65
        DB      63
        DB      63
        DB      61
        DB      60
        DB      59
        DB      57
        DB      56
        DB      55
        DB      52
        DB      51
        DB      49
        DB      47
        DB      45
        DB      42
        DB      41
        DB      39
        DB      37
        DB      34
        DB      32
        DB      28
        DB      26
        DB      25
        DB      21
        DB      18
        DB      16
        DB      14
        DB      11
        DB       9
        DB       6
        DB       3
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 180H
;
;Part 3 of table-group 1 routine
;
LBL51:  mov a,r0                ;get the table pointer
        add a, r7               ;subtract one from the table indicator
        mov r0,a                ;put new value back in r0
        jc THIS11               ;if result not negative, jump
        jmp THIS0               ;otherwise, jump to THIS0
;
```

```
;
THIS1:  jb5 TOP1                ;if near top of the table, jump to TOP
BOTTM1: anl a,r2                ;mask off table number bits
        xrl a,r3                ;compare rest with 22
        jnz BEGIN1              ;if not equal, jump to BEGIN1
        mov a,r0                ;get the table pointer
        orl a, r6               ;set pointer to loc 23 of correct table
        mov r0,a                ;put new pointer value back in R0
        clr f0                  ;clear the f0 flag
        jmp START1              ;jump to START1
;
;
;
;
        ORG 196H
;
;Table for on-time at 70% current level
;
        DB      81
        DB      81
        DB      80
        DB      79
        DB      79
        DB      78
        DB      78
        DB      77
        DB      75
        DB      75
        DB      74
        DB      73
        DB      71
        DB      70
        DB      67
        DB      66
        DB      64
        DB      62
        DB      60
        DB      57
        DB      56
        DB      53
        DB      51
        DB      48
        DB      46
        DB      44
        DB      40
        DB      38
        DB      34
        DB      32
        DB      29
        DB      25
        DB      23
        DB      20
```

```
        DB      16
        DB      14
        DB       9
        DB       7
        DB       4
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 1C0H
;
;Part 4 of table-group 1 routine
;
THIS11: jmp THIS1
LBL311: jmp LBL31
LBL411: jmp LBL41
;
;
;
TOP1:   anl a,r2                ;mask off table bits
        xrl a, r2               ;compare counter with 63
        jnz BEGIN1              ;if not equal, jump to BEGIN1
        mov a,r0                ;otherwise, get the table pointer
        anl a, r4               ;set the counter to 61
        mov r0,a                ;put new value back in r0
        cpl f0                  ;set the F0 flag to one
        jmp START1              ;jump to START1
;
;
;
BEGIN1: nop                     ;
        nop                     ;
        nop                     ;
        mov a,r0                ;get table pointer
        jmp START1              ;jump to START1
;
;
;
        ORG 1D6H
;
;Table for on-time at 80% current level
;
        DB      93
        DB      93
        DB      92
        DB      92
        DB      91
        DB      90
        DB      89
        DB      88
```

```
        DB      87
        DB      86
        DB      85
        DB      83
        DB      82
        DB      80
        DB      77
        DB      76
        DB      74
        DB      71
        DB      69
        DB      66
        DB      64
        DB      61
        DB      59
        DB      55
        DB      53
        DB      50
        DB      46
        DB      44
        DB      39
        DB      37
        DB      33
        DB      29
        DB      26
        DB      23
        DB      19
        DB      15
        DB      11
        DB       8
        DB       5
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 200H
;
;
;
        jmp RESET               ;jump to RESET
        nop                     ;
;
;
;
        ORG 203H
;
;Part 1 of table-group 2 routine
;
START2: movp a,@a               ;get on-time from table entry
        outl BUS, a             ;send entry to counter
```

```
        anl P1, #00000000b      ;load counter
        movp3 a,@a              ;take out for .6 Hz
        orl P1, #00000100b      ;
        movp3 a,@a              ;take out for .6 Hz
;       call WAIT               ;put in for .6 Hz
        jf0 LBL12               ;if 0-90 degrees, jump
        inc r0                  ;increment table pointer
        jni LBL322              ;if sync signal is high, jump
        jt0 LBL422              ;if power increment signal is high, jump
        jt1 LBL52               ;if power decrement signal is high, jump
        jmp LBL72               ;otherwise, jump to LBL72
;
;
;
        ORG 216H
;
;Table for on-time at 85% current level
;
        DB      99
        DB      98
        DB      98
        DB      97
        DB      97
        DB      96
        DB      96
        DB      94
        DB      93
        DB      92
        DB      90
        DB      89
        DB      87
        DB      85
        DB      83
        DB      80
        DB      79
        DB      75
        DB      74
        DB      70
        DB      68
        DB      66
        DB      61
        DB      59
        DB      56
        DB      53
        DB      50
        DB      46
        DB      42
        DB      39
        DB      36
        DB      32
        DB      27
        DB      24
```

```
        DB      20
        DB      16
        DB      12
        DB       9
        DB       5
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 240H
;
;Part 2 of table-group 2 routine
;
LBL12:  dec r0                  ;decrement table pointer
        jni LBL322              ;if sync signal is high, jump
        jt0 LBL422              ;if power increment signal is high, jump
        jt1 LBL52               ;if power decrement signal is high, jump
        nop                     ;
        nop                     ;
LBL72:  nop                     ;
        nop                     ;
        mov a,r0                ;get table pointer
        jmp THIS2               ;jump to THIS2
;
;
;
        ORG 256H
;
;Table for on-time at 90% current level
;
        DB      104
        DB      104
        DB      104
        DB      103
        DB      103
        DB      102
        DB      101
        DB      101
        DB       98
        DB       97
        DB       96
        DB       94
        DB       93
        DB       90
        DB       88
        DB       86
        DB       83
        DB       81
        DB       78
        DB       74
```

```
        DB      72
        DB      70
        DB      66
        DB      63
        DB      59
        DB      57
        DB      52
        DB      49
        DB      45
        DB      42
        DB      37
        DB      33
        DB      30
        DB      25
        DB      21
        DB      18
        DB      13
        DB       9
        DB       5
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 280H
;
;Part 3 of table-group 2 routine
;
LBL52:  mov a,r0                ;get the table pointer
        add a, r7               ;subtract one from the table indicator
        mov r0,a                ;put new value back in r0
        jc THIS22               ;if result is not negatime, jump
        jmp THIS1               ;otherwise, jump to THIS1
;
;
THIS2:  jb5 TOP2                ;if near top of the table, jump to TOP
BOTTM2: anl a,r2                ;mask off table number bits
        xrl a,r3                ;compare rest with 22
        jnz BEGIN2              ;if not equal, jump to BEGIN2
        mov a,r0                ;get the table pointer
        orl a, r6               ;set pointer to loc 23 of correct table
        mov r0,a                ;put new pointer value back in R0
        clr f0                  ;clear the f0 flag
        jmp START2              ;jump to START2
;
;
;
        ORG 296H
;
;Table for on-time at 95% current level
;
```

```
        DB      111
        DB      111
        DB      109
        DB      109
        DB      109
        DB      108
        DB      107
        DB      105
        DB      104
        DB      103
        DB      101
        DB       99
        DB       97
        DB       95
        DB       93
        DB       90
        DB       88
        DB       86
        DB       83
        DB       79
        DB       76
        DB       73
        DB       70
        DB       67
        DB       63
        DB       59
        DB       56
        DB       52
        DB       47
        DB       44
        DB       40
        DB       35
        DB       31
        DB       27
        DB       23
        DB       18
        DB       14
        DB       10
        DB        5
        DB        1
        DB        1
        DB        1
;
;
;
        ORG 2C0H
;
;Part 4 of table-group 2 routine
;
THIS22: jmp THIS2
LBL322: jmp LBL32
LBL422: jmp LBL42
```

```
;
;
;
TOP2:   anl a,r2                ;mask off table bits
        xrl a,r2                ;compare counter with 63
        jnz BEGIN2              ;if not equal, jump to BEGIN2
        mov a,r0                ;otherwise, get the table pointer
        anl a, r4               ;set the counter to 61
        mov r0,a                ;put new value back in r0
        cpl f0                  ;set the F0 flag to one
        jmp START2              ;jump to START2
;
;
;
BEGIN2: nop                     ;
        nop                     ;
        nop                     ;
        mov a,r0                ;get table pointer
        jmp START2              ;jump to START2
;
;
;
        ORG 2D6H
;
;Table for on-time at 100% current level
;
        DB      116
        DB      116
        DB      115
        DB      115
        DB      115
        DB      114
        DB      112
        DB      111
        DB      110
        DB      109
        DB      106
        DB      104
        DB      103
        DB      101
        DB       98
        DB       95
        DB       93
        DB       90
        DB       86
        DB       84
        DB       81
        DB       77
        DB       73
        DB       70
        DB       67
        DB       62
```

```
        DB      58
        DB      55
        DB      50
        DB      46
        DB      42
        DB      37
        DB      33
        DB      29
        DB      24
        DB      19
        DB      15
        DB      11
        DB       6
        DB       1
        DB       1
        DB       1
;
;
;
        ORG 300H
;
;Part 5 of table-group 0 routine
;
LBL30:  mov a,r0                ;get the table pointer
        orl a, r2               ;set pointer to the top of the table
        add a, #-3              ;subtract 3
        mov r0,a                ;put new value back in r0
        clr f0                  ;clear the f0 flag
        cpl f0                  ;set the f0 flag to one
        jmp THIS0               ;jump to THIS0
;
;
;
LBL40:  mov a,r0                ;get the table pointer
        add a, r5               ;increment the table counter
        mov r0,a                ;put new value back in r0
        jc NEW1                 ;if counter overflows, jump to NEW1
        jmp THIS0               ;otherwise, jump to THIS0
;
;
;
NEW1:   jmp THIS1               ;jump to THIS1
;
;
;
;
;
;Part 5 of table-group 1 routine
;
LBL31:  mov a,r0                ;get the table pointer
        orl a, R2               ;set pointer to the top of the table
```

```
        add a, #-3              ;subtract 3
        mov r0,a                ;put new value back in r0
        clr f0                  ;clear the f0 flag
        cpl f0                  ;set the f0 flag to one
        jmp THIS1               ;jump to THIS1
;
;
;
LBL41:  mov a,r0                ;get the table pointer
        add a, r5               ;increment the table counter
        mov r0,a                ;put new value back in r0
        jc NEW2                 ;if counter overflows, jump to NEW2
        jmp THIS1               ;otherwise, jump to THIS1
;
;
;
;Part 5 of table-group 2 routine
;
LBL32:  mov a,r0                ;get the table pointer
        orl a, r2               ;set pointer to the top of the table
        add a, #-3              ;subtract 3
        mov r0,a                ;put new value back in r0
        clr f0                  ;clear the f0 flag
        cpl f0                  ;set the f0 flag to one
        jmp THIS2               ;jump to THIS2
;
;
;
LBL42:  mov a,r0                ;get the table pointer
        add a, r5               ;increment the table counter
        mov r0,a                ;put new value back in r0
        jc NEW2                 ;if counter overflows, jump to NEW2
        jmp THIS2               ;otherwise, jump to THIS2
;
;
;
NEW2:   jmp THIS2               ;jump to THIS2
;
;
;
;Initialization routine
;
INIT:   anl P1, #00000000b      ;clear the load signal
        clr f0                  ;
        cpl f0                  ;set the F0 flag to one
        mov r0, #00111101b      ;set up table pointer
        mov r1, #00010010b      ;set up control word for timer #0
        mov r2, #00111111b      ;set up mask
        mov r3, #00010101b      ;set up mask
        mov r4, #11111101b      ;set up mask
        mov r5, #01000000b      ;set up mask
        mov r6, #00010111b      ;set up mask
```

```
        mov r7, #11000000b      ;set up mask
        mov a,r0                ;get the table pointer
        jmp START0              ;jump to START0
;
WAIT:   mov a, #63              ;this routine is used when
        xch a,r0                ;the fundamental frequency
        mov @r0,a               ;is .6 Hz
        dec r0                  ;
        mov a,r1                ;
        mov @r0,a               ;
        mov r1, #20             ;
WT1:    mov r0, #96             ;
        nop                     ;
WT2:    djnz r0, WT2            ;
        djnz r1, WT1            ;
        nop                     ;
        mov r0,#62              ;
        mov a, @r0              ;
        mov r1,a                ;
        inc r0                  ;
        mov a, @r0              ;
        mov r0,a                ;
        ret                     ;
;
;
        end
```

```
;
;                *** SOFTWARE FOR THE CONTROL PROCESSOR ***
;
;
;
        ORG 00H
;
;
;
        jmp INIT                ;jump to the initialization routine
;
;
;
        ORG 03H
;
;
;
INT:    xch a, r0               ;get output word
        outl P2,a               ;send to Port 2
        anl a, #11111100b       ;clear the up/down signals
        orl a, #00000100b       ;clear the sync signal
        xch a,r0                ;put signal status back in r0
        inc r7                  ;increment the cycle location counter
        inc r3                  ;increment the power wait counter
        mov r2, #00000000b      ;clear the signal status register
        retr                    ;return
;
;
;
INIT:   clr a                   ;set the accumulator to zero
        outl BUS, a             ;disable the GTO drive signal
        outl P2, a              ;reset processor #2
        mov r7,a                ;clear the cycle location counter
        mov r6,a                ;clear the consecutive syncs counter
        mov r5,a                ;clear the desired power counter
        mov r4,a                ;clear the present power counter
        mov r3,a                ;clear the power wait counter
        mov r2,a                ;clear the signal status register
        mov r1,a                ;clear the GTO drive enabled flag
        clr f0                  ;clear the sync signal detected flag
        cpl a                   ;set the accumulator to all ones
        outl P1,a               ;prepare port 1 for input
        mov a, #11111100b       ;
        outl P2,a               ;prepare port 2 and clear Pattern reset
        mov r0,a                ;set up signal status register
        en i                    ;enable the interrupt
        jmp MAIN                ;jump to the main routine
;
;
;
MAIN:   call OFF                ;call the turn-off routine
        call SYNC               ;call the synchronization routine
```

```
        mov a,r7                ;if the expected zero crossing is
        add a, #-150            ;pending, continue calling the
        jc MAIN                 ;SYNC routine
        call POWER              ;call the POWER routine
        call STATUS             ;call the STATUS routine
        jmp MAIN                ;repeat
;
;
;
SYNC:   jt0 NOSIG               ;if no sync signal is present, jump
        jf0 SKIP                ;if signal already detected, skip
        cpl f0                  ;set signal detected flag high
        mov a,r7                ;get the cycle location counter
        add a, #-156            ;if counter is less than 156
        jnc STP                 ;or greater than 163,
        add a, #-8              ;jump to stop
        jc STP                  ;
        mov a,r0                ;get signal status
        anl a, #11111011b       ;set sync signal low
        mov r0,a                ;put signal status back in r0
        mov r2, #00000100b      ;change signal status register r2
        inc r6                  ;increment the in-sync counter
        mov r7, #00             ;clear the cycle location counter
        ret                     ;return
;
;
;
NOSIG:  clr f0                  ;clear the signal detected flag
        ret                     ;return
;
;
;
SKIP:   ret                     ;return
;
;
;
POWER:  mov a,r1                ;if GTO drive enable flag is high, jump
        jnz NORM                ;to NORM
        ret                     ;otherwise, return
;
NORM:   mov a,r2                ;get the signal status register
        jnz EQUAL               ;if not cleared, skip this routine
        in a,P2                 ;get the Port 2 inputs
        cpl a                   ;
        jb6 NVALID              ;if bit 6 is not high, input is not valid
        jb7 FULL                ;the the 100% bit is high, jump to FULL
        in a,P1                 ;get the two lower BCD digits
        cpl a                   ;
        movp3 a,@a              ;get corresponding tbl number from pa.3
        jmp CONT                ;jump to CONT
FULL:   mov a, #11              ;set the accumulator to table #11
CONT:   mov r5,a                ;put tbl number in desired power counter
```

```
NVALID: mov a,r3              ;get the power wait counter
        add a, #-1            ;subtract one
        jnc EQUAL             ;if result is negative, jump
        clr a                 ;
        mov r3,a              ;clear the power wait counter
        mov a,r4              ;get the present power counter
        jz PWR1               ;if zero, jump to PWR1
        cpl a                 ;get its negative value
        inc a                 ;
        add a,r5              ;add the desired power counter value
        jz EQUAL              ;if the two are equal, jump
        jc UP                 ;if desired power is higher, jump to UP
DOWN:   mov a,r0              ;get siganl status
        orl a, #00000001b     ;set down bit high
        mov r0,a              ;put status back in r0
        mov r2, #00000001b    ;change the signal status register r2
        dec r4                ;decrement the present power counter
        ret                   ;return
PWR1:   mov a,r5              ;get desired power counter value
        jnz UP                ;if not zero, jump to up
        ret                   ;otherwise, return
;
UP:     mov a,r0              ;get signal status
        orl a, #00000010b     ;set up bit high
        mov r0,a              ;put signal status back in r0
        mov r2, #00000010b    ;change the signal status register
        inc r4                ;increment the present power counter
EQUAL:  ret                   ;return
;
;
;
STATUS: mov a,r1              ;get the GTO drive enabled flag
        jnz ST1               ;if high, jump to ST1
        in a, P2              ;get the port 2 inputs
        cpl a                 ;
        jb4 ST1               ;if not started, jump to ST1
        mov a,r6              ;get the consecutive in sync counter
        add a, #-16           ;if not greater than 16,
        jnc ST1               ;jump to ST1
        mov a, #00000001b     ;set up accumulator
        mov r1,a              ;set GTO drive enabled flag
        outl BUS, a           ;enable the GTO drive
ST1:    ret                   ;return
;
;
;
STP:    mov a,r1              ;get GTO drive enabled flag
        jnz INIT              ;if high, jump to INIT
        mov r7, #00           ;clear location counter
        ret                   ;otherwise, return
;
;
```

```
;
OFF:    mov a,r7                ;if the expected zero-crossing
        add a, #-155            ;is pending, check the STOP
        jnc SP1                 ;button
        in a, P2                ;
        cpl a                   ;
        jb5 SP1                 ;if not activated, skip
        jmp INIT                ;jump to INIT routine
SP1:    ret                     ;return
;
;
;
        ORG  300H
;
;
;
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
;
;
;
        ORG  310H
;
;
;
        DB      0
        DB      0
        DB      0
        DB      0
        DB      0
        DB      1
        DB      1
        DB      1
        DB      1
        DB      1
;
;
;
        ORG  320H
;
;
;
        DB      1
        DB      1
```

```
        DB      1
        DB      1
        DB      1
        DB      2
        DB      2
        DB      2
        DB      2
        DB      2
;
;
;
        ORG   330H
;
;
;
        DB      2
        DB      2
        DB      2
        DB      2
        DB      2
        DB      3
        DB      3
        DB      3
        DB      3
        DB      3
;
;
;
        ORG   340H
;
;
;
        DB      3
        DB      3
        DB      3
        DB      3
        DB      3
        DB      4
        DB      4
        DB      4
        DB      4
        DB      4
;
;
;
        ORG   350H
;
;
;
        DB      4
        DB      4
        DB      4
```

```
        DB      4
        DB      4
        DB      5
        DB      5
        DB      5
        DB      5
        DB      5
;
;
;
        ORG   360H
;
;
;
        DB      5
        DB      5
        DB      5
        DB      5
        DB      5
        DB      6
        DB      6
        DB      6
        DB      6
        DB      6
;
;
;
        ORG   370H
;
;
;
        DB      6
        DB      6
        DB      6
        DB      6
        DB      6
        DB      7
        DB      7
        DB      7
        DB      7
        DB      7
;
;
;
        ORG   380H
;
;
;
        DB      7
        DB      7
        DB      7
        DB      8
```

```
        DB      8
        DB      8
        DB      8
        DB      8
        DB      9
        DB      9
;
;
;
        ORG   390H
;
;
;
        DB      9
        DB      9
        DB      9
        DB      0AH
        DB      0AH
        DB      0AH
        DB      0AH
        DB      0AH
        DB      0BH
        DB      0BH
;
;
;
        END
```

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