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MoS_2 Dual-Gate MOSFET With Atomic-Layer-Deposited Al_2O_3 as Top-Gate Dielectric

Han Liu and Peide D. Ye, *Senior Member, IEEE*

***Abstract*—We demonstrate atomic-layer-deposited (ALD) high-k dielectric integration on 2-D layer-structured molybdenum disulfide (MoS_2) crystals and MoS_2 dual-gate n-channel MOSFETs with ALD Al_2O_3 as the gate dielectric. Our C–V study of MOSFET structures shows good interface between 2-D MoS_2 crystal and ALD Al_2O_3. Maximum drain currents using back gates and top gates are measured to be 7.07 and 6.42 mA/mm, respectively, at $V_{\rm ds} = 2$ V with a channel width of 3 μm, a channel length of 9 μm, and a top-gate length of 3 μm. We achieve the highest field-effect mobility of electrons using back-gate control to be 517 $\rm cm^2/V \cdot s$. The highest current on/off ratio is over 10^8.**

***Index Terms*—Atomic layer deposition, MOSFET, MoS_2.**

I. Introduction

EVER since the advent of graphene in 2004 [1], the electronic properties of 2-D layer-structured materials have been intensively investigated since their thickness can be pushed down to a few nanometers or even less, where a series of novel physical, chemical, and mechanical properties is observed. The layer-structured material family includes graphene, boron nitride (BN), MoS_2, topological insulators such as Bi_2Te_3 and Bi_2Se_3, and many others [1]–[5]. As Moore's law is approaching its physical limit, an alternative material is urgently needed as a substitute for future logic transistor applications [6], [7]. Although graphene has been widely believed as a promising candidate, its gapless nature limits its potential application as logic transistors [8], [9]. However, in great contrast to graphene, MoS_2 enjoys its uniqueness in the device applications due to its semiconductor-like bandgap [5]. Also, due to the nature of their layered structure, single-atomic-layer MoS_2 transistors with an ultrathin body channel have the advantage in nanometer-scale MOSFETs of being immune to the short-channel effects, compared to the state-of-the-art SOI counterparts which are greatly limited by short-channel effects. Research in MoS_2 electronics is still in its infancy. The first experimentally demonstrated single-layer MoS_2 transistor has already been shown to have a mobility of over 200 $\rm cm^2/V \cdot s$, a subthreshold swing (SS) of 74 mV/dec, and an on/off ratio of $\sim 10^8$ [3]. NEGF simulations reveal that the theoretical limit for MoS_2 thin-film transistors is an on/off ratio of over 10^{10}, a sub-10-mV/V drain-induced barrier lowering, and a near-perfect SS ($SS = 60$ mV/dec), owing to the absence of dangling bonds in their layered structure [10]. In this letter, we focus on the integration of atomic-layer-deposited (ALD) high-k oxides on this kind of layered structure with potentially chemical inert surface. We demonstrate a top-gated Al_2O_3/MoS_2 MOSFET with an electron mobility of 517 $\rm cm^2/V \cdot s$ and an on/off ratio of 10^8.

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II. Experiment

MoS_2 thin flakes were mechanically exfoliated by the classical scotch-tape technique and then transferred to a heavily doped Si substrate capped with 300-nm SiO_2. Al_2O_3 was deposited on MoS_2 flakes within an ASM F120 ALD reactor. Trimethylaluminum (TMA) and water were used as precursors at a temperature between 200 °C and 400 °C with 111 cycles, which yields $\sim$10-nm Al_2O_3 for an ideal ALD process. Pulse times are 0.8 and 1.2 s for TMA and water, respectively, while purge time is 6 s for both. A Dimension 3100 AFM system was used to examine the surface morphology before and after ALD deposition. MOSFET fabrication was then performed after identifying the appropriate ALD process window. A 16-nm ALD Al_2O_3 was deposited on MoS_2 flakes under 200 °C growth temperature. After Al_2O_3 growth, source and drain regions were defined using optical lithography with a spacing of 9 μm. A 20-nm/50-nm Ni/Au film was deposited as the source/drain contacts, and a Ti/Au film was used for the gate. The gate length is $\sim$3 μm with $\sim$3-μm spacings to source/drain. HP 4284A and Keithley 4200 were used for C–V and I–V characterizations.

III. Results and Discussion

Fig. 1(a) and (b) shows the representative AFM images of MoS_2 surface morphology after 111 cycles of Al_2O_3 deposition under 200 °C and 400 °C, respectively. In the absence of intensive research of ALD growth on 2-D electronic materials, we can simply take the graphene as a reference. Earlier studies have shown that direct Al_2O_3 growth by TMA and water is not possible on the graphene basal plane, while growth occurs only at the graphene edges. This is understood by the fact that dangling bonds only exist in graphene edges but not on the basal

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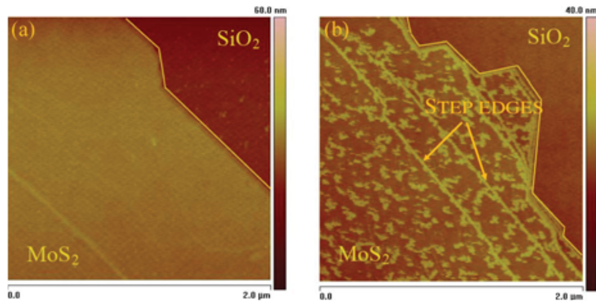

Fig. 1. AFM images showing MoS_2 flakes with 111 cycles of Al_2O_3 grown at (a) 200 °C and (b) 400 °C.

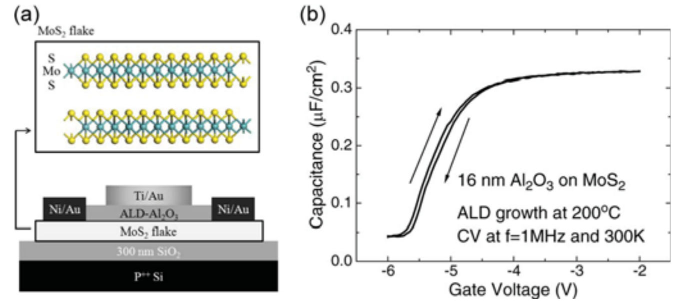

Fig. 2. (a) Device structure of MoS_2 dual-gate MOSFET and (b) 1-MHz high-frequency C–V characteristic of the MOSFET device measured at room temperature in darkness.

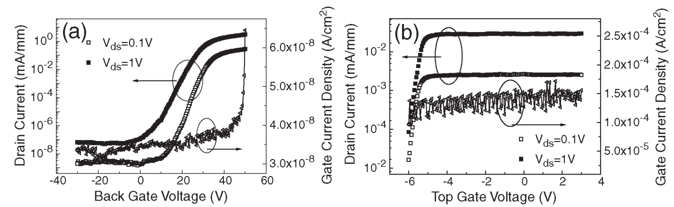

Fig. 3. Transfer characteristics of the MoS_2 dual-gate MOSFET from (a) back-gate and (b) top-gate controls. The back- and top-gate leakage current densities from 300-nm SiO_2 and 16-nm Al_2O_3 are also presented.

plane [11], [12]. However, for MoS_2, it is obvious that the ALD growth is easier than that on graphene. From Fig. 1(a), we can see that, at 200 °C, the Al_2O_3 thin film is visually uniform. In addition, the step height between the flake and SiO_2 substrate is around 8 nm, which is similar to that before ALD growth. At the elevated temperature of 400 °C, although we still observe continuous ALD growth at flake edges, as shown in Fig. 1(b), the step height has disappeared as Al_2O_3 is growing only on SiO_2, while only small areas of Al_2O_3 are formed on the MoS_2 basal plane. This temperature sensitivity observed in Al_2O_3 deposition indicates that the growth mechanism on MoS_2 mostly relies on physical absorption on the basal plane during the initial growth stage, whereas desorption is greatly enhanced at higher temperature. At the step edges of the layers, stronger chemical bonds between MoS_2 and ALD precursors are formed due to dangling bonds; thus, even at higher temperature, the ALD growth on step edges is still uniform and continuous. Al_2O_3 films grown at 300 °C on MoS_2 also show nonuniformity and poor electrical insulating properties. The ALD window for 2-D layered-structure materials is significantly reduced, compared to that of bulk materials, such as Si, Ge, and III–V. Therefore, the ALD process must be carefully optimized to simultaneously achieve geometrical uniformity and good electrical properties (high dielectric constant, large electrical strength, low gate leakage current, etc.).

The MoS_2 MOSFET was fabricated on an ~15-nm-thick flake which contains about 23 MoS_2 monolayers, which has a bulklike bandgap of ~1.2 eV. The final device structure is shown in Fig. 2(a). We did not reduce the flake thickness to a monolayer since the bandgap of ultrathin MoS_2 crystal increases and could become 1.8 eV for the monolayer [5]. C–V measurement is carried out in order to evaluate the interface quality between ALD Al_2O_3 and MoS_2 crystals, as shown in Fig. 2(b). The source and drain are grounded, while a voltage bias on the top gate is applied. The area of the capacitor is only ~12 μm^2, making the low-frequency C–V curve rather noisy (not shown). The high-frequency C–V curve (with hysteresis) at 1 MHz shows a clear transition from accumulation to depletion for a typical n-type MOS capacitor. A moderate hysteresis of ~80 mV is exhibited in the curves, showing that the ALD Al_2O_3 film grown at 200 °C on MoS_2 and the interface are both of good quality.

Fig. 3(a) and (b) shows the transfer characteristics and transconductance of the device from both the top gate and the back gate. The charge neutrality level of MoS_2 is located slightly under the conduction band, thus making it easy for an accumulation-type nMOSFET [13], [14]. The transfer characteristics of the top gate suffer from a very large negative threshold voltage $(V_{\rm th})$ shift, as attributed to the existence of large amount of positive fixed charges in the bulk oxide, due to the comparatively lower deposition temperature [15]. The leakage current is also measured in the same device and is less than 2×10^{-4} A/cm^2 in the measurement range of -6 to $+3$ V. The highest drain current density achieved at $V_{\rm ds} = 1$ V using back-gate modulation is 3.07 mA/mm, and an on/off ratio greater than 10^8 is also obtained. This superior on/off ratio compared to graphene exists because of the 1.2-eV bandgap. The greatest current density from the top gate is about two orders of magnitude smaller than that from the back gate. This big difference comes from the non-self-aligned top-gate device structure. From Fig. 2(a), we can see that the heavily doped Si substrate has a "global" control over the entire flake. With increasing back-gate voltage, the carriers in the MoS_2 flake are accumulated, and thus, the contact resistance between the Ni/Au source/drain and the MoS_2 flake would be reduced, as the flake is being heavily "doped" by the electric field, while the top gate can only modulate part of the channel underneath the top gate. The peak extrinsic transconductance (g_m) from back-gate control is 0.165 mS/mm at $V_{\rm ds} = 1$ V. We can extract the field-effect mobility to be 517 $\rm cm^2/V \cdot s$, which is a factor of 2.6 larger than the reported value in [3], mainly because of the smaller bandgap of our multilayer MoS_2 as the channel material, compared to the single-layer one used in [3]. Since the significant contact resistance is not subtracted, the intrinsic field mobility of the MoS_2 channel is even larger. The extrinsic g_m from top-gate modulation is 0.61 mS/mm, corresponding to a reduced surface mobility of 4.13 $\rm cm^2/V \cdot s$, which is much smaller than the back-gate surface mobility, due to the large

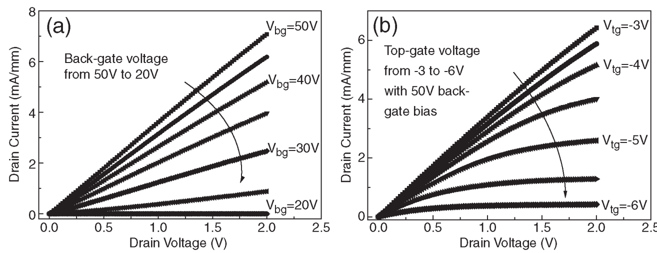

Fig. 4. I_d–V_d characteristics of MoS_2 dual-gate MOSFET with back-gate voltage stepped from 50 to 20 V. (b) I_d–V_d characteristics of MoS_2 dual-gate MOSFET with top-gate voltage stepped from −3 to −6 V while a back-gate voltage of 50 V is applied.

contact resistance and access resistance when the back gate is floating, which will be discussed hereinafter. The hysteresis of the top-gate transfer curves is much smaller than that of the back-gate curves, similar to the C–V curves. The SS for the top gate is ∼140 mV/dec at $V_{\rm ds} = 1$ V. The interface trap density is estimated to be $2.4 \times 10^{12}/\text{cm}^2 \cdot \text{eV}$ at the MoS_2 and ALD Al_2O_3 interface and would be further reduced by optimizing the process. Considering that there is minimal process refinement, such as no surface passivation and the low ALD growth temperature, this may imply that the interface state issue between 2-D crystals and ALD high-k dielectrics is very forgiving.

Fig. 4(a) and (b) shows the drain current versus drain voltage under a variety of back- and top-gate biases. The gate biases range from 50 to 20 V with a −5-V step for the back gate and from −3 to −6 V with a −0.5-V step for the top gate. For the top-gate measurement, a back-gate voltage of 50 V is applied to reduce the contact resistance and access resistance. Consequently, the maximum current density for top-gate modulation has now been increased to 6.42 mA/mm, back to the same level of that from back-gate modulation. The maximum extrinsic g_m's at $V_{\rm ds} = 2$ V are 0.318 and 2.83 mS/mm for back- and top-gate modulations, respectively. By roughly extracting the contact resistance, the quasi-intrinsic field-effect mobility from the top-gate device is increased to 125 $\text{cm}^2/\text{V} \cdot \text{s}$. The big difference between field-effect mobilities from top- and back-gated devices could be ascribed to the different interface conditions between the MoS_2/SiO_2 interface and MoS_2/Al_2O_3 interface. For the former, after the flake is transferred to the substrate and is in physical contact, the interface remains intact throughout the fabrication. However, the top interface is strongly correlated with the ALD process, similar to the challenges found in our previous work on the topological insulator Bi_2Te_3 [16]. Compared to III–V or topological insulators, we may consider the interface on MoS_2 to be much more forgiving due to its chemically stable layered atomic structure which is shown in Fig. 2(a). The physical absorption process during the initial ALD growth of high-k dielectrics still needs a comprehensive study in order to develop a deep understanding of the ALD growth mechanism on these novel 2-D electronic materials. The definition of the "interface states" at these 2-D atomic crystal/Al_2O_3 interfaces needs to be revised since there are no traditional dangling bonds at these interfaces at all.

IV. Conclusion

In summary, we have experimentally demonstrated MoS_2 MOSFET with ALD Al_2O_3 as the top-gate dielectric. AFM, C–V, and I–V studies show that ALD high-k dielectrics can be directly deposited on MoS_2 at low growth temperatures and the MoS_2/Al_2O_3 interface is of good quality. The high electron field mobility, good SS, and excellent drain current on/off ratio are demonstrated on the fabricated MoS_2 nMOSFET.

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