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MoS2 Nanoribbon Transistors: Transition From Depletion Mode to Enhancement Mode by Channel-Width Trimming

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MoS_2 Nanoribbon Transistors: Transition From Depletion Mode to Enhancement Mode by Channel-Width Trimming

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***Abstract*—We study the channel width scaling of back-gated MoS_2 metal–oxide–semiconductor field-effect transistors from 2 μm down to 60 nm. We reveal that the channel conductance scales linearly with channel width, indicating no evident edge damage for MoS_2 nanoribbons with widths down to 60 nm as defined by plasma dry etching. However, these transistors show a strong positive threshold voltage (V_T) shift with narrow channel widths of less than 200 nm. Our results also show that transistors with thinner channel thicknesses have larger V_T shifts associated with width scaling. Devices fabricated on a 6-nm-thick MoS_2 crystal underwent the transition from depletion mode to enhancement mode.**

***Index Terms*—MoS_2 nanoribbon, threshold voltage shift, width scaling.**

I. Introduction

THE triumph of the aggressive scaling of silicon-based integrated circuits has dramatically changed our lifestyle in the past couple of decades. However, as the scaling of silicon approaches its physical limit, efforts in finding alternative channel materials have been made for the extension of the Moore's law. Of these materials, Ge and III-V materials are among the most promising candidates because of their high carrier mobilities. They have been widely studied for logic applications in the past years [1]–[4]. Although graphene, a single layer of carbon atoms having superior carrier mobilities of up to 200 000 $cm^2/V \cdot s$, has been recognized as another material candidate, its gapless nature limits its further application in logic devices [5]. Nevertheless, the discovery of graphene has spurred the research of other 2-D layered structures, including boron nitride, topological insulators (Bi_2Te_3, Bi_2Se_3, etc.), and transitional metal dichalcoginides (TMDs) [6]–[10]. TMDs, e.g., MoS_2, have enjoyed several advantages in device applications because they have large bandgaps (usually > 1 eV), satisfactory electron mobilities of up to several hundreds, and good thermal stability and can be used to form ultrathin-body transistors with atomic layers, which make them a desirable channel material with superior immunity to short-channel effects [11]–[13]. The MoS_2 devices are mostly n-type transistors in experimental observations, which might be attributed to the stoichiometric composition in the channel [10], [15], [16]. Also, the charge neutrality level at the metal/MoS_2 interface could be in the vicinity of the conduction band (E_C); thus, n-type contacts are more easily made. The fabricated MoS_2 transistors behave as depletion-mode n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) with large negative threshold voltages [14]. The 2-D nature of MoS_2 (as well as other layered materials) makes it difficult to realize channel doping as a way to achieve a desirable positive V_T or enhancement-mode operation for various desirable circuitry configurations. Therefore, making an enhancement-mode MoS_2 MOSFET is quite challenging.

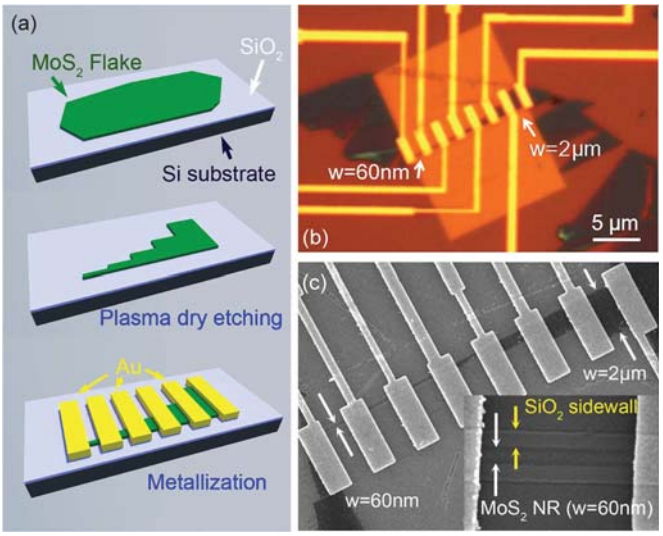

Fig. 1. (a) Schematic illustrations of device fabrication. (b) Optical image of one set of transistors (D1) fabricated on a 6-nm-thick MoS_2 crystal. (Scale bar: 5 μm.) (c) SEM image of another set of devices (D2). (Inset: Magnified image of the 60-nm-wide MoS_2 nanoribbon transistor.)

II. Experiments

In this letter, we study the width scaling of MoS_2 transistors by forming nanoribbon channels and show that the V_T of MoS_2 transistors can be modulated to be both positive and negative through appropriate width selection. The fabrication process of sets of MoS_2 transistors is shown in Fig. 1(a), as described hereinafter. MoS_2 flakes were mechanically exfoliated from bulk ingot (SPI Supplies) and then transferred to a heavily p-doped silicon substrate (0.01–0.02 $\Omega \cdot$ cm) with a 300-nm SiO_2 capping layer. The silicon substrate served as a global back gate, while the 300-nm SiO_2 served as the gate dielectric. After the flake transfer, we used electron beam lithography to pattern

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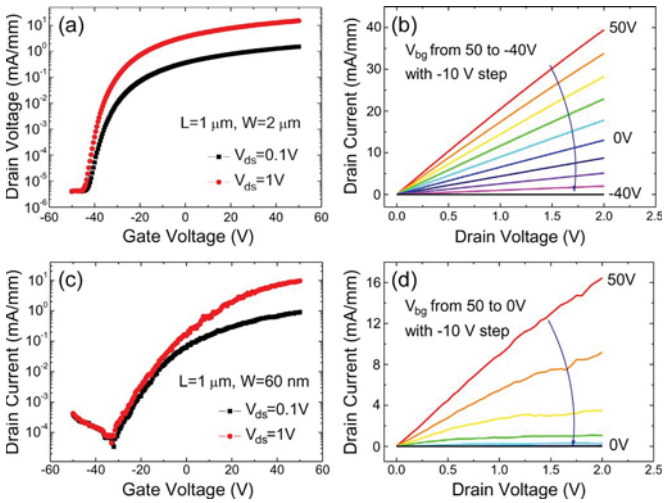

Fig. 2. (a) and (b) Transfer and output curves, respectively, of a transistor with a 2-μm channel width on a 6-nm-thick MoS_2 crystal (D1s). (c) and (d) Transfer and output curves, respectively, of the transistor with a 60-nm channel width on the same crystal.

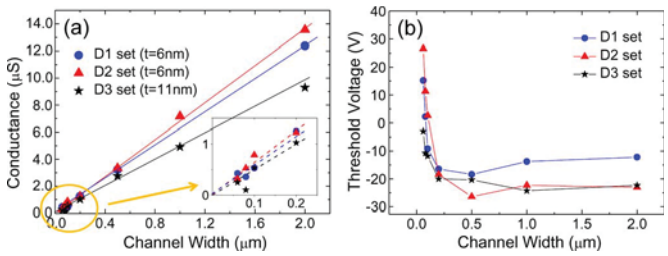

Fig. 3. (a) Extracted channel conductance of all sets of devices versus channel width. The dashed lines in the inset are guided by eye. (b) Extracted threshold voltage of all sets of devices versus channel width.

the flake, followed by plasma dry etching (BCl_3: 15 sccm; Ar: 60 sccm; pressure: 0.6 Pa; RF source power: 100 W; RF bias power: 50 W; time: 5 min) to remove the excess parts of the flakes, leaving connected rectangles with a fixed length (2 μm) but various widths to be used as device channels. The widths of these rectangles were varied from 2 μm down to 60 nm. Finally, contacts were defined by electron beam lithography, followed by a 50-nm Au metallization by electron beam deposition. The contact bars were 1 μm wide, centered on the edge between two neighboring channel areas. The final set of devices has a fixed channel length of 1 μm and widths of 2 μm, 1 μm, 500 nm, 200 nm, 100 nm, 80 nm, and 60 nm. Three sets of devices were fabricated on three large flakes with thicknesses of 6, 6, and 11 nm, as determined by atomic force microscopy. The optical image and scanning electron microscopy (SEM) image of these sets of devices are shown in Fig. 1(b) and (c). The overetching of the MoS_2, in order to guarantee complete removal of excess MoS_2 crystals, created a rectangular step in the SiO_2 capped substrate surrounding the flake and also created SiO_2 sidewalls at the edges of the MoS_2 channels (Fig. 1(c) inset). Smooth edges without obvious damage by dry etching were observed at the MoS_2 nanoribbons.

Fig. 2(a)–(d) shows the transfer and output characteristics of the devices with 2-μm and 60-nm widths, selected from one of three sets of devices. These devices were fabricated using one of the 6-nm-thick crystals (D1). Fig. 2(a) shows well-behaved transfer curves from the 2-μm-wide transistor. The current on/off ratio is approximately 10^7, as the ultrathin MoS_2 crystal can be easily depleted at negative gate biases. The extrinsic field-effect mobility of this device is 21.8 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, which can be further improved by high-k dielectric passivation [10], [15]. The transfer curve of the 60-nm-wide nanoribbon device is shown in Fig. 2(c). Compared to Fig. 2(a), the transfer curves are noisy, due to fewer conduction modes in the nanoribbons, as well as an increased leakage current at negative bias. This increased gate leakage could be ascribed as dielectric degradation in SiO_2 by dry etching. We also observe a larger subthreshold swing (SS). The SS for the 2-μm-wide device is around 2 V/dec; however, for the 60-nm-wide device, this value increases to almost 10 V/dec. The SS value of the 2-μm-wide device indicates a reasonably good interface (interface trap density $D_{\mathrm{it}} \sim 2.3 \times 10^{12}/\mathrm{cm}^2\cdot\mathrm{eV}$) between the MoS_2 crystal and SiO_2 dielectric. If we replace the 300-nm SiO_2 layer with 5 nm of Al_2O_3, while assuming that D_{it} remains unchanged, the SS would be significantly reduced to ~75 mV/dec by simply applying $SS = kT/q(1+C_{\mathrm{it}}/C_{\mathrm{ox}})$, where k is the Boltzmann's constant, T is the temperature, and C_{ox} and C_{it} are capacitances modeling the oxide and interface traps, respectively. The differences in SS for the two devices are expected because edge roughness and defects play more important roles in nanoribbon transistors. We also observe a large difference in threshold voltages for these two devices. At a 2-V drain voltage with zero gate bias, the drain current for the 2-μm-wide device is 13.0 mA/mm, showing a typical depletion-mode operation. However, for the narrower device, the drain current is near zero with zero gate bias, indicating an obvious V_T shift to the positive side, signaling an enhancement-mode operation. At the same $V_{\mathrm{ds}} = 2$ V and $V_{\mathrm{gs}} = 50$ V, we achieve the highest drain current density to be 39.4 mA/mm for the 2-μm-wide device and 16.4 mA/mm for the 60-nm-wide device. This difference in normalized drain current suggests that V_T is different for these two devices, assuming that the current scales linearly with the channel width, which is verified hereinafter.

In order to confirm that the current scales linearly with various channel widths, we plot the total conductance (one over on-resistance) versus channel width for all three sets of devices, as shown in Fig. 3(a). The on-resistance (R_{on}) of the transistor has contributions from the contact resistance and channel resistance. Since the contact area and width for all transistors scale with channel width, the contact resistance should scale linearly with the channel width. The same is true for the channel resistance. After determining V_T via linear extrapolation from transfer characteristics, R_{on} is extracted at the same reference voltage point $V_{\mathrm{gs}} = V_T + 26$ V. Our result shows that the R_{on} or total conductance scales linearly with channel width. As expected, MoS_2 acts as a conventional semiconductor, in great contrast to 3-D topological insulators such as Bi_2Te_3 or Bi_2Se_3, where edge or surface conductance could be enhanced or dominate [17]. The width-dependent conductance is about 6–7 $\mu\mathrm{S}/\mu\mathrm{m}$ for the two 6-nm-thick devices (D1 and D2) and 5 $\mu\mathrm{S}/\mu\mathrm{m}$ for the 11-nm device (D3). We are not clear about why the thicker device has a lower conductance, and this result needs further investigation. As shown in the inset of Fig. 3(a), with much reduced channel widths, the extracted conductance becomes noisier as fewer conduction modes are available in the nanoribbons. However, the data points still fall along the scaling trend.

Lastly, we studied the V_T shift of all devices associated with the channel width. The V_T is extracted from the linear extrapolation method at a low drain voltage. V_T is calculated by $V_T = V_{\mathrm{GSi}} - V_{\mathrm{ds}}/2$, where V_{GSi} is the intercept gate voltage and V_{ds} is the drain voltage [18]. Threshold voltages for all three sets of devices are plotted in Fig. 3(b). Similar trends can be observed for all sets of devices. The V_T remains constant for transistors with a wider channel width ($W > 500$ nm). As the width of the channel is narrowed down to 200 nm, we start to observe the V_T shift to positive values. Apparently, transistors with thinner bodies (D1 and D2) are more likely to be influenced by this effect. For one of the 6-nm-thick set of transistors (D2), the threshold voltage ultimately shifts from -20 to 30 V, indicating a clear transition from being a depletion-mode transistor to being an enhancement-mode operation just by trimming down the channel width. The geometry of these nanoribbon transistors with a channel width less than 100 nm has a similar structure to that of Si FinFETs, if we ignore that the MoS_2 channel is modulated only from the back gate. Similar trends of V_T shift have also been observed in Si FinFETs as well as InGaAs nanowire transistors [19]. We believe that our V_T shift is due to edge depletion, similar to what has been observed in majority carrier GaN nanoribbon devices [20]. The edge depletion could be induced by either electric fields or ambient molecules (e.g., H_2O) adsorbed at the MoS_2 surface. Given our previous surface study of atomic-layer-deposition growth on 2-D crystals, these polarized molecules can be strongly adsorbed at the MoS_2 surface and even persist at 300 °C–400 °C [21]. The geometrical edge effects could also lead V_T positive shift and SS degradation for nanoribbon transistors as observed in experiments [22]. As expected, the V_T of the devices fabricated on the thicker crystal (D3) shows relatively minor shifts compared to that of the devices with thinner flakes, as shown in the same figure. The observation of V_T shifts for MoS_2 transistors with width scaling is important. The 2-D nature of MoS_2 and other TMD-based transistors makes it difficult to engineer the channel through doping. This demonstrated approach, using the width to achieve V_T adjustments on the same starting channel material in order to realize both enhancement-mode and depletion-mode operations, is a simple and favorable method for circuit designs such as to realize an enhancement-mode/depletion-mode-based inverter.

III. Conclusion

In summary, we have studied the effect of width scaling on MoS_2 transistors. We have demonstrated that the channel conductance scales linearly for the sets of devices with various channel widths down to 60 nm. We have also revealed that the threshold voltage has a significant shift from negative to positive for transistors with channel widths of less than 200 nm. As a result, these transistors have shown a clear transition from depletion-mode to enhancement-mode operation simply by channel-width trimming. Our result provides a new approach for threshold voltage engineering and is favorable for circuit applications based on large-area 2-D crystal nanomaterials [23]–[26].

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