HermesD: A High-Rate Long-Range Wireless Transmission System for Simultaneous Multichannel Neural Recording Applications

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***Abstract*—HermesD is a high-rate, low-power wireless transmission system to aid research in neural prosthetic systems for motor disabilities and basic motor neuroscience. It is the third generation of our "Hermes systems" aimed at recording and transmitting neural activity from brain-implanted electrode arrays. This system supports the simultaneous transmission of 32 channels of broadband data sampled at 30 ks/s, 12 b/sample, using frequency-shift keying modulation on a carrier frequency adjustable from 3.7 to 4.1 GHz, with a link range extending over 20 m. The channel rate is 24 Mb/s and the bit stream includes synchronization and error detection mechanisms. The power consumption, approximately 142 mW, is low enough to allow the system to operate continuously for 33 h, using two 3.6-V/1200-mAh Li-$SOCl_2$ batteries. The transmitter was designed using off-the-shelf components and is assembled in a stack of three 28 mm $\times$ 28-mm boards that fit in a 38 mm $\times$ 38 mm $\times$ 51-mm aluminum enclosure, a significant size reduction over the initial version of HermesD. A 7-dBi circularly polarized patch antenna is used as the transmitter antenna, while on the receiver side, a 13-dBi circular horn antenna is employed. The advantages of using circularly polarized waves are analyzed and confirmed by indoor measurements. The receiver is a stand-alone device composed of several submodules and is interfaced to a computer for data acquisition and processing. It is based on the superheterodyne architecture and includes automatic frequency control that keeps it optimally tuned to the transmitter frequency. The HermesD communications performance is shown through bit-error rate measurements and eye-diagram plots. The sensitivity of the receiver is -83 dBm for a bit-error probability of 10^{-9}. Experimental recordings from a rhesus monkey conducting multiple tasks show a signal quality comparable to commercial acquisition systems, both in the low-frequency (local field potentials) and upper-frequency bands (action potentials) of the neural signals. This system can be easily scaled up in terms of the number of channels and data rate to accommodate future generations of Hermes systems.**

***Index Terms*—High-rate frequency-shift keying (FSK) transmitter, in-vivo neural recording, neural prosthetics, wireless high-rate multichannel biotelemetry.**

I. Introduction

NEURAL recordings from freely-moving animals are an emerging area of neuroscience research. The approach presented in this paper enables the study of complex behaviors, such as social behavior, locomotion, or navigation [1], [2]. Wired systems are not feasible for studying freely-moving animals since cables significantly restrain movements and the animals tend to remove any cable connection attached to them. Another recording challenge is that the neural population under analysis by implanted multielectrode arrays changes. Therefore, overnight recording is necessary to track neurons over time for learning studies, or for combining experimental trials across days [3]. Wireless systems can be used in preclinical safety and efficacy trials to test the effect of various medical treatments on brain activity and behavior over long time periods. They also find applications in the field of neural prosthesis, in which brain activity is measured through various means and transformed into command signals for an external device. Using a wireless approach, algorithms can be tested in a less constrained setting. However, regardless of the neural prosthetic application, the use of many simultaneous neural channels is required, which can pose a substantial challenge for wireless design.

For human clinical systems, neural implants with transcutaneous connections should ideally be avoided since they are a potential source of infections, besides being aesthetically displeasing. Optimally, the wireless telemetry device would also be implanted along with electrode array and power source [4], [5]. Several research groups are developing single-chip systems that may eventually be small enough to enable a fully implantable solution. However, single-chip solutions are not optimized for neuroscience research. For example, several systems require the external use of a power coil [6], [7] that cannot be worn by a freely-moving animal. Other systems are limited to short-range

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wireless links [8], [9]. Due to power and bandwidth limitations, single-chip systems often compress data, transmit lower resolution signals [6], or use threshold crossings to represent individual action potentials [10], [11].

In contrast to clinical systems, large animals used for neuroscience research, such as monkeys, can carry a substantial power supply that can be changed every 24 h as part of an experimental routine. Since the full bandwidth of neural signals is of interest for neuroscience experiments, the acquisition of full action potential waveforms as well as lower frequency neural signals, such as electrocorticograms and local field potentials (LFP), is very desirable in recording systems. These different constraints underlie the need for a system optimized for neuroscience research using inexpensive commercial off-the-shelf (COTS) hardware.

Several implementations of high-rate multichannel wireless transmitters for neurological acquisition systems using off-the-shelf components were reported earlier. Rizk and colleagues propose a 96-channel, 1-Mb/s system capable of transmitting one channel of broadband data over a range of 2 m using an amplitude-shift keying (ASK) RF data transceiver; it requires 150 mW of power for the transmitter and an additional 300 mW for each of the 32-channel analog interface circuits [6]. Obeid and colleagues took a rather different approach that employed an embedded computer and 802.11b wireless local-area network (WLAN) equipment to implement a wearable telemetry system. It is capable of transmitting 12 channels of broadband neural data and requires 4 W of power, which is far too high for multiday recordings [12]. Other multichannel analog-based transmitter systems [13]–[15] can be economical in terms of power consumption since no analog-to-digital conversion stage is required. However, it is very difficult to ensure a controlled signal fidelity under various channel impairments, such as multipath or shadowing. Systems encoding data in the pulse duration or in the pulse position can also be impaired by the delay spread of the wireless channel. Moreover, multiplexing and demultiplexing waveforms in the analog domain are not a straightforward operation, requiring additional circuitry to generate synchronization markers inside the multiplexed signal.

Several other systems employ onboard spike detection and/or spike sorting algorithms [6], [7], but the hardware-processing resources are usually too scarce to provide high-quality spike classification on a large number of channels simultaneously, within a reasonably low-power budget. The approach followed in the system reported here is to move the computational complexity of the neural signal processing away from the transmitter into the receiver processor. The availability of high-speed computing resources in the receiver is plentiful, thus enabling the experimentation of a wide range of processing algorithms.

To meet the required specifications at sufficiently low power and small size for use with a rhesus macaque, we have developed HermesD, which provides simultaneous transmission of 32 channels of neural data sampled at 30 ks/s. This a miniaturization of the system introduced in [16] to fit a smaller form factor enclosure (detailed in [10]). While the prototype in [16] occupied five boards of approximately 70 mm × 70 mm in size, the system presented in this paper is assembled in a stack of three 28 mm × 28-mm boards, whose details are presented in the following sections. Neural data are collected and stored by a custom-designed bench-top stand-alone receiver, improved with tunability and automatic carrier frequency tracking characteristics over the initial design presented in [16]. HermesD is mainly targeted for neuroscience research applications that involve multiday freely behaving experiments. It can measure action potentials and local field potentials from all 32 electrodes by virtue of transmitting broadband signals. It also provides the unique capability to transmit neural data beyond 20 m, allowing the study of macaques embedded in social colonies in very large housing rooms. It can be further scaled up to 96 channels by expanding the analog amplifier array and the number of analog-to-digital converters (ADCs). This is the third generation of the Hermes systems that brings the capability of a wireless recording of a large number of wideband neural channels. Table I compares the main characteristics of HermesD with the previous generations.

TABLE I
SPECIFICATIONS OF SEVERAL HERMES GENERATIONS

System	HermesB [3]	HermesC [10]	HermesD
Connectivity	local storage	Wireless	Wireless
Channels	2 (BB)	1 (BB)+20 (TC)	32 (BB)
Transmission	PATA to CF	900 MHz/FSK	3.9 GHz/FSK
Range	–	4 m	> 20 m
Sampling	30 kSps	16 kSps	30 kSps
Resolution	12 bits	10 bits	12 bits
Data Rate	768 kbit/s	346 kbit/s	24 Mbit/s
Power	250 mW	63 mW	142 mW
Enclosure	60×70×45 mm³	38×38×51 mm³	38×38×51 mm³

Notes: BB – Full bandwidth neural channel; TC – Neural channel threshold crossings only; PATA – Parallel AT Attachment; CF – Compact Flash

In the following sections, we describe in detail the HermesD wireless acquisition hardware, its communications performance (antenna pattern, bit-error rate (BER), eye diagrams, link budget), and we present and discuss in-vivo recordings from a a rhesus macaque resting or engaged in a reaching task while comfortably seated and head posted in an experimental rig.

II. HERMESD SYSTEM

The block diagram of the HermesD system is shown in Fig. 1. The transmitter is implemented using only COTS components assembled in a stack of three printed-circuit boards (PCBs). They are housed in a 38 mm × 38 mm × 51-mm aluminum enclosure secured to the subject's head. This enclosure is also used for HermesCnano, the previous generation system [10]. It includes the batteries and an external microstrip patch antenna that was specifically designed for the frequency range of HermesD, as shown in Fig. 2. The receiver is built out of a combination of off-the-self radio-frequency (RF) modules and custom-made circuits. The recovered data packets are acquired by a digital input/output (I/O) board interfaced to a PC for storage and processing. The receiver is described in detail in Section II-B.

The neurological signals are captured by a 400-μm pitch 10×10 microelectrode array developed originally at the University of Utah [17] and now commercially available from BlackRock Microsystems, Inc., Salt Lake City, UT. HermesD was designed to process 32 of the 96 available channels,

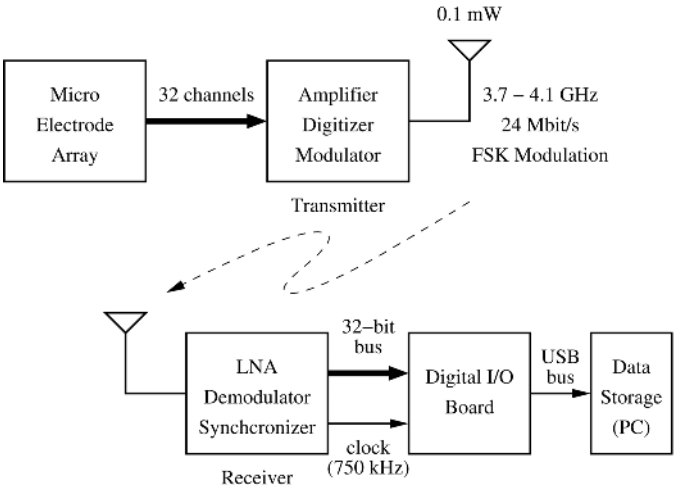

Fig. 1. HermesD system block diagram.

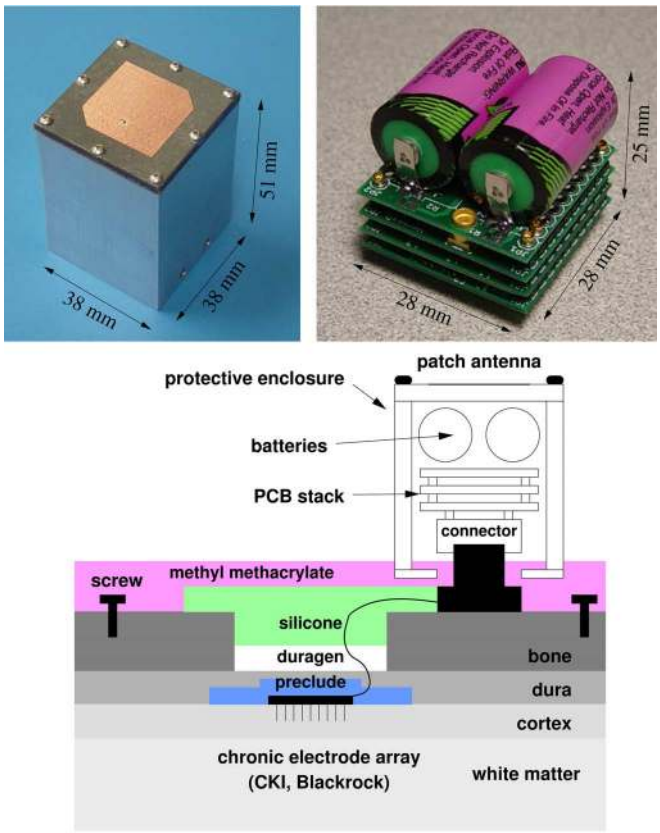

Fig. 2. Left: HermesD enclosure with a transmitter patch antenna; Right: Transmitter board stack with batteries attached. Bottom: Physical design of HermesD. 100-electrode array is implanted in macaque motor cortex. Preclude, duragen, a silicone elastomer, and methyl methacrylate protect the brain, skull, and array. AZIF connector attaches to the skull (CKI). A custom connector provides 32 of 96 channels to the PCB stack. The aluminum housing embedded in methyl methacrylate protects electronics and batteries.

with possible future expansion to support all of them. After signal amplification and multiplexing, the neural data from each channel are digitized at 30 ks/s with a resolution of 12 b/sample, followed by packetization and modulation. The frequency-shift keying (FSK) modulation method is used due to its low power consumption, the simplicity of its modulator (a VCO is the only required device), and its relative robustness against multipath channels. This modulation type also enables the use of noncoherent techniques at the receiver.

The HermesD transmitter can be tuned to any frequency between 3.7 GHz and 4.1 GHz. Since the transmission bandwidth is 60 MHz, it is possible to have six transmitters operating simultaneously and to have their signals collected by independent receivers. This is an interesting option if social interaction between several animals within a housing room is to be studied. There are a few reasons for the choice of this frequency band. First, the allocated services for the band are commercial satellite broadcast and fixed point-to-point microwave links, which pose virtually no risk of interference to this system, and vice versa. The UWB devices also operate in this frequency range, but since the maximum allowed power density is -41.3[18] dBm/MHz, corresponding to a power level 19 dB below the HermesD transmitted power (in the 60-MHz bandwidth), these devices represent a low interference risk. UWB interference probability is further minimized if the UWB devices are not located in the same room where the recordings take place due to the wall attenuation. Second, man-made electromagnetic noise, such as that originated by electric motors in some appliances, has a low-power density in this microwave region and is also unlikely to cause interference. Third, the frequency is high enough to enable the design of small- and high-efficiency antennas such as the one built for HermesD, which will be described in Section II-A.IV. Finaly, a high carrier frequency enables the use of high bandwidth signals to accommodate high bit rates — important for scalability purposes. This system can easily achieve more than 100 MHz of bandwidth for a larger number of channels. The standard animal cages used during the recording experiments have a small mesh aperture, on the order of 2.5 cm $\times$ 2.5 cm. If low carrier frequencies are used (below 1 GHz), the cage attenuation can be very significant. Transmission tests showed that frequencies around 4 GHz suffer very little attenuation.

The RF output power of the transmitter, approximately 100 μW, is enhanced by an antenna gain of 7 dB, providing enough power to cover a range over 20 m with a comfortable link margin of about 22 dB.

A. Transmitter

The detailed HermesD transmitter block diagram is shown in Fig. 3.

1) Amplifier Array and ADC: The 32-channel signals are amplified and filtered by two 16-channel biopotential array amplifiers from Intan Tech, LLC (RHA1016) [19]. These provide 46 dB of voltage gain and a configurable upper cutoff frequency, which was set to 5 kHz in our experiments, while the lower cutoff frequency was fixed at 0.05 Hz. Channels are multiplexed before being digitized by the dual channel ADC, the Linear Technology LTC1407A-1. Both multiplexed outputs from the amplifier arrays are sampled simultaneously and converted into 14-b samples. Only 12 b/sample are transmitted since the useful dynamic range is not improved by increasing the number of bits beyond this resolution. This dynamic range is limited by the noise level of the amplifier array and the maximum expected neural spike amplitude. The measured input-referred noise level

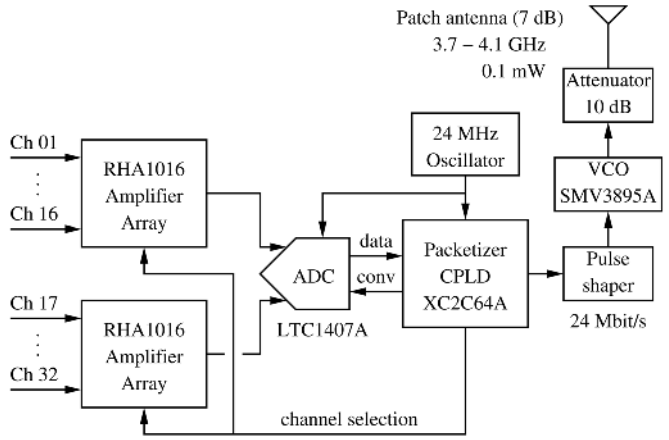

Fig. 3. HermesD transmitter block diagram.

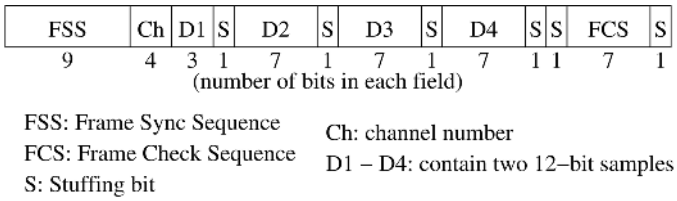

Fig. 4. HermesD frame format.

of each channel is 3.2 μVrms. The value of each least-significant bit (LSB) was set to 1.5 μ V and spike amplitudes can be as high as 6.3 mV before clipping occurs. This is a reasonable limit since both action potentials and LFPs are expected to be within this range. The sampling rate of the multiplexed channels is 480 ks/s which corresponds to a data sample rate of 480/16= 30 ks/s per individual channel. This rate is compatible with the frequency content of neural signals, which is negligible above 8 kHz.

2) Stream Packetizer and Frame Structure: The stream packetizer collects samples from the ADC and organizes them in structured frames that contain additional information for synchronization and error detection. The packetizer is implemented in a Xilinx XC2C64A CPLD (Complex Programable Logic Device), and utilizes 43 of its 64 available macrocell blocks. The maximum clock frequency at which the CPLD could run is 58 MHz, a limit considerably higher than the value needed by HermesD (24 MHz). This limit is primarily imposed by the check sum generator. Since this frequency also sets the system bit rate, this same CPLD device can be used for future Hermes versions with a higher channel count or higher channel sampling rate. The frame format is depicted in Fig. 4. These frames contain 50 bits and are continuously transmitted back-to-back. There are four 7-bit fields that contain neural data information (payload) as well as auxiliary fields that have relevant framing tasks. Their purpose and justification are described as follows.

- FSS: Frame Sync Sequence—a 9-b synchronization pattern of alternating zeros and ones (010101010) that marks the start of a frame and aids the task of the clock recovery circuit at the receiver (this pattern acts as a short clock burst). The frame construction mechanism prevents this sequence from appearing anywhere else in the body of the frame.
- Ch: Channel—a 4-b number that corresponds to the channel being scanned by the amplifier arrays; this field also acts as a frame-sequence number, useful to detect missed frames during transmission errors.
- D1..D4: a pair of 12-b samples from the selected channel of each amplifier array in two's complement format.
- FCS: a 7-b checksum that is used to validate the frame integrity; this checksum is obtained by simply summing the four 7-b data fields (Ch and D1 to D4) and by discarding any overflow bits (sum modulo 128) so that $\mathrm{FCS} \equiv ([\mathrm{Ch}, \mathrm{D1}] + \mathrm{D2} + \mathrm{D3} + \mathrm{D4}) \pmod{128}$.

Each frame also contains stuffing bits (**S** fields) that are added at the end of every group of 7 b, starting after the FSS. The value of each S bit is the complement of the value of the second bit that precedes it. This not only ensures that the FSS pattern is not created but also guarantees that the maximum sequence of equal bits is limited to 8, so that the receiver bit recovery circuit can operate flawlessly. The last stuffing bit has a different purpose: it allows extra time for the FCS field to be computed in real time, which is an important consideration if more complex error checking methods or if higher speeds are used.

With this bit stuffing technique, in addition to a small frame size, frame synchronization can be very fast, minimizing the number of rejected frames during a resynchronization event. This comes at the expense of 44% of frame overhead, with 12% contributed by stuffing bits.

The sampling frequency of each neural channel is determined by $f_\mathrm{s} = f_\mathrm{clk}/(16N) = (24 \times 10^6)/(16 \times 50) = 30$ ks/s, where f_clk is the system clock and N is the number of bits in the frame.

3) Modulator: The FSK modulator is built around a miniature VCO module, the SMV3895A from Z-Communications, Inc. The output frequency is set by a simple resistor divider and the VCO is left in a free-running mode. No frequency stabilizing mechanism is used, such as a phase-locked loop (PLL), due to power saving reasons: current low-power PLL integrated circuits (ICs) consume more than 30 mW [20]. In fact, as the occupied bandwidth of the modulated signal is fairly large, approximately 60 MHz, the VCO frequency stability or phase noise is not a major concern. The typical temperature drift of this VCO is about 0.44 MHz/°C. This drift has a low system impact since the room where the experiments take place is temperature controlled, causing an offset smaller than ± 2 MHz (the animal temperature self-control reduces the effects of ambient temperature variation even more). To further enhance the frequency stability, a 10-dB attenuator was inserted at the output of the VCO. This allows the output frequency to be fairly independent of any impedance variation of the antenna due to its occasional proximity to external objects (frequency pulling). The worst-case frequency pulling was ± 3 MHz, measured with a moving short connected to the transmitter output. On the receiver side, the maximum frequency instability is typically less than ± 2 MHz, caused by the first local oscillator (LO). The combined effect of all frequency error sources is limited to ± 7 MHz, an offset easily corrected by the receiver frequency tracking mechanism described in Section II-B.III.

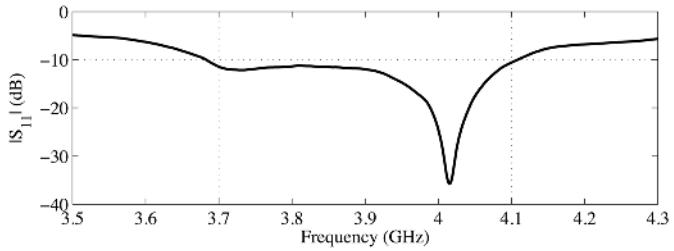

Fig. 5. Measured return loss of the HermesD RHCP patch antenna mounted on the electronics enclosure. Its 10-dB impedance bandwidth is 420 MHz and covers the 3.7–4.1-GHz frequency range.

Using a wide signal bandwidth has clear advantages in gigahertz wireless telemetry systems that do not employ frequency control or phase locking. A previously reported system using a free-running VCO at 3.2 GHz and a signal bandwidth of only 10 kHz [21] becomes impractical without frequency stability control mechanisms or fine frequency tracking at the receiver side.

The chosen VCO has a low modulation input capacitance ($C_{\rm in} \approx 11$ pF), making it suitable for large signal bandwidths. In HermesD, the source impedance driving the VCO is $R_{\rm s} = 100\,\Omega$, which sets the maximum modulation bandwidth to

$$\mathrm{BW}_{\rm mod} = \frac{1}{(2\pi R_{\rm s} C_{\rm in})} = \frac{1}{(2\pi \times 100 \times 11 \times 10^{-12})} = 145\ \mathrm{MHz}$$

thus enabling a maximum transmitter bit rate in excess of 100 Mb/s. In HermesD, the pulse-shaping filter is a third-order Bessel filter with a cutoff frequency of 30 MHz. The frequency deviation for the FSK signal is set to $f_d = 20$ MHz, which corresponds to a modulation index of $h = 2f_d/R = 2 \times 20/24 = 1.7$.

4) Antennas: The transmitter antenna sits on top of the aluminum housing and is shown in Fig. 2. Its microstrip patch design allows a very low profile construction: the patch area is 24 mm × 24 mm and the substrate used is 3.2 mm thick made out of Teflon (RO5880 laminate from Rogers Corp.). The antenna has an impedance bandwidth of 420 MHz for 10 dB of return loss, as shown by the $|S_{11}|$ plot of Fig. 5, and its operation frequency is matched to the transmitter frequency range. Basic microstrip patch antennas have a relatively low fractional impedance bandwidth, usually in the 1%–10% range. The use of a thick and low relative permittivity substrate (2.2 in the present case) in conjunction with the circular polarization (CP) characteristic were key in obtaining a fractional bandwidth of 11%. CP was obtained by truncating two opposite corners at 45° [22] and its truncation extension was optimized to minimize the axial ratio across the frequency range, using Agilent's Momentum EM simulator. The measured gain is 7.0 dB and its 88% of efficiency was enabled by the very low loss properties of the substrate ($\tan\delta = 0.0009$). The antenna can cover a full hemisphere with a maximum signal variation of 13 dB as shown in Fig. 6, which is well within the signal margin for a 20-m link distance (see Table II). This wide angular antenna coverage is a very desirable feature for reliable communications when the animal subjects are freely moving. The radiation pattern was measured in a standard room with the HP8720B vector network analyzer, using a bandpass time-domain technique [23] to mitigate the effect of signal reflections on the pattern.

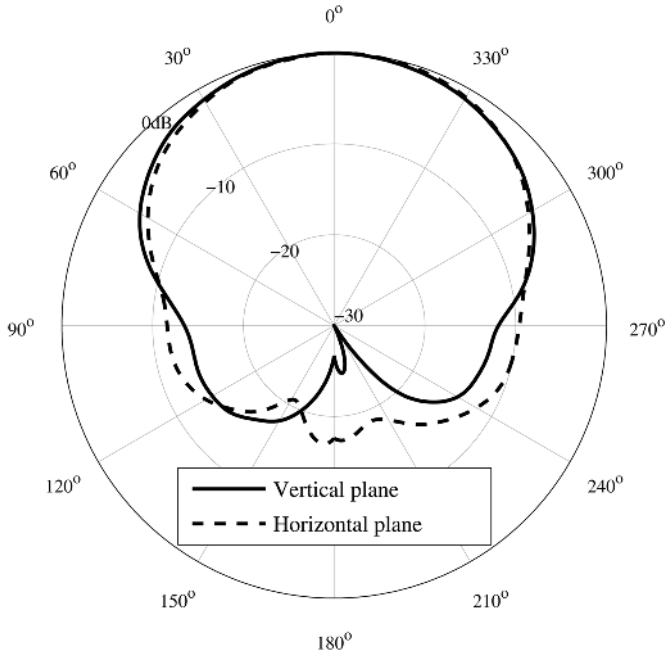

Fig. 6. Measured relative radiation plot of the HermesD transmitter antenna assembled on the enclosure at 3.9 GHz. The 0° angle corresponds to the boresight of the antenna.

TABLE II
HERMESD COMMUNICATIONS LINK BUDGET

Parameter	Value	Unit
Link distance	20	m
Frequency	4.0	GHz
Transmitter power	−10	dBm
Cable loss	1	dB
Tx antenna gain	7.0	dB
Free-space attenuation	70	dB
RX antenna gain	13	dB
Received signal power	−61	dBm
Receiver sensitivity for QEF*	−83	dBm
Signal margin	**22**	**dB**

* QEF – Quasi Error Free (error probability of 10^{-9})

Both receiver and transmitter antennas employ right-hand circular polarization (RHCP). This is particularly useful to attenuate single-bounce reflections that occur in an indoor environment, which are the main cause of signal fluctuation due to destructive interference. The first and all odd-ordered bounce reflections that arrive at the receiver have their polarization rotation reversed since incidence angles are generally below the pseudo-Brewster angle of typical wall material (60° to 70°) [24]. These echoes are attenuated by the receiving antenna which is configured for the original polarization rotation. In order to quantitatively assess the advantage gain of the circular polarization, we performed channel measurements in a 8.8 m × 5.8 m × 2.8 m room at 4 GHz, using three different transmitter antennas: an RHCP patch, a linear-polarized (LP) patch, and a quarter-wavelength monopole for the same RHCP

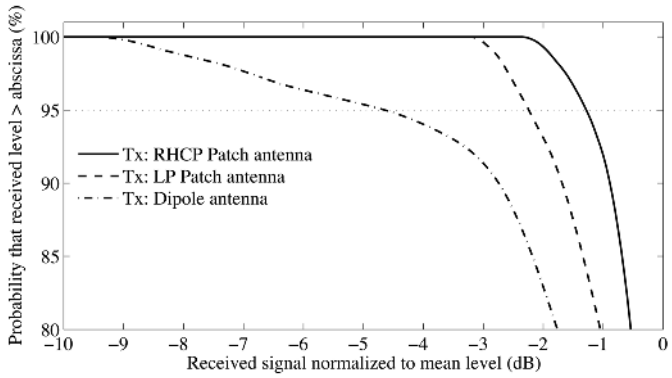

Fig. 7. Measured CCDF of the received signal envelope at 4 GHz for various transmitter antennas for a 8.8 m × 5.8 m × 2.8-m room. The measurements are for a transmitter-receiver separation range between 0.5 m and 5 m.

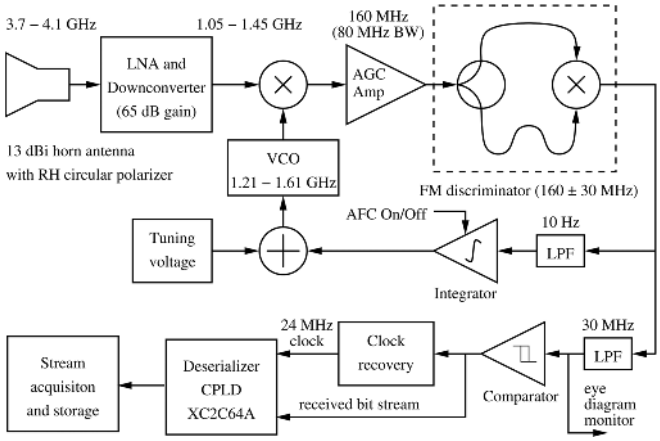

Fig. 8. HermesD receiver block diagram.

receiving antenna. The comparison is depicted in Fig. 7, using the complementary cumulative distribution function (CCDF) of the received signal envelope, for a varying transmitter-receiver separation between 0.5 m to 5 m. This plot clearly indicates that circular polarization has about 1 dB better performance over an LP patch antenna, and 4 dB over a monopole for a confidence level of 95%. This experimental data are in agreement with simulated data presented in [25], which also shows that the delay spread of the channel can be reduced by a factor of two if circular polarization is used instead of linear polarization. Reducing the delay spread is important since it is the major contributor of intersymbol interference that limits the maximum achievable data rate in single carrier communication systems such as the present one. Another advantage of circular polarization is that there is no need for polarization alignment between the transmitter and receiver antennas, a major concern for moving subjects. Also, cage attenuation effects are minimized if circular polarization is used. Linear polarization creates deep signal fades when the polarization direction happens to align with the mesh orientation.

B. Receiver

The HermesD receiver (Fig. 8) is based on the classic superheterodyne architecture with two frequency conversion stages. This receiver is based on the one described in [16] but was considerably redesigned to provide tunability and automatic carrier frequency tracking. Its main blocks and functionality are described in the following sections:

1) RF and IF Sections: The received signal is captured by a 13-dBi conical horn antenna coupled to a right-hand circular polarizer waveguide. Having a receiver antenna with a narrow beamwidth further reduces the effect of the bounced signals since their arriving angle is off the main beam direction. The receiver antenna in this experiment has 35° of 3-dB beamwidth, which is enough for complete coverage of the animal cage.

In the first receiver stage, there is a low-noise downconverter block (LNB) that amplifies and downshifts the incoming frequency to a first intermediate frequency (IF) in the 1.05-GHz to 1.45-GHz range. This device is a standard C-band LNB for commercial receiver satellite systems that inexpensively provide a very high gain (65 dB) and low-noise figure (0.5 dB). There is a second IF conversion stage that serves two purposes: 1) allows receiver tunability by varying the VCO frequency and 2) enables the action of the frequency tracking loop (AFC) to correct for any transmitter frequency drifts.

The automatic gain control (AGC) amplifier operating on the final IF frequency (160 MHz) maintains a constant output level at the demodulator input and has 70 dB of dynamic range. The AGC amplifier can process signal bandwidths up to 80 MHz, which is 20 MHz larger than the occupied bandwidth of the transmitted HermesD signal. This provides the headroom required for the operation of the AFC tracking circuit.

2) FM Discriminator: For high data rates, it is usually difficult to find well-matched FM demodulators as off-the-shelf modules. For this reason, a custom FM demodulator was designed and implemented for HermesD. It is based on the delay-and-multiply architecture shown inside the dashed block of Fig. 8. The discriminator mixer produces a voltage that varies as the $\cos(\Delta\phi)$, with $\Delta\phi$ being the phase difference between the input ports of this mixer. This phase difference is generated by using different lengths for the transmission lines connecting the signal splitter to this mixer. The main design parameter for this type of demodulator is the transmission-line length difference (Δl). The following procedure is used to obtain its value:

1) from the required frequency deviation, (f_d) and center frequency (f_c) determine k, the integer number of odd multiples of 90° phase shifts in the extra Δl length, using $k = \lfloor (f_c/f_d + 1)/2 \rfloor$;
2) then find Δl from the velocity of propagation in the transmission lines (v_p) by using $\Delta l = (2k-1)(v_p/f_c)/4$.

The Δl parameter also directly influences the maximum transition rate that the demodulator can sustain before the maximum amplitude deflection at the output starts to be attenuated. The maximum theoretical rate is limited to $R_{\max} = v_p/\Delta l = 4f_c/(2k-1)$, with a modulation index of $h = 2f_d/R = 0.5$, which corresponds to minimum-shift keying (MSK) modulation.

In the specific case of HermesD, we use the following parameters: $f_c = 160$ MHz, $f_d = 30$ MHz, $v_p = 2 \times 10^8$ m/s (RG-174 coaxial cable); $k = \lfloor (160/30 + 1)/2 \rfloor = 3$; and $\Delta l = (2 \times 3 - 1)/4 \times (2 \times 10^8)/(160 \times 10^6) = 6.25$ m.

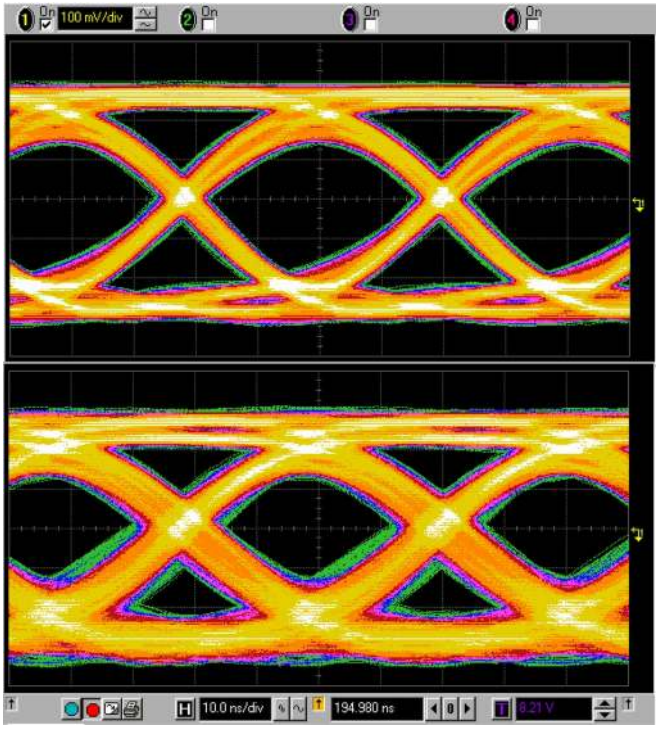

Fig. 9. Received signal eye diagrams at 20 m (top) and 30 m (bottom) away from the transmitter at 24 Mb/s. The eye heights and widths are, respectively, 300 mV/32 ns for the first case, and 250 mV/24 ns for the second.

Note that f_d is set to 10 MHz larger than the frequency deviation used for the HermesD signal in order to accommodate carrier frequency offsets. The coaxial cable that introduces the extra delay in the frequency discriminator can be replaced by a lumped delay line device for a more compact implementation.

A snapshot of the demodulated signal eye diagram at 24 Mb/s with a transmitter-receiver separation of 20 m and 30 m is displayed in Fig. 9. This measurement took place in a 30-m-long interior hallway, with the transmitter and receiver antennas pointing at each other. For this test, the transmitter CPLD was reconfigured to continuously generate a $2^9 - 1$ pseudorandom sequence ($x^9 + x^5 + 1$ generator polynomial) and a BER tester was used at the receiver side. Inboth cases, the eye height and width provided a comfortable operation margin, and no errors were detected. These diagrams show that the system is still usable beyond 30 m, especially in an outdoor environment where the signal degradation due to multipath is not as severe as in the indoor case.

3) AFC Loop: The automatic frequency control loop maintains the receiver optimally tuned to the transmitter carrier frequency that is subject to variations over time. Any error that exists between transmitter and receiver appears as a dc offset voltage at the output of the frequency discriminator. This voltage is low-pass filtered (to remove the modulation component) and then integrated to provide a correction voltage to the VCO control input. During the initial adjustment, the receiver is manually tuned with the AFC loop turned off. After the FSK signal enters the discrimination range of the demodulator, the AFC tracking loop can be activated, which then constantly adjusts the VCO frequency to maintain the final

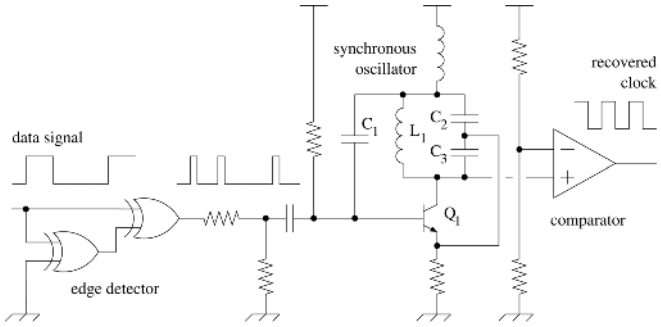

Fig. 10. Synchronizer circuit of the clock-recovery subsystem.

intermediate-frequency (IF) signal centered about 160 MHz. The AFC loop can correct frequency offsets up to ± 20 MHz, a range higher than the maximum estimated frequency error in Section II-A.III (± 7 MHz).

4) Bit Synchronizer: Synchronization is an essential operation in digital communication receivers. Carrier synchronization is not required for FSK since it can be demodulated by using noncoherent methods as is the case of this work. However, symbol synchronization must be included to provide a correct bit sampling instant. In HermesD, the bit synchronization is achieved by the clock recovery circuit this is based on a single transistor oscillator with injection locking called the synchronous oscillator (SO). It has several attractive features that are exploited in this system: 1) its acquisition time is very fast—less than 1 μs, corresponding to less than half a frame—thus minimizing the number of lost frames during reacquisition events (PLL-based synchronizers require acquisition times of one order of magnitude higher); 2) wide tracking range—1% of the clock frequency—which is wide enough for the transmitter bit clock frequency tolerance (± 100 ppm); and 3) low circuit complexity that is easy to tune.

The implemented synchronizer circuit shown in Fig. 10 is a simplification of the original design in [26], where a single transistor oscillator is used instead of the original two. The additional sensitivity and noise rejection capabilities provided by the original two-transistor synchronous oscillator are not required in clock-recovery applications where the input signal has low-noise content. The oscillator transistor is configured as a free-running sinusoidal Colpitts oscillator, whose frequency (f_0) is determined by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{C_2 + C_3}{L_1 C_2 C_3}}.$$

The SO transistor conducts only during very short periods of time and synchronization occurs when the pulses from the edge detector force the short conduction time windows of transistor Q_1 to be time aligned. The acquisition time depends inversely on the tracking bandwidth of the SO, the latter being mainly set by the amplitude of the input pulses, transconductance of Q_1, and C_3. A very unique feature of SO is its storage time during which the oscillator retains input frequency information when there are no synchronization pulses at the input. This time is partly decoupled from the tracking bandwidth and can be increased by increasing the feedback capacitor C_1[27]. This property is especially useful if the input data sequence contains long

runs of the same bit level. Tests to this property of the designed SO showed a storage of about 30 b, which is in agreement with data provided in [27]. This storage exceeds the requirement set by the HermesD frame format that has a maximum run length of 8 b.

5) Computer Interface: The receiver also includes a CPLD to convert the recovered serial data stream into a 32-b parallel bus for computer storage. This bus has a clock rate that is 32 times lower than the incoming serial stream (750 kwords/s) which makes the computer data acquisition more efficient and cost effective. The digital I/O interface device is a National Instruments USB-6259. Frame storage, synchronization, disassembly, and error check are performed offline by software developed in the C and Matlab languages.

III. Measurement Results

A. Device Validation

This system was used to obtain neural data *in vivo*. One adult male rhesus macaque was implanted with a 96-electrode array (BlackRock Microsystems, Inc., Salt Lake City, UT [17]) using standard neurosurgical techniques similar to those described in [28] 22 months prior to the current study. The electrode array was implanted in a region spanning the arm representation of the dorsal aspect of premotor cortex (PMd) and primary motor cortex (M1), as estimated visually from local anatomical landmarks. All of the surgical procedures were approved by Stanford University's Institutional Animal Care and Use Committee (IACUC.) The HermesD prototype was tested inside an RF-shielded experimental room while the animal was seated in a primate chair. All 32 channels of neural data were received wirelessly at a distance of 1 m (this was a small room that did not allow longer distances).

B. Neural Data Recordings

Some of the initial recordings performed are shown in Fig. 11. Samples acquired by the receiver were aligned sequentially in time based upon when the corresponding frame was recovered. In order to produce the four panels on the leftmost column of Fig. 11, a second-order high-pass Butterworth filter with a 250-Hz cutoff frequency was applied to the data to isolate the neural spike band. The root mean square (rms) of each channel was calculated from 120 s of recorded data by taking the standard deviation of the spike band. For the channels shown, from top to bottom, the rms values measured were 15.4 μV, 14.3 μV, 8.1 μV, and 15.9 μV. Across all 32 channels, the rms has a mean of 15.7 μV and a standard deviation of 4.8 μV. The distribution of rms values is similar to the distribution measured on the same electrodes with a commercially available wired recording system, Cerebus (Blackrock Microsystems Inc., Salt Lake City, UT), with a mean of 17.2 μV and a standard deviation of 5.5 μV. In order to find neural spikes in the data, a threshold of three times the rms value was set. If this value was crossed, a snippet of data around this time was extracted and a shape heuristic was applied. This heuristic filters for events in which the negative deflection is followed by a positive deflection. To reduce the timing jitter in each waveform snippet that is created by thresholding a discrete signal, the snippets

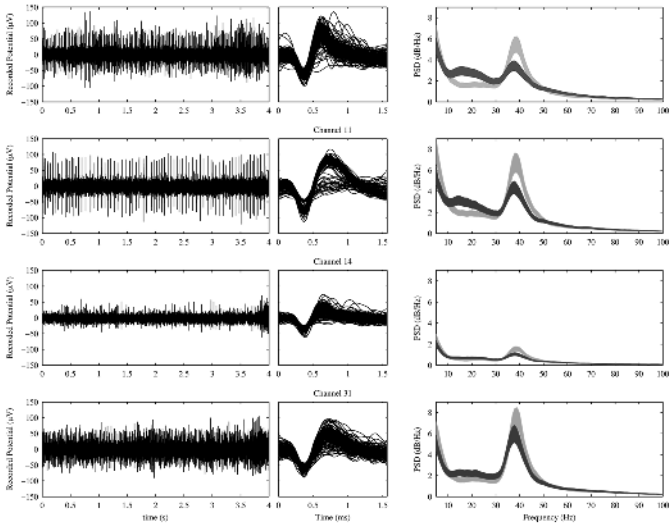

Fig. 11. Wireless in-vivo recording of neural activity of a rhesus macaque. The left plots show 4 s of neural activity for channels 1, 11, 14, and 31. The extracted action potentials from the data in the left are shown in the middle column. The plots on the right column show the power spectrum density of the local field potential during reaching (light gray) and idling (dark gray). The width of the spectrum traces represents the 95% confidence intervals of the spectral energy estimation.

are upsampled by a factor of 8, center of mass aligned, and downsampled to the original sampling rate. Action potentials extracted from the 4 s of data in the left column are shown in the middle column of the same figure.

In order to verify the ability to record local field potentials (LFPs), data were collected under two behavioral conditions, reaching and idling. In the reaching condition, the animal was actively engaged in a point-to-point reaching task to targets in a 2-D plane with the contralateral limb. During the idle condition, the animal was seated in the same posture, but was not engaged in a task and remained relatively still. LFPs were analyzed by applying an 8th order Chebyshev Type I lowpass filter with a cutoff frequency of 160 Hz and downsampling the data from 30 kHz to 400 Hz. The power spectrum density (PSD) traces were constructed by using the Thomson Multitaper Method as in [29]. This plot is shown on the right column of the figure, with the idle condition in blue and the reaching condition in red. The width of the PSD traces represents the 95% confidence intervals of the spectral energy estimation. The decrease in power around 20 Hz (beta band) and increase of around 40 Hz (gamma band) during reaching are consistent with previous reports [3], [30], thus providing evidence that the LFP signal captured by this system is meaningful.

C. BER Performance and Link Budget

In order to characterize the HermesD system communication performance, we measured the BER for two receiver conditions: 1) with perfect clock recovery in which the transmitter BER tester clock was directly connected to its clock receiver input after optimum delay adjustment and 2) with clock recovery performed by the synchronous oscillator circuit presented in Fig. 10. The test sequence used was a $2^9 - 1$ maximum-length PN sequence, which contains a maximum run length of 9 (one

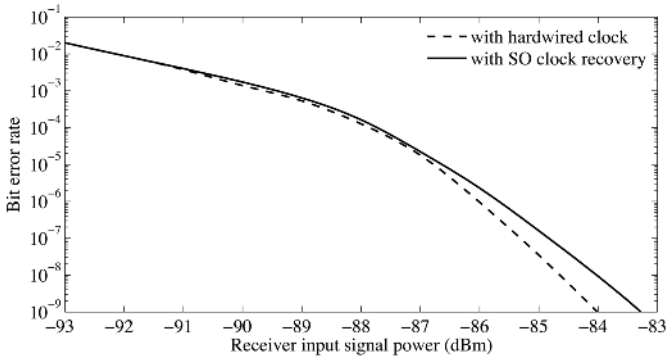

Fig. 12. Bit-error-rate performance of HermesD with perfect clock recovery (hardwired receiver clock) and with the synchronous oscillator clock-recovery circuit. The input signal power is the power level at the receiver site, before the antenna.

TABLE III
POWER BREAKDOWN OF HERMESD

Device	Amp. Array	ADC	CPLD	VCO	OSC	Total
Power (mW)	68	14	26	30	5	142

bit more than the maximum run length of the frame format). The BER curves in Fig. 12 show that the performance degradation introduced by the bit synchronizer is minimal, less than 1 dB for error probabilities higher than 10^{-9}. This error level can be considered a quasi-error-free operation (QEF), corresponding to about 1 error event per a million transmitted samples, and it defines the receiver sensitivity level: -83 dBm. Table II lists the main parameters of the link budget at 4 GHz for 20 m of separation. The obtained margin (22 dB) is adequate to cope with other factors affecting the received signal level, such as antenna radiation pattern variations (13 dB in a full hemisphere) and additional multipath-related signal fluctuations.

IV. POWER AND SYSTEM SCALABILITY

Power consumption in wireless biomedical systems is the major parameter to be optimized since one desires long recording times with the smallest battery volume possible. The largest power contributor for the HermesD transmitter is its analog section as shown in Table III.

The power-supply subsystem includes three dc-dc switching voltage regulators to meet the supply needs of the different circuit modules:

- 5.0 V for the amplifier arrays (LTC3525, Linear Technology Corp., Milpitas, CA);
- 2.8 V for the ADC, VCO and CPLD I/O ports (LM3671–2.8, National Semiconductor, Santa Clara, CA);
- 1.8 V for the CPLD core (LM3671–1.8, National Semiconductor, Santa Clara, CA).

The overall efficiency of the regulator ensemble is 87% which accounts for an additional 21 mW of power dissipation. Power is provided by two parallel-connected 3.6 V Li-$SOCl_2$ batteries, the SAFT LS14250, Bagnolet, France, with a nominal

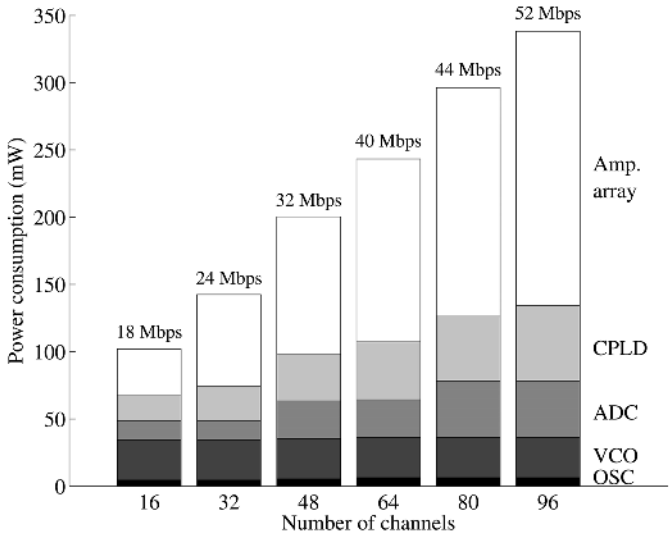

Fig. 13. HermesD power scalability projection.

capacity of 1200 mAh each. The measured effective capacity was 800 mAh when used with the HermesD transmitter, with an achieved life time of 33 h.

The HermesD architecture was designed with scalability in mind. Increasing the number of simultaneous transmitted channels is just a matter of adding more amplifier arrays and ADCs. Each additional ADC can digitize up to 32 channels. Importantly, no other hardware modifications are required since the CPLD and modulator can currently handle higher data rates, up to 58 Mb/s. On the receiver side, the AGC and demodulator bandwidths are the only parameters that need to be matched to the new data rates.

The bar plot of Fig. 13 shows the estimated data rates and the power consumption contribution of the different devices for other number of channels, assuming we use the same IC device types. We notice that the data rate does not scale linearly with the number of channels; the data rate/per channel efficiency actually improves with the number of channels. This is due to a lower frame overhead achieved for higher channel count, using the same frame design of HermesD. As an example, for the 96-channel case, each frame would contain six 12-b samples, a 4-b channel field, an 11-b FSS, a 9-b FCS, and 10 stuffing bits, totaling 108 b, reducing the frame overhead to 28% from the 44% of this design. While most of the transmitter components scale linearly with the number of channels, the modulator and system clock oscillator powers are almost insensitive to it. From this chart, it is clear that the analog power portion becomes even more relevant for a large number of channels (about 60% for 96 channels). However, by using more power-efficient amplifier arrays, described in recent publications, it would be possible to greatly reduce the overall power consumption of HermesD. As an example, Harrison *et al.* presents an integrated amplifier array with 100 channels in which the total power consumption is only 3.5 mW [11]. This device is not available commercially and could not be used as an off-the-shelf part in HermesD. But when this part becomes available, we can have a very significant power reduction, going from 345 mW to about 130 mW for the 96-channel case.

V. Discussion

HermesD is designed to wirelessly transmit, receive, and store 32 channels of broadband neural data from a freely-moving primate at a rate of 30 ks/s and 12-b/sample of resolution. The power consumption of the system is sufficiently low to make it possible to operate for more than a day from two small and lightweight batteries before recharge or replacement. This time period is long enough to allow many different experiments with freely-moving animals.

Due to the high-data-rate property of the system, the storage requirements are demanding: 3 MB/s or about 250 GB/day of data are continuously generated. The signal recordings are usually synchronized with video capture, which adds 80 GB/day more for standard video graphics array (VGA) at 30 fps. The stored data can then be processed by a cluster of computers to perform neurobehavioral analyses or even real-time processing.

Another important aspect in neural prosthetic systems is latency—the time between neural signal acquisition and actuation of the output device. The latency amount should be limited to a few tens of milliseconds for a smooth operation of the prosthetics. The HermesD transmitter latency is about 1.8 μs (43 b) which will have a negligible impact on the overall latency if the system is used as an instrument to perform prosthetic tasks.

A. Applications

Preliminary studies with freely-moving primates using existing systems have already resulted in several interesting findings. For example, Jackson and colleagues reported neural plasticity brought about through paired stimulation over many days in the motor cortex [31]. For neural prosthetic applications, Santhanam and colleagues showed that action potential waveforms can change over time, requiring that long-term clinical devices track and adapt to these changes [3]. However, it was not possible to do a full population study of waveform shape over time until a system, such as HermesD, is made available. HermesD can initially be used to extend these findings, tracking many neurons simultaneously over many days. Furthermore, simultaneous video for behavioral measurements can be combined with neural recording and used to develop simple algorithms for behavioral state classification. This represents the first step toward implementing neural prosthetic algorithms in a freely-moving animal. Recently, there has been increased interest in using several kinds of neural signals in neural prosthetics. For example, it may be possible to combine spike waveforms with lower frequency local field potential, or to record simultaneously from electrocorticogram arrays (ECoG) as well as from high-impedance electrode arrays. HermesD allows these types of signals to be recorded simultaneously in experiments with freely-moving animals. Beyond neural prosthetic applications, the long range of this system enables experiments with animals in a far less constrained environment. Some laboratories perform behavioral research on rhesus macaques embedded in social colonies. With this device, it would be possible to record neural activity from animals interacting freely in a complex setting. This represents a fundamentally new source of data for the neuroscience community. Also, the ability to certify neuron identity across days should allow neural plasticity to be studied across much longer time periods. Therefore, a wireless neural recording may lead to important new discoveries about processing in the cerebral cortex.

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References

[1] U. Jurgens and S. Hage, "Telemetric recordings of neuronal activity," *Methods*, vol. 38, pp. 195–201, 2006.

[2] A. B. Schwartz, "Cortical neural prosthetics," *Annu. Rev. Neurosci.*, vol. 27, pp. 487–507, 2004.

[3] G. Santhanam, M. D. Linderman, V. Gilja, S. I. R. Afsheen Afshar, T. H. Meng, and K. V. Shenoy, "Hermesb: A continuous neural recording system for freely behaving primates," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 11, pp. 2037–2050, Nov. 2007.

[4] K. Wise, D. Anderson, J. Hetke, D. Kipke, and K. Najafi, "Wireless implantable microsystems: High-density electronic interfaces to the nervous system," *Proc. IEEE*, vol. 92, no. 1, pp. 76–97, Jan. 2004.

[5] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-Electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[6] M. Rizk, I. Obeid, S. H. Callender, and P. D. Wolf, "A single-chip signal processing and telemetry engine for an implantable 96-channel neural data acquisition system," *J. Neural Eng.*, vol. 4, no. 3, pp. 309–321, Sep. 2007.

[7] A. M. Sodagar, K. D. Wise, and K. Najafi, "A fully integrated mixed-signal neural processor for implantable multichannel cortical recording," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 6, pp. 1075–1088, Jun. 2007.

[8] K. S. Guillory, A. K. Misener, and A. Pungor, "Hybrid RF/ir transcutaneous telemetry for power and high-bandwidth data," in *Proc. IEEE 26th Annu. Int. Conf. IEEE EMBS*, San Francisco, CA, Sep. 2004, pp. 4338–4340.

[9] D. M. Ackermann, B. Smith, K. L. Kilgore, and P. H. Peckham, "Design of a high speed transcutaneous optical telemetry link," in *Proc. 28th Annu. Int. Conf. IEEE EMBS*, New York, Sep. 2006, pp. 2932–2934.

[10] C. A. Chestek, V. Gilja, P. Nuyujukian, R. J. Kier, F. Solzbacher, S. I. Ryu, R. R. Harrison, and K. V. Shenoy, "Hermesc: Low-Power wireless neural recording system for freely moving primates," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 17, no. 4, pp. 330–338, Aug. 2009.

[11] R. Harrison, R. Kier, C. Chestek, V. Gilja, P. Nuyujukian, S. Ryu, B. Greger, F. Solzbacher, and K. Shenoy, "Wireless neural recording with single low-power integrated circuit," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 17, no. 4, pp. 322–329, Aug. 2009.

[12] I. Obeid, M. A. Nicolelis, and P. D. Wolf, "A multichannel telemetry system for single unit neural recordings," *J. Neurosci. Meth.*, no. 133, pp. 33–38, 2003.

[13] P. Mohseni, K. Najafi, S. J. Eliades, and X. Wang, "Wireless multichannel biopotential recording using an integrated FM telemetry circuit," *IEEE Trans. Neural Syst. Rehab. Eng.*, vol. 13, no. 3, pp. 263–271, Sep. 2005.

[14] G. A. DeMichele and P. R. Troyk, "Integrated multi-channel wireless biotelemetry system," in *Proc. IEEE 25th Annu. Int. Conf. EMBS*, Cancun, Mexico, Sep. 2003, pp. 4338–4340.

[15] 31 Channel Wireless Neural Headstage System. Durham, NC, Triangle Biosystems, Inc., 2008. [Online]. Available: http://www.tbsi.biz/Files/W31Spec.pdf

[16] H. Miranda, V. Gilja, C. A. Chestek, K. V. Shenoy, and T. Meng, "A high-rate long-range wireless transmission system for multichannel neural recording applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 2009, pp. 1265–1268.
[17] E. M. Maynard, C. T. Nordhausen, and R. A. Normann, "The Utah intracortical electrode array: A recording structure for potential brain-computer interfaces," *Electroencephalograp. Clin. Neurophysiol.*, vol. 102, no. 3, pp. 228–239, Mar. 1997.
[18] I. Oppermann, M. Hämäläinen, and J. Iinatti, "Introduction," in *UWB Theory and Applications*. New York: Wiley, 2004, pp. 1–7.
[19] Fully integrated 16-channel biopotential amplifier array.. Salt Lake City, UT, Intan Technologies, LLC, 2006. [Online]. Available: http://www.intantech.com/products.html
[20] "ADF4113: single, integer-N 4.0 GHz PLL with programmable prescaler and charge pump," Analog Devices, Inc., 2004. [Online]. Available: http://www.analog.com/en/rfif-components/pll-synthesizersvcos/adf4113/products/product.html
[21] P. Irazoqui-Pastor, I. Mody, and J. Judy, "In-vivo EEG recording using a wireless implantable neural transceiver," in *Proc. 1st Int. IEEE EMBS Conf. Neural Eng.*, Mar. 2003, pp. 622–625.
[22] R. Garg, P. Bhartia, I. Bahl, and A. Ittipihoon, "Circularly polarized microstrip antennas and techniques," in *Microstrip Antenna Design Handbook*. Norwood, MA: Artech House, 2001, pp. 495–500.
[23] Appl. Note 1287–12: Agilent Time Domain Analysis Using a Network Analyzer Agilent Technologies, Inc., 2007.
[24] U. S. Inan and A. S. Inan, "Reflection, transmission, and refraction of waves at planar interfaces," in *Electromagnetic Waves*. Englewood Cliffs, NJ: Prentice-Hall, 2000, pp. 120–232.
[25] A. Kajiwara, "Line-of-sight indoor radio communication using circular polarized waves," *IEEE Trans. Veh. Technol.*, vol. 44, no. 3, pp. 487–493, Aug. 1995.
[26] V. Uzunoglu and M. H. White, "The synchronous oscillator: A synchcronization and tracking network," *IEEE J. Solid-State Electron.*, vol. SC-20, no. 6, pp. 1214–1226, Dec. 1985.
[27] V. Uzunoglu and M. H. White, "Synchronous and the coherent phase-locked synchronous oscillators: New techniques in synchronization and tracking," *IEEE Trans. Circuits Syst.*, vol. 36, no. 7, pp. 997–1004, Jul. 1989.
[28] N. Hatsopoulos, J. Joshi, and J. G. O'Leary, "Decoding continous and discrete behaviors using motor and premotor cortical ensembles," *J. Neurophysiol.*, vol. 92, pp. 1165–1174, 2004.
[29] B. Pesaran, J. S. Pezaris, M. Sahani, P. P. Mitra, and R. A. Andersen, "Temporal structure in neuronal activity during working memory in macaque parietal cortex," *Nat Neurosci.*, vol. 5, no. 8, pp. 805–811, Aug. 2002.
[30] J. P. Donoghue, J. N. Sanes, N. G. Hatsopoulos, and G. Gaal, "Neural discharge and local field potential oscillations in primate motor cortex during voluntary movements," *J Neurophysiol.*, vol. 79, no. 1, pp. 159–173, Jan. 1998.
[31] J. Mavoori, A. Jackson, C. Diorio, and E. Fetz, "An autonomous implantable computer for neural recording and stimulation in unrestrained primates," *J. Neurosci. Meth.*, vol. 148, pp. 71–77, Oct. 2005.

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