Heterodyne Phase Locking: A Technique for High-Speed Frequency Division

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***Abstract*—A phase-locked loop incorporating a cascade of mixers can provide integer or fractional divide ratios at high frequencies. The circuit topology and its variants are presented, and their advantages over static, dynamic, and injection-locked dividers are described. The effect of nonidealities such as the spurious response and noise of the mixers is also analyzed. A divide-by-two prototype realized in 0.13-μm CMOS technology operates from 64 GHz to 70 GHz while consuming 6 mW from a 1.2-V supply.**

***Index Terms*—Frequency synthesizers, injection locking, *LC* oscillators, lock range, millimeter-wave dividers, Miller dividers flip flops.**

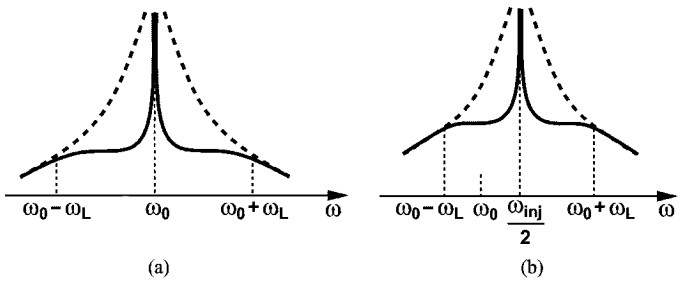

Fig. 1. Phase noise degradation in an ILD.

I. Introduction

THE interest in millimeter-wave communications for broadband wireless applications has motivated work on high-frequency CMOS circuits, e.g., oscillators, frequency dividers, and phase-locked loops (PLLs) [1]–[3]. The design of dividers, especially for use within a synthesizer loop, entails serious challenges that manifest themselves as the input frequency is pushed toward the f_T of the transistors.

This paper introduces the concept of "heterodyne phase locking" as a versatile technique for high-speed frequency division with integer or fractional moduli [4]. The concept is demonstrated in a divide-by-two prototype that achieves a lock range of 64–70 GHz in 0.13-μm CMOS technology.

Section II presents a brief analysis of conventional frequency-division techniques and their limitations. Section III describes the heterodyne phase-locking principle, its variants, and its design issues. Section IV deals with the design of the prototype, and Section V summarizes the experimental results.

II. Limitations of Conventional Dividers

Frequency dividers are typically realized in one of three forms: flip-flop-based ("static") topologies, Miller ("dynamic") regenerative loops, and injection-locked oscillators. Current-steering static dividers, even with inductive peaking, reach a maximum speed of about 25 GHz in 0.13-μm CMOS technology. As the load resistance in the latches is reduced, the maximum toggle frequency increases further, but the circuit topology approaches that of an *LC* quadrature oscillator that is injection-locked to the input and, hence, provides a narrower lock range. Miller dividers operating at millimeter-wave (mm-wave) frequencies must also employ purely resonant loads while satisfying certain selectivity and phase-shift requirements [5]. As such, they too exhibit a narrow lock range.

While achieving high frequencies, injection-locked dividers (ILDs) suffer from several drawbacks. First, both their lock range and output phase noise are inversely proportional to the tank Q, thus incurring a direct tradeoff. The relative lock range is roughly given by

$$\frac{\omega_L}{\omega_{\rm inj}} = \frac{2}{\pi}\frac{I_{\rm inj}}{I_{\rm osc}} \cdot \frac{1}{Q} \tag{1}$$

where $I_{\rm inj}$ and $I_{\rm osc}$ denote the peak values of the input current and the oscillation current [6]. The relative phase noise is given by Leeson's equation and is proportional to $[\omega_0/(2Q\Delta\omega)]^2$, where $\omega_0 = \omega_{\rm inj}/2$ and $\Delta\omega$ denotes the frequency offset. The tradeoff between the two manifests itself as higher operation frequencies are sought: (1) requires that Q remains constant whereas Leeson's equation recommends that Q be scaled with ω_0.

If injection-locked to an input, an oscillator exhibits lower phase noise at frequency offsets up to the edge of the lock range [Fig. 1(a)]. However, this suppression becomes less pronounced if the oscillator must lock near $\omega_0 \pm \omega_L$ [Fig. 1(b)] [6]. For an ILD, this occurs if the natural oscillation frequency ω_0 deviates from $\omega_{\rm inj}/2$ due to mismatches between the oscillator generating $\omega_{\rm inj}$ and the ILD itself. In fact, even systematic mismatches appear to be inevitable here. Shown in Fig. 2(a) is an example, where the oscillation frequency is scaled by a nominal factor of two by placing two inductors in parallel and halving transistor widths. Unfortunately, the parallel inductors exhibit *twice* (rather than one-half of) the parasitic capacitance, and their mutual coupling alters their net value.

It is possible to simultaneously tune the main oscillator and the ILD [7], but this technique does not overcome the effect of frequency mismatches. As illustrated by the tuning characteristics of Fig. 2(b), the frequency mismatch between $f_{\rm VCO}/2$ and $f_{\rm ILD}$ persists across the entire range if the two characteristics

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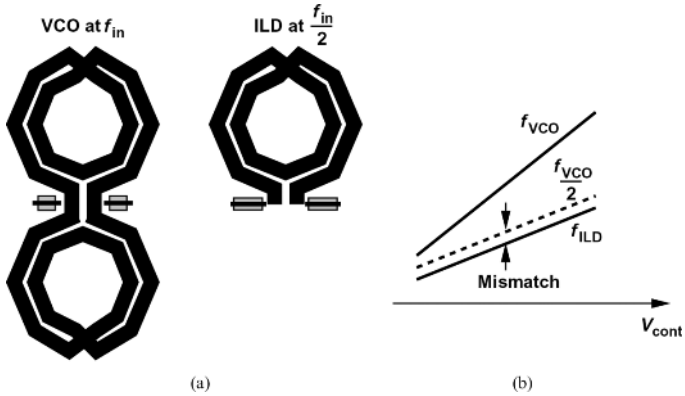

Fig. 2. (a) Layout of a VCO and an ILD with scaled inductors. (b) Problem of frequency mismatch in simultaneous tuning of a VCO and an ILD.

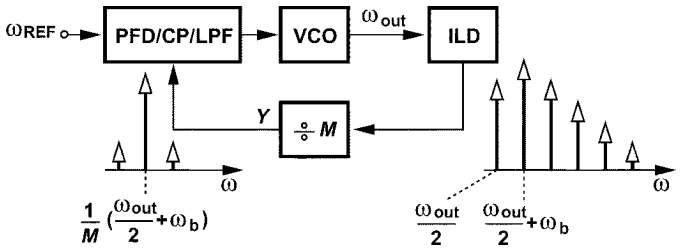

Fig. 3. False lock due to failure of the LD.

exhibit equal slopes. Otherwise, $f_{\rm VCO}/2$ and $f_{\rm ILD}$ intersect at one value of $V_{\rm cont}$ and diverge for other values.

Another critical drawback of ILDs is that they can cause false lock in a PLL environment. Suppose, as shown in Fig. 3, an ILD senses a frequency $\omega_{\rm out}$ that is somewhat outside its lock range, thereby producing an asymmetric (pulled) spectrum. The key point here is that the largest component in this spectrum occurs not at $\omega_{\rm out}/2$, but at $\omega_{\rm out}/2+\omega_b$, where ω_b denotes the beat frequency due to injection pulling. After experiencing limiting and frequency division in the $\div M$ circuit, the spectrum emerges at Y with a main component at $(\omega_{\rm out}/2+\omega_b)/M$ and small sidebands at an offset of $\pm\omega_b$. If the sidebands fall outside the loop bandwidth, the PLL locks such that

$$\omega_{\rm REF}=\frac{1}{M}\left(\frac{\omega_{\rm out}}{2}+\omega_b\right) \tag{2}$$

and hence $\omega_{\rm out}=2(M\omega_{\rm REF}-\omega_b)$.

The above false lock phenomenon occurs if the ILD provides an inadequate lock range or if it employs discrete tuning [2]. In the latter case, while the PLL searches for the proper tuning of the ILD, false lock may take place—a condition that is difficult to discern from correct lock. In other words, discrete tuning of ILDs may not be practical.

Another divider topology employs a VCO operating at $\omega_{\rm in}/2$ and providing an output at $\omega_{\rm in}$ (e.g., at the common-source node of a cross-coupled pair) such that the VCO can be phase-locked to the input [8]. However, this approach suffers from a relatively narrow lock range because both the frequency-doubling mechanism and the input phase detector exhibit a high loss.

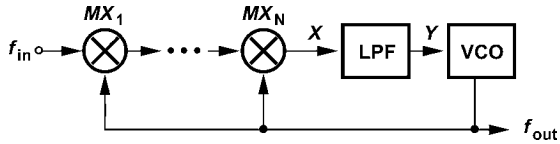

Fig. 4. Heterodyne PLL.

III. Heterodyne Phase Locking

A. Basic Principle

Consider the PLL depicted in Fig. 4, where the phase detector (PD) (e.g., a single mixer) is replaced with a cascade of N mixers that are driven by the VCO. It is assumed that each mixer is followed by "mild" filtering so as to suppress the sum-frequency component produced by that mixer. As will be explained in Section IV, the low-pass filter (LPF) need not provide much suppression. In a manner similar to a heterodyne receiver, the cascade of mixers downconverts the input N times, thereby generating a dc component at node X if $f_{\rm in}=Nf_{\rm out}$. Thus, the loop locks such that $f_{\rm out}=f_{\rm in}/N$. We call the mixer ports driven by the VCO the local-oscillator (LO) port and those sensing $f_{\rm in}$ or its downconverted versions the RF port.

Heterodyne phase locking offers a number of advantages over conventional frequency-division techniques. First, divide ratios greater than two—whether odd or even or a power of two or not—are almost as easily afforded as a divide ratio of two. As N increases, the VCO must drive a larger number of mixers while operating at a proportionally lower frequency, thus suffering little tradeoff between its phase noise and tuning range. Nonetheless, as N increases, the frequency sensed by the *second* mixer in the cascade exceeds $f_{\rm in}/2$ and approaches $f_{\rm in}$ for large N, raising the conversion loss of this mixer to some extent.

The ability to readily provide various divide ratios without significant speed degradation proves to be a critical advantage of heterodyne phase locking. By contrast, if realized with flip-flops, divide-by-three circuits are typically twice as slow as their divide-by-two counterparts. Moreover, Miller and injection-locked dividers cannot easily provide arbitrary divide ratios.

The second advantage of heterodyne phase locking is its much more relaxed tradeoff between the lock range and phase noise than that of ILDs. The lock range of PLLs can reach the entire tuning range of the VCO, which is typically about five times as wide as the injection lock range of an ILD operating at the same frequency. The key point here is that, unlike in ILDs, maximizing the tank Q in the PLL does not impact its lock range.

The third advantage of heterodyne phase locking relates to its ability to provide fractional divide ratios. For example, insertion of a $\div M$ circuit in the feedback path of Fig. 4 yields a divide ratio of M/N. Fig. 5 depicts a more general case, where the LO port of mixer number j is preceded by a $\div K_j$ circuit, thereby leading to

$$f_{\rm out}=\frac{M}{\frac{1}{K_1}+\cdots+\frac{1}{K_N}}f_{\rm in}. \tag{3}$$

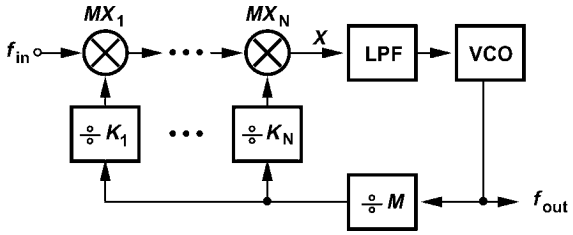

Fig. 5. General heterodyne PLL.

It is also possible to insert dividers in the RF port of mixers MX_2-MX_N to create more complex expressions. Furthermore, a quadrature VCO can be employed so as to produce quadrature outputs. Also, external continuous or discrete tuning can be utilized to widen the range.[1]

The heterodyne PLL of Fig. 4 merits several observations. First, unlike typical PLLs, this topology operates the phase detector at very high frequencies. Thus, to provide a constant and well-defined gain, the PD transistors must experience relatively complete switching and, hence, the VCO must produce large swings. Second, if placed in a synthesizer loop, the frequency divider must negligibly impact the overall settling behavior. For this reason, and to maximize the suppression of the oscillator phase noise, the loop bandwidth of the divider must be maximized. Third, the high operation frequencies, even at the input of MX_N, prohibit the use of standard phase/frequency detectors and charge pumps. Consequently, the circuit behaves as a type I PLL.[2] Note that the sum frequency produced by MX_N is equal to $2f_{\text{in}}/N$ under locked conditions and needs not be suppressed much because it modulates the VCO at twice its operation frequency. Thus, the LPF bandwidth ω_{LPF} can be chosen to be large to allow a wide lock range and a reasonable damping factor ($\propto \sqrt{\omega_{\text{LPF}}}$ in type I PLLs).

While targetting mm-wave frequencies, the heterodyne PLL principle can be applied to lower frequencies as well, e.g., to create noninteger divide ratios. Also, if the last mixer in the chain senses sufficiently low frequencies, it can be replaced with a phase/frequency detector and charge pump so as to widen the lock range. In the 90-nm and 65-nm generations, it is expected that static divide-by-two circuits achieve speeds up to a few tens of gigahertz, Miller dividers (with reasonable lock range) up to 50 GHz, and heterodyne PLLs up to 100 GHz.

B. Spurious Response of Mixers

The above description of heterodyne PLLs has assumed that only the difference frequency produced by one mixer is applied to the next. In practice, however, simple first- or second-order inter-mixer filtering may suppress the sum frequency only to some extent. Moreover, the harmonics generated in the RF and LO ports of each mixer give rise to various spurious components.

Consider the $\div 2$ realization shown in Fig. 6. Frequency components that produce a finite dc quantity at X can potentially cause false lock. With the aid of Fig. 7, we observe the following.

[1]However, external tuning issues related to ILDs apply here as well.

[2]Unless the LPF is implemented as an integrator, in which case the flicker noise of the integrator may prove problematic.

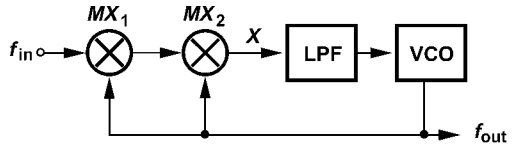

Fig. 6. Divide-by-two heterodyne PLL.

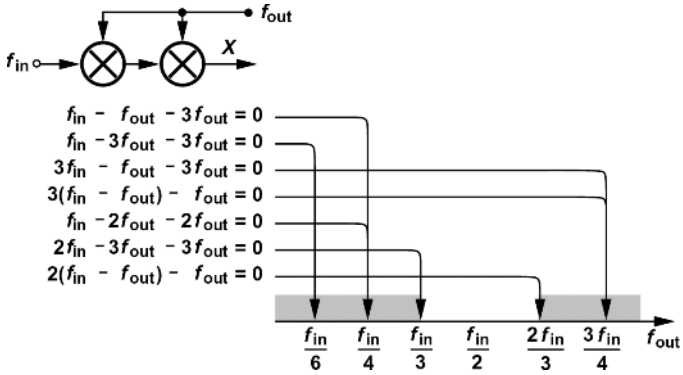

Fig. 7. Summary of mixer spurs and possible false lock frequencies.

1) The sum frequency generated by MX_1 and mixed with f_{out} by MX_2 appears as $f_{\text{in}} + f_{\text{out}} \pm f_{\text{out}}$ at X and is removed by the LPF.
2) The third harmonic of f_{out} yields $f_{\text{in}} - f_{\text{out}} - 3f_{\text{out}}$ and $f_{\text{in}} - 3f_{\text{out}} - 3f_{\text{out}}$ at X, making $f_{\text{out}} = f_{\text{in}}/4$ or $f_{\text{out}} = f_{\text{in}}/6$ possible solutions.
3) The third harmonic of f_{in} produces $3f_{\text{in}} - f_{\text{out}} - 3f_{\text{out}}$ at X, making $f_{\text{out}} = 3f_{\text{in}}/4$ a possible solution.
4) The third harmonic of $f_{\text{in}} - f_{\text{out}}$ (produced by the input port of MX_2) is mixed with f_{out}, making $f_{\text{out}} = 3f_{\text{in}}/4$ a possible solution.
5) Due to random asymmetries, the second harmonic of f_{out} may also be mixed with the input, generating $f_{\text{in}} - 2f_{\text{out}} - 2f_{\text{out}}$ at X and yielding $f_{\text{out}} = f_{\text{in}}/4$ as a possible solution.
6) Similarly, $2f_{\text{in}} - 3f_{\text{out}} - 3f_{\text{out}}$ and $2(f_{\text{in}} - f_{\text{out}}) - f_{\text{out}}$ may emerge at X, raising $f_{\text{in}}/3$ and $2f_{\text{in}}/3$ as possible solutions.

Fig. 7 depicts the possible solutions along a frequency axis. Arising from second or third harmonics, these mixing products experience a smaller loop gain than the main component does and are therefore unlikely to cause false lock. Nonetheless, since all of the possible solutions fall outside the range $[f_{\text{in}}/3\ 2f_{\text{in}}/3]$, one can simply choose the VCO tuning range to avoid such solutions. *LC* oscillators readily satisfy this condition as their tuning range is typically much narrower than one octave.

In addition to the above components, higher order mixing products appear but with negligible impact on the operation. For example, a component at $2f_{\text{in}} - 2f_{\text{out}} - 3f_{\text{out}}$ raises the possibility of $f_{\text{out}} = 2f_{\text{in}}/5$, but its amplitude is given by the *product* of three small components.

As the number of mixers in the cascade increases, the input frequency range that avoids potentially troublesome components becomes narrower. The practical limits arising from spurious mechanisms may manifest themselves for divide ratios greater than four.

C. Noise of Mixers

The cascade of mixers serving as the phase detector in Fig. 4 introduces noise in the downconversion operation, modulating the VCO and generating phase noise at the output. Fortunately, the mixers do not need to be linear even with respect to their RF port and, hence, can be optimized for noise and conversion gain. To analyze the effect of the noise of the mixers, suppose the entire cascade is characterized by an input-referred noise voltage $\overline{V_{n,\mathrm{mix}}^2}$ (per unit bandwidth) and a voltage conversion gain K_{mix}. We represent the mixer noise in 1 Hz around a frequency of ω_n by $\sqrt{2}V_{n,\mathrm{mix}}\cos\omega_n t$, assume the input is $V_{\mathrm{in}}\cos\omega_{\mathrm{in}}t$, and express the output as $V_{\mathrm{VCO}}\sin[\omega_{\mathrm{out}}t+\phi_n(t)]$. The objective is to calculate $\phi_n(t)$.

Mixing with the output N times is equivalent to multiplication by $V_{\mathrm{VCO}}\sin[N\omega_{\mathrm{out}}t + N\phi_n(t)]$. Thus, the output at node X in Fig. 4 is of the form $(\sqrt{2}V_{n,\mathrm{mix}}\cos\omega_n t + V_{\mathrm{in}}\cos\omega_{\mathrm{in}}t)V_{\mathrm{VCO}}\sin[N\omega_{\mathrm{out}}t + N\phi_n(t)]$. Incorporating the conversion gain and expanding this expression, we obtain the signal at node Y as

$$\begin{aligned} V_Y(t) =& K_{\mathrm{mix}}V_{\mathrm{in}}\sin[N\phi_n(t)] \\ &+ K_{\mathrm{mix}}\sqrt{2}V_{n,\mathrm{mix}}\sin(\omega_{\mathrm{in}}-\omega_n)t \end{aligned} \tag{4}$$

where $N\phi_n(t)$ is assumed to be much less than 1 rad and $\omega_{\mathrm{in}}-\omega_n$ within the bandwidth of the low-pass filter. The VCO is modulated by this waveform, generating an excess output phase given by

$$\begin{aligned} \phi_n(t) =& K_{\mathrm{VCO}}\int K_{\mathrm{mix}}V_{\mathrm{in}}\sin[N\phi_n(t)]dt + K_{\mathrm{VCO}} \\ &\times \int K_{\mathrm{mix}}\sqrt{2}V_{n,\mathrm{mix}}\sin(\omega_{\mathrm{in}}-\omega_n)t\,dt. \end{aligned} \tag{5}$$

Approximating $\sin[N\phi_n(t)]$ with $N\phi_n(t)$, differentiating both sides with respect to t, and regrouping the terms yields

$$\begin{aligned} &\frac{d\phi_n}{dt} - K_{\mathrm{VCO}}K_{\mathrm{mix}}V_{\mathrm{in}}N\phi_n \\ &\qquad = K_{\mathrm{VCO}}K_{\mathrm{mix}}\sqrt{2}V_{n,\mathrm{mix}}\sin(\omega_{\mathrm{in}}-\omega_n)t. \end{aligned} \tag{6}$$

In other words, $\phi_n(t)$ is a sinusoid having a frequency of $\omega_{\mathrm{in}}-\omega_n$ and an rms value of

$$\phi_{n,\mathrm{rms}} = \frac{K_{\mathrm{VCO}}K_{\mathrm{mix}}V_{n,\mathrm{mix}}}{\sqrt{(\omega_{\mathrm{in}}-\omega_n)^2+(K_{\mathrm{VCO}}K_{\mathrm{mix}}V_{\mathrm{in}}N)^2}}. \tag{7}$$

The maximum occurs if the first term in the denominator is negligible with respect to the second, hence

$$\phi_{n,\mathrm{rms,max}} = \frac{V_{n,\mathrm{mix}}}{NV_{\mathrm{in}}}. \tag{8}$$

For example, if the cascade of mixers exhibits a noise figure of 20 dB, then $V_{n,\mathrm{mix}} = 9.1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$, and the output phase noise reaches -153 dBc/Hz for $V_{\mathrm{in}} = 0.2$ V and $N = 2$.

IV. Divide-by-Two Prototype

A heterodyne PLL for divide-by-two operation (Fig. 6) has been designed and fabricated. Fig. 8 shows the realization of the first mixer, where a passive structure is followed by an amplifier. With nearly rail-to-rail swings produced by the VCO, simulations indicate that, for a given input capacitance, such a topology provides a greater conversion gain than an active mixer does. Transistors M_1-M_4 downconvert f_{in} to $f_{\mathrm{in}}/2$ and apply the resulting signal to the stage consisting of M_5–M_6 and L_1–L_2. Realized as a single symmetric spiral, L_1 and L_2 resonate with their surrounding capacitance at $f_{\mathrm{in}}/2$ and attenuate the component at $3f_{\mathrm{in}}/2$.

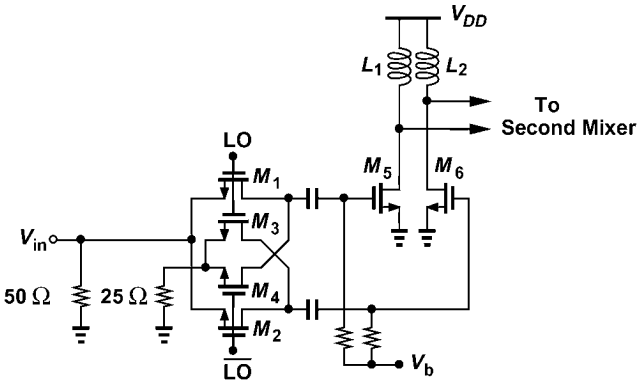

Fig. 8. Realization of the first mixer.

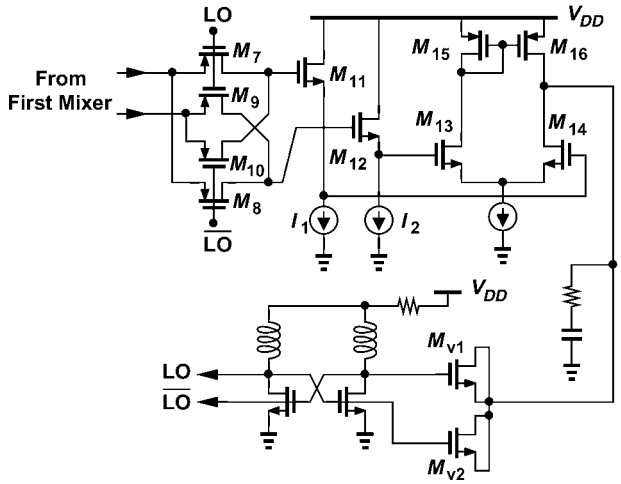

Fig. 9. Implementation of the second mixer, baseband amplifier, and VCO.

The circuit of Fig. 8 employs a double-balanced mixer as it would receive differential inputs when placed in an on-chip synthesizer. For test purposes, however, one input is tied to ground through a 25-Ω resistor. With their small dimensions ($W/L = 2.5\ \mu\mathrm{m}/0.13\ \mu\mathrm{m}$), M_1-M_4 present a small capacitance at the RF input or to the VCO. When loaded by the second mixer, the circuit exhibits a voltage conversion of 0 dB while drawing a supply current of 1.5 mA.

Fig. 9 depicts the second mixer, the baseband amplifier, and the VCO. With the output common-mode (CM) level of the first mixer near V_{DD}, the second mixer can incorporate either capacitive coupling and NMOS devices or direct coupling and PMOS transistors. The former suffers from the parasitics of the coupling capacitors and the latter from the lower mobility of PMOS devices, both yielding comparable gains. The latter is chosen here because it provides a high CM level for the level-shift source followers M_{11}–M_{12}.

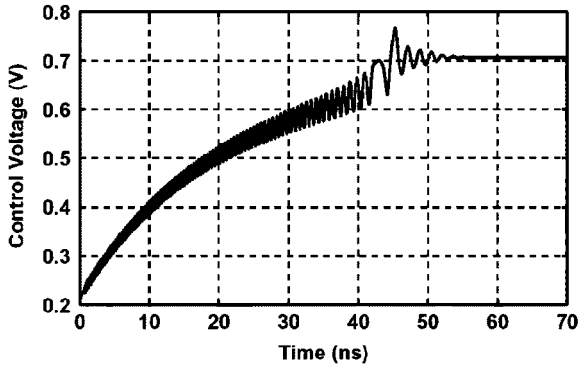

Fig. 10. Lock transient of divide-by-two circuit.

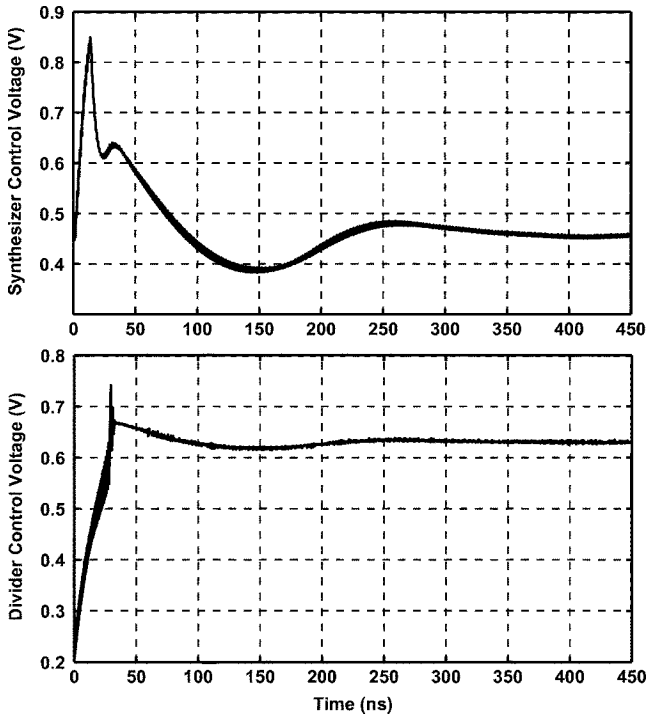

Fig. 11. Transient behavior of a synthesizer employing a heterodyne PLL divider.

Two measures are taken to maximize the VCO tuning range. First, the baseband amplifier comprising M_{13}–M_{16} provides a relatively wide output voltage range. Second, the VCO CM level is around $V_{\rm DD}/2$ so that MOS varactors M_{v1} and M_{v2} can sustain both negative and positive voltages, yielding the maximum capacitance range. The cascade of the second mixer and the baseband amplifier exhibits a voltage conversion gain of 10 dB while drawing a supply current of 1.2 mA. The VCO drains 2.3 mA.

Fig. 10 shows the simulated lock transient of the divider in the worst case, namely, with the control voltage at which the gain of the VCO is maximum (≈7.2 GHz/V). The loop takes approximately 60 ns to settle—which is much faster than typical synthesizers.

The dynamic behavior of the divider has also been studied in a synthesizer environment. A 66-GHz charge-pump PLL has been simulated whose feedback divider incorporates the above circuit

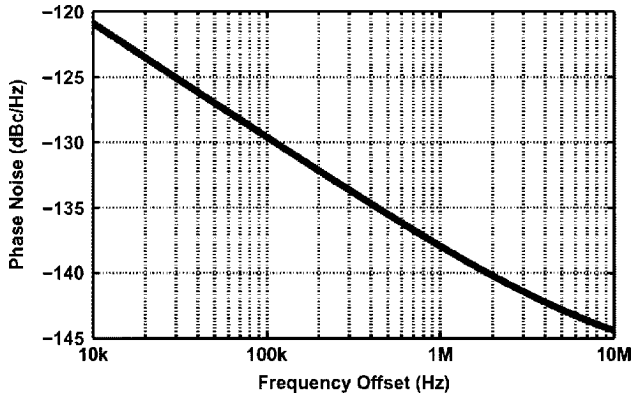

Fig. 12. Output phase noise of the divider.

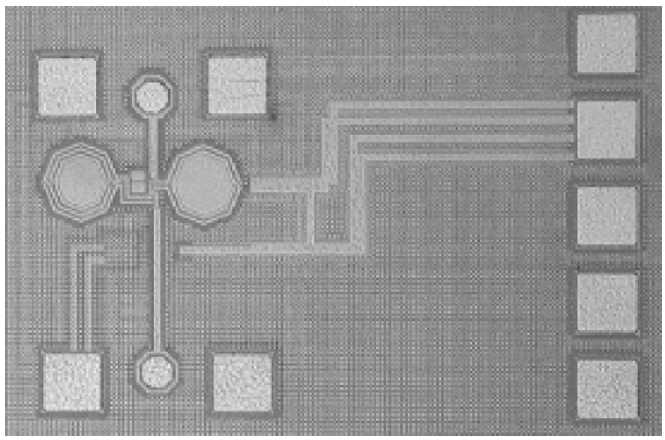

Fig. 13. Divider die photograph.

followed by a $\div 32$ chain. Fig. 11 plots the control voltages of the synthesizer and the divider as a function of time. We observe that, for $t < 30$ ns, the divider is not locked, prohibiting the synthesizer from correct lock transient. After the divider locks, the synthesizer proceeds with its natural settling and the divider tracks the frequency variation.

Fig. 12 plots the simulated output phase noise of the divide-by-two heterodyne PLL with a noiseless sinusoid applied to the input. It is observed that the phase noise is far below that of synthesizers in which this divider may be embedded. Interestingly, simulations suggest that the phase noise at 1-MHz offset arises primarily from the flicker noise of the baseband circuitry M_{11}–M_{16} and I_1–I_2 in Fig. 9. The -10-dB/dec slope from 10-kHz to 100-kHz offset arises because the flicker-noise-dominated phase noise is shaped by the first-order high-pass transfer of the PLL.

V. Experimental Results

The divide-by-two prototype has been fabricated in 0.13-μm CMOS technology. Fig. 13 shows the photograph of the die, whose active area measures approximately 200 μm × 100 μm. The circuit has been tested on a high-speed probe station with a supply voltage of 1.2 V. The V-band generator serving as the input produces a level of -2 dBm but the input probe and pad attenuate the signal by approximately 1.5 dB.

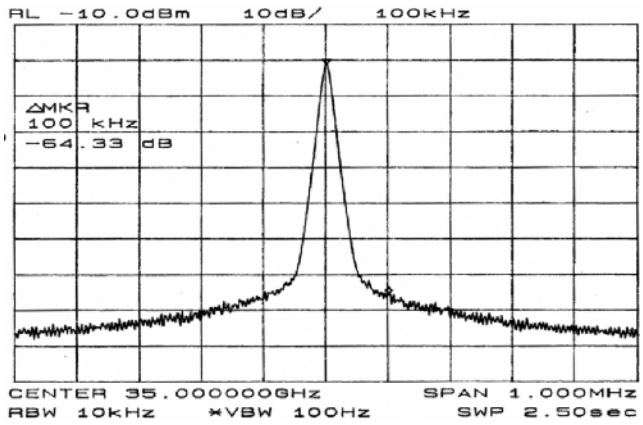

Fig. 14. Measured output spectrum.

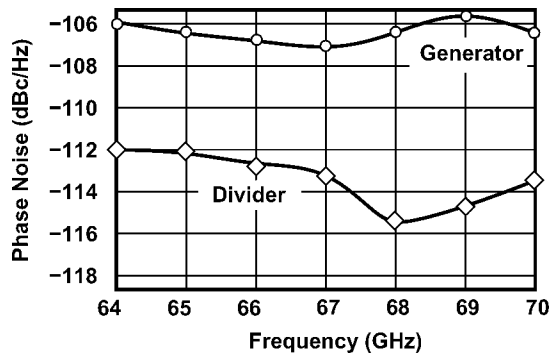

Fig. 15. Measured generator and output phase noise.

TABLE I
COMPARISON OF PERFORMANCE

	Divider in [2]	This Work
Lock Range *	1.3%	9.4%
Maximum Required Input Level	0 dBm	−3.5 dBm
Power Dissipation	2.75 mW	6 mW
Supply Voltage	0.5 V	1.2 V
Technology	90−nm CMOS	0.13−um CMOS

*Excluding external tuning.

Fig. 14 shows the measured output spectrum when the circuit is locked to a 70-GHz input. The output spectrum has been examined with different spans, and no spurious components have been observed.

Fig. 15 plots the output phase noise of the divider and the V-band generator across the lock range. With the high noise of the generator (which multiplies a 14-GHz source by a factor of 5), the divider contributes negligible noise, simply tracking the input with a 6-dB reduction. The larger difference around 68 GHz is attributed to measurement uncertainties and/or additional amplitude noise at the output of the generator that is suppressed by the divider.

Table I compares the performance of this design with that of the injection-locked divider described in [2].

VI. CONCLUSION

This paper proposes the concept of heterodyne phase locking as a means of frequency division. The ability to provide integer or fractional divide ratios while maintaining a high speed makes this topology attractive for mm-wave applications. A divide-by-two prototype demonstrates the potential of this technique by operating at 70 GHz in 0.13-μm CMOS technology while consuming 6 mW.

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