Heterogeneous Nano-electronic Devices Enabled by Monolithic Integration of IIIV, Ge, and Si to expand future CMOS functionality

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ABSTRACT

Compound-Semiconductor-on-Silicon is a field that has been actively pursued for years with success for mixed-signal applications [1]. This has been in parallel to the aggressive CMOS scaling roadmap. As the demand for higher performance and functionality grows for digital components, to address power and density scaling, the need drives the convergence of new materials and nano-devices. This paper discusses the important aspects of materials, integration, device and circuit implementation of such processes to target 7nm and 5nm CMOS technology nodes. Specifically, defect engineering of III-V and Ge hetero-epitaxy in fin replacement process, III-V FinFET device design, Vertical nanowire process and circuits. Since there is no one universal material or device that can address the power and performance need of future electronics, we show that the integration of different device-types will be needed and the method to enable such integration become an important approach.

Keywords: Direct monolithic integration. Compound semiconductor on Si, III-V, Ge, SiGe, FinFET, Nanowires, Tunnel FETs.

1 INTRODUCTION

The proliferation of smart mobile devices and the ever growing user expectations for bandwidth and connectivity will drive the continual need for software and hardware advancements. At the core of the hardware will be new process technologies that not allow for more power-efficient CMOS transistors but also increasing level of integration to enable higher level of functionality.

3D-IC's by stacking and connecting dies of different functions with through-silicon via processes are emerging as an upcoming heterogeneous SOC enabler. Since connectivity between stacked layers may be limited by nearest-neighbor layers, the stagnation of performance/density scaling of the components of the stacked 2-D layers, will again limit the 3-D system scaling in the near future. Hence, there is still strong value proposition to enhance the density and functionality at the transistor/circuit level, especially enabling specialized devices that can be applied to boost specific functionality. At the finest grain, co-integration of high-density heterogeneous transistors has been challenged by ability to combine disparate materials and structures while maintaining low enough complexity and defectivity.

2 MATERIAL & PROCESS INTEGRATION

With the maturation of epitaxy process technology, ability to combine materials of large lattice mismatch is becoming possible with lowering defectivity. Through defect engineering, we will soon have options to integrate IIIV and Ge-based material on Si at different scale, from global wafer level to fine-grain local levels of the order of circuits and devices (Figs. 1 and 2). This opens up possibilities to integrate heterogeneous devices that leverage the unique properties offered by epitaxial combination of materials.

In that context, the heterogeneous integration of III-V high mobility semiconductors on a Si platform for a non-planar architecture such as FinFET is an option to enhanced the performance of future CMOS generations. The indium gallium arsenide compound semiconductor, with high Indium concentration has been considered as a candidate for n-channel MOS devices 7nm and beyond CMOS technologies, due to its intrinsically superior electron mobility. A straight-forward option for the growth of such a complex ternary compound would be to start with a binary compound buffer like InP that is lattice-matched to $In_{0.53}Ga_{0.47}As$ channel. Nevertheless, there is still a need to absorb the 8% lattice mismatch between the Si substrate and the InP buffer. In addition, the polar/non-polar interfaces resulting in the generation of crystalline defects in high density: misfit and threading dislocations, twins, stacking faults, anti-phase boundaries (APBs). Several options have been considered to obtain high quality single crystal III-V compounds on Si with low defect density: strain relaxed buffers, epitaxial lateral overgrowth, rapid melt growth, and the defect confinement technique [2,3,4,5].

To achieve heterogeneous channel material integration at a fine-grain level where different devices can share similar process modules and integration, it is necessary to develop process methods that ease process complexity while allowing for design flexibility. Aspect-ratio-based

defect trapping to epitaxially integrate IIIV/Ge material on Si appear to offer a good option. Unlike global wafer-level stress-relaxed buffer (SRB) methods, selective epitaxy is applied locally where the depth and volume of material can be adjusted per application (Fig.1).

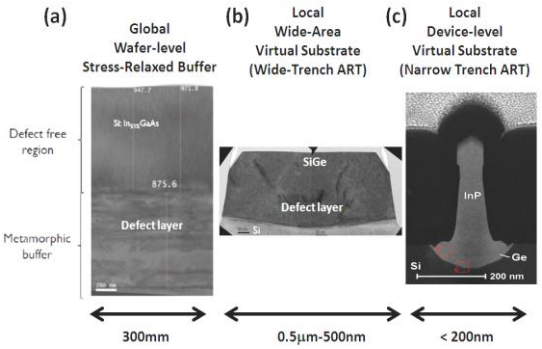

Fig. 1 Epitaxial methods of integrating mismatched materials on Si substrate. Cross-section TEM images showing (a) Wafer level strain-relaxed buffer growth on Si wafer, (b) local wide-area epitaxial Si replacement by defect trapping in wide trenches, & (c) device level replacement by defect-trapping in narrow trenches.

At the most aggressive device level, low-defectivity epitaxy can be produced in narrow trenches of 80-90nm depth, compatible with Si bulk FinFET structures. This is accomplished by replacing existing Si Fins with III-V or Ge-based epitaxial buffers (Fig. 2), leading to structures that share aspect ratio and feature sizes to those of conventional Si FinFET devices.

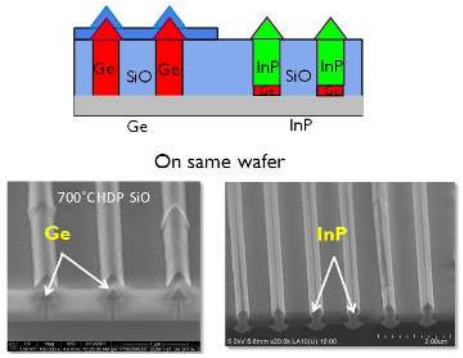

Fig. 2 Co-integration of IIIV & Ge on Si by method of sequentially masked narrow trench epitaxial growth.

We report in detail here, a low-defectivity and low-temperature InP epitaxy method by selective-area metal organic vapor phase epitaxy (SA-MOVPE) on patterned 300mm Silicon wafer with trimethylindium (TMIn), tertiarybutylarsine(TBAs) and tertiarybutylphosphine(TBP) sources. The growth template is formed from fully-formed Si fins with oxide isolations. The Si fins are controllably wet etched using TMAH (5% @ 80C) to produce a trench cavity with (111)-V groove at the base of the cavity (Fig. 3). This (111)-V groove structure is necessary to promote rapid Si-InP lattice mismatch relief and mitigate APB formation (Fig. 3(a)). The residual <111> -oriented - threading dislocation defects (TDs) that propagate up from the trench bottom are terminated at the sidewalls. The TDs are visibly confined in a defect network located within 20nm-30nm from the bottom (Fig. 3 (b)), leading to a low-defectivity InP top layer as a buffer for subsequent InGaAs channel epitaxy.

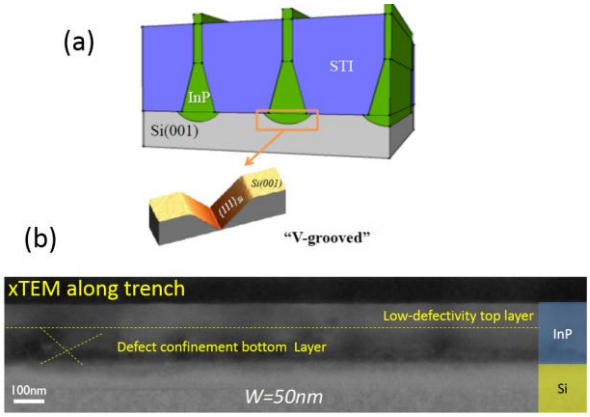

Fig. 3 (a) Schematic showing the fin trench structure with (111)-V groove, defect-mitigated epitaxial growth of III-V on Si. (b) The xTEM along the trench showing the epitaxy of InP on Si, and the confined defective layer.

Following low-defectivity InP buffer $In_xGa_{1-x}As$ with x > 0.5 on InP buffer layer is selectively grown by a "TBP-to-TBAs" switch. Reproducibly faceted growth of InGaAs above the trench indicate quality of the underlying epitaxial layers (Fig. 4)

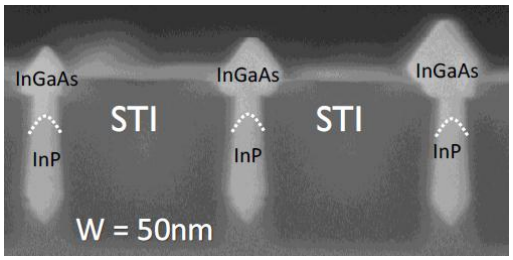

Fig. 4. InGaAs/InP hetero-eptaxy on Si in 50nm wide trenches, showing faceted InGaAs above the trench structures.

3 HIGH-MOBILITY HETEROGENOUS DEVICES

InGaAs/InP and Ge/SiGe FinFETs have been successfully demonstrated on 300mm Si substrate using the selective epitaxial fin replacement process that involves epi growth in trenches and aspect-ratio defect trapping (Fig. 5). Besides high-channel carrier mobility, integrating compound semiconductors heterostructures into multi-gated

nano-devices like FinFETs combines Fin structural confinement with quantum well confinement enhancing the electrostatics of FinFET structures.

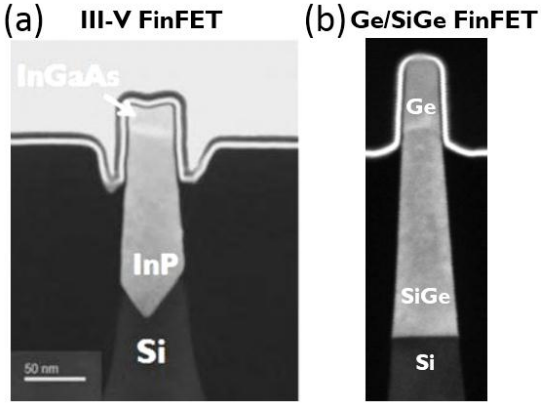

Fig. 5 InGaAs/InP and Ge/SiGe Quantum-well FinFET devices enabled by the selective epitaxial fin replacement processes.

The quantum-well due to the channel and buffer interface offers additional electrostatic carrier confinement (Fig. 6).

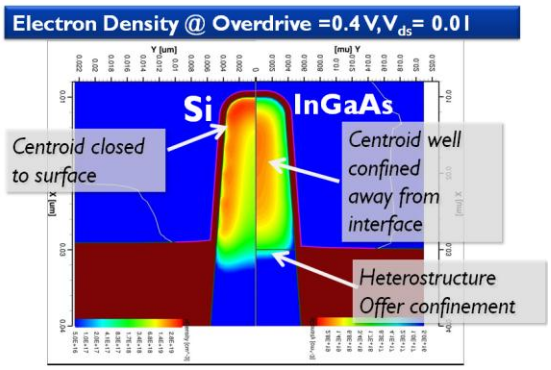

Fig. 6 Simulations of charge confinement differences between Si fin Vs. InGaAs-InP QW FinFET.

We have shown that such confinement effect is evident in device electrical leakage behavior as a function gate and QW placement (Fig. 7).

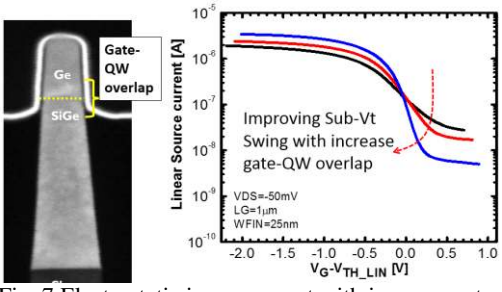

Fig. 7 Electrostatic improvement with increase gate-quantum-well overlap showing the increase isolation effect of the quantum well.

Due to the intrinsic lower band-gap of high-mobility channels (InGaAs, Ge, etc.), which leads to increased band-to-band tunneling (BTBT) leakage. Since typical low-power technologies need devices designed to different leakage (Vth) points to allow for efficient power management, increased BTB leakage renders such high-mobility channel unsuitable as low-leakage devices. Simulations show that the effective fields at the drain of such devices would lead to BTBT leakages exceeding the leakage specifications for low-operating and stand-by power devices (Fig. 8).

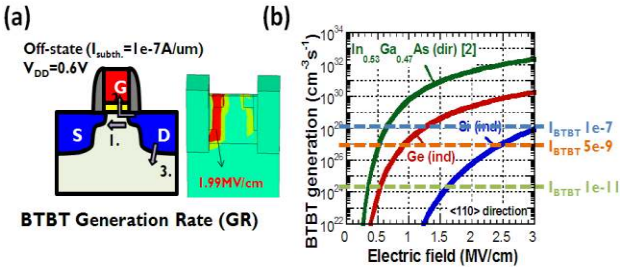

Fig. 8 Process-calibrated band-to-band tunneling (BTBT) model applied to model drain leakage as a function of high-mobility channel material.

Due to the leakage limitations of these channel materials, the need to co-integrate wider band-gap devices to address the low-leakage components (Eg. Low-standby leakage circuits, High-density SRAM, etc.) at the system level is needed. A selective epitaxial technique as detailed here is most suitable for this purpose

4 NEXT-GENERATION NOVEL DEVICES

The ability to direct epitaxial growth to assemble nanostructures is a natural evolution of heterogeneous epitaxy. Figure 9 depicts a process of using a template in combination with the surface property of Si (111) to direct vertical InAs nanowires. Nanowire diameter can be controlled throuh modulating the Group III to Group V precursor flow rates.

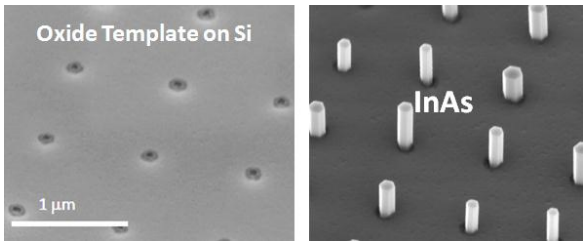

Fig. 9. SEM image showing deterministic growth of InAs nanowire by oxide template on Si(111) using MOCVD.

New logic and SRAM circuits base on vertical nanowires are being investigated. Being more compact than conventional 2-D lateral layouts (Fig. 10), they are very promising options to enable continual density scaling beyond 7nm and 5nm, while easing the requirements on optical lithography

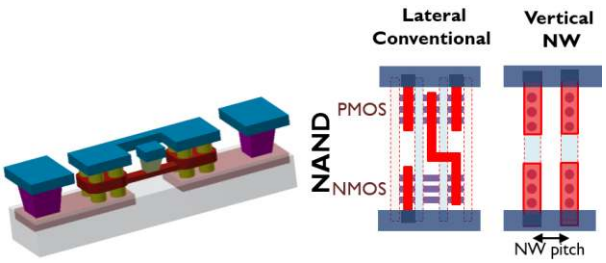

Fig. 10 (Left) 3-D Schematics of an CMOS Inverter circuit with vertical nanowire devices. (Right) A circuit layout comparison of a NAND logic gate with convetional 2D lateral devices Vs. Vertical nanowires.

Besides Nanowire MOSFETs, Nanowire Tunnel FETs that are capable of switching with steeper subthreshold swing are being investigated as well [6]. With steeper subthreshold swing, such devices may be operated at much lower supply voltages, suitable for ultra-low-V_{dd} and low-leakage operations. However, such devices with intrinsically lower drive current capability may have to be co-integrated with MOSFETs to cover the full power-performance operational range of future low-power technologies. Again, a heterogeneous integration of different material and device structures are sought.

We demonstrate here a process integration that allows for co-integration of vertical Nanowire MOSFETs and TFETs. By a source replacement process, asymmetric vertical TFET device structures can be enabled (Fig. 11). Polarity and performance of TFETs can be selectively modulated by the source material replacement process where n-TFETs with Ge source on Si can be integrated with p-TFET with InAs source on Si. Ge-source n-TFET has been fabricated and tested (Fig. 12), showing the BTBT current enhancement with Ge source, compared to control devices with Si, and SiGe sources (Fig. 13).

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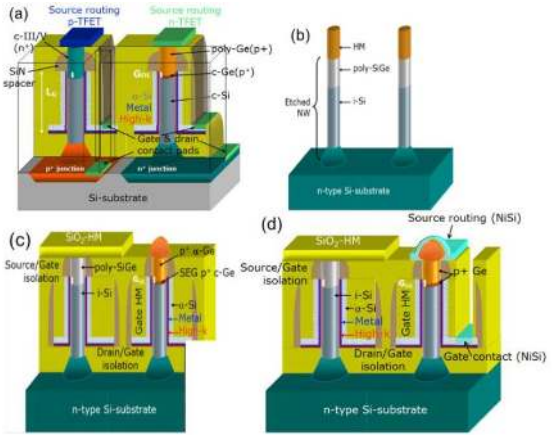

Fig. 11 Schematic of proposed vertical TFET integration (a) Complementary final hetero-junction TFETs structure, (b) the etched Si NWs with a sacrificial poly-SiGe source and oxide hardmask (c) the device after drain/gate isolation, gate formation, source/gate isolation, source replacement and removal of the B-doped Ge on the source/gate isolation oxide, (d) the device after opening of the gate contact pads and silicidation of the source routing layer simultaneously with the gate contact pad.

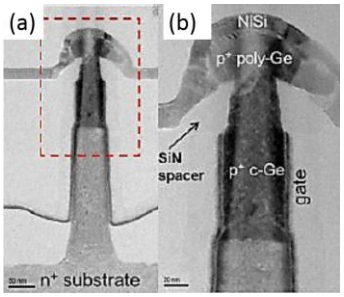

Fig. 12. (a) Cross section TEM image of the Ge hetero-junction n-TFET (b) Close-up image of the gatestack and Ge source.

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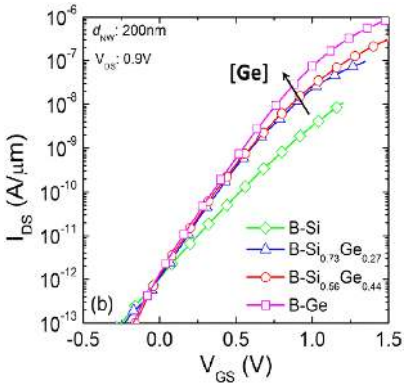

Fig. 13 Transfer characteristics for different vertical Si, $Si_{1-x}Ge_x$ ource TFETs, normalized at the same off-current (1pA/μm).