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Heterogeneous wafer-scale circuit architectures

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Heterogeneous Wafer-Scale Circuit Architectures

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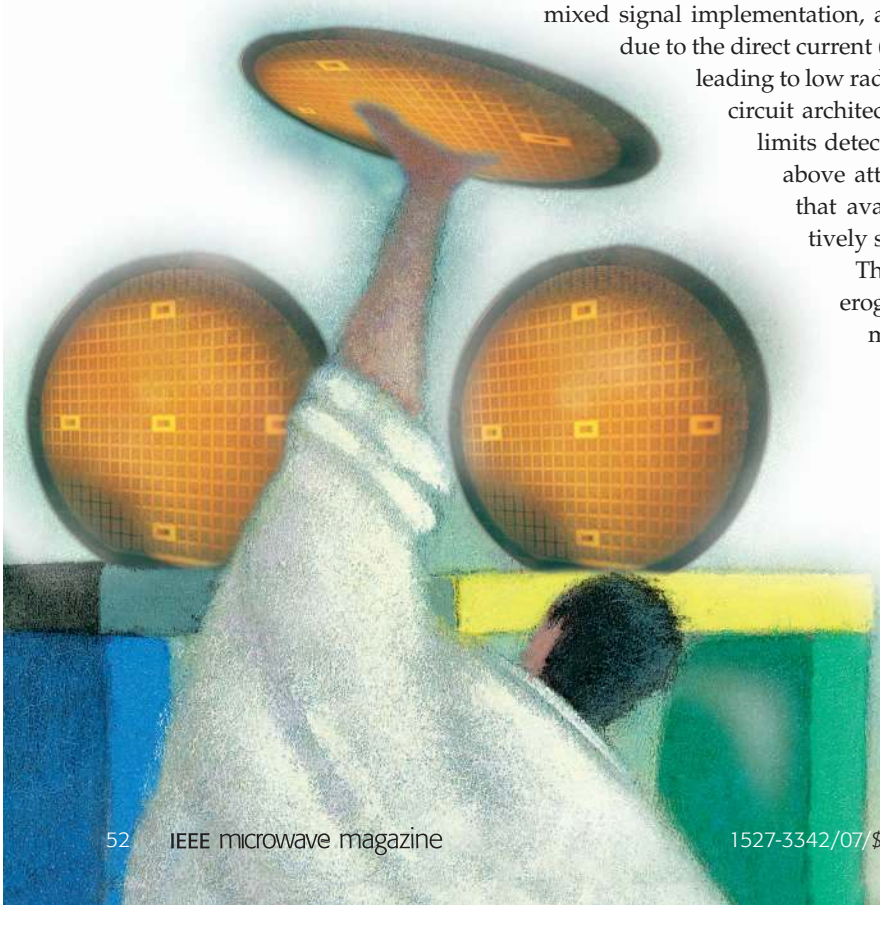
Future military and commercial communication systems require a new generation of circuits with cognitive, deployable, agile, versatile, survivable, and sustainable capabilities. For these future system concepts to materialize, there is a need to substantially reduce size and cost and increase functionality and density, thus leading to high operating frequencies and wide bandwidths. However, at high frequencies and with wide analog and digital bandwidths, conventional chip-substrate integration techniques (e.g., solder bumps and wire-bonds) and filtering technologies limit system capability and compromise efficiency.

The super-heterodyne radio architecture, most prevalent in present technologies, necessitates multiple passive off-chip components including intermediate frequency (IF) filters adapted to the channel filtering requirements for various standards. Direct conversion (including low IF) architectures have evolved as they lend themselves to single- or few-chip mixed signal implementation, although performance may be compromised primarily, due to the direct current (dc) offset shift and the loss (finite Q) of on-chip passives leading to low radio frequency (RF) efficiency and high phase noise. In this circuit architecture, digital noise coupled into the RF circuitry further limits detectability. For future military communication systems, the above attributes must be obtained with performance superior to that available commercially and delivered with volumes relatively small in comparison to that in the commercial world.

These performance requirements put a premium on heterogeneous wafer-scale integration whereby various optimized chip and component technologies can be combined to obtain improved overall performance.



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For example, combining the high power of a gallium arsenide (GaAs) power amplifier chip with the wide operating frequency range and compactness of a CMOS mixed-signal chip operating with 1.2 V supply can provide circuits with the density of flash memory and with the agility afforded by the evolving technologies of ferroelectrics and microelectromechanical system (MEMS) actuators.

The requirement of good performance and low cost at high operating frequencies cannot be achieved either by monolithic or hybrid integration. It is the synergistic development of technologies and RF architectures that will enable excellent performance while constraining costs and achieving multifunctionality and agility. Three-dimensional (3-D) integration and on wafer packaging of heterogeneous wafers are the future in high-frequency circuit design and circuit architecture. It leads to the development of RF front-end transceiver architectures [1]–[3] that consume less power, are compact, are characterized by low cost and high performance and are appropriate for advanced systems (Figure 1).

The advantages of 3-D heterogenerous integration [4]–[6] can be shown easily on two known system architectures. The first architecture is based on a low IF frequency and uses low-cost analog-to-digital (A/D) converters that can be fabricated on the same mixed-signal chip as the RF receiver. This architecture relies on the availability of a high-Q receive filter or a filter bank that can be integrated with a silicon (Si)- or III-V wafer. The second RF architecture, known as matched linearization, depends on the use of ultra linear on-chip RF amplifiers that track temperature, process variations, and aging and may minimize the need for transmit filters. Both architectures rely on the use of high quality factor (Q) distributed and lumped passives that directly impact the performance of the circuit.

Tranceiver Architecture

Herein, we present a futuristic 3-D transceiver architecture that utilizes a high-Q integrated filter and relies on vertical integration for the development of a compact 3-D wireless front end. This system (Figure 2) has an antenna structure intimately integrated with the highly selective multifrequency substrate and incorporates a novel mixed-signal digital IF circuitry including integration of the integrated circuits (ICs) with the mixed-signal circuitry through a uniquely designed Si interposer

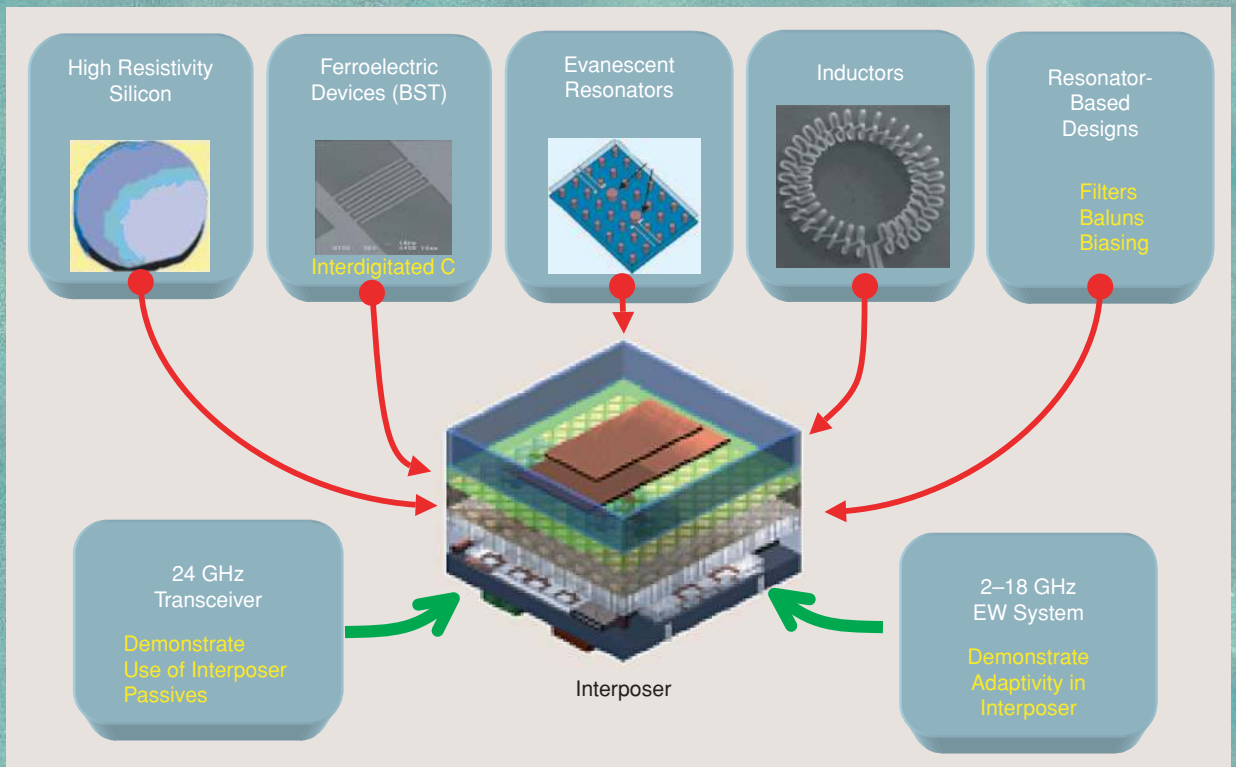

Figure 1. *Multiwafer 3-D integration.*

layer. The design of this transceiver can be accomplished effectively through a holistic mixed-circuit approach that accurately takes into account high-frequency effects including dispersion, radiation, and electromagnetic coupling. This transceiver has the potential to outperform many existing systems such as Joint Tactical Radio Systems (JTRS) and Satellite Communication Systems (SATCOM). Further, it demonstrates the potential of many novel circuit technologies to provide the functionality and density needed in systems such as cognitive radio, next-generation sensors, etc.

This 3-D architecture promises compatibility with multiple standards for multifunction, high-density of integration for very small volume and lower fabrication cost, and low power consumption. Some of the important aspects of this architecture are RF-compatible packaging; low-frequency IF; all-Si-based circuit realization for up to Ka-band frequency; relaxed specifications on linearity, dynamic range, image frequency rejection; phase noise and digital IF down-conversion; filtering; demodulation; and signal processing [1]–[3].

Good transceiver performance critically depends on the ability to integrate on-wafer heterogeneous materials, technologies, and high-Q embedded passives with the active chips. Cost reduction is a major reason for the use of the interposer concept. The ability to integrate a very high-Q filter with the low-noise amplifier (LNA), voltage-controlled oscillator (VCO), and antenna allows for a direct conversion as shown in the schematic in Figure 3.

Direct conversion receivers are very sensitive to Local Oscillator (LO) leakage, dc offset, and baseband noise sources, which cause severe performance degradation compared to super-heterodyne architectures. The ability to integrate a high-Q filter allows for the use of a low IF selected close to the baseband, above the 1/f noise corner frequency, but still low enough for A/D conversion. With good RF channel selectivity, system specifications such as the linearity of the LNA, the phase noise of the VCO, the image frequency rejection requirement and the dynamic range of the A/D converter can be substantially relaxed (Figure 3). The value of the IF that can be utilized in this architecture critically depends on the characteristics of the receiver, including the quality factor of the RF filters. Traditional analog signal processing such as in-phase and quadrature-phase (I and Q) separation, channel-select filtering, down-conversion to baseband frequency, and moving target indication (MTI) can be moved into the digital domain, thereby avoiding the sensitivity of this process to various analog circuit impairments and providing adaptation to the multiplicity of standards and multifunctional capability.

The receiver architecture of Figure 3 requires a number of novel technologies that have been developed and are described below. These technologies, when applied to transceiver designs, can lead to state-of-the-art system architectures with unparalleled performance. A detailed description of the development effort for each of these novel technologies is described in the following sections.

Heterogeneous Integration and the Interposer Concept

To achieve high performance in the transceiver architecture of Figure 3, the passives are required to exhibit high Q, small size, and low cost. It is known that on-chip passives suffer from low Q while off-chip components are occupying a large volume and are not easy to integrate with the active chips. A new concept introduced recently, the use of a high-frequency interposer layer (Figure 3), allows for the combination of high performance, low cost, and the ability to integrate in three dimensions. The use of an interposer layer, as shown in Figure 2, that can tightly integrate active chips with passives in a multiwafer environment also provides multifunctionality due to the ability to integrate with high and intermediate permittivity dielectrics (relative permittivity of 600 and 25, respectively). The use of these dielectrics on the interposer leads to low parasitics, high density, and low cost in addition to providing more functionality. For example,

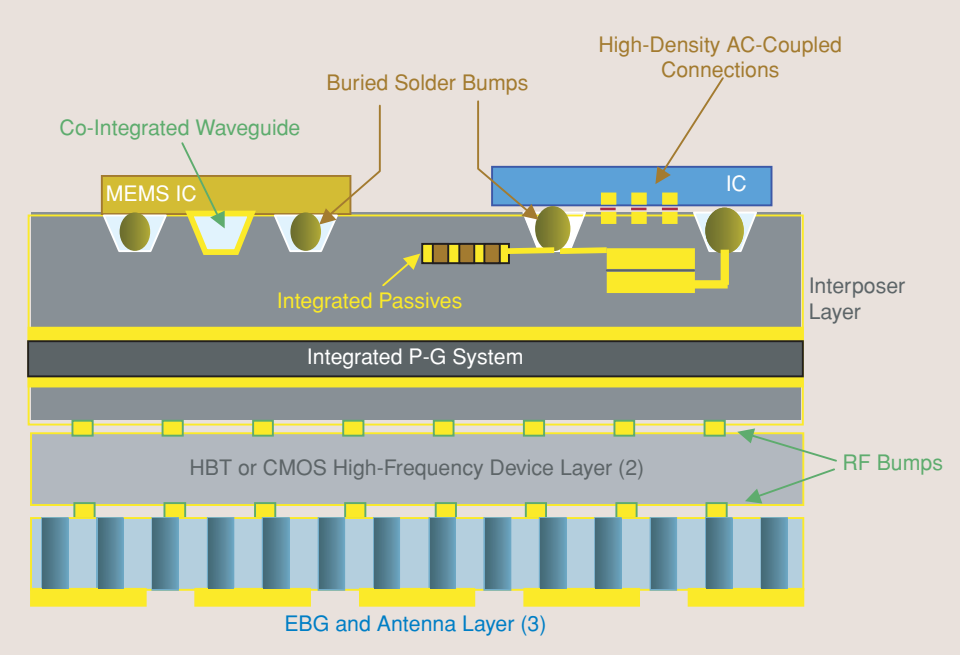

Figure 2. *Highly integrated advanced transceiver module.*

ferroelectric components using barium strontium titanate (BST) and designs that exploit their tunable characteristics have been developed. The BST has been integrated into the interposer using a heterogeneous integration method [41].

The integration of heterogeneous layers may compromise reliability as operating power increases due to thermal mismatch issues. In this case distributed cooling will be required to provide better control of the thermal environment. The use of passive or active cooling via use of 3-D cooling channels is compatible with the 3-D technology presented herein. Integrated cooling is a growing research area in high-frequency circuit design.

Through the Defense Advanced Research Projects Agency's (DARPA) TEAM project led by Purdue University and North Carolina State University, we have demonstrated the use of interposer integration and packaging techniques using high-frequency CMOS and silicon-germanium (SiGe) circuits. The potential of using high-density, low-loss interconnects and integrated high-quality passives, in order to complement the advances in high-speed device technology, has been shown to provide maximum benefit for integrated microwave systems. Both design cycle times and system performance have been advanced through the use of high-resistivity Si in a unique Si-based self-aligned wafer-level integration technology (SAWLIT) [7] (Figure 4) that was developed as part of this project. In this technology, the CMOS or SiGe ICs are integrated within the Si interposer using low-loss interconnects with a definition better than a few micrometers. This integration approach allows the removal of passives from the expensive IC chip and their integration on the interposer for lower cost and better performance. Additionally, the use of a multilayer package integrated with the interposer allows for the high-density integration of high-quality components such as cavity-based filters with unloaded Qs greater than 1,500.

High-valued components such as decoupling capacitors or choke inductors, high-Q components with quality factors greater than 100, or tunable components that require precise fabrication conditions not compatible

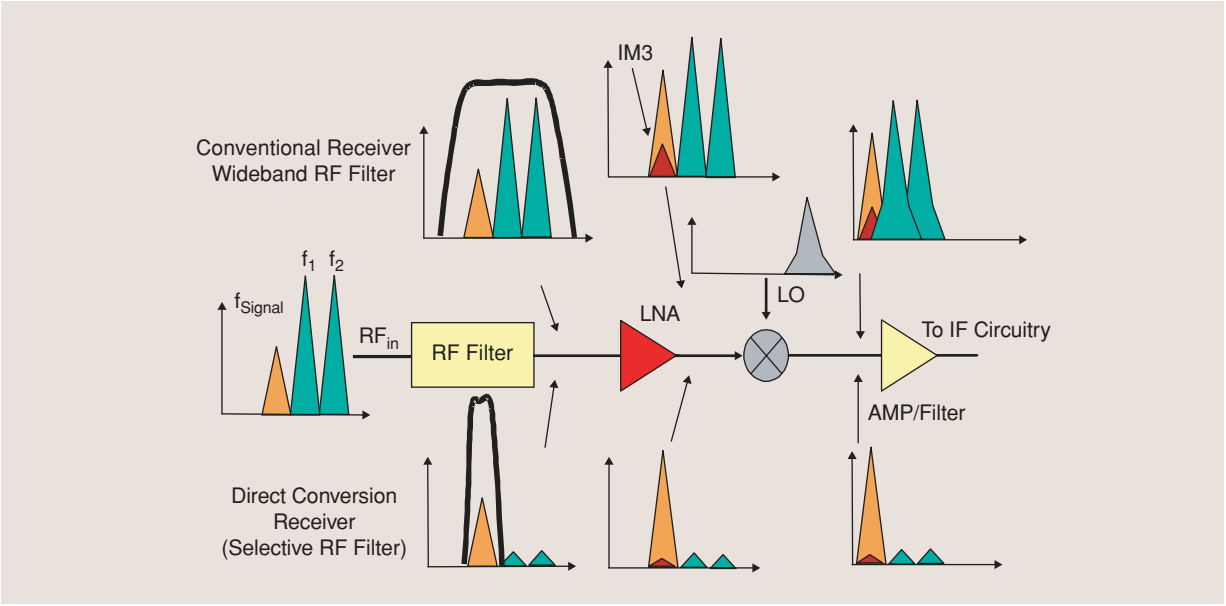

Figure 3. *Comparison of conventional and direct conversion receivers.*

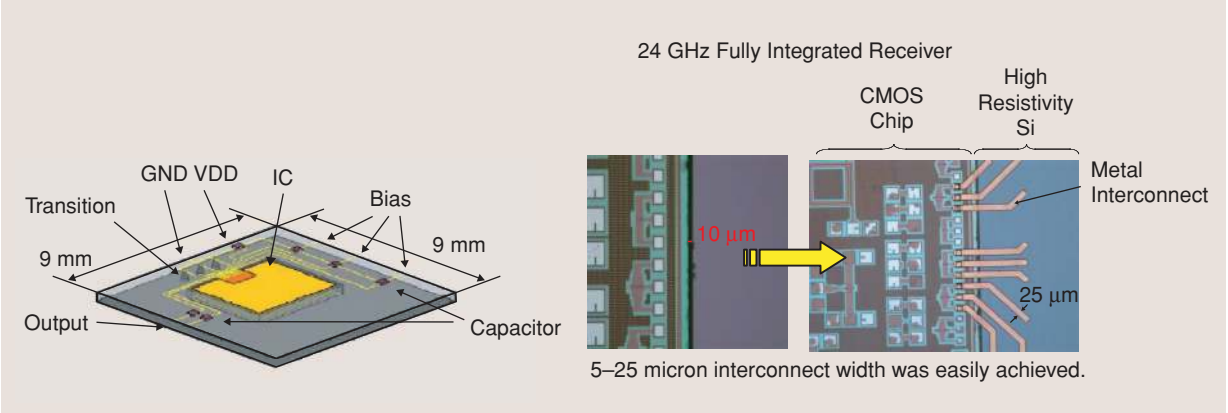

Figure 4. *Silicon-based, self-aligned wafer-level integration technology (SAWLIT).*

with CMOS fabrication lines cannot be integrated into a single piece of Si despite the advances of high-frequency transistors. Through the use of an Si interposer as a heterogeneous integration platform, each of these components can be added to a mixed-signal system-on-a-chip (SOC) design providing improved performance in fully integrated systems. Additionally, the use of high-quality passives in an interposer, which are in close proximity to the circuit through high-density interconnects, allows for circuit rework without altering the expensive mask set needed for the CMOS/SiGe components, greatly reducing circuit design cycle and cost.

By developing novel 3-D integration schemes, we have demonstrated, for the first time, a fully integrated Si receiver at 10 GHz using an Si-based interposer. Using SAWLIT [42], the 10-GHz receiver designed in 180-nm CMOS technology has been integrated with an embedded Si-based matching network, BST bypass capacitors, and an integrated high-Q filter. The overall receiver system performance has been characterized, showing substantial improvement over other fully integrated systems operating at the same frequency and with similar bandwidth. Due to its inherent self-aligned characteristics, this technology allows for batch integration of multiple chips and is key to developing low-cost and high-performance fully integrated RF circuits and systems.

The high-Q filter for the receiver in Figure 2 is a 3-D structure that has been designed to provide high Q along with small size and the ability to become fully integrated with the interposer. In this arrangement, using the interposer as an integration platform, cavities within an Si wafer or a multilayer polymer materials have been fabricated to provide a multipole filter performance. For the polymer material, a 3-D laser fabrication method has been utilized to create evanescent filters with unprecedented Qs greater than 1,000.

The multiwafer architecture discussed above (Figure 1) comprises three main structural and functional layers: the interposer layer (1), the HBT/CMOS device layer (2), and the electromagnetic bandgap (EBG)/filtering and antenna layer (3). These layers are shown in the schematic of Figure 2. In this architecture the various ICs are bonded using SAWLIT to the multilayered interposer layer, which incorporates high-performance integrated passives and RF routing and is then integrated with a high-Q filter using Si or polymer. Alternatively, it can be integrated with an EBG layer and antenna layer for high-Q filtering and high-efficiency radiation.

An IBM 0.18 μm CMOS technology has been used for the implementation of the low-power RF. In the following we will present the implementation of the interposer concept on a transceiver architecture that easily lends itself to a 3-D heterogeneous integration along with the passives that make this integration possible. The 3-D circuit architecture is demonstrated on a 10-GHz CMOS receiver.

SAWLIT

SAWLIT allows for integration of chips fabricated using different technologies on one substrate. In this heterogeneous integration scheme, instead of using wire bonds or flip-chip bumps to make the chip-to-package connection, lithographically defined interconnects with very narrow (~25 μm) footprints, as shown in Figure 5, are utilized. Input/output (I/O) pads on the chip with current dimensions of 25 μm × 25 μm occupy slightly smaller area than the pads for flip chip or wire bond (state of the art is 35 μm × 35 μm). By further optimization of the SAWLIT integration technology, as compared to current standard technologies, not only higher interconnect density can be achieved but also the size of the active chip is reduced as the area allocated to I/O pads shrinks.

Bulky passive components such as inductors and capacitors used in RF and mixed-signal circuits can be removed from the active chips and placed on the carrier substrate. Since the chip-to-package interconnect width is only 25 μm, there is no additional penalty in terms of excess dc power dissipation or extra loss associated with the off-chip passive components. In fact,

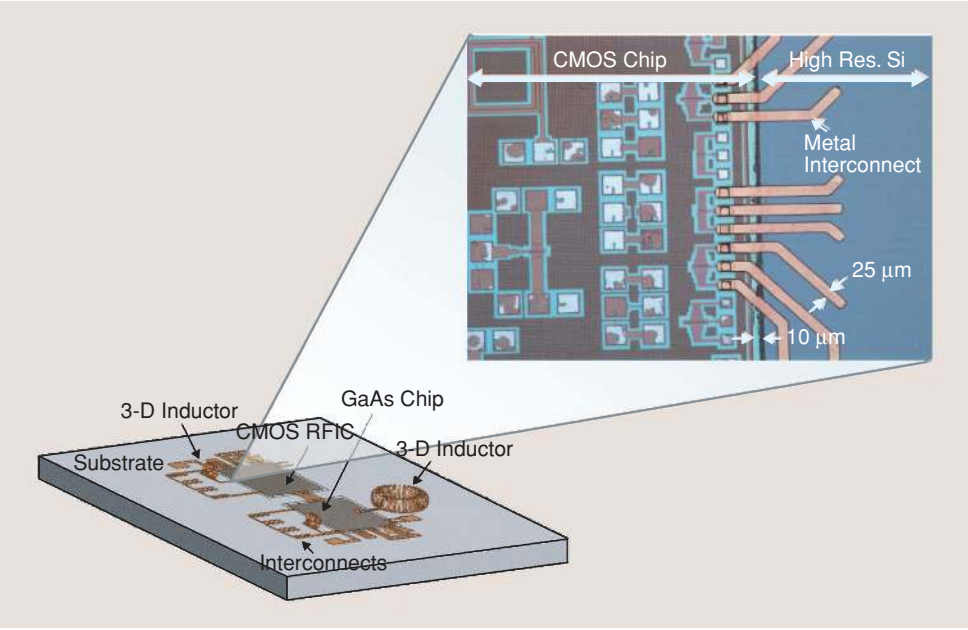

Figure 5. *SAWLIT concept for a wireless transceiver system. A CMOS chip integrated inside a high resistivity silicon. Interconnects as narrow as 25 μm are used.*

by using a low-loss carrier substrate such as high resistivity Si, or quartz, the quality factor of the inductors or transmission lines can be improved, resulting in better performance of RF modules. At the same time, since the bulky inductors and capacitors are relocated from the active chip to the carrier substrate, the size of active RF or mixed-signal chips are significantly reduced.

The following describes step-by-step the SAWLIT integration process. While the carrier substrate in SAWLIT can be any machinable and planar substrate, a high-resistivity Si wafer is chosen for its mechanical and thermal match to Si chips as well as its low-loss RF characteristics for high-frequency applications. First, using a deep reactive ion etcher (DRIE), holes are etched all the way inside the high-resistivity Si wafer. The size of the holes etched inside the carrier wafer is about 10 μm larger on each side of the diced disparate chips. A minimum trace width of 25 μm and a separation of 25 μm between the interconnect lines assures that a small misalignment will not cause a short or open circuit in this self-aligned process. The etched high-resistivity Si wafer is then attached to a handling substrate, typically an Si wafer coated with photoresist. Next, active chips are placed upside down inside the DRIE holes as shown in Figure 6(a). Polydimethylsiloxane (PDMS) is dispensed and polymerized at room temperature to fill the ~10 μm gaps between the chips and carrier substrate as illustrated in Figure 6(b).

After PDMS (or an appropriate thermal interface material) polymerization, the carrier substrate and the chips are detached from the sticky surface. A 6-μm amount of SU-8 (a photo-curable polymer) is then spun for planarization, resulting in a seamless transition between the high-resistivity Si substrate and the chips as shown in Figure 6(c). Finally, standard microfabrication steps including photolithography, etching, and lift-off are used to add chip-to-package interconnect lines and embedded passive components such as transmission lines, inductors, capacitors, and resistors [Figure 6(d)]. The chip placement in the SAWLIT process is done in a self-aligned manner. The etch profile of the carrier wafer and tight gap that exists between the chip and carrier wafer forces the chip to stay at the desired location with the possibility of only a few micrometers of misalignment.

Integrated Inductors

In designs of on-chip inductors the frequency-selective nature of the spiral inductors must be taken into account. In mixed-signal circuits, in general, a small amount of feedback is allowed to avoid compromising efficiency, bandwidth, and operating frequency.

Differential or pseudodifferential designs can eliminate the need for feedback and are ideal for circuits that incorporate large numbers of on-chip components such as spiral inductors. Printed lumped inductors are extensively used for off-chip and on-chip interstage matching and in bias circuits so that transistor drains can be biased at the supply rail. This increases the efficiency of RF circuits significantly or enables bias currents to be reduced in size for same functionality. Spiral inductors are an important area of focus in circuit design because

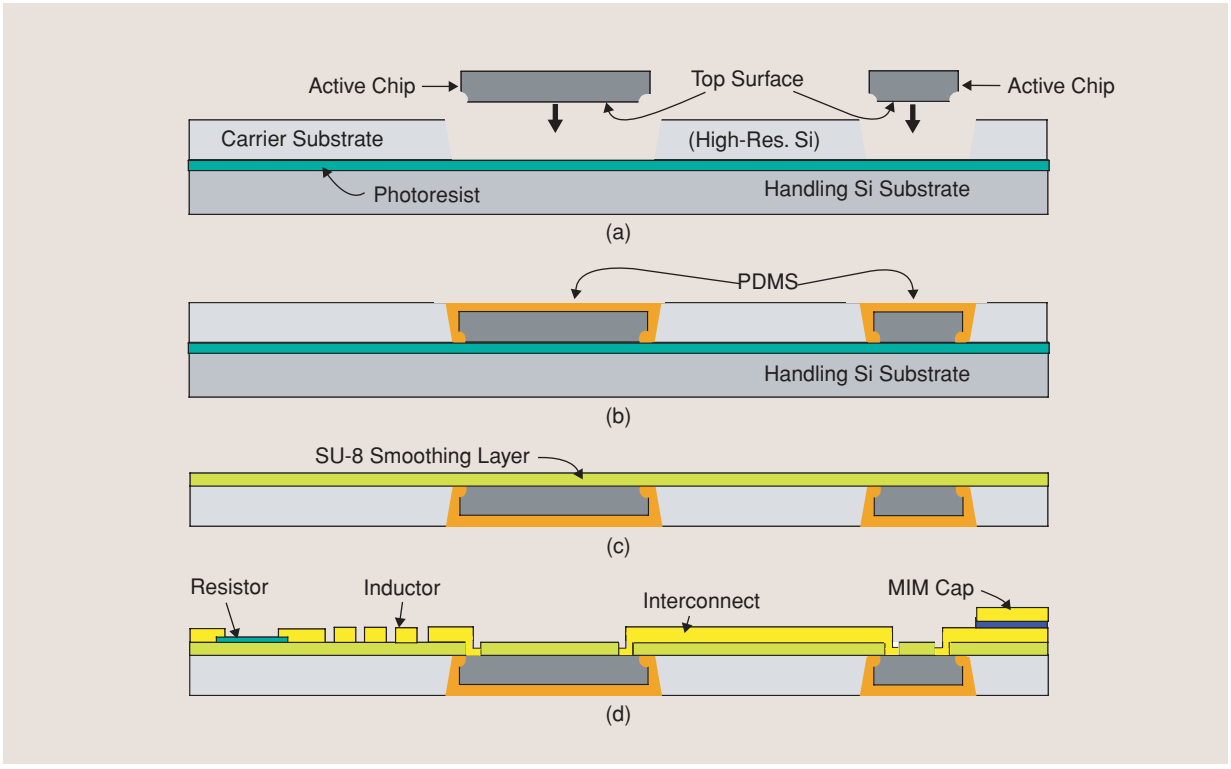

Figure 6. *Fabrication process for SAWLIT.*

of their dominant influence on chip size (and hence cost), chip current drain, effect on phase noise performance, noise mechanism through generation of surface waves and magnetic coupling to other parts of the circuit, and noise susceptibility through coupling to surface waves arising from the rest of the circuitry including digital circuitry.

For inductors operating at RF frequencies (up to Ka-band), a number of micromachined technologies have been proposed that can realize a high Q. Two of these technologies are presented in the following subsections.

Micromachined Planar Inductors

The basis of this novel technology is the use of bulk micromachining to reduce ohmic loss and as a result increased Q. Recent work has demonstrated that by removing the Si wafer around a spiral inductor through selective etching as shown in Figure 7, inductors with a high resonant frequency (38 GHz for a 1.5-nH inductor), high Q (~30), and high linearity are possible [8], [9]. These high-Q spiral inductors can also be used to design dividers, hybrids, and couplers up to Ka-band with substantial reduction in size (up to 10X) and improved electrical performance in terms of insertion loss and bandwidth, as compared to standard printed circuit technology. In this approach the Q is compromised by the parasitic capacitance of the Si substrate supporting the metallic spirals. To further improve the Q, the inductor spirals need to be separated from the substrate, as described next.

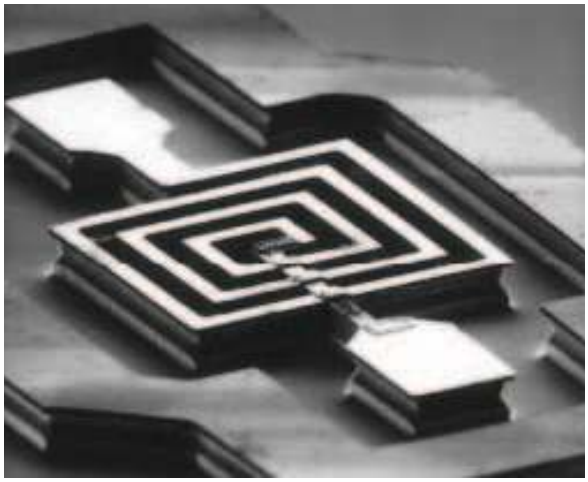

Figure 7. *Micromachined inductor.*

Micromachined 3-D Inductors

The Q and resonant frequency of integrated spiral inductors on a CMOS substrate are usually very low, because of substrate and ohmic losses due to the finite thickness of inductor metals. Several papers have reported unconventional on-chip inductors integrated with RF circuits, such as VCOs [10], [11] and power amplifiers [12]. There have been reports on suspended spiral inductors [13]–[15] and vertical spiral inductors [16], all of them limited to modest quality factors and relatively low self-resonance frequencies. Recently, spiral inductors with a quality factor above 100 and self-resonant frequency above 50 GHz have been demonstrated. These inductors were suspended over a low-loss ceramic substrate and had a copper metal thickness above 50 μm [17].

Using a combination of micromachining and a 3-D metal technology, inductors on a CMOS-grade Si substrate (10~20 Ω·cm) exhibit a very high Q and a high resonant frequency. A 1.2-nH inductor in this process can achieve a record high Q of ~140 at 12 GHz, with Q > 100 for frequencies between 8 to 20 GHz. The technology to fabricate these inductors is based on one-step deposition and electroplating of a stressed layered metal combination of chromium (Cr) and gold (Au) and is fully compatible with the CMOS technology.

The inductors presented herein are based on a recently developed stressed metal technology [18] in

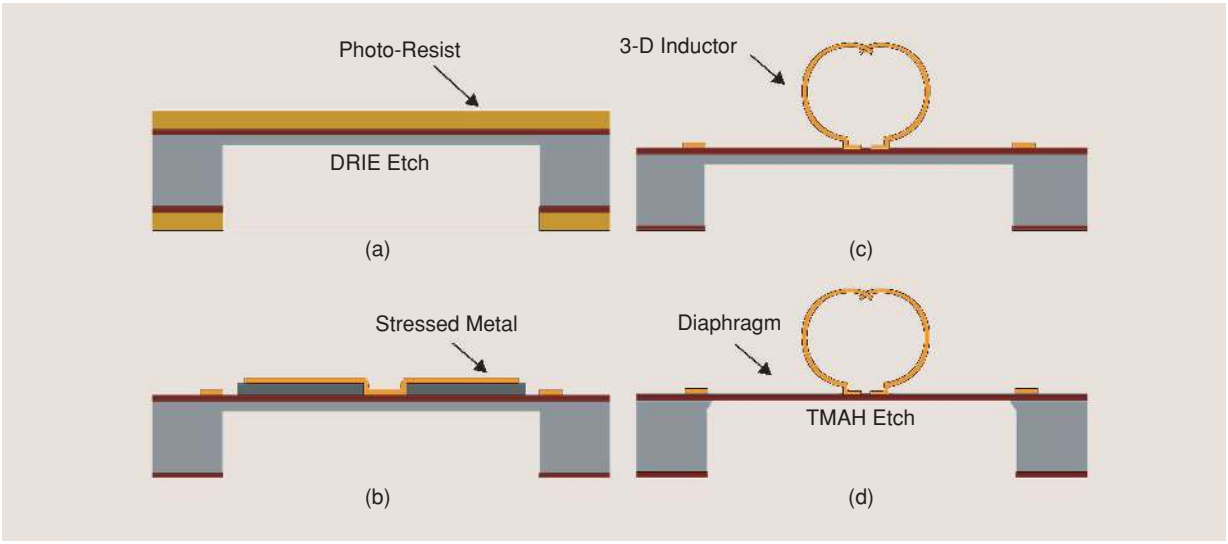

Figure 8. *Schematic cross-sectional views of the fabrication process flow for a 3-D inductor on silicon oxide (SiO_2) diaphragm.*

which a Cr/Au metal layered-combination is deposited to create a metal with a built-in stress. This built-in stress is used to create a spiral inductor printed on a thin dielectric membrane. The CMOS substrate underneath the inductor is removed by using a combination of dry and wet etching. This post-CMOS fabrication method results in 3-D inductors with excellent high-frequency performance. This technology has allowed us to use a CMOS-grade substrate to achieve record high-performance inductors.

Figure 8 shows the process sequence that is followed to fabricate the demonstrated micromachined inductors. First, the oxidized Si substrate is etched by a DRIE from the backside of the areas underneath the inductors to achieve a thinned Si substrate with a thickness of less than 100 μm. Then, the 3-D inductors are fabricated [Figure 8(b) and (c)] on these areas using the previously reported stressed metal technology [18]. An Au electroplating step is then performed to improve the metal contact resistance and also the rigidity of the structure. Finally, the remained Si substrate is etched from the back using TMAH [Figure 8(d)]. The 3-D inductors on a 0.8-μm silica (SiO_2) diaphragm after TMAH etch are shown in Figure 9. With the lossy Si substrate underneath the inductors replaced by a thin SiO_2 diaphragm, the inductors show an exceptionally high Q and high self-resonant frequency.

To investigate the effects of the substrate and resulting loss and parasitic capacitances on the performance of the inductors, we have fabricated and characterized inductors with one and two turns and metal line widths of 25 μm, 35 μm, and 45 μm before and after substrate etch. In addition, to assess the impact of the substrate loss we compared the performance of inductors fabricated on low- and high-resistivity substrates.

The S-parameters of the fabricated inductors were measured using the Agilent 8722 network analyzer. To perform accurate Q measurements when the values are very high, a very thorough calibration and accurate de-embedding of pads parasitics is needed [19]. Herein, several inductors of the same geometry were measured to ensure repeatability in the measurements. The deviation of the measurement values was within 3%.

Figure 10 shows the measured Q and inductance (L) extracted from the measured S-parameters for one-turn and two-turn inductors fabricated using the presented technology. As can be seen from this figure, for a one-turn inductor, a peak Q of 138 is achieved at 12 GHz. The self-resonant frequency of the inductor is over 40 GHz. For the two-turn inductor, a maximum Q of 66 and self-resonant frequency of 38 GHz are achieved. The following conclusions have been derived from the study: a) The inductance value increases with the number of turns in a perfectly quadratic manner, due to the high mutual inductance in the two-turn inductors; b) increasing the width of the conductor increases the Q significantly while it changes the self-resonant frequency only marginally. These inductors, while 3-D, can be easily packaged, using an Si cavity wafer, and this way they can be used in a multiwafer interposer arrangement.

Filters

High-Q embedded cavity resonators and filters have been realized by both Si micromachining [21] and layer-by-layer polymer stereolithography processing [31]. They have demonstrated very high Q (>2,000) and excellent out-of-band rejection. However, cavity filters,

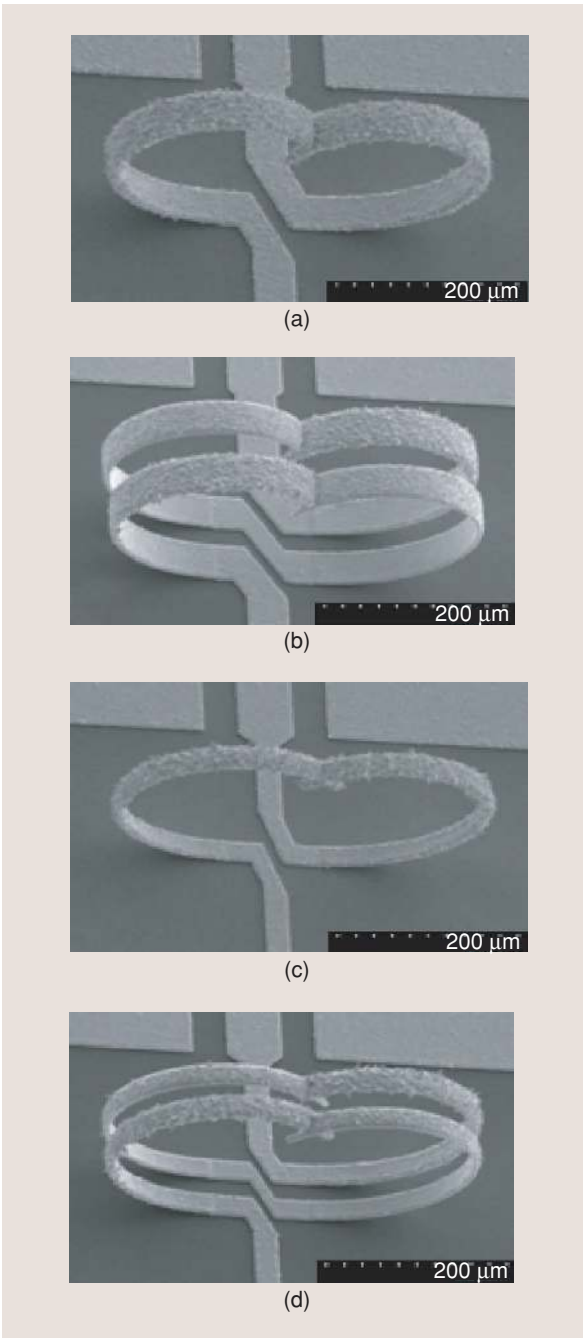

Figure 9. *Scanning electron micrographs of 3-D inductors fabricated on partially thinned Si substrate: (a) one turn and 45-μm width, (b) two turn and 45-μm width, (c) one turn and 25-μm width, and (d) two turn and 25-μm width.*

even if capable of wafer integration, have very large lateral dimensions due to the required size of the resonating cavities. Capacitively loaded distributed cavities can be reduced to a size much smaller than a wavelength but still have a much higher unloaded Q than lumped elements. The loaded resonators are utilized as a basis for reduced-size filters with a low insertion loss enabled by the relatively high quality factor. The size reduction of loaded resonators and filters relative to empty cavities can be one order of magnitude depending on the loading percentage. Herein, we will present some recent developments on 3-D integrated evanescent-mode filters. These filters are ideal for integration with the interposer due to the reduced size and compatibility of fabrication with the interposer layer.

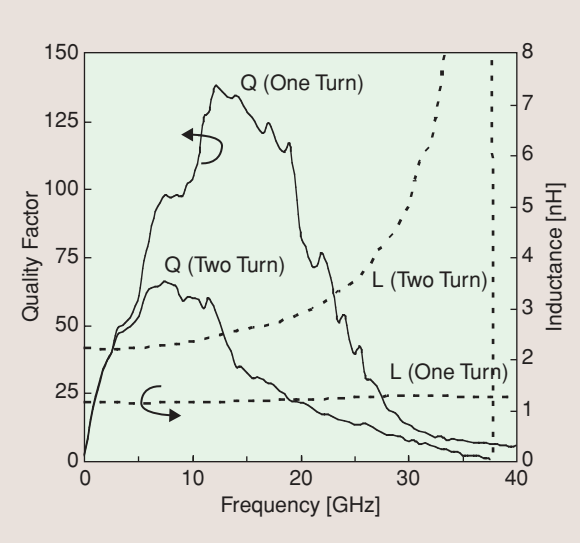

Figure 10. *Measured quality factor and inductance value of one-turn and two-turn inductors fabricated with 45-μm width on silicon oxide (SiO_2) diaphragm.*

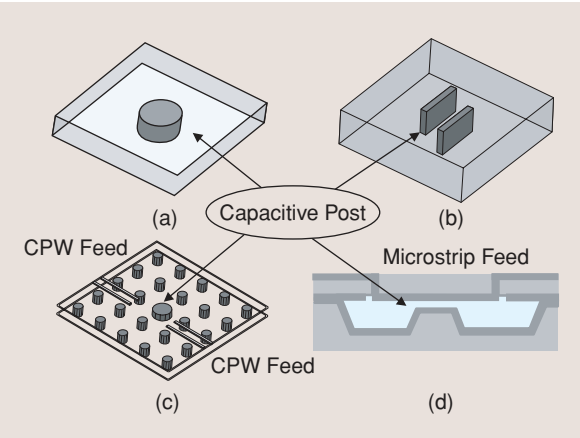

Figure 11. *Evanescent-mode resonators of different geometries: (a) cavity resonator loaded by a cylindrical post, (b) cavity resonator loaded by vertical parallel plates, (c) post-loaded resonator inside periodic array of vias, and (d) silicon micromachined evanescent-mode resonator loaded by a square post.*

Evanescent-mode filters have advantages over half-wavelength cavity-based filters such as smaller size and improved spurious-free region and low insertion loss [20]. In many situations, size reduction is required due to space and weight limitations; however, filter performance cannot be greatly sacrificed. Thus, compact, low-loss filters are commonly designed utilizing the evanescent-mode concept [21].

High-Q evanescent-mode filters have been widely implemented in waveguides in the form of combline and ridge waveguide filters. Reduced-size evanescent-mode resonators have also been implemented in band-stop filter design [22]. Nevertheless, all the above-mentioned topologies are difficult to be monolithically integrated with other RF components. To enable an integrated RF front-end design, new fabrication methods such as Si micromachining and layer-by-layer polymer stereolithography processing are investigated in this article to realize small, high-Q, and integrated resonators and filters.

By loading a resonant cavity with a capacitive post, we can reduce the resonant frequency of the cavity while still maintaining a relatively high unloaded Q [20]. The size reduction of the cavity can be one order of magnitude depending on the post height. However, the sensitivity analysis in [20] points out that fabrication tolerances are extremely important when the post height is close to the cavity height, representing a high loading factor. Previous work on evanescent-mode filters inside low temperature cofired ceramic (LTCC) substrates achieved limited size reduction due to the variations in the thickness of each ceramic layer [23], [24]. The uncertainties of the individual layer's tape thickness prevented LTCC from reducing the resonator size further. It remains an interesting challenge to design and fabricate small-volume, high-Q resonators and filters.

In order to achieve greater size reduction, precision manufacturing techniques such as Si micromachining and layer-by-layer polymer stereolithography processing are used to realize capacitively loaded cavities in different geometries (Figure 11). The small fabrication tolerances of these two methods enable the accurate prediction of the desired post height and, in turn, achieve desired resonant frequencies. The highly loaded cavity can be considered a quasi-lumped-element resonator since the electric field is concentrated on the top of the capacitive post but the magnetic field distribution remains relatively unchanged. Thus, the resonant frequency is significantly reduced due to the increased capacitance when the top of the capacitive post is in close proximity to the top of the cavity. However, the metal loss that is associated with the tangential magnetic field on metal surfaces does not change significantly. As a result, the unloaded Q of the resonator does not reduce as quickly as does the resonant frequency.

A wide spurious-free range is another advantage of evanescent-mode filters. Evanescent-mode ridge wave-

guide filters with wide spurious-free operating frequency range were reported in [25]–[27]. The first higher-order mode resonant frequency is not altered significantly by the presence of the post owing to the electric field null at the center of the cavity and therefore is not reduced along with the lowest order mode. This results in a much wider spurious-free region.

For Si micromachining, the fabrication processes necessary to create controlled post dimensions are detailed, and the effect of fabrication steps on the geometry and eventually performance is given. As an alternative to creating these filters with even more unique geometries, larger structures with a higher unloaded Q have been demonstrated in a maskless layer-by-layer polymer stereolithography process. The 3-D process is utilized to create different geometries to load the enclosed resonators.

In the following section we present both Si-micromachined and polymer-based high-Q evanescent-mode filters that can effectively be integrated with CMOS and SiGe ICs.

Evanescent-Mode Resonators and Filters Using Si Micromachining

Silicon micromachined resonators and filters have already been demonstrated and have shown competitive RF performance [28]–[30]. Even though the attainable Q values were less than those reported for waveguide-based systems, their smaller size and weight make them very appealing for many applications. Furthermore, the Si processed filters can be monolithically integrated with a conventional planar processing technology, thus making possible the design of complete communication systems on a single chip. In this study, the same Si micromachining techniques are utilized for the fabrication of evanescent-mode filters, where the capacitive post is created by anisotropically etching the Si wafer.

Fabrication of the evanescent-mode resonators and filters is a multiphase process involving both surface and bulk micromachining as shown in Figure 12. The samples used are a 500-μm and a 100-μm thick high-resistivity double-side polished Si wafers, with 8,700 Å of SiO_2 thermally grown on both sides to allow for dual-side processing.

On the lower wafer, (a) SiO_2 is patterned on the top and lower side of the wafer; (b) the SiO_2 is etched partially in the post region and fully in the remaining cavity using buffered hydrofluoric acid (BHF); (c) the oxide-patterned cavities are etched in tetramethyl amonium hydroxide (TMAH) up to a depth of 440 μm, while the post remains protected by a thin SiO_2 layer; (d) the SiO_2 from the post is striped and the wafers are placed in TMAH for an additional 10-μm etching, resulting in a 450-μm depth and a 10-μm gap for the post; (e) a 400/800 Å of Cr/Au seed layer is deposited via sputtering in order to ensure uniformity and subsequently 4 μm of Au are electroplated inside the cavity.

For the top feed wafer, a 100-μm-thick high-resistivity double-side polished Si wafer is utilized. At first, 500/9,500 Å of Cr/Au is deposited on the backside using lift-off process to form the coupling slots. SiO2 is patterned on the top side of the wafer using infrared alignment and etched fully in BHF. The oxide-patterned vias are etched in potassium hydroxide (KOH) and a seed layer of Cr/Au is deposited via sputtering and, subsequently, 4 μm of Au is electroplated to form the microstrip lines. Then 1,000 Å of plasma enhanced chemical vapor deposition (PECVD) SiO_2 is patterned over the location of the post and etched using reactive ion etching (RIE). This thin layer isolates the two Au surfaces (the top wall of the cavity and the post) and prohibits their bonding during the final fabrication step.

For accurately aligning the two wafers together prior to the thermo-compression bonding, specially designed shapes are etched on both wafers using deep reactive ion etching, ensuring vertical sidewalls. Similarly shaped alignment keys are then placed inside the grooves and the two wafers are locked in place. After that, the wafers are placed inside an EV-501 bonder. The outcome of this process is presented in Figure 13, which shows that the filters are fed through a microstrip (shown top left) to slot-line transition [Figure 13(b)]. A via is used to short the

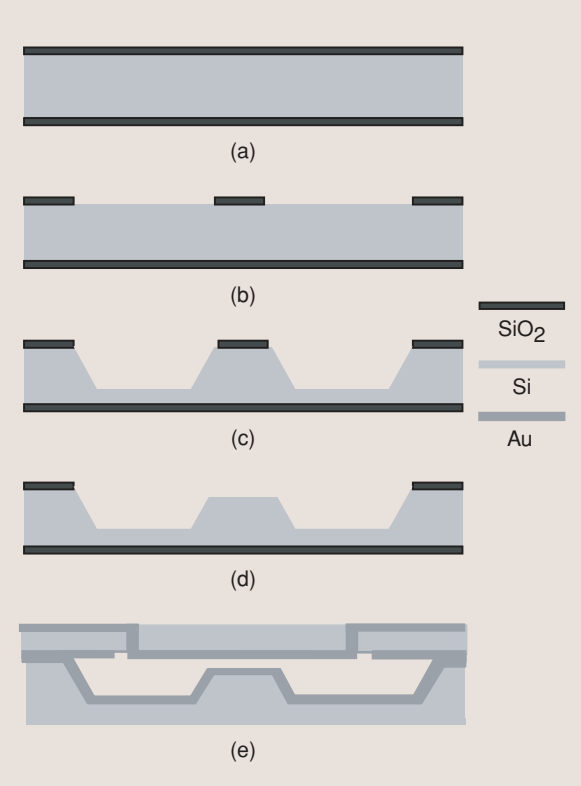

Figure 12. *Fabrication process for a silicon micromachined evanescent-mode resonator: (a) grow SiO_2 on silicon, (b) pattern SiO_2, (c) etching cavity, (d) etching post, and (e) metallization and bonding with feeding wafer.*

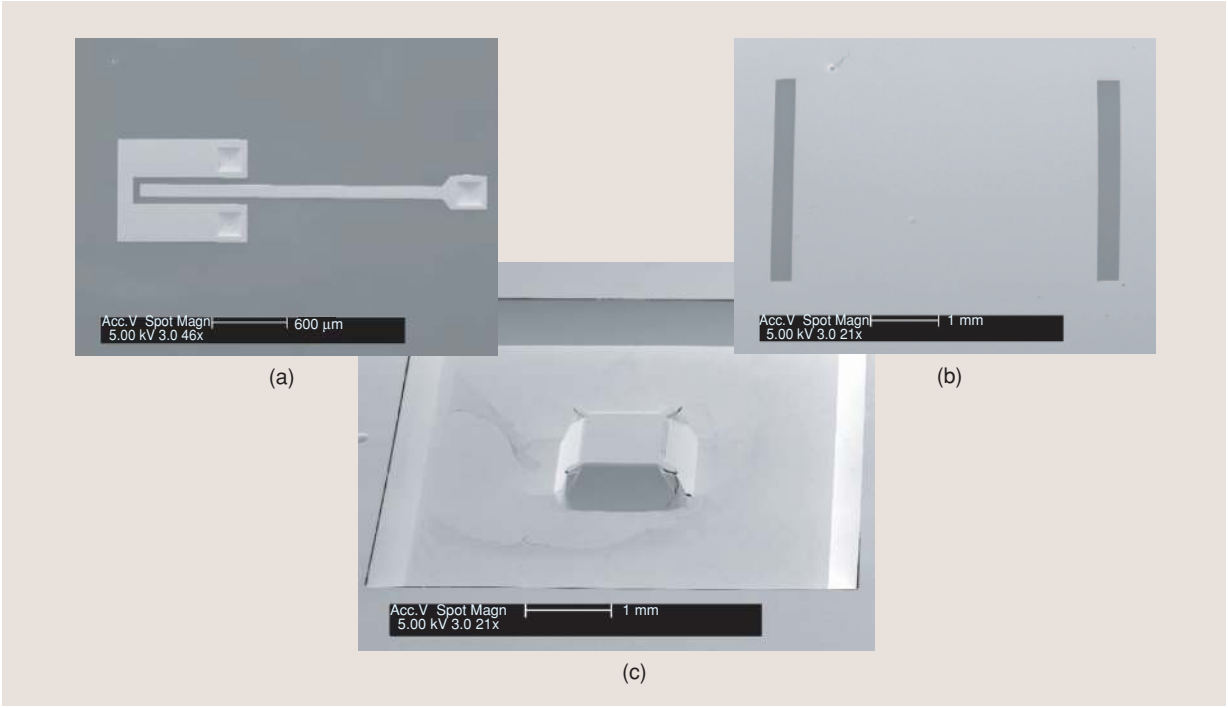

Figure 13. *Scanning electron micrograph of the fabricated silicon micromachined resonator: (a) coupling microstrip, (b) ground plane slots, and (c) capacitively loaded cavity.*

microstrip, instead of the usual open stub, due to size restrictions. The total size of the resonator is 5 mm × 5 mm × 450 μm.

The results for the single-pole resonator are summarized in Figure 14. The resonant frequency occurs 1.4 GHz higher than the theoretically predicted value. This, as was verified by an optical microscope and scanning electron images, is due to the fact that the gap between the top of the capacitive post and the bonded upper wafer is approximately 12 μm instead of the desired value of 10 μm. Due to the consistency of the fabrication error, a filter can still be created utilizing this resonator but with only a known frequency shift. The unloaded Q can be extracted from measurement to be 310. The measured response of the two-pole filter is presented in Figure 15, where a 2.7% bandwidth is observed with an insertion loss of 2.1 dB at 13.4 GHz. Ansfot HFSS3D simulations including dielectric and conductor losses predicted a bandwidth of 3% with an insertion loss of 1.4 dB at 12.7 GHz. There are again some minor discrepancies on the total gap of the capacitive posts. However, this discrepancy is consistent between resonators without corrupting filter performance and can be compensated in future designs. The size of the filter is 5 mm × 12 mm × 450 μm. On the same wafer, microstrip lines of various lengths have been fabricated. By measuring their response it is possible to evaluate the loss of each component of the feed line. The loss of the Finite Ground Coplanar (FGC)-to-microstrip transition is 0.2–0.3 dB in the bandwidth of operation while the loss of the feeding microstrip (i.e., the microstrip line up to the coupling slot) is approximately 0.26 dB at 13.4 GHz. Thus, by taking these losses into account, the insertion loss on the filter passband is 1.54 dB; only 0.14 dB from the simulated result, which did not include feed losses. The frequency reductions for the Si micromachined resonator and filter are 66.8% and 68.4%, respectively, compared to an unloaded cavity with similar dimensions.

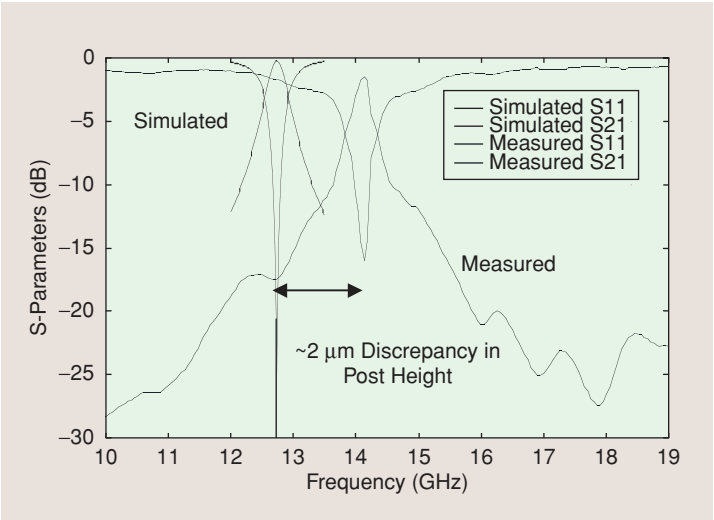

Figure 14. *S-parameters of a silicon micromachined resonator. From [21].*

High-Q Evanescent-Mode Resonators and Filters Using Layer-by-Layer Polymer Stereolithography Processing

While the Si approach is necessary for highly loaded, precision fabrication, larger yet higher-Q evanescent- mode resonators and filters can be realized by laser-based maskless stereolithography fabrication. Polymer stereolithography is a layer-by-layer processing approach. Stereolithography creates a 3-D part by scanning a laser beam on a liquid monomer and laser curing it into polymer (polymerization) in a line-by-line and layer-by-layer sequence.

The layer-by-layer polymer fabrication allows for the creation of 3-D structures and the ability to create a vertically integrated filter in one piece. In this example, the repeatability of the layer-by-layer dimensions that can be achieved is necessary for the accurate creation of the loaded high-Q narrowband filters. The fabrication tolerance analysis has been detailed in [31]. Nearly any arbitrary 3-D shape can be achieved using this rapid fabrication method and therefore multiple loading geometries were used to demonstrate this type of resonators.

As shown in Figure 16, to metallize the inside of the resonator, the evanescent-mode resonator loaded by a capacitive post is fabricated in two pieces and bonded together after metallization. The 3-D metallization is accomplished by applying a thin conductive ink inside the cavities and bulk copper electroplating later. The surface current shown in Figure 16 is in parallel with the cutting plane and, as the bonding does not disturb the current flow, the effect of the seam on the cavity performance (unloaded Q) is reduced. A cavity (10.35 mm × 10.35 mm × 2.77 mm) was fabricated, loaded with a capacitive post of 3.248 mm diameter. Two resonators were fabricated with post heights of 2.27 mm and 2.42 mm, which were measured to resonate at 11.250 GHz and 9.707 GHz using coax feed (Figure 17).

The measured resonant frequencies match closely with simulation due to the small fabrication tolerances of the stereolithography and the larger dimension of the resonators than Si micromachined resonators. The

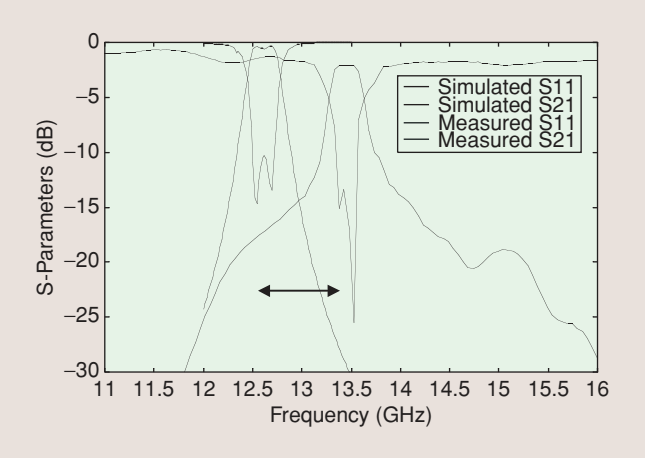

Figure 15. *S-parameters of a silicon micromachined two-pole filter. From [21].*

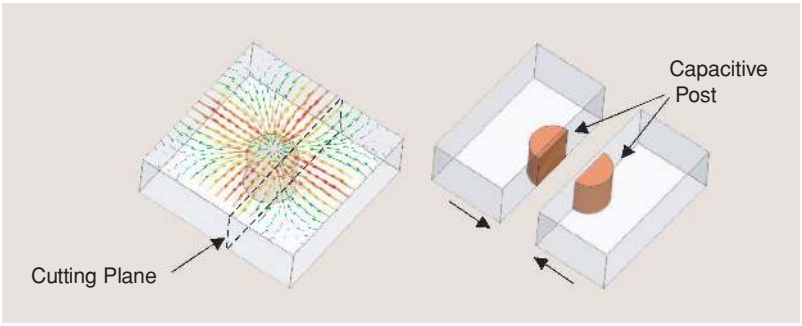

Figure 16. *Simulated surface current distribution on the capacitively loaded cavity resonator.*

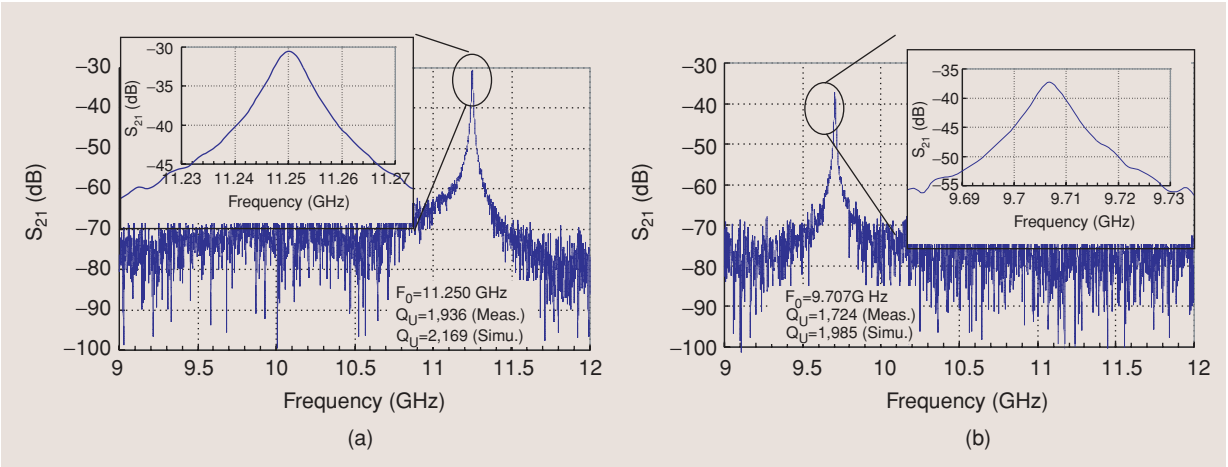

Figure 17. *Measured S-parameters for evanescent-mode cavity resonators loaded by cylindrical posts: (a) post height = 2.27 mm and (b) post height = 2.42 mm.*

measured unloaded Qs of the two resonators are 1,936 and 1,724, respectively. The achieved frequency reductions with respect to an empty square cavity are 45% and 53%, respectively. For a given frequency of operation, the cross-sectional area is reduced by 70% and 78% from the original cross-sectional area. Figure 18 shows the spurious-free band demonstrated by the evanescent mode filter for two post heights. In the case of the evanescent-mode filter, the spurious-free frequency band is about 2.5 times wider than the one exhibited by a cavity resonator. These filters are effectively used for the development of the 10-GHz CMOS receiver, which will be described in the sections below.

Three-Dimensional Integration and Packaging

Integration in the vertical direction is critical to increasing packaging density. Three-dimensional integration and on-wafer packaging (Figure 19) require novel interconnect structures that are critically needed for the successful implementation of the scheme [32], [33]. These are a) multilayer interconnects, b) vertical through-wafer transitions, c) RF bumps for wafer-to-wafer transitions, and d) wafer-to-wafer bonding and on-wafer packaging. The development of these components in micromachined form has provided substantially reduced size and excellent performance for microwave- and millimeter-wave frequencies and is described in detail in the following sections.

Multiplanar RF interconnects can be integrated vertically using a multitude of techniques, which are strongly dependent on the interconnect architecture. Among the various recently demonstrated interconnect integration methods, the following three have demonstrated compatibility with microwave monolithic integrated circuits (MMIC) technology: 1) microstrip or coplanar waveguide interconnects on multiple organic layers, 2) coplanar strip line or coplanar waveguide interconnects on dielectric layers, and 3) high-isolation, on-wafer packaged interconnects on Si wafers. The selective use of these interconnects in a high-density environment is dictated by the desired functionality and leads to effective, low-cost integration. The development of these complicated RF structures requires a multilayer process based on bulk Si micromachining. Specifically, Si micromachining has been utilized to remove the dielectric material from the aperture regions and reduce losses substantially [34]. High isolation, as previously discussed, and low loss makes this micromachined line a good candidate for multilayer thin-Si integrated multichip modules (Figure 19).

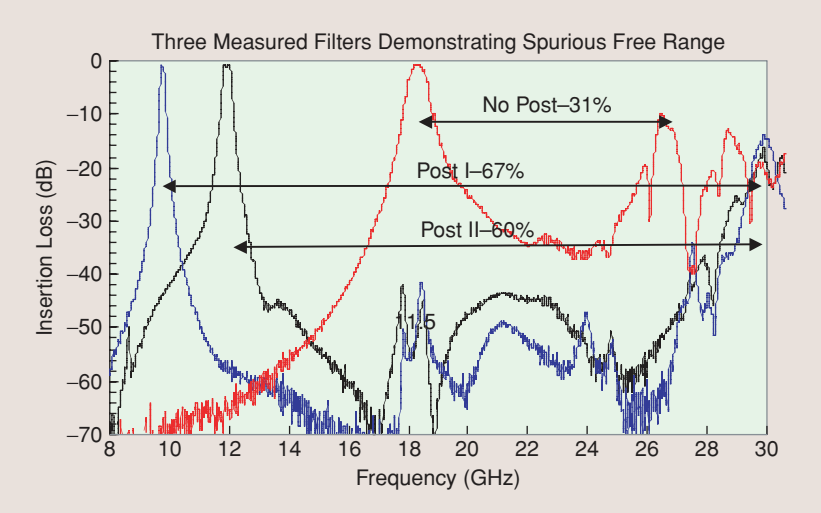

Figure 18. *Spurious-free bandwidth comparison (measured results). Post I height = 1.7 mm and post II height = 1.5 mm. From [13].*

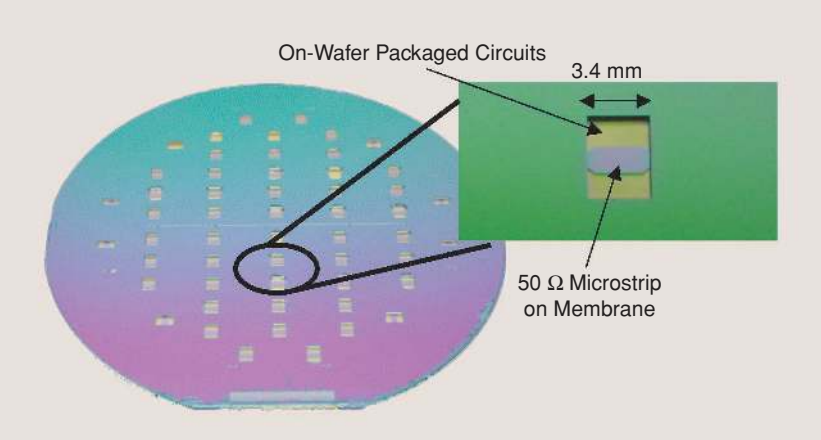

Figure 19. *On-wafer packaged circuits. Micromachined windows to provide access.*

Vertical Through-Wafer Transitions

In 3-D integration, a transition through the full thickness of the wafer becomes a building block for the circuit architecture. A variety of high-performance transitions appropriate for multilayer interconnect geometries have been demonstrated and have indicated the viability of this vertical interconnection concept at very high frequencies. A FGC line transition from the top surface of an Si wafer using the sidewalls of a micromachined window anisotropically etched to a depth of 100 μm [34] has been developed and exhibited excellent performance in the microwave- and millimeter-wave spectrum with an insertion loss of less than 0.1 dB (equivalent to the measurement error) at K-band (Figure 20).

A similar transition can be made from the top surface to the bottom surface of the same wafer by wrapping the FGC line around the sharp edge of the sidewall. A 3-via transition has also been developed for frequencies up to W-band [6] and has demonstrated excellent performance of 0.1–0.2 dB at 20 GHz to 0.4–0.5 dB at 94 GHz with a better than 15% bandwidth.

RF Bumps for Wafer-to-Wafer Transitions

In a multiwafer stack such as the one shown in Figures 2 and 20, an opportunity for better space utilization comes from the ability to place circuit elements on both the bottom surface of an upper wafer and the top surface of a lower wafer, and then to make electrical connection between them directly across the interface. This means that each interface between wafers can contain two separate but interconnected circuits, with each of these circuits connected to the other side of their respective wafers using the through-wafer transitions discussed above. A novel technique used to make the low-loss vertical connection between facing circuit wafers was developed based on RF electroplated bumps on the FGC transmission lines (Figure 20). Measurements of the transition in a back-to-back configuration have shown low loss of 0.1 dB up to W-band [35], [6].

Wafer-to-Wafer Bonding

The bonding of Si wafers is a well-established commercial technology for applications such as power devices, silicon on insulator (SOI), MEMS sensors, die attachments, sealing, and other MEMS components. Thermocompression bonding of Au-to-Au intermediate layers is the bonding method selected for the multilayer architecture of Figures 2, 19, and 20 because it can be achieved at a sufficiently low temperature so that metallization and interconnects of the circuits on the various layers are undisturbed. This type of wafer-to-wafer bonding can be hermetic, so that the final multilayer structure forms a complete hermetically sealed package. This wafer bonding technique is used for vacuum cavities in MEMS pressure sensors and shows exceptional promise for RF circuits as well. This is the same technique used to form the RF bump electrical transitions described above, and these RF bump bonds form part of the mechanical bonding of the wafer layers as well as an electrical connection [9].

Wafer-to-wafer bonding is an essential component to the amplifier microsystem packaging. Thermocompression bonding is chosen based on the previous success with Si, and the process is integrated between the frontside and backside standard MMIC processing. The first step is the prebonding surface preparation, which involves solvent cleaning and ultraviolet exposure followed by baking at 150 °C. The second step is to properly align the two wafers and bring the bonding patterns on both wafers in contact. Finally, bonding energy is provided by applying pressure to the wafers while being heated.

The bonding time, pressure, temperature, as well as the uniformity and the cleanliness of the surface, are all important factors determining the quality of the bond. Generally, increasing temperature enhances wafer bonding. However, to protect those devices that are

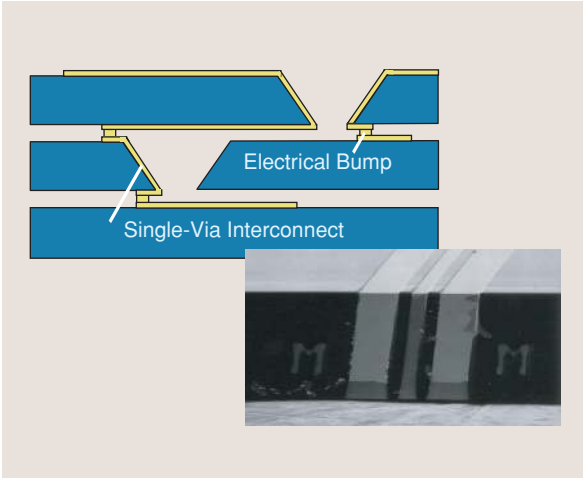

Figure 20. *Through-wafer transition.*

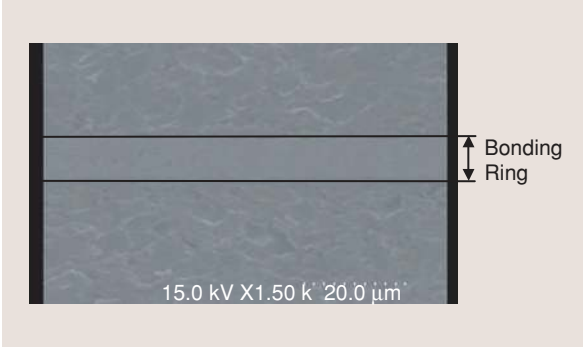

Figure 21. *Scanning electron micrograph of bonded gallium-arsenide wafers with 4 µm of metallization on each inner face. The mated 8 µm of metallization shows vertical uniformity, indicating a strong thermocompression bond.*

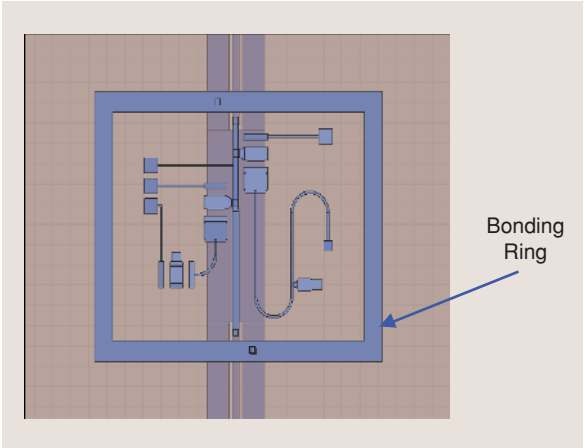

Figure 22. *Example of matching network layout with bonding ring.*

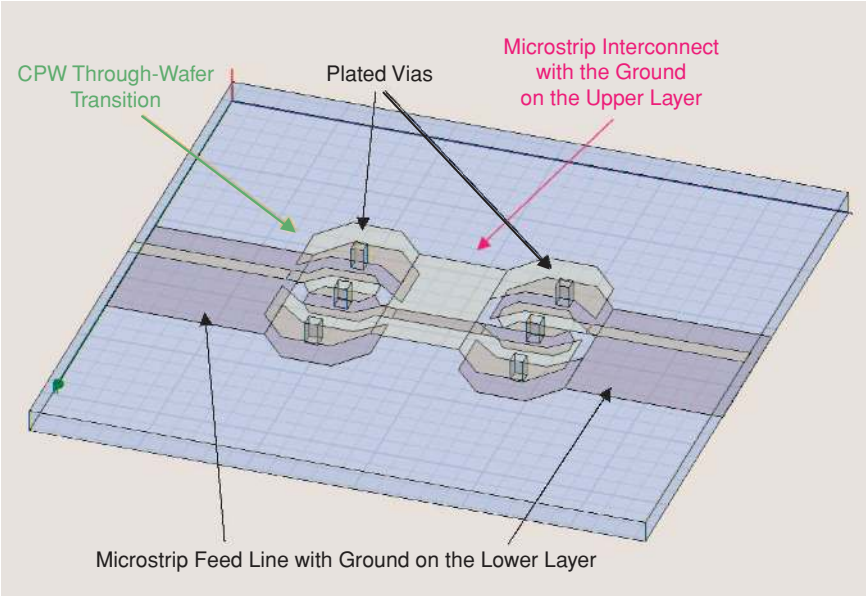

Figure 23. *Through-wafer transition using a CPW section.*

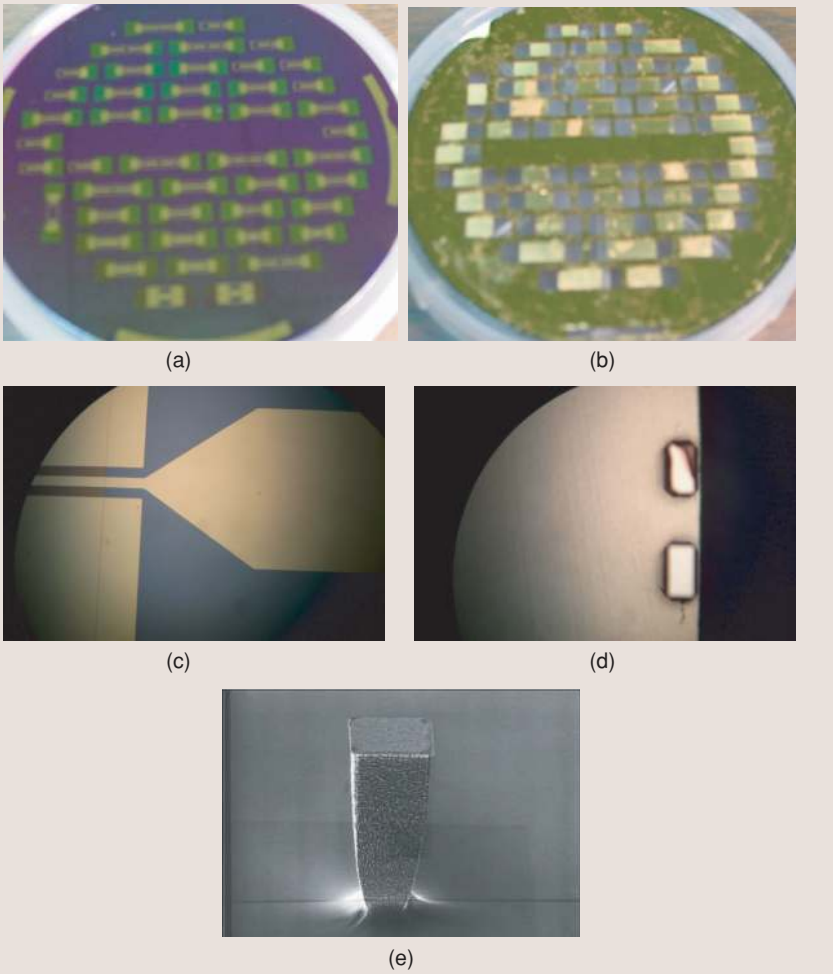

Figure 24. *Photographs of fabricated improved transition: (a) membrane wafer, (b) ground plane wafer, (c) CPW-to-microstrip transition, (d)–(e) details of ground plane via contacts.*

sensitive to high processing temperatures, it is necessary to develop a low-temperature bonding process for packaging in this work. Experiments of Au-Au bonding at 290 °C on GaAs provide excellent results (Figure 21). Other low-temperature bonding techniques in consideration include Au-In and Ag-In bonding [36], [37]. Using these techniques, successful bonding at or below 206 °C has been demonstrated, with debonding temperatures of 459 °C (±5°) (Au-In) and 765–780 °C (Ag-In) (Figure 21).

Packaging Approach

Previous work at the University of Michigan [33] successfully demonstrated the ability to create a hermetic on-wafer package for individual RF MEMS switches using Si micromachining. This technology has been extended and integrated into amplifier circuits on GaAs with reconfigurable input and output matching networks requiring multiple RF MEMS. Key to the success of the hermetic packaging is the removal of any unwanted resonances caused by the metal bonding ring, which surrounds the structure, and the dc bias lines used for the MEMS activation.

The metallic ring resonates at the frequencies where its total length equals a wavelength. Moreover, the dc bias lines, when directly connected to the RF circuitry, behave as open stubs adding parasitic resonances in the response. Optimization of the design [39], [40] is made by adjusting the RF circuit layout to reduce the total length of the ring and by separating the dc bias lines from the RF by high-impedance sections. Furthermore, vias can be strategically placed on the sealing ring in order to provide a direct connection to the ground. The via-holes must

be located in close proximity to the RF input and output (where the standing wave created by the bonding ring is stronger) in order to suppress any unwanted resonances. Figure 22 shows a typical packaging design for a RF MEMS based matching network.

RF Transition Development

The first step for a packaged microsystem is the creation of hermetic RF and dc transitions that will provide low-loss access to the encapsulated Field Effect Transistors (FETS) and RF MEMS devices. The schematic of a through-wafer GaAs transition combining microstrip and CPW, along with the fabricated version of a back-to-back configuration are presented in Figures 23 and 24.

The fabricated improved design of the layout of the transition to provide a better confinement of the fields has demonstrated very good performance up to 60 GHz (see Figure 25).

Interposer and Heterogeneous Integration

As discussed previously, many-chip integration is facilitated by a thermally matched Si interposer layer. The use of an Si interposer as proposed herein leads to good dimensional control and accurate frequency-selective designs. The heterogeneous interposer structure (Figure 26) uniquely integrates three presently separate technologies. Specifically, an Si substrate that incorporates a number of embedded printed passives and RF interconnects, a high-temperature processed thin-film BST deposited on the substrate, and a multilayer Cu/polymer technology (SAWLIT) that embeds connect lines and passive components [7]. Direct integration of passives into/onto the interposer is utilized to reduce size and improve performance. The SAWLIT integration (Figure 27), described previously, has been implemented to develop a 10-GHz CMOS receiver as described below. The interposer is also integrated with a high-Q evanescent-mode filter with vertically integrated loaded cavities that is then electromagnetically coupled to a resonating antenna as shown on Figure 26. The filter has been designed as described above with a Q > 1,000, a bandwidth of 2.5%, and a center frequency of about 10 GHz.

10-GHz CMOS Integrated Receiver

Using the concepts developed above, a 10-GHz CMOS receiver was designed and fabricated. The CMOS chip was fabricated on 7 RF and was designed to operate at 10 GHz. The amplifier was tuned using a matching network printed on the interposer as shown in Figure 27. Using high-Q passives on the low-loss high-resistivity Si interposer, the input matching of the amplifier was improved from 13 dB at 11 GHz to -30 dB at the design frequency (10.2 GHz) (Figure 28). This improved matching increased the convergence gain of the receiver from 21 dB to 23 dB as shown in Figure 29.

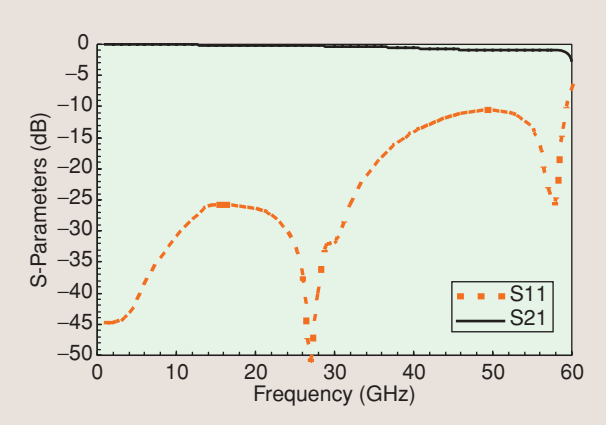

Figure 25. *Measured scattering parameters of the transition shown in Figure 24.*

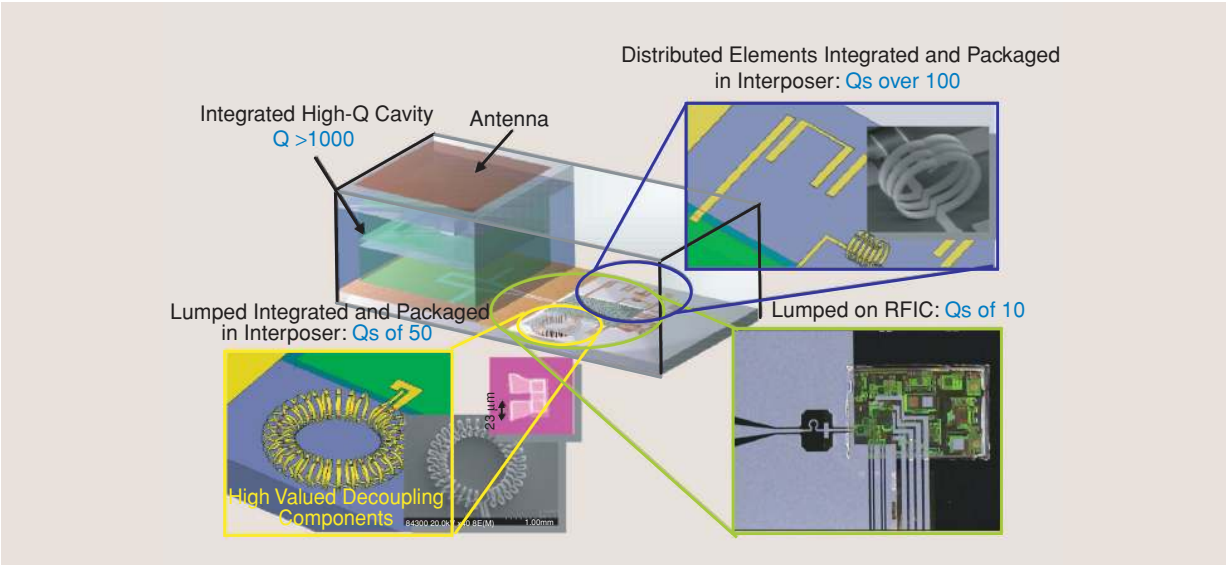

Figure 26. *Fully integrated chip/silicon interposer.*

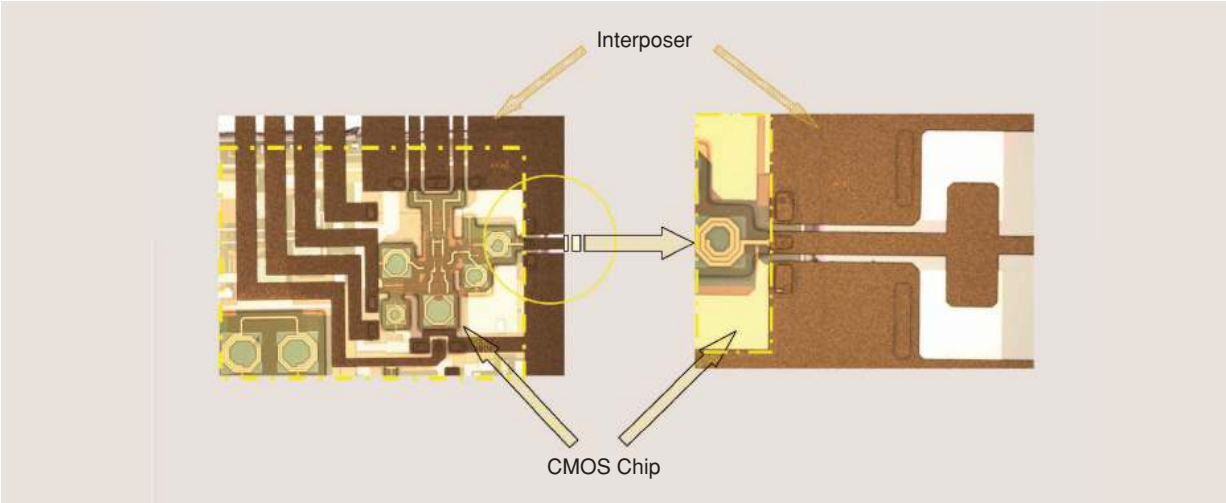

Figure 27. *CMOS chip integrated in the interposer using SAWLIT.*

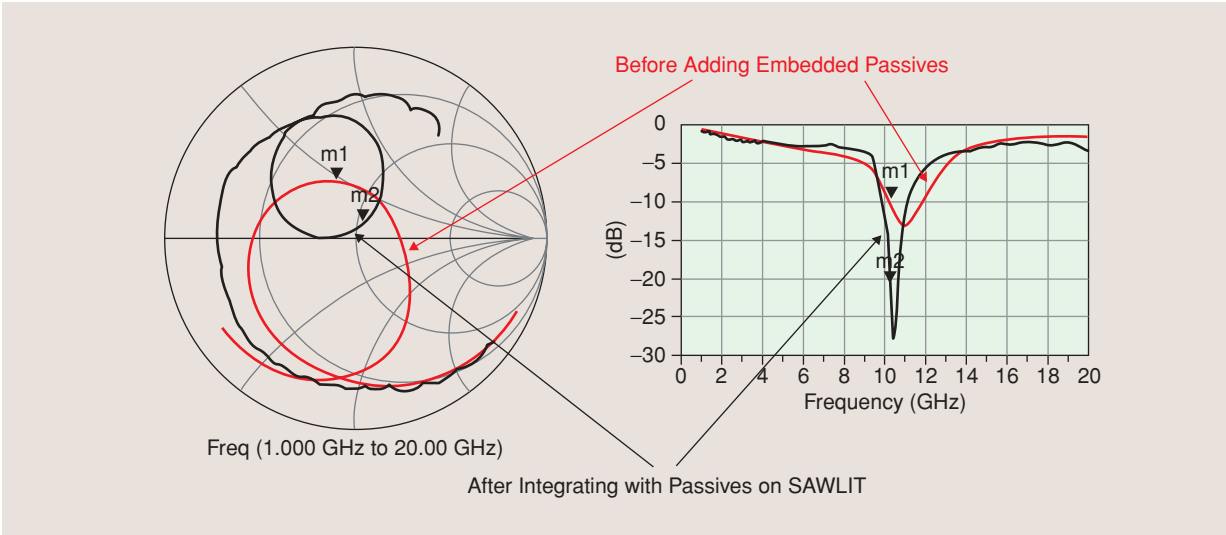

Figure 28. *Input matching network of the 10 GHz RFIC before and after adding embedded passives.*

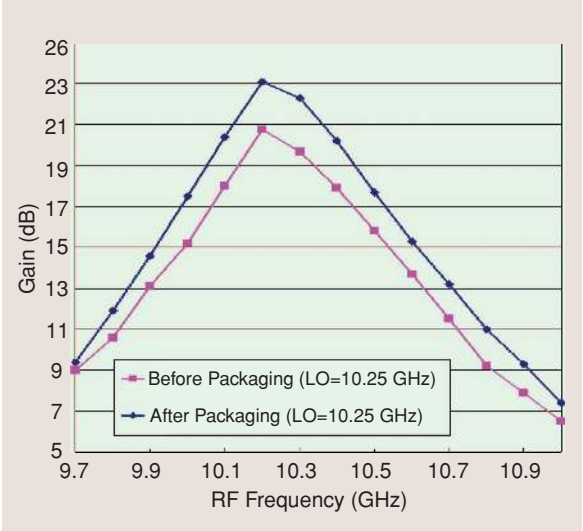

Figure 29. *Covergence gain of a 10 GHz RFIC before and after adding the embedded passives.*

In this initial design the conversion gain at the center frequency was about 7 dB (about 2 dB higher than anticipated due to additional losses introduced by the coupling to the filter). Currently, design changes are implemented that are expected to reduce the noise figure to almost 5.5 dB at 10 GHz.

Summary

This article has presented circuit architectures that allow for the 3-D integration and on-wafer packaging through the concept of an Si interposer. The presented 3-D integration schemes have allowed for the design and fabrication of a fully integrated receiver that performs at 10 GHz. High-Q passives and 3-D interconnects allow for the design of low-cost, high-density circuits that also exhibit very high performance.

Acknowledgments

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