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Heterogeneously Integrated III-V on Silicon for Future Nanoelectronics

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Shrinking feature sizes of CMOS transistor has enabled increase in transistor densities and this rising number of transistors increases the power consumption in ICs. Thus, the computing power is primarily constrained by power consumption and high-speed operation. Beyond sub 22 nm technology node, high mobility III-V materials and new device architectures have the potential to provide higher switching speeds and to operate at lower voltage <0.5V than Si FETs. Heterogeneous integration of such high mobility materials with quantum well field effect transistor architecture configuration have recently emerged a promising transistor option for ultra-high speed and low voltage operation. This paper reviews the recent development of the heterogeneous integration of high indium InGaAs quantum well FETs on Si and provide a technological solution for making nanoscale transistors, various integration scheme and solve the physics issues of the origin of defects and dislocations to InGaAs quantum well transistors. As a result, InGaAs quantum well FETs are poised to achieve higher drive current, low-off-state leakage, higher I_{ON}/I_{OFF} ratio, higher f_T, controlled short channel effect and thus have a potential for future high-speed and ultra-low-power electronics.

Introduction

With the scaling of Si CMOS technology, each transistor has become smaller, faster, cheaper (reducing the cost per function), leading to unprecedented increase in microprocessor performance, while the rising number of transistors increases the power consumption in ICs (1-3). The computing power and density of ICs is primarily constrained by power consumption and high-speed operation. Low-power consumption would imply lower heat dissipation, prolonged battery life and reduced cooling requirements, which all add up to significant reductions in cost and energy savings. Going forward, transistor scaling will require the introduction of new high mobility channel materials, including III-V and Ge, novel device architectures and their heterogeneous integration on highly dense Si CMOS could be a key enabler for lowering power consumption and enhance performance of microprocessor. Also, heterogeneous integration of such high mobility III-V materials with Si CMOS is one of the most promising ways to harvest the potential of III-Vs for optical chip-to-chip communication on Si platform and prohibit the need for developing large area and expensive III-V wafers. Moreover, multi-core processor architecture and interconnect bottlenecks for both inter-chip and intra-chip communication are projected to be major impediments to energy-efficient performance. An enticing alternative is the integration of low bandgap III-V materials based electronic and photonic devices with well-established Si CMOS technology. In fact, integration of high-efficiency III-V photovoltaics (PVs) on low-cost, large area readily available Si wafers, compared to Ge or GaAs wafers, would enable much higher yield per die and thus cost/watt of high efficiency PV cells.

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InGaAs and InSb-based quantum well (QW) transistors have shown channel electron mobilities of over 10k $cm^2V^{-1}s^{-1}$ at carrier charge densities of ~$2x10^{12}$ cm^{-2} at 300K (4-10). Quantum well field effect transistors (QWFETs) fabricated from these materials exhibit 2x higher speed but with 5-10x lower power dissipation than the state-of-the-art Si n-MOSFETs (4-9, 11-23) and demonstrated significant improvements in intrinsic gate delay. This significant improvement implies that low bandgap III-V semiconductors have enormous potential for electronic, photonic and energy conversion devices.

Several approaches namely bonding (24), III-V on semiconductor on lattice engineered substrate (25, 26), aspect ratio trapping (27), PDMS epitaxial transfer (28, 29), and flip-chip (30-32), etc are currently being considered for the integration of III-V materials and devices on Si. However, heterogeneous integration of III-V materials on Si (5-7, 9, 11, 12, 33, 34) is believed to be the most promising option for integrating *high-density* III-V devices on large area Si through careful investigation of materials science options. However, the large lattice mismatch and thermal expansion differences between III-V semiconductors and Si presents the biggest challenge to overcome heterogeneous integration of III-V materials and devices on Si. Lattice strain relaxation leads to defects and dislocations that propagate through the epitaxial layers at densities approaching $10^9$$cm^{-2}$. Considerable progress has been made in reducing the dislocation density to as low as $1.2x10^6$ cm^{-2} using graded buffer layers and strained-layer superlattices (35-41), thermal cycle annealing (42-49), and growth on nano-patterned surfaces (50). Fig. 1 shows the bandgap versus lattice constant of III-V compound semiconductors and their lattice mismatch with respect to Si. Clearly, the low bandgap, high-mobility channel materials have larger lattice mismatch with respect to Si and needs buffer architecture to mitigate the defect generation associated with the strain relaxation.

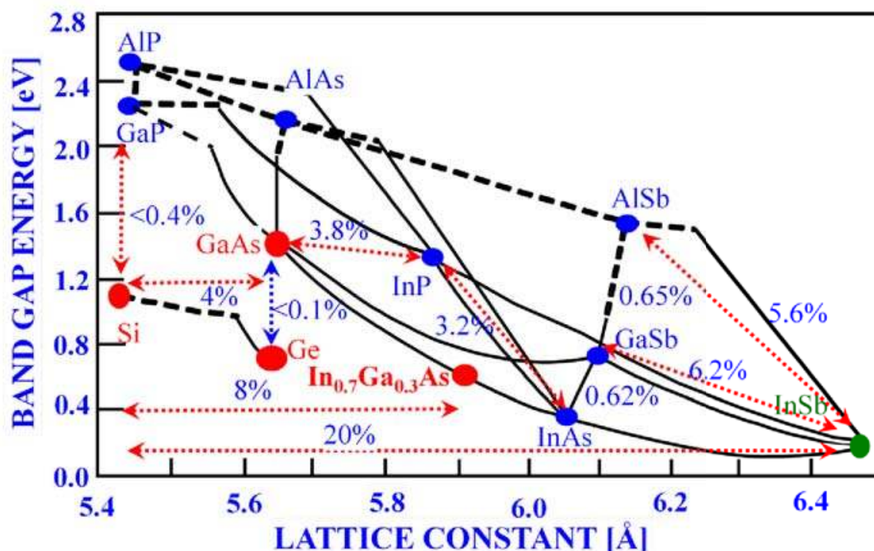

Fig. 1. Bandgap versus lattice constant of III-V semiconductors and its lattice mismatch to Si substrate.

Several efforts have been devoted to determine the QW mobility at 300K of the low bandgap (i.e., InAs or InSb) materials on Si or only the device performance on Si using >6μm buffer thicknesses (51, 52). There is no clear path how to reduce the buffer layer thickness below 6μm for integration of InSb on Si and the reported QW mobility of >27,000 at $3x10^{12}$ cm^2/Vs without any modulation doping in the device structure (51). The most important figure of merits of the heterogeneous integration of low bandgap III-V quantum well devices on Si are (i) QW mobility and (ii) sheet carrier density (N_s), at 75K.

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Often, these figure-of-merits are not considered in designing a metamorphic buffer for realizing low bandgap, high mobility III-V devices on Si. In addition, there are several other issues that need to be addressed, namely, (i) defects density of the III-V active layer grown on Si is $>10^7$ cm^{-2}, (ii) thermal budget for the Si CMOS processing should be below 550°C, (iii) total buffer layer thickness show be <0.5μm, (iv) common buffer platform for both electronic and photonic devices on Si, (v) "*insulating*" nature of buffer layer for eliminating substrate conduction, and (v) the polar/non-polar interface between III-V/Si. To overcome these challenges, novel material innovations and radical changes in buffer architecture design are essential.

Heteroepitaxial growth of III-V on Si involves complex material issues, such as (i) polar-on-nonpolar mismatch, (ii) lattice mismatch, (iii) chemical mismatch and (iv) thermal mismatch. These problems typically result in poor crystalline quality due to formation of various defect types such as anti-phase domains (APDs), misfit and threading dislocations, twining and stacking faults. As a result, the electrical quality of such grown film is not-device worthy. The InGaAs QWFETs on Si system is investigated in this study as an example for addressing heterogeneous integration of low band gap III-V device structures on Si growth issues, and as a potential NMOS channel material for low-power logic application on Si (5-7, 11, 12). In order to achieve the APD-free III-V buffers growth on nonpolar Si substrate and the high-quality InGaAs metamorphic QWFET device structure on such buffer, careful design of various aspects of growth, buffer architecture and strain-relaxation were considered. *This paper reviews* a comprehensive outline of III-V on Si materials integration strategies (5-7, 9, 11, 12) using buffer and strain engineering for obtaining higher QW mobility and present a device level results to evaluate the materials integration success. High-quality and low dislocation density of modulation doped $In_{0.7}Ga_{0.3}As$ metamorphic QWFET structures were grown on Si using solid source molecular beam epitaxy (MBE).

Growth of InGaAs quantum well structure on Si

Materials synthesis

The InGaAs QW device structures were grown on Si (100) substrates that are off-cut by 4° towards the [110] directions using metamorphic buffer layer (5-7, 9, 11, 12). The off-cut, combined with a thermal treatment, migration enhanced epitaxy (MEE) process with As pre-layer, two-step growth process consisting of (i) low temperature and low growth rate, and (ii) high temperature and high growth rate, will allow the formation of two-atomic layer steps on the Si surface, and will thereby eliminate APDs at the GaAs/Si heterointerface. The use of GaAs and ternary $In_xAl_{1-x}As$ graded buffer layers, including the effects of growth temperature, growth rate, layer thickness, and group-III grading rate were used to demonstrate the device worthy InGaAs QW structures. The GaAs and $In_xAl_{1-x}As$ metamorphic buffer architecture was used to mitigate the defects and dislocations in strain and bandgap engineered InGaAs QWFETs on Si (7). Figures 2 (a), 2 (b) and 2 (c) show the buffer architecture for integration of InGaAs QWFET structure on Si using GaAs and graded $In_xAl_{1-x}As$ layers, (b) lattice constant grading scheme for structure (a); and (c) Schrödinger-Poisson solution of spatial redistribution of confined carrier population in various sub-bands in the InGaAs QW at Vg = 0V with higher ΔEc for carrier confinement inside the InGaAs QW. It also avoids the parallel conduction to the active channel due to large bandgap nature of both GaAs and InAlAs layers. Throughout the effort, significant emphasis was made on the identification of defect types and their relation to variations in growth conditions, buffer characterization, carrier mobility, carrier density and benchmarking so that guidelines towards a robust methodology for heterogeneous integration of InGaAs QWFET on Si heteroepitaxy were established.

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The nucleation of GaAs on Si is a crucial step during MBE growth process using MEE. The GaAs nucleation and buffer layers were grown using two-step growth process which consisting of layer at reduced temperature and low growth rate as described above, and carefully monitor the surface to ensure that no APDs or other defects are generated at the GaAs/Si interface using *in-situ* reflection high energy electron diffraction (RHEED) during growth of MBE. The nucleation step will be followed by the deposition of a thicker GaAs with high temperature and higher growth rate followed by graded ternary $In_xAl_{1-x}As$ layer. This way the lattice constant was bridged from the Si surface to the active InGaAs channel. Key to the success of metamorphic structures is the efficient relaxation of misfit strain with minimum threading dislocations. Thus, it is vital to determine the complete structural properties, including strain, defect densities and surface roughness. The entire InGaAs QW structure was characterized using x-ray diffraction, cross-sectional TEM, and atomic force microscopy.

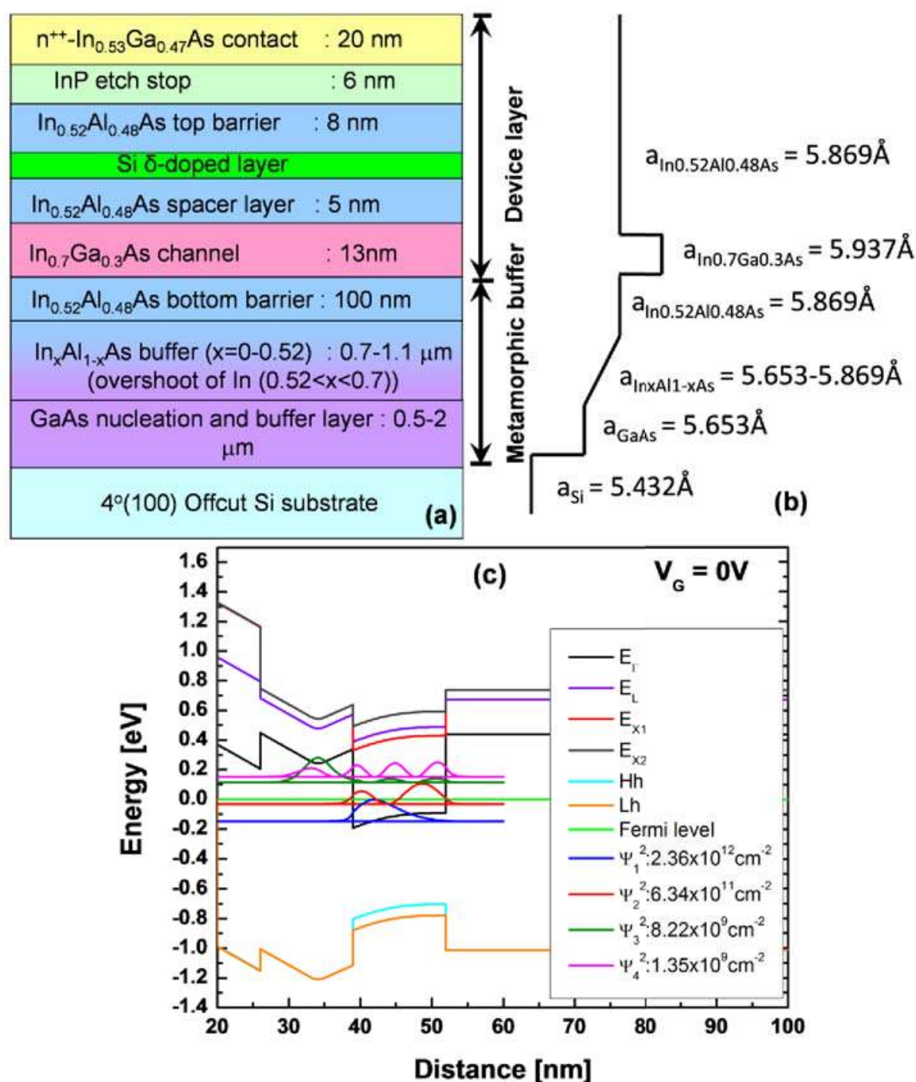

Fig. 2: (a) The n-channel normal InGaAs QW device structure on Si using large bandgap metamorphic buffer layer. The Si delta-doped layer is placed above the InGaAs QW, (b) lattice constant grading, and (c) energy band diagram of InGaAs QWFET using Schrödinger-Poisson solution at Vg = 0V.

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Elimination of parallel conduction

The resistivity of the buffer layer has a significant role to the active device layer conductivity. Since the resistivity of the Si wafer is not too high and it is important that the buffer layer is a large bandgap material so that the conductivity contribution from the buffer layer as well as from the Si wafer to the active InGaAs layer is less significant and it can behave as an *insulating layer*. Therefore, the InGaAs active layer on Si using large bandgap materials behave as a “SOI” (silicon-on-insulator) and the conductivity should exhibit only from the device layer. On one hand, the bandgap of the buffer layer should be large enough so that it prevents parallel conduction from the Si substrate; on the other hand, the bandgap of the buffer layer should not be *too large* since large bandgap needs higher temperature to relax the misfit strain. There is a trade-off between the bandgap of the buffer layer and the growth process temperature. The detailed mobility analysis was performed of InGaAs QWFETs grown on Si using quantitative mobility spectrum analysis (QMSA) as a function of temperature and to separate mobility contribution from carriers inside the buffer layer.

Origins of defects in InGaAs

Defects in InGaAs films grown directly on Si substrates result from at least three sources: i) the polar on nonpolar III-V/Si interface, ii) the large lattice constant mismatch, and iii) the atomic interdiffusion across the interface. These problems typically result in poor crystalline quality due to formation of various defect types such as (i) anti-phase domains, misfit and crystal defects such as (ii) threading dislocations, (iii) stacking faults, and (iv) micro-twins. All these defects have an adverse effect on the device performance. A low-defect density III-V-material growth on Si is achieved through monolayer scale control using MBE for the formation of the III-V/Si interface and coupled with optimization of compositionally graded buffer layers. Appropriate thin buffer layer was designed for filtering defects and

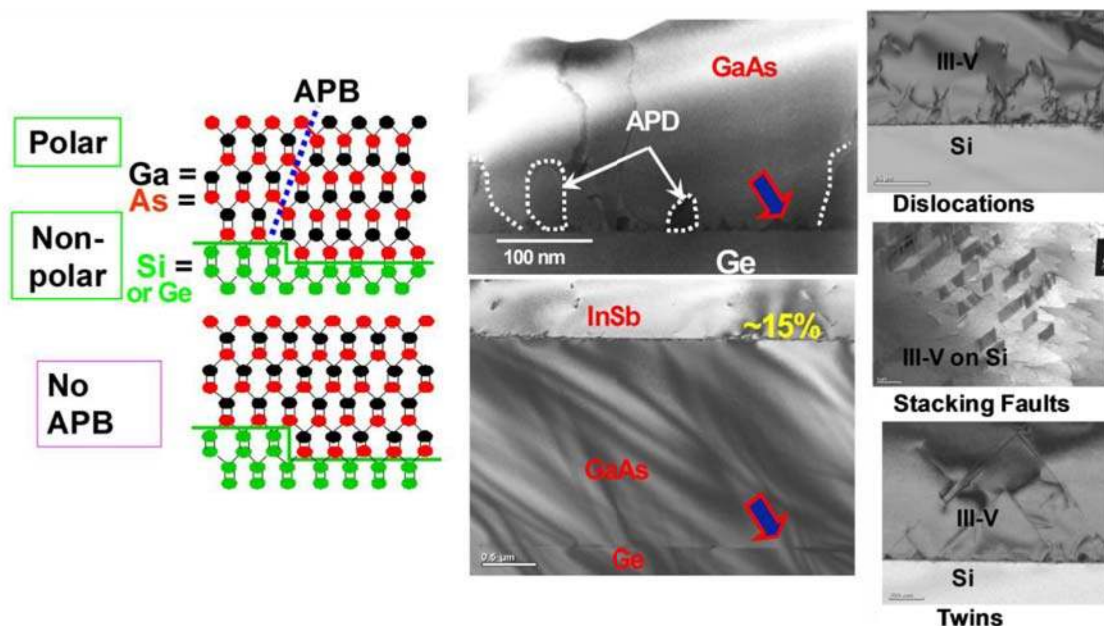

Fig. 3: Growth of polar (III-V) on nonpolar (Si) epitaxy where (a) APDs were eliminated utilizing proper substrate off-cut and nucleation conditions and (b) various crystal defects due to lattice mismatch.

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dislocations and for successful strain engineering. Figure 3 shows the APD-free GaAs on Ge where anti-phase boundaries (APBs) were eliminated by utilizing appropriate off-cut substrate and leveraging migration enhanced epitaxy (6, 7, 11, 12). In this case, Ge substrates have been selected to address the problem of polar/nonpolar interface by growing lattice matched GaAs on Ge crystal. The similar process generally used for the growth of GaAs on offcut Si substrate using MBE growth technique to create a "virtual" polar III-V surface on Si. As a result, the InGaAs QW is free from APDs, stacking faults and micro-twins.

Results and discussion

Structural properties

The structural quality and the defect properties of the InGaAs QWFET structures were examined by cross-sectional TEM. Figure 4 (a) and (b) shows low and high-resolution cross-sectional bright field TEM images of $In_{0.7}Ga_{0.3}As$ QWFET structure grown on Si substrate using metamorphic graded composite $In_xAl_{1-x}As$ and GaAs buffers (7, 12). The image of figure 4 shows a high contrast at the graded buffer layers and the misfit and threading dislocations are predominantly contained in the composite buffer with no threading dislocations (TDs) observable in the $In_{0.7}Ga_{0.3}As$ QW using cross-sectional TEM. This image reveals that the threading dislocation density (TDD) decreases monotonically along the growth direction and the dislocation density confined within 0.5μm of the InAlAs buffer layer. Beyond this region, the TDD decreases abruptly due to annihilation of dislocations with opposite Burgers vectors and virtually dislocation-free $In_{0.7}Ga_{0.3}As$ channel layer.

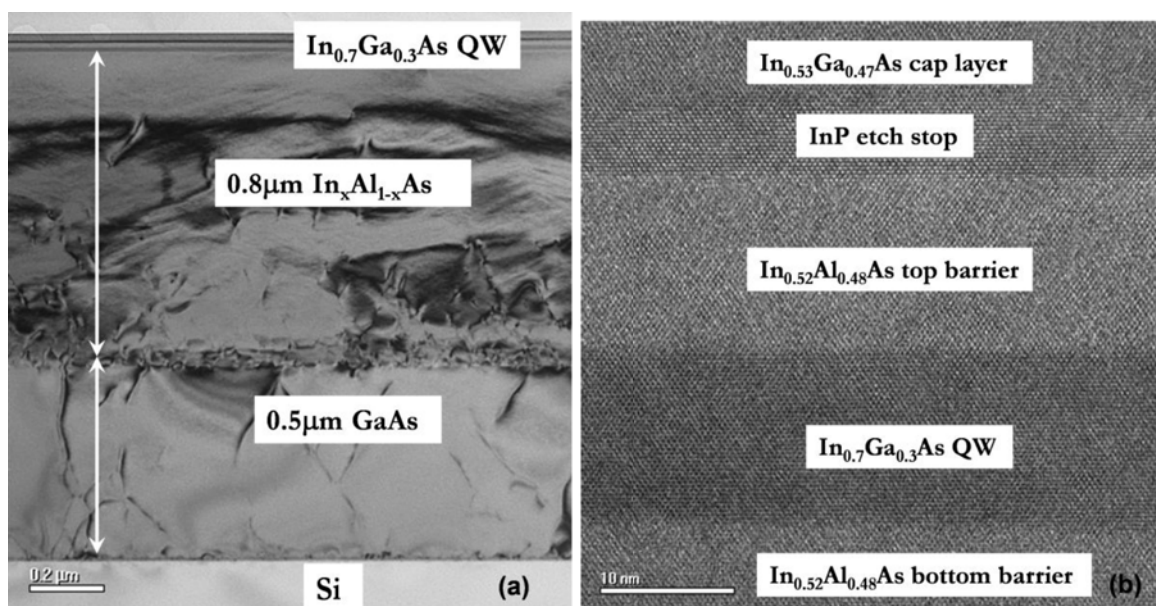

Fig. 4: (a) Cross-sectional TEM image of $In_{0.7}Ga_{0.3}As$ QWFET structure on Si using metamorphic buffer architecture; and (b) high-resolution TEM of $In_{0.7}Ga_{0.3}As$ QW, $In_{0.52}Al_{0.48}As$ barriers, InP etch stop and $In_{0.53}Ga_{0.47}As$ cap layer. The misfit and threading dislocations are predominantly contained in the composite buffer.

The grading scheme and the relaxation state of the InGaAs QWFET structures were evaluated using high-resolution double crystal x-ray rocking curves, as shown in figure 5 (7, 12), the structure of which is

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shown in Fig. 2 (a). The angular separation Δθ between the (004) diffraction peaks of $In_xAl_{1-x}As$, GaAs and Si resulting from the difference in lattice plane spacing Δd/d, along with their diffraction line profiles, provided information about the microstructural quality of the these films, which in turn can affect the active InGaAs channel film quality. The Δθ separation between the diffraction peaks of GaAs with respect to Si confirms full relaxation of the GaAs layer. The indium composition of the $In_xAl_{1-x}As$ buffer layer is graded from 0 to 52%, with an overshoot of indium concentration ($0.52<x<0.7$) in-between, as evidenced by the two peaks existing in the $In_xAl_{1-x}As$ buffer region of figure 5. This overshoot was employed to ensure full relaxation of this buffer layer while minimizing its total thickness. The relaxation of the entire composite buffer layer allows the growth of a defect-free $In_{0.7}Ga_{0.3}As$ QW on Si (Figs.4a-2b). Figures 4 (b) and 5 suggest the $In_{0.7}Ga_{0.3}As$ QW layer is compressively strained with respect to the $In_{0.52}Al_{0.48}As$ barrier.

The surfaces of the InGaAs metamorphic QWFET structures were secular and under Nomarski microscope contrast exhibited a characteristics cross hatch pattern of metamorphic growth. Figure 6 shows the surface morphology of InGaAs QWFET grown on Si using AFM. The cross-hatching of the metamorphic QWFET structure is the result of continual introduction of strain and the consequent relaxation of strain by generating misfit dislocations along the two orthogonal <110> misfit dislocation directions. Analyzing the AFM surface morphology of the $In_{0.7}Ga_{0.3}As$ QW layer grown on Si with 1.3μm composite buffers exhibit a cross-hatch pattern, as shown in figure 6, demonstrating excellent metamorphic growth of the buffer layer. The surface rms roughness of $In_{0.7}Ga_{0.3}As$ QW grown on Si was measured over an area of 5x5μm2 to be less than 4 nm (7) which is similar to that of $In_{0.7}Ga_{0.3}As$ QW grown on GaAs (7). This is also consistent with RHEED observation during growth, which displayed a more streaky (2x4) surface reconstruction pattern for metamorphic buffer as well as InGaAs channel layer. The vastly improved surface morphology for the InGaAs QWFET on Si substrate is believed to be due to proper controlled of nucleation and glide of dislocations in the composite buffer layers.

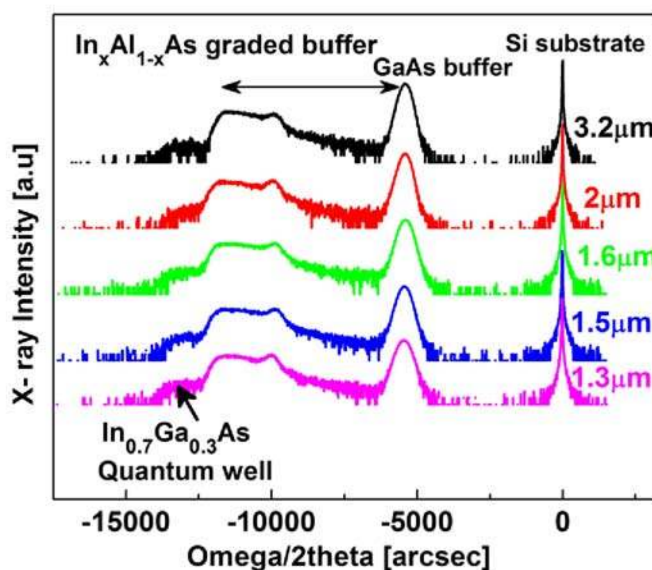

Fig. 5: High-resolution x-ray rocking curves from the (004) Bragg lines of $In_{0.7}Ga_{0.3}As$ QWFET structures on Si substrates with different composite buffer thicknesses ranging from 1.3-3.2μm.

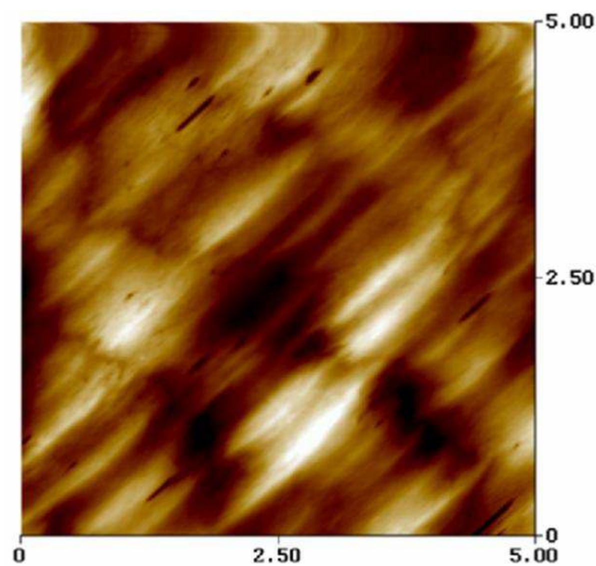

Fig. 6: AFM image from the surface of $In_{0.7}Ga_{0.3}As$ QW layer on Si with 1.3μm composite buffer shows cross-hatch pattern with surface *rms* roughness of 39Å.

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Electrical transport properties

To further investigate the electrical quality of the InGaAs QWFET as well as the parallel conduction to the $In_{0.7}Ga_{0.3}As$ channel layer, temperature and field dependent mobility measurements were performed and the results are analyzed using QMSA® method. For epitaxial crystal growers, Hall effect measurements are typically carried out to assess the quality and control of doping in semiconductor layers with the Hall mobility as an important figure of merit. Figure 7 (a) shows the $In_{0.7}Ga_{0.3}As$ QW mobility at 300K and 77K as a function of total buffer thickness ranging from 3.2μm to 1.3μm of the composite buffer grown on Si (7, 9, 11, 12). No mobility degradation is observed for all the buffer thicknesses, demonstrating that the thin composite metamorphic buffer architecture is effective in filtering dislocations. Figure 7 (b) compares the Hall mobility versus sheet carrier density (Ns) measured in the $In_{0.7}Ga_{0.3}As$ QW layers grown on Si, GaAs and InP substrates at 300K and 77K. For a given Ns, the mobility in the $In_{0.7}Ga_{0.3}As$ QW layer grown on Si via the composite buffer is equivalent to those in the $In_{0.7}Ga_{0.3}As$ QW layers grown on III-V substrates such as GaAs and InP (7). The high mobility of $In_{0.7}Ga_{0.3}As$ QWFET on Si substrate is due to low dislocation density inside the InGaAs channel, supports our structural results. No degradation in QW mobility on Si is observed despite the >8% lattice mismatch, demonstrating effective dislocation filtering using the composite buffer on Si. Figure 8 (a) shows the quantitative mobility spectrum analysis (QMSA) for $In_{0.7}Ga_{0.3}As$ QW on Si at different temperatures (7, 11, 12). The large conductivity ratio between the majority carrier (electrons) and the minority carrier (holes) at all temperatures and also the increase in electron mobility with decreasing temperature suggest no parallel, parasitic conduction in Si or through the composite buffer layer. In addition, both Ns and mobility exhibit no dependence on magnetic field at different temperatures, as shown in figure 8 (b) (7, 11, 12), further indicating no parallel, parasitic conduction in the buffer layer or in Si.

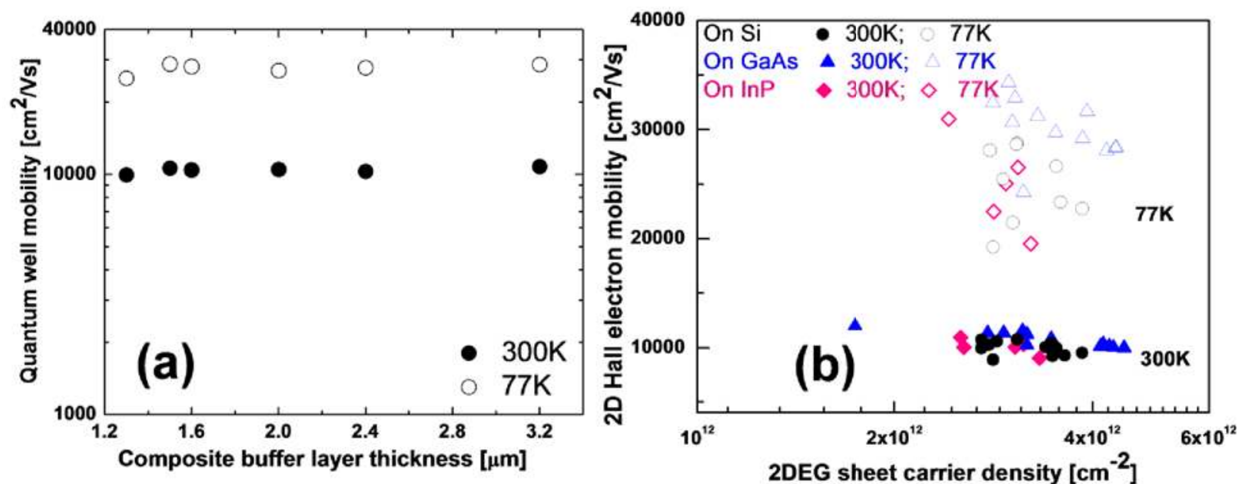

Fig. 7: **(a)** $In_{0.7}Ga_{0.3}As$ QW electron mobility versus composite buffer layer thickness on Si at 300K and 77K; and (b) electron mobility versus sheet carrier density (N_s) in $In_{0.7}Ga_{0.3}As$ QW grown on Si (via novel composite buffer), GaAs and InP substrates at 300K and 77K. No degradation in QW mobility on Si despite >8% lattice mismatch, demonstrating effective dislocation filtering with the composite metamorphic buffer architecture on Si.

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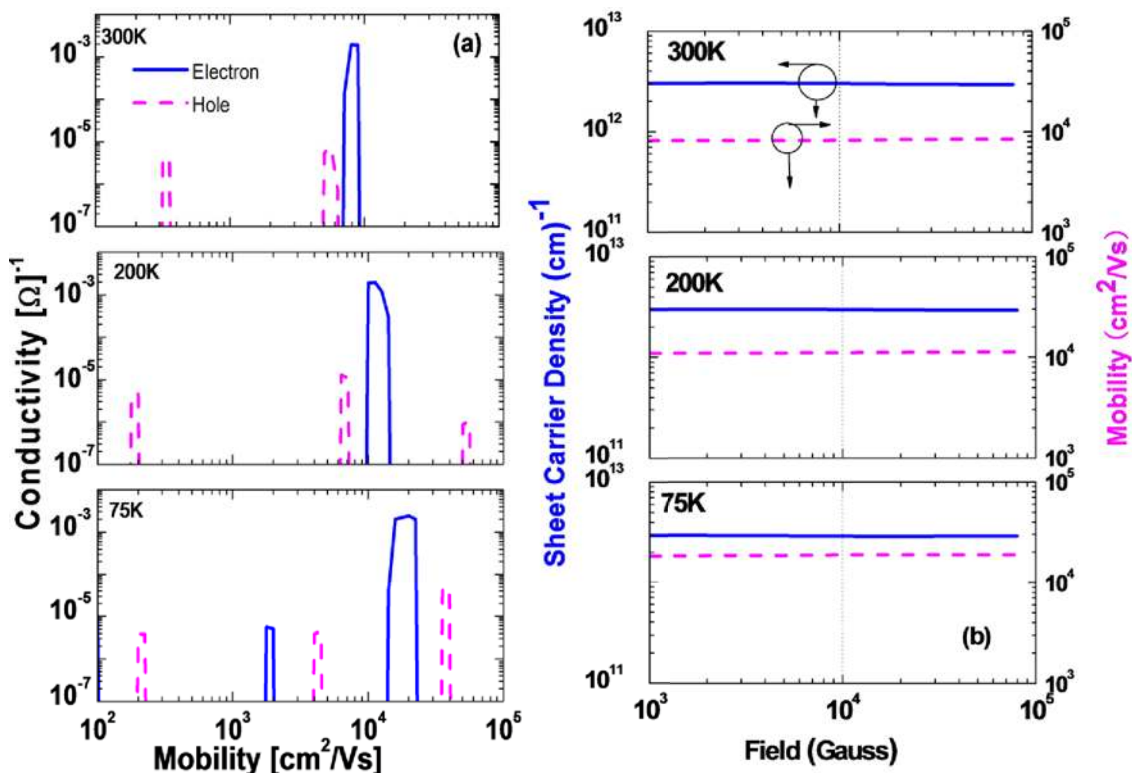

Fig. 8: (a) QMSA mobility spectra for $In_{0.7}Ga_{0.3}As$ QW on Si at different temperature demonstrating no parallel, parasitic conduction to the active $In_{0.7}Ga_{0.3}As$ channel, and (b) sheet carrier density and mobility show no dependence on magnetic field at different temp, indicating no parallel conduction in the composite buffer layer on Si.

Device properties

In order to evaluate the success of the heterogeneous integration of n-channel InGaAs material and device structure on Si, the QW transistors have been fabricated and benchmarked with the n-channel Si MOSFET. The use of a combination of wet and reactive ion etch to recess the gate towards the channel, as well as Pt/Au Schottky gates, enable enhancement-mode (e-mode) operation and improve short channel performance of the device. The details of the fabrication procedure were reported elsewhere (7, 9). The output characteristics, I_{DS}-V_{DS} of the e-mode with gate length of L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer layer is shown in figure 9 (a) (7, 11, 12). Figure 9 (b) shows the transfer characteristics, I_{DS}-V_{GS} of the e-mode with L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFETs on Si. The Schottky gate leakage is also included for reference (7, 11, 12). This device exhibits good transistor characteristics and high performance at supply voltage of V_{DS} = 0.5V. The L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer achieves threshold voltage (V_T) = + 0.11V, saturation current, I_{Dsat} = 0.32mA/μm and I_{ON}/I_{OFF} = 2150 at V_{DS}=0.5V with 0.5V gate voltage, V_G swing. Figures 10 (a) and 10 (b) show the sub-threshold slope (SS) and drain induced barrier lowering (DIBL), respectively as a function of L_G for $In_{0.7}Ga_{0.3}As$ QWFETs on Si (7, 11, 12), demonstrating improved SS and DIBL of e-mode over d-mode devices. Figure 11 shows the transconductance (G_m) characteristics of L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFETs on Si with different composite buffer thicknesses at V_{DS} = 0.5V (7, 11, 12). These e-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si substrate exhibit superior high-speed performance even at low supply voltage. Fig. 12 shows the cut-off frequency as a function of DC power dissipation comparing the e-mode L_G = 80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si at V_{DS}=0.5V versus the standard L_G = 60nm Si n-MOSFET transistor at both

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V_{DS} = 0.5V and 1.1V. Comparing to the Si n-MOSFET, the e-mode $In_{0.7}Ga_{0.3}As$ QWFET on Si exhibits >10X reduction in DC power dissipation for the same speed performance or >2X gain in speed performance for the same power (7, 11, 12).

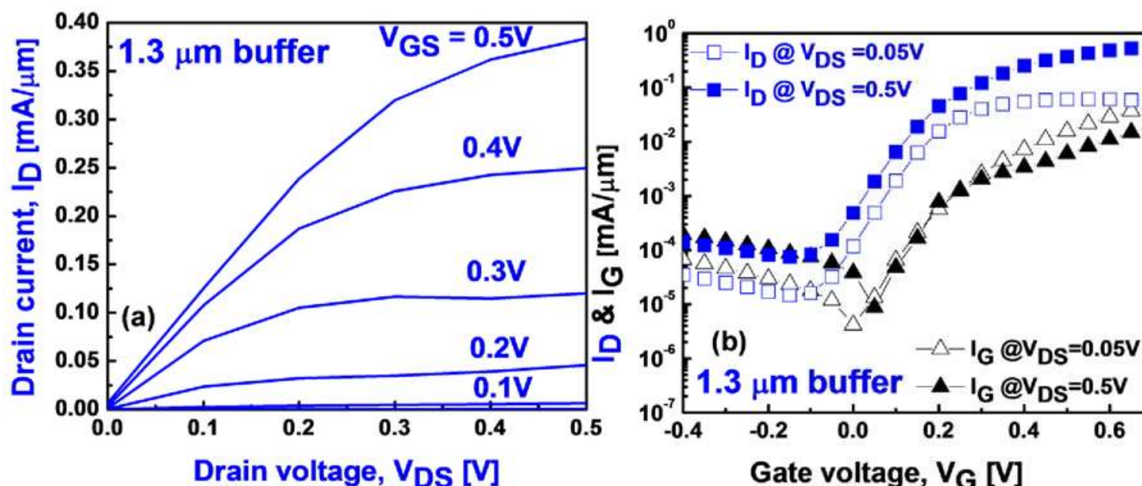

Fig. 9: (a) I_D-V_{DS} characteristics and (b) I_D-V_{DS} and gate leakage (I_G) versus V_G of enhancement-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si with 1.3μm composite buffer at room temperature. V_T = +0.11V, I_{Dsat} = 0.32mA/μm, I_{ON}/I_{OFF} = 2150 at V_{DS}=0.5V with 0.5V V_G swing.

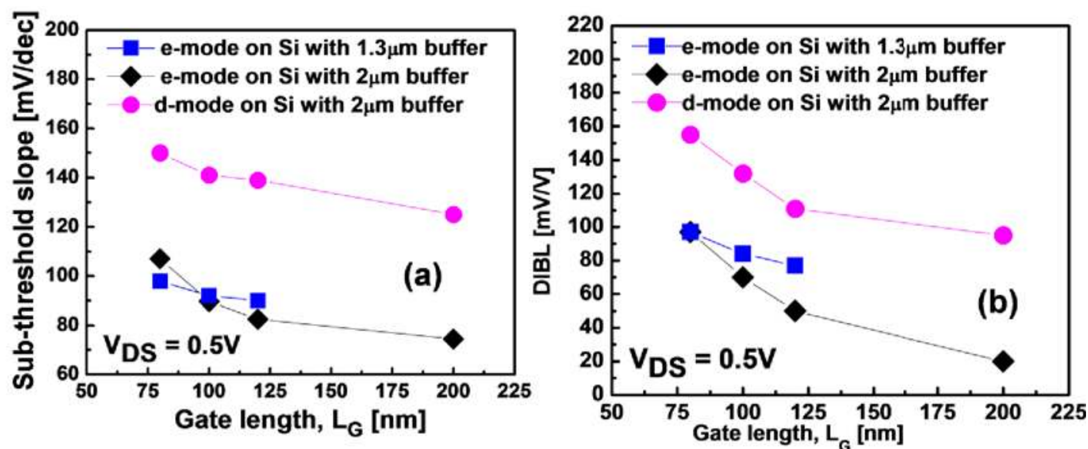

Fig. 10: (a) Sub-threshold slope (SS) and (b) DIBL as a function of L_G for e-mode and d-mode $In_{0.7}Ga_{0.3}As$ QWFETs on Si, showing improved SS and DIBL of e-mode over d-mode devices due to shorter gate to channel separation in e-mode.

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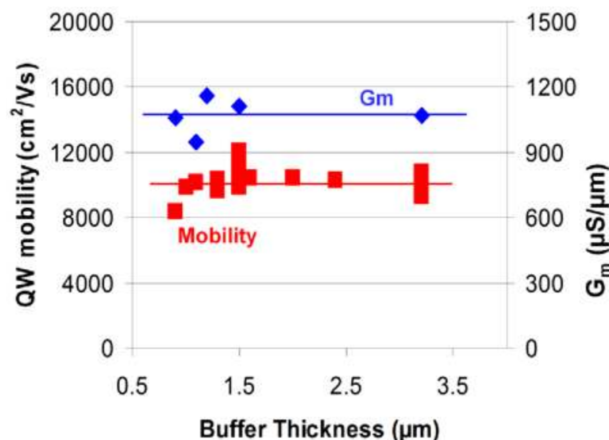

Fig. 11: QW mobility and transconductance (G_m) as a function of composite buffer layer thickness.

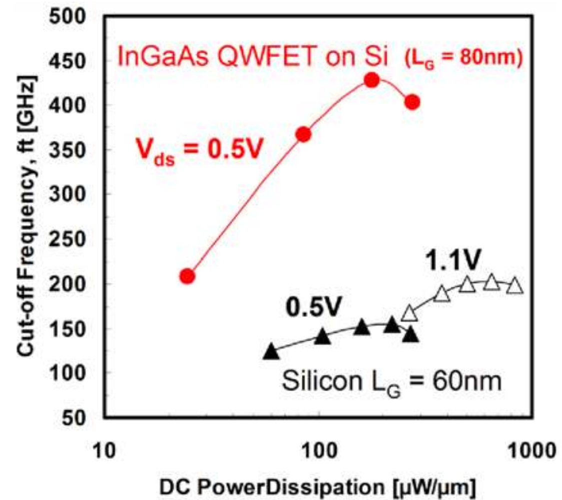

Fig. 12: Cut-off frequency as a function of DC power dissipation for the e-mode L_G=80nm $In_{0.7}Ga_{0.3}As$ QWFET on Si at V_{DS}=0.5V, versus standard Si n-MOSFET transistor with L_G = 60nm at V_{DS}=0.5V and 1.1V.

Conclusions

In conclusion, high quality $In_{0.7}Ga_{0.3}As$ QWFET structures on Si substrates have grown using solid source MBE with excellent material properties. Cross-sectional TEM micrographs showed no threading dislocation inside the QW and the surface cross-hatched pattern indicates with full relaxation. The electron mobilities and sheet carrier densities of the $In_{0.7}Ga_{0.3}As$ QWFET structures grown on Si were nearly equivalent to the structures grown on either GaAs or InP substrates. The $In_{0.7}Ga_{0.3}As$ QWFET structures with thin composite GaAs and $In_xAl_{1-x}As$ buffer layers did not showed any parallel path to the active $In_{0.7}Ga_{0.3}As$ channel. Quantum well transistors fabricated on these $In_{0.7}Ga_{0.3}As$ QW structures exhibit high-performance short-channel enhancement-mode characteristics and thus have a potential for future ultra-high speed and low-power logic applications.

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