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Heterojunction Diode Shielded SiC Split-Gate Trench MOSFET With Optimized Reverse Recovery Characteristic and Low Switching Loss

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ABSTRACT A split-gate SiC trench MOSFET with a hetero-junction diode (HJD) is proposed and numerically analyzed in this paper. The proposed structure features the HJD to effectively suppress the turn-on of the parasitic body diode and reduce the depletion region in the JFET area. A P+ shielding layer surrounding the HJD and the gate oxide layer is used to alleviate the concentration of the electric field under the gate trench and improve the switching performance. As a result, not only the breakdown voltage is increased by 20.8% at the same level of the on-state resistance but also the miller charge and the switching loss of the proposed structure are reduced by 52% and 39.1%, respectively when compared with those of the conventional SiC trench MOSFET.

INDEX TERMS Silicon carbide, heterojunction diode, high breakdown voltage, low on-state resistance, low switching loss.

I. INTRODUCTION

Because of the high power density of the cell-pitch, silicon carbide (SiC) trench MOSFET with the ultra-low on-state resistance and excellent switching characteristic is commonly recognized as to be one of the best candidates used in the power systems [1]–[3]. Recently, many studies about the device structures have been conducted for SiC devices [4]–[9]. A critical issue for the SiC trench MOSFET is to increase the gate oxide reliability at the trench bottom but without increasing of the resistance of junction field-effect transistor (JFET) area. Conventional SiC trench MOSFET (C-TMOS) with the shielding structure and carrier spreading layer (CSL) by using a high doping P+ layer and n layer under the trench oxide layer and channel, respectively, is one of the solutions to get a tradeoff between gate reliability and JFET resistance. The advantage of the C-TMOS over the planar one has been experimental demonstrated in [10]–[13]. Usually, when the C-TMOS operates in the power system, a SiC Schottky barrier diode (SiC SBD) should be in parallel with it to prevent aged deterioration due to the bipolar operation of the parasitic body diode. This can lead to the extra chip cost, power system loss, and undesirable stray inductance. Those factors generate the new challenges to the design of the C-TMOS.

Several literatures about the optimized structures have been proposed recently by the experimental demonstration or the numerical analysis, aiming to decreasing power system loss, improving the reverse recovery characteristic and reducing the chip cost, such as the SiC MOSFET with the merged junction barrier controlled schottky rectifier [10], the SiC MOSFET with the built-in SBD [11] and the SiC split-gate MOSFET with merged SBD [12]. In addition, an SBD-wall-integrated SiC trench MOSFET (SWITCH-MOS) is provided in [13] and presents a result of the mitigation of the forward degradation under extremely high current density condition. However, those devices still face the problems of the complex and costly for the requirement of extra photolithography and fabrication process. Especially, the SBD structure closed to the gate electrode cannot avoid introducing the metallization

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contamination to the gate oxide layer, leading to the reliability and unstable problems for the gate oxide layer and threshold voltage [14].

Heterojunction diode (HJD) combined with the Poly-Si and SiC has considerable impact as regards of achieving the good reverse recovery because of unipolar action similar with that of the SiC SBD [15], [16]. The HJD is thus to be considered as a new option to not only improve the device performance but also reduce the whole power system cost.

In this paper, a novel split-gate SiC trench MOSFET with the P-poly/SiC heterojunction diode (HJD-STMOS) is proposed and analyzed by the numerical simulation. The proposed structure has a trench gate composed of the split-gate electrode and the thicker P-poly to reduce the total gate charge and optimize the switching performance. In order to further increase the breakdown voltage (BV) of the device and eliminate the dynamic degradation induced by the float P+ shielding layer [17], a grounded P+ shielding layer is introduced and surrounded the whole P-poly. Due to the merged HJD structure, the proposed device does not require an anti-parallel SiC SBD at reverse conduction. The simulation results show that this new structure greatly improves the on-state and the reverse recovery characteristics and decreases the power loss without increasing of the extra fabrication process compared with the C-TMOS.

II. DEVICE STRUCTURE AND BASIC SETUP

Figs. 1(a) and (b) show the schematic structure of the C-TMOS and the proposed HJD-STMOS. Compared with the C-TMOS, the proposed HJD-STMOS has a split gate and a HJD structure surrounding the gate oxide layer. The split gate means that only half of trench space is used for the gate electrode, and the other is thicker P-poly which is one part of the HJD structure. In order to classify the mechanism of the HJD structure, the Energy-band diagrams between the P-poly region and the SiC CSL in the thermal equilibrium state are shown in Fig. 1(c). The energy gaps of the HJD for conduction and valence bands are 0.45 eV and 1.73 eV, respectively. The barrier height Φ_{BN} for electrons is determined by the Fermi level energy E_f and the peak of the conduction band E_c, which is about 1.48 eV. This barrier height gives the HJD the small forward voltage (V_F) and high breakdown voltage (BV) when the device is forward and reverse biased, respectively, making the HJD operation as the SBD. In addition, a grounded P+ shielding layer is surrounded the whole P-poly and gate oxide layer to reduce the electric field in the P-poly and the gate oxide layer and to eliminate the dynamic degradation. In order to reduce the process defect to the device characteristics, the P+ shielding layer as well as the floating guard rings are formed at same time by a heavy dose aluminum implantation at 500 °C ambient temperature at first.

To make a fair comparison, the C-TMOS and the HJD-STMOS keep the same doping profiles and the closed device dimensions. The thickness and the doping concentration of the drift layer are 6.5 μm and 7.5×10^{15} cm^{-3}, respectively,

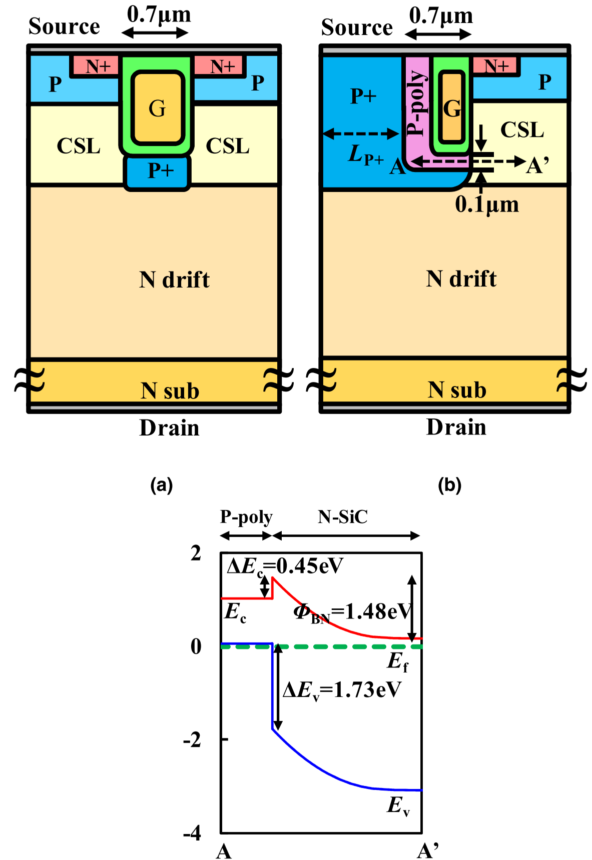

FIGURE 1. Cross-sectional views of (a) C-TMOS, (b) HJD-STMOS, and (c) Band diagram along line AA.

for a 650 V rated BV. The thickness and the doping concentration of the channel layer are 0.6 μm and 3×10^{17} cm^{-3}, respectively. The width and the depth of the trench are 0.7 and 1.2 μm, respectively. The thickness of the gate oxide layer in the wall and bottom are 60 and 120 nm, respectively. The thickness of P-poly under the gate oxide layer is 0.1 μm and the gate electrode for the HJD-STMOS is 0.3 μm based on the process limitation. The doping concentration of CSL is 2×10^{16} cm^{-3}.

Devices simulations using Sentaurus TCAD [18] are deployed to reveal the electric performances of the devices. While making the simulations, SRH, AUGER, OkutoCrowell are used as recombination models to describe the trap-assisted recombination, the non-radiative process involving three carriers and the breakdown analysis, respectively. At same time DopingDependence, HighFieldSaturation and Enormal are used as mobility models. In order to fit the real device process, the trap with the doping concentration of 5×10^{12} eV^{-1}cm^{-2} is uniformly distributed at the interface between SiO_2 and SiC for both devices.

III. RESULTS AND DISCUSSION

Fig. 2 shows the simulation results of the dependence of the BV, the specific on-resistance (R_{on}), the V_F, and the turn-on voltage of the parasitic body diode (V_{PN}) on the width of the

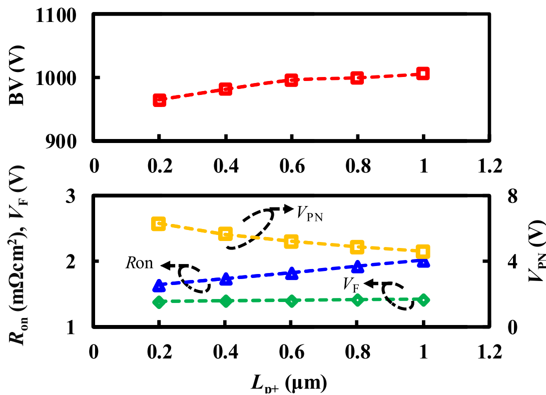

FIGURE 2. The tradeoff results of L_{P+} as functions of the BV (V_{gs} = 0 V), the R_{on} (V_{gs} = 15 V), the V_F (V_{gs} = −5 V) and the V_{PN} for the HJD-STMOS.

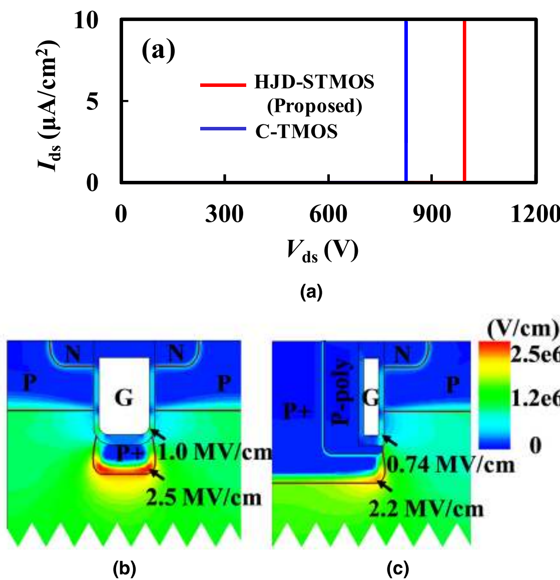

FIGURE 3. Breakdown characteristics of the C-TMOS and the HJD-STMOS. (a) The BVs of the C-TMOS and HJD-STMOS. (b) The electric field distribution for C-TMOS. (c) The electric field distribution for HJD-STMOS. For the electric field distributions, V_{ds} is 650 V.

P+ shielding layer (L_{P+}). As increase of the L_{P+}, the BV and R_{on} are increased while the opposite results can be achieved for the V_{PN}. The BV curve is gradually smooth when the L_{P+} increase to 0.6 μm. This is because the electric field crowding is mainly located at the junction corner of the P+ shielding layer. This electric field concentration is no longer relieved when the L_{P+} increases to its limitation. The change of the V_F is not obvious with different L_{P+}. Although the thin P-poly of 0.1 μm is used in the HJD-STMOS, the optimized V_{PN} of 5.2 V is over two times larger than the turn-on voltage of pn junction (~2.5V), indicating a good suppression in turn-on of the body diode.

The optimized L_{P+} for the HJD-TMOS is set to be 0.6 μm. The BVs of two optimized devices are shown in Fig. 3 (a). As shown in Fig. 3(b) and (c), since the electric fields of both devices can be significantly reduced in the gate oxide layer at the drain-source voltage of 650 V, the electric field of the HJD-STMOS in P+ shielding layer is much lower compared with that of the C-TMOS due to the wider L_{P+}. In addition, the electric field of 0.74 MV/cm in the trench corner makes the proposed structure has a high level gate reliability.

Fig. 4 (a) shows the first- and third-quadrant I-V characteristics of the C-TMOS and the HJD-STMOS at the gate voltage (V_{gs}) of 15 and −5 V, respectively. Although the forward characteristic of the HJD-STMOS at current density of 100 A/cm^2 is better than that of the C-TMOS due to the optimized depletion area in the JFET region, which can be seen in Fig 4 (b), the saturation current of the proposed HJD-STMOS is smaller than that of the C-TMOS, leading to a promising short-circuit capability. As shown in Fig. 4 (c), because the current can flow from the HJD structure when device is reverse conduction, the reverse V_F of the HJD-STMOS is much lower than that of C-TMOS (body diode

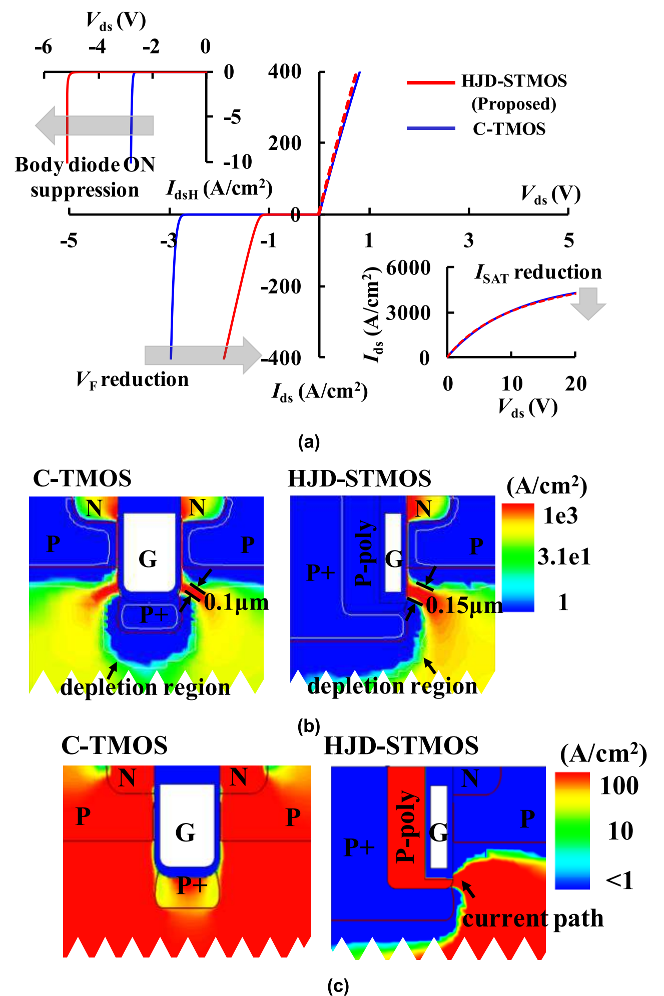

FIGURE 4. (a) Forward I-V and reverse conduction characteristics of the two devices at V_{gs} = 15 and −5 V, respectively. The I_{dsH} as a function of the V_{ds} in the insert picture shows a significant suppression in body diode ON and the saturation current for HJD-STMOS. The active area of each device is 1 cm^2. (b) The current distribution of the two devices at current density of 100 A/cm^2 at V_{gs} = 15 V. (c) The current distribution of the two devices at current density of −100 A/cm^2 at V_{gs} = −5 V.

operation), leading to the remarkable reduction in dead-time loss. Moreover, the drain hole current (I_{dsH}) as a function of the V_{ds} in the insert picture shows that the V_F of the optimized HJD-STMOS is increased to −5.19 V at the I_{dsH} of 10 A/cm^2, indicating a significant suppression of the turn-on of the P-well/N-drift junction.

Gate charges for both devices extracted from numerical simulation are shown in the Fig. 5. Due to similar height of miller plateau, the both devices have similar threshold voltage. Since the gate charge required to reach the plateau voltage increases because of the shortened of distance of the gate and source electrodes, the ultra-small gate-to-drain charge (Q_{gd}) of the proposed structure with 60 nC/cm^2, which is 52% smaller than that of the C-TMOS (125 nC/cm^2), resulting in a dramatic reduction in power loss. The electrical characteristics of the C-TMOS and the HJD-STMOS are summarized in Table 1.

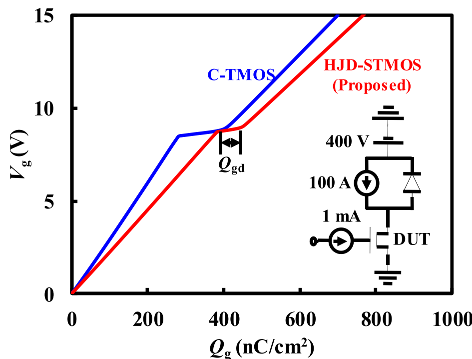

FIGURE 5. Gate charge test of the C-TMOS and the HJD-STMOS. The insert picture is test circuit.

TABLE 1. Device characteristics.

Symbol	C-TMOS	HJD-STMOS (Proposed)	Unit
BV	824	993	V
R_{on}^*	1.87	1.82	mΩ·cm^2
Q_{GD}	125	60	nC/cm^2
V_F^*	2.9	1.4	V

* I_{ds}= 100/-100 A/cm^2, V_{gs} =15/ -5 V.

The switching test circuit and characteristics of the both devices are shown in Fig. 6. Although a SiC SBD is anti-paralleled with the C-TMOS, the reverse recovery charge (Q_{rr}) of the proposed HJD-STMOS is great reduced while the reverse recovery current spike of the proposed one is 51 A (24% reduction) smaller than that of the C-TMOS/SBD during the turn-on state. The switching loss of the C-TMOS and the HJD-STMOS are shown in Fig 6 (c). The switching loss of the proposed HJD-STMOS reduces 39.1% when compared with that of the C-TMOS. This is due to the smaller Q_{gd} and excellent reverse recovery characteristic compared with the C-TMOS. Therefore, the merged HJD structure and the optimized P+ shielding layer play the critical roles to contribute the device with the low switching loss, resulting in the advanced device performance.

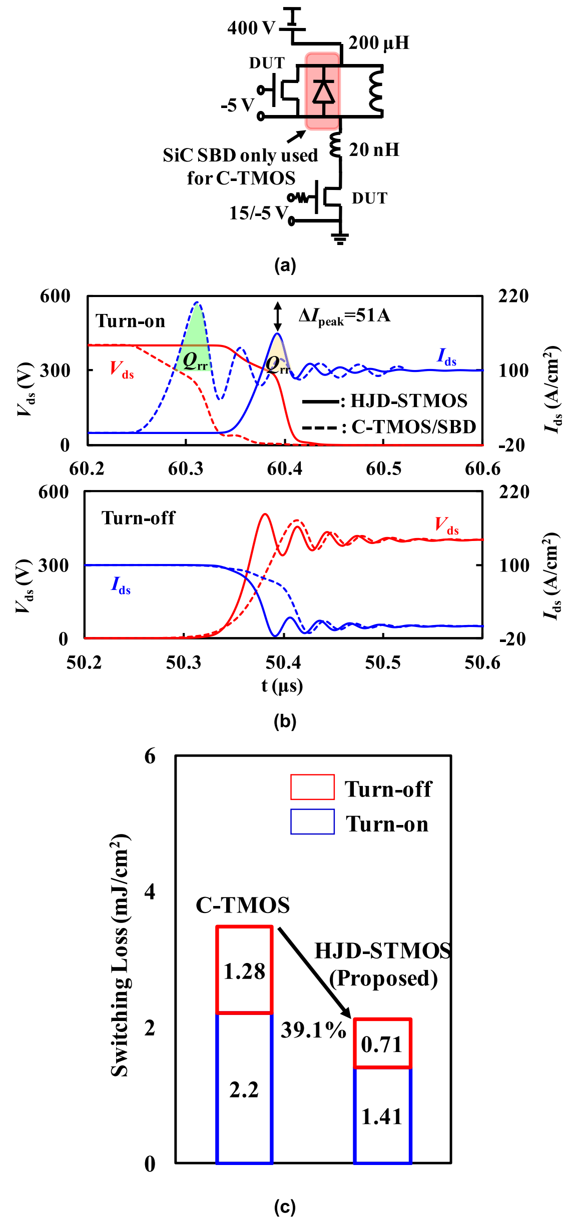

FIGURE 6. (a) Double pulse test circuits and (b) switching waveforms of the C-TMOS/SBD and the HJD-STMOS at the drain current of 100 A/cm^2. The minority carrier lifetime of each device is 1.2 μs. The active area of anti-parallel SBD for the C-TMOS is 1 cm^2.

IV. CONCLUSIONS

A novel SiC HJD-STMOS is proposed in this paper, which features a heterojunction diode and a high doping P+ type shielding layer with the grounded connection to reduce the JFET resistance and protect the gate oxide corner from the concentration of the electric field. The outstanding characteristics with the improved breakdown voltage, on-state resistance, reverse recovery characteristic and switching

performance make the proposed HJD-STMOS to be a superior candidate for power system applications.

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