HfO$_2$ Based Resistive Switching Non-Volatile Memory (RRAM) and Its Potential for Embedded Applications

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Abstract. In this letter, HfO$_2$ based RRAM with varying device sizes are discussed with an analysis on their electrical characteristics. Device sizes of 60nm and 120nm were achieved by using different thickness of nitride spacer after 200nm contact hole is formed. Platinum (Pt) bottom electrode and Titanium Nitride (TiN) top electrode were used with HfO$_2$ dielectric as the resistance switching layer. Uniform bipolar switching characteristics with a low I$_{reset}$ of about 100μA are achieved with self-compliance effect. It is demonstrated that RRAM has a potential to be used as the embedded memory fabricated directly at the backend of CMOS process.

Keywords: RRAM, Reset Current reduction, Bipolar Switching, Self-compliance.

1. Introduction

Resistive random access memory (RRAM) devices have proven to be one of the most promising candidates for next generation non-volatile memory (NVM) due to their high switching speed, good endurance, sub-22nm scalability and good compatibility with CMOS process [1-3]. Recent findings reveal Hafnium dioxide (HfO$_2$) to be a very good switching dielectric material owing to its high scalable and reliable nature [2-3]. In this paper, we show that the HfO$_2$ devices of smaller sizes demonstrate uniform bipolar switching characteristics similar to the larger devices [4], without using multilayer dielectrics [5]. Reduced I$_{reset}$ and self-compliance effect are also observed.

2 Discussion

2.1 Fabrication

HfO$_2$ based RRAM with varying device sizes have been fabricated by using nitride spacer of different thicknesses [6] after the contact holes are formed over Pt/Ti/Si substrates. Higher the thickness of nitride, smaller is the device size. Three different splits with no nitride spacer and two different nitride thicknesses- 50nm and 90nm, have been designed to form devices of the sizes 200nm, 120nm and 60nm respectively. This is followed by physical vapour deposition (PVD) of HfO$_2$ to form a thin film of around 5nm over the wafer surface which is further annealed at 450°C in O$_2$ ambience for 5 minutes. TiN top electrode (TE) of 100nm is then deposited by reactive sputtering and then devices are patterned with optical lithography and dry etching to form the contact pad. Backside metallization of Al/TaN is performed for the bottom electrode connection. Fig. 1 is a schematic illustration of the complete fabrication process and the corresponding SEM images are depicted in Fig. 2 (a) and (b).

2.2 Electrical Characterization

A High Resolution Transmission Electron Microscopy (HRTEM) image which elucidates the thickness of the HfO$_2$ dielectric to be around 5nm is shown in Fig. 2(c). Backside metal gives an electrical connection for bottom electrode through in-situ silicon. Electrical characterization is

performed in an Agilent 4156C semiconductor parameter analyser. Electrical characterization of the device includes grounding the wafer backside and applying voltage through probe pins to the TE.
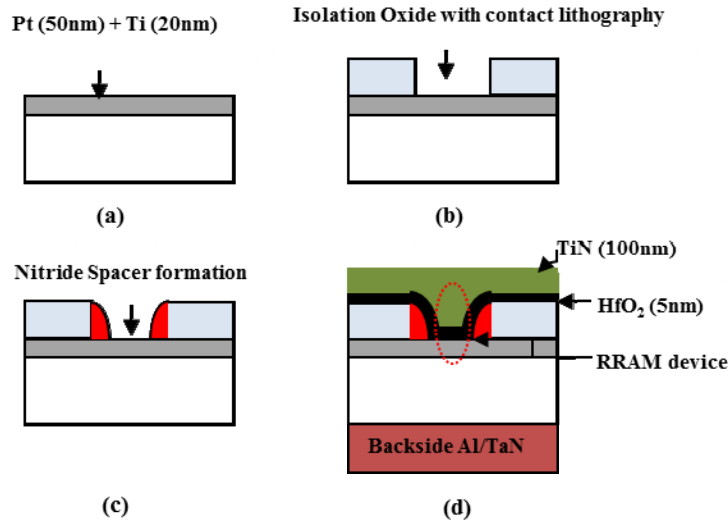

Fig. 1 (a) 50nm Platinum bottom electrode with 20nm Titanium adhesive layer deposited on silicon substrate; (b) Isolation oxide deposition with contact lithography and etch; (c) Nitride spacer formation using self-aligned etch; (d) PVD of HfO2 with TiN top electrode deposition and metal litho followed by backside metallization of Al/TaN.
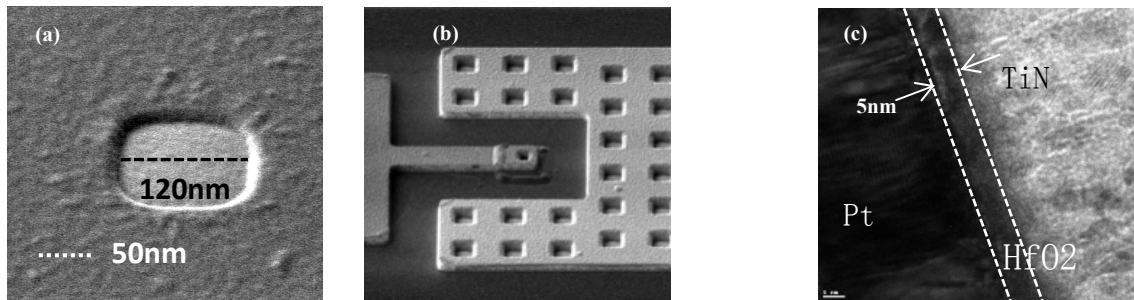

Fig 2: (a) Contact hole formation and hole size reduction (~120nm) after 50nm Nitride spacer formation ; (b) Metal lithography and contact pad formation; (c) HR-TEM image of a larger device showing the RRAM stack.

2.3 Results

Uniform bipolar switching can be observed in the scaled device for 200 DC cycles from Fig. 3(a), after the occurrence of soft-breakdown in a fresh device at 1.5V when using a positive DC voltage sweep. A surge of current is observed in the dielectric between two metal lines and the resistance of the dielectric sharply decreases which can be attributed to the electroforming process. Forming is followed by a series of resistance switching cycles when DC voltage sweeps of opposite polarities are applied alternatively.

The application of negative voltage sweep on the TE after forming the device switches the dielectric from low resistance state (LRS) to a high resistance state (HRS) at -1.25V. We can find a sharp decrease in current and this process is called RESET. Changing the polarity of the sweep switches back the dielectric to a LRS at +0.85V called SET state. The uniformity in switching cycles have been illustrated statistically using Fig. 3(b) and 3(c), where ON and OFF resistance at |0.5V|, reset voltage and set voltage have been plotted against their distribution probability. The ON and OFF resistance at |0.5V| hovers around $10^3\Omega$ and $10^5\Omega$ respectively with reset and set voltages maintaining at -1.25V and +0.85V for 200 DC cycles.

The physical mechanism involved in switching can be explained by a hybrid model involving both filament-formation rupture and REDOX reactions at the electrode-dielectric interface [7]. Locally conductive filaments formed during set process tend to overshoot the current, causing reliability issues. Although compliance current I_{comp} is set to restrict the current during set process, the overshoot can be observed for a very short interval of time which may be sufficient to cause reliability concerns [8-9]. Our scaled devices exhibit a self-compliance set phenomenon in which the current is self-limited by parasitic resistance without overshoot and the filament size is therefore controlled. The corresponding reset current required to eliminate the filament is also reduced [10]. Fig. 3(d) demonstrates this phenomenon in a 120nm device.
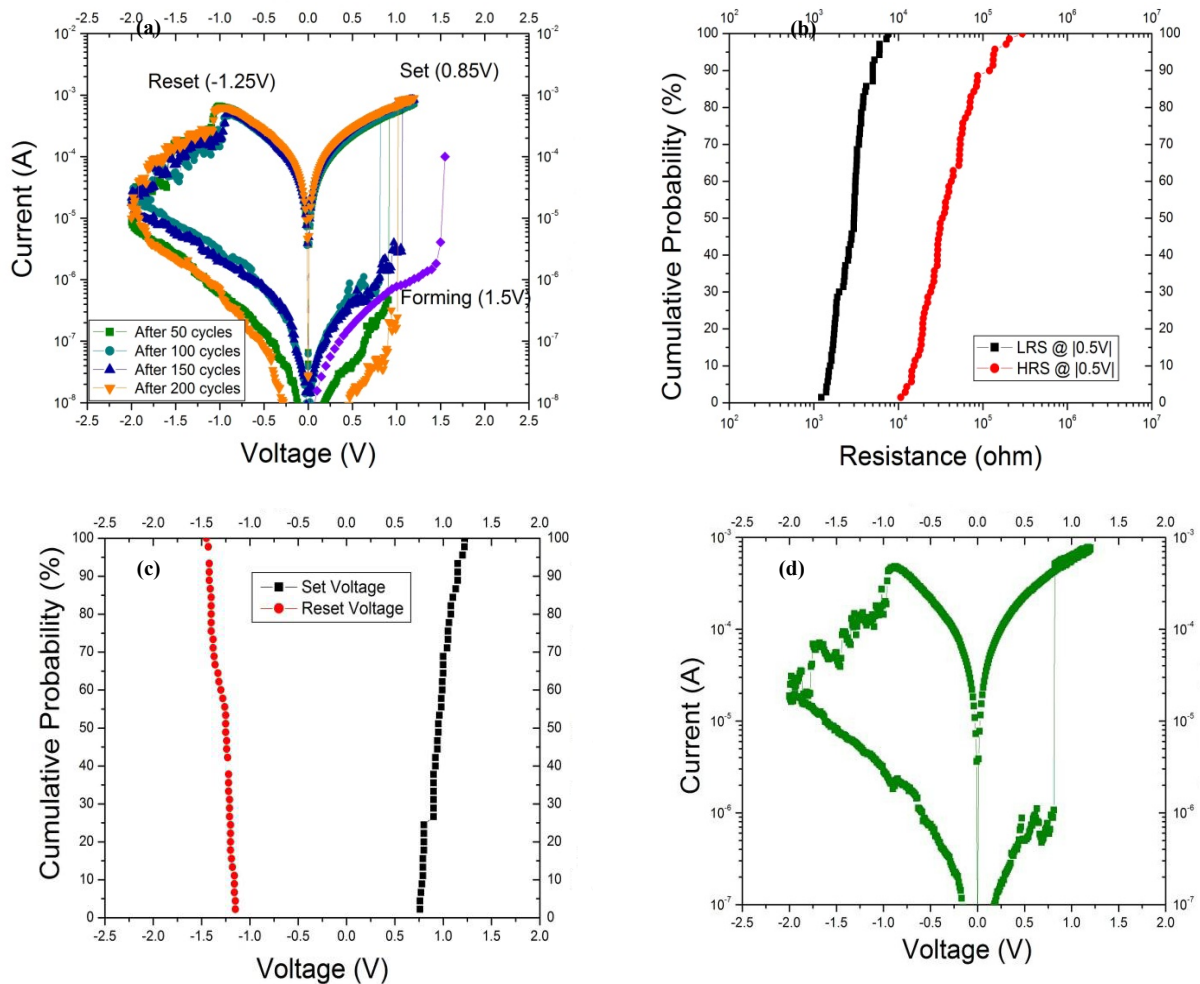

Fig.3: (a) Switching characteristics of a 120nm contact-hole device; (b) Probability distribution of ON and OFF resistance read at 0.5V; (c) Probability distribution of Reset and Set voltage; (d) Self-compliance effect observed during SET at 1.2V for the same device

Further, as the device size is scaled down from 200nm to 60nm, I_{reset} tends to be reduced as presented in Fig. 4(a) where 25 devices from each device-size are sampled. It can be seen that, I_{reset} of the 60nm device is around 100μA as compared to a 200nm device which has a reset current of 2mA. This can be explained by the reduction in the number of locally-formed conductive filaments as the area of the device is reduced. Reset current being a direct function of filament size, tends to get lowered as the device size shrinks [10-12].

Rigorous retention measurements that have been conducted at 85°C for 3000 s confirms the data retention capability of the 120nm scaled device to be similar to the device of larger size. The measurement is performed by reading back the current at |0.5|V after a set and reset process separately. A plot between time and resistance in Fig. 4(b) substantiates 10 years of data retention with a uniform HRS/LRS ratio of 10^2.
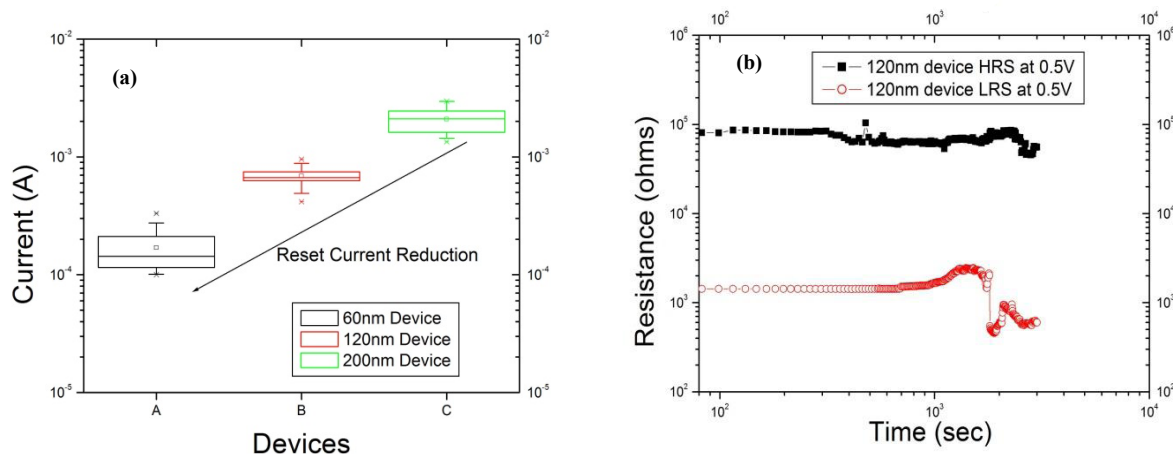

Fig. 4: (a) Box-plot of 25 samples from each devices showing Ireset reduction trend from larger devices to smaller contact-hole devices; (b) Retention characteristics of a 120nm device with HRS/LRS ratio 102.

3. Conclusion

In summary, a uniform bipolar switching RRAM device has been discussed with evidence of device scaling down to 60nm. Self-compliance effect is presented in the scaled devices which eliminate reliability concerns caused by current overshoot during Set programming. Reset current reduction has also been observed as the device size is scaled down. This is of prime importance, for it reduces the power consumption. 1D-1R or 1T-1R integration can be realized using a diode or a transistor as the selection device at the backend of standard CMOS process. The low programming voltage, high endurance and retention characteristics of RRAM demonstrated its high potential to be used in embedded applications like code storage in microcontroller chips.

4. References

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