Hierarchical Approach to "Atomistic" 3-D MOSFET Simulation

Asen Asenov, *Member, IEEE,* Andrew R. Brown, John H. Davies, and Subhash Saini

***Abstract*—We present a hierarchical approach to the "atomistic" simulation of aggressively scaled sub-0.1-μm MOSFET's. These devices are so small that their characteristics depend on the precise location of dopant atoms within them, not just on their average density. A full-scale three-dimensional drift-diffusion atomistic simulation approach is first described and used to verify more economical, but restricted, options. To reduce processor time and memory requirements at high drain voltage, we have developed a self-consistent option based on a solution of the current continuity equation restricted to a thin slab of the channel. This is coupled to the solution of the Poisson equation in the whole simulation domain in the Gummel iteration cycles. The accuracy of this approach is investigated in comparison to the full self-consistent solution. At low drain voltage, a single solution of the nonlinear Poisson equation is sufficient to extract the current with satisfactory accuracy. In this case, the current is calculated by solving the current continuity equation in a drift approximation only, also in a thin slab containing the MOSFET channel. The regions of applicability for the different components of this hierarchical approach are illustrated in example simulations covering the random dopant-induced threshold voltage fluctuations, threshold voltage lowering, threshold voltage asymmetry, and drain current fluctuations.**

***Index Terms*—Deep submicron, device models, modeling, simulation, very large scale integration (VLSI).**

I. Introduction

WHEN MOSFET's are scaled to deep submicron dimensions, the discreteness and randomness of the dopant charges in the channel region start to introduce significant fluctuations in the device characteristics. This effect, predicted 30 years ago [1], [2], has been confirmed recently in several experimental [3]–[7] and simulation studies [8]–[14]. The impact of these fluctuations on the functionality, yield, and reliability of the corresponding systems [15], [16] shifts the paradigm of numerical device simulation. It is no longer sufficient to simulate a single device with a continuous distribution of charge to represent a macroscopic design. Instead, we must perform an "atomistic" simulation, in which the precise location of the dopant atoms is specified. Each device is different at this level of detail, so an ensemble of macroscopically identical but microscopically different devices must be characterized. The aim of numerical simulation, therefore, shifts from predicting the characteristics of a single device with continuous doping toward estimating the mean values and the standard deviations of basic design parameters, such as threshold voltage, subthreshold slope, transconductance, drive current, etc. for the whole ensemble of atomically different devices in the system. It must be emphasized that even the mean values obtained from atomistic simulations are not identical to the values obtained from continuous-doping simulations, [10], [14] and that these differences increase when the devices are scaled further to decanano dimensions [17].

Simulations have shown that fluctuations in MOSFET parameters are not purely a result of a variation in the average doping density associated with a fluctuation in the number of dopants, but also the particular random distribution of dopants in the channel region [14]. This demonstrates the need for full-scale three-dimensional (3-D) atomistic simulations with fine-grain discretization, where the charge associated with each individual dopant is resolved. Thus, the statistical atomistic simulations become essentially a four-dimensional (4-D) problem, where the fourth dimension is the size of the statistical sample. Due to a sheer computational intensity, very few statistical atomistic simulation studies have yet been published. All used a drift-diffusion approximation [10], [13], [14] with only one exception [8]. They typically investigated only a small range of devices with small statistical samples, and aimed mainly to illustrate the atomistic effects. The use of atomistic simulations in the practical design of the next generation of MOSFET's along the Silicon Roadmap [18] requires the development of efficient atomistic simulation strategies.

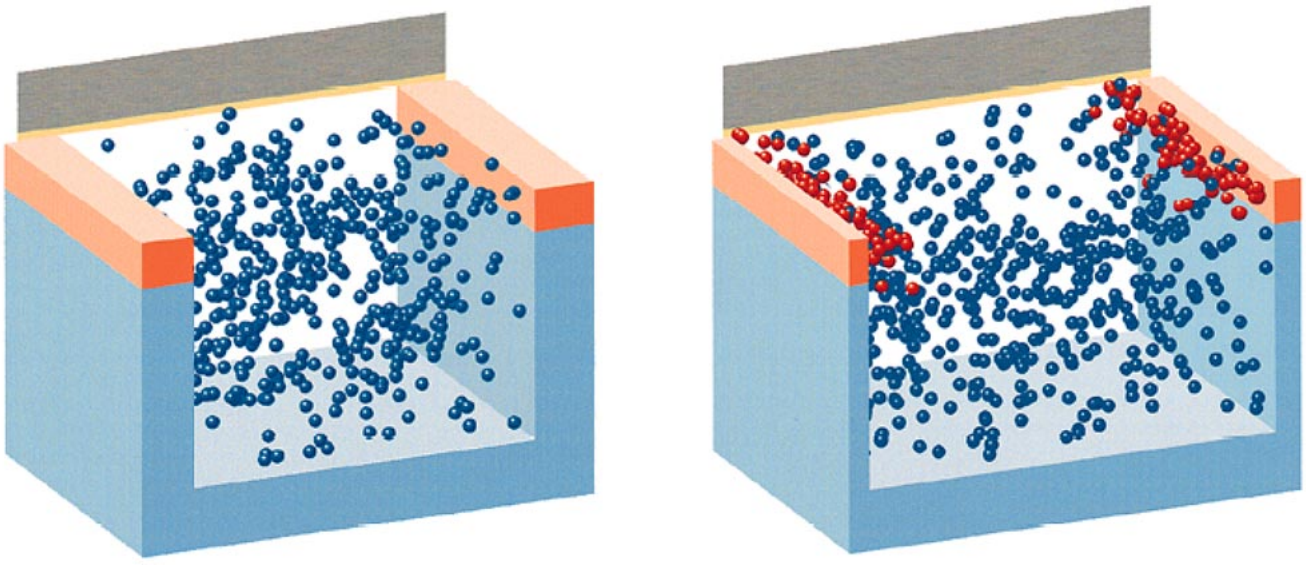
In this paper, we present a hierarchical approach to the atomistic simulation of sub-0.1-μm MOSFET's utilizing a range of strategies to save memory and processor time. In Section II, we introduce the basics of the full-scale 3-D atomistic simulations in the drift-diffusion context, focusing on the choice of solution domain, discretization, doping-charge assignment, and solution techniques. A downscaled version of the full 3-D atomistic solver is described in Section III, where the current continuity equation is solved in a thin slab of silicon engulfing the channel and is coupled to the full 3-D solution of the Poisson equation through a two-dimensional (2-D) extension of the electron quasi-Fermi level. A low drain voltage version based on a single solution of the nonlinear Poisson equation and calculation of the corresponding channel resistivity is described in Section IV. Finally, Section V highlights the applicability of each approach to particular investigations depending on device structure and bias conditions.

Manuscript received April 13, 1999; revised July 2, 1999. This work was supported by NASA under Grant NAG 2-1241. This paper was recommended by Associate Editor Z. Yu.

A. Asenov, A. R. Brown, and J. H. Davies are with the Department of Electronics and Electrical Engineering, The University of Glasgow, Glasgow G12 8LT, Scotland, U.K. (e-mail: a.asenov@elec.gla.ac.uk).

S. Saini is with NASA Ames Research Center, Moffett Field, CA 94035-1000 USA.

Publisher Item Identifier S 0278-0070(99)09474-9.



(a) (b)

Fig. 1. Solution domains in 3-D atomistic MOSFET simulations. (a) Random dopants only in the channel region and (b) random dopants in the channel and in the source/drain regions.

II. Basics of the 3-D Atomistic Simulations

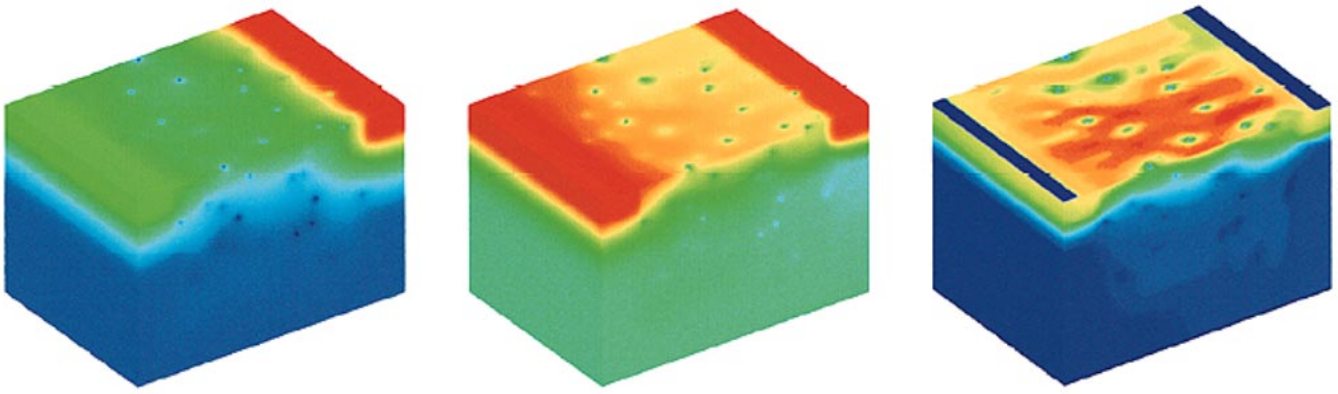
The 3-D atomistic approach to MOSFET simulation described in this section is based on a self-consistent solution of Poisson's equation and the steady-state current continuity equation for the channel carriers in a drift-diffusion approximation. As in the majority of previously published atomistic simulations a constant mobility is assumed. The drift-diffusion approach does not properly represent the nonequilibrium carrier dynamics and the related overshoot effects in short-channel devices and, hence, underestimates the drain current. However, it can be used with confidence to estimate the threshold voltage based on a current criterion. The field in the channel near the source remains low until the threshold current is defined in the subthreshold region, and overshoot does not significantly affect the current. At the same time, since the subthreshold current is exponentially controlled by the gate, its underestimation produces a minute error in the calculated value for the threshold voltage. Although the above threshold drift-diffusion approach underestimates the drive current and the transconductance [19], it can still be used to evaluate their percentage variation associated with the electrostatic influence of the randomly distributed dopants and their screening from the channel charge.

Quantum-mechanical effects in the inversion layer are not yet included within this atomistic drift-diffusion picture. To estimate their scale, the wavefunction of the lowest quantized state extends about 5 nm from the Si–SiO_2 interface. This becomes a significant fraction of the depletion depth and channel length in a small, highly doped device and we, therefore, plan to include quantum-mechanical effects in future.

A typical solution domain, used in this and also in most of the previously reported atomistic MOSFET simulations [10], [14], is shown in Fig. 1(a). The discrete dopants are placed in the outlined channel region between the source and drain. In the rest of the simulation domain, the doping charge has a continuous distribution. Although the best way to introduce the doping distributions in the atomistic simulations will be to use the output from an atomic scale process simulator [20], here we apply a simpler approach. The expected number of dopants in the atomistic region is estimated by integrating the continuous-doping distribution, obtained for example from a standard process simulator. The actual number of dopants in each MOSFET from the simulated ensemble is chosen randomly from a Poisson distribution with the above mean. Then, using a rejection technique, the dopants are placed randomly according to the initial continuous-doping distribution. The atomistic region can be extended to incorporate part of the source and drain pn junctions, as shown in Fig. 1(b). In this figure, similar to Fig. 1(a), uniform doping is used to generate the random dopants in the channel region but the impurities in the source and drain region follow a 2-D Gaussian distribution. The atomistic picture destroys the concept of a metallurgical pn junction in decanano devices. Although there are indications that the fluctuations in the MOSFET parameters are dominated by the randomness of dopants in the *middle* of the channel [14], atomistic doping in the source and drain will introduce fluctuations in the effective length of the channel, even for a perfectly defined gate pattern.

A uniform grid with small step size h (typically 1 nm) is used in the discretization of the Poisson and current continuity equations in order to uniformly resolve the Coulomb potential associated with each doping atom. This results, for example, in a grid with $51 \times 51 \times 71 = 184\,671$ nodes to simulate a MOSFET with $W_{\text{eff}} = L_{\text{eff}} = 50$ nm. The number of nodes increases by a factor of ten for a device with the same channel length, but with $W_{\text{eff}} = 500$ nm. The random dopants are assigned to the nearest grid node by introducing a local doping density $1/h^3$.

The coupled Poisson and current-continuity equations are solved by Gummel iterations [21]. The nonlinear Poisson solver, employing a one step Newton-SOR scheme, occupies



(a) (b) (c)

Fig. 2. Typical results of 3-D atomistic simulation for a MOSFET with $W_{\text{eff}} = L_{\text{eff}} = 50$ nm, $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm. The bias conditions are $V_D = 1$ V and $V_G = 0.7$ V. (a) Potential, (b) electron concentration, and (c) current density.

a minimum amount of memory. Only two arrays with dimensions equal to the grid size, one for the potential and one for the doping, are associated with the solver. Due to the simple seven-point discretization star, all matrix coefficient are calculated on the fly. The black/red ordering in updating the potential makes the Newton-SOR method inherently parallelizable [22]. The 3-D solution of the current-continuity equation, however, significantly increases the memory requirement. The use of expensive Bernoulli functions in the Sharfetter–Gummel discretization scheme [23] and more complex mobility models requires all seven diagonals of the discretization matrix to be stored. The use of a BiCGSTAB solver for solving the corresponding nonsymmetrical and nondiagonally dominant linear system introduces 13 additional arrays with dimensions equal to the grid size. The option of polynomial preconditioning [24] is provided as this retains the parallel scalability of the BiCGSTAB solver.

Fig. 2(a)–(c) illustrates the potential distribution, electron concentration, and current density in an n-channel MOSFET with $W_{\text{eff}} = L_{\text{eff}} = 50$ nm, uniform doping in the channel region $N_A = 5 \times 10^{18}$ cm^{-3}, oxide thickness $t_{ox} = 3$ nm, and junction depth $x_j = 7$ nm. The random dopants have the distribution shown in Fig. 1(a). The gate and drain voltages $V_G = 0.7$ V and $V_D = 1$ V correspond to the pinch-off condition. The current flows through valleys determined by the pattern of the random dopants.

The size of the statistical sample is equivalent to a fourth dimension in atomistic simulations, and a small sample leads to errors in our estimates of the statistics for the population. Let σ be the standard deviation of an electrical parameter of interest over the population. The standard deviation in the estimate of the mean from a sample of size N is then $\sigma/\sqrt{N}$. Similarly, the estimate of the standard deviation itself has a standard deviation of $\sigma/\sqrt{2N}$, which can be kept between 10% and 5% if N lies between 50 and 200. This is comparable to the typical number of nodes in one spatial dimension of the simulation domain.

III. Economic Self-Consistent Option

The computing power typically available today is still limiting for the use of full-scale 3-D atomistic statistical simulations in a practical MOSFET design, even in a drift-diffusion context. An efficient approach to reduce both the simulation time and the memory requirement in the atomistic simulations is to solve the current continuity equation in only a thin slab extending from the interface to a depth d, much smaller than the total depth of the solution domain. Neumann boundary conditions for the current are applied at the top (the Si/SiO_2 interface) and at the bottom surfaces of the slab. After solving the current continuity equation in the slab, during each Gummel iteration, the 2-D quasi-Fermi level distribution calculated at the bottom surface of the slab is extended to the bottom of the whole solution domain. In such a way the current-continuity equation is properly coupled to Poisson's equation, which is solved in the whole solution domain.

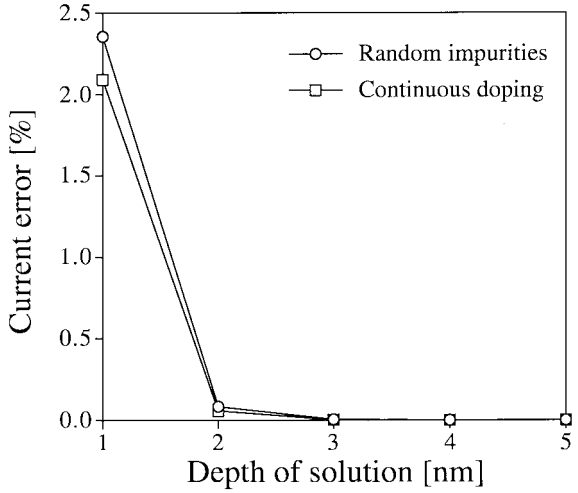


Fig. 3. Percentage error in the current calculated using a slab solution of the current-continuity equation, compared to the full 3-D solution, as a function of the slab thickness. The two sets of data correspond to discrete and continuous-doping distributions in a 50×50 nm MOSFET with $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm. The applied voltages are $V_D = 1$ V and $V_G = 0.7$ V.

The percentage error in the current calculated using this economic option, in comparison with the results from a full 3-D solution, is plotted in Fig. 3 as a function of the thickness of the slab. The two sets of data correspond to two 50×50 nm

TABLE I
THRESHOLD VOLTAGE STANDARD DEVIATION σV_T CALCULATED USING FULL 3-D AND A SLAB SOLUTION AT $V_D = 1$ V

	Full 3D	Slab with thickness	
		1 nm	3 nm
σV_T [mV]	60.9	60.6	60.9

MOSFET's with discrete and continuous-doping, respectively. Both devices have identical structure with constant doping concentration in the channel region $N_A = 5 \times 10^{18}$ cm^{-3}, oxide thickness $t_{ox} = 3$ nm, and junction depth $x_j = 7$ nm. The comparison is made at drain voltage $V_D = 1$ V and gate voltages corresponding to current 10^{-8} A, chosen according to the current criterion $10^{-8} W_{\text{eff}}/L_{\text{eff}}$ [A] used throughout in this paper to estimate the threshold voltage. The error in the current calculated from a slab solution for both MOSFET's is less than 3% for a slab of 1 nm thickness and decreases to less than 0.1% for a 3 nm slab. Samples of 200 MOSFET's with the above macroscopic structure are used to compare in Table I the threshold voltage standard deviation σV_T obtained from a full 3-D solution and slab solutions with different thicknesses at drain voltage $V_D = 1$ V. The difference between the full 3-D result and the result from a slab with thickness 1 nm is less than the 5% statistical error determined by the sample size.

In general, there is no difference between the number of Gummel iterations needed for the full 3-D solution and the slab solution to converge using the same convergence criterion. Thus, the saving in computational time comes from the difference between the full 3-D and the slab solution of the current continuity equation, which is approximately equal to the ratio between the total depth of the solution domain and the thickness of the slab. The use of a slab solution also dramatically reduces the memory requirement for the current-continuity equation from 20 arrays (seven for discretization and 13 for BiCGSTAB solver) with grid size dimensions to typically less than the equivalent storage requirements of only one array with the grid size. The advantages of this reduction are threefold. The simulations can be farmed on all available computers without significantly disturbing their interactive use. It also becomes possible to hold a substantial part of the simulation in the Level-2 cache of some platforms, speeding up the simulations significantly. Finally, large solution domains with fine-grain grids and millions of nodes can be used in the atomistic simulations without paging which, otherwise, dramatically reduces the speed of computation.

It must be pointed out, however, that the thin slab solution works well only if the MOSFET is properly scaled and the current flows predominantly in the channel along the interface. If the behavior of the MOSFET is dominated by drain-induced barrier lowering (DIBL), the slab solution becomes less accurate and efficient. Fig. 4 shows a comparison of I_D-V_G characteristics calculated using a 1-nm slab solution and a full 3-D solution for the atomistic MOSFET from the previous examples and for a poorly scaled device with the same dimensions but a doping concentration in the channel of $N_A = 1 \times 10^{17}$ cm^{-3}. The comparison is carried out at drain voltage $V_D = 1$ V. The slab solution significantly underestimates the current in the second device, where it flows predominantly below the interface due to DIBL. The percentage difference between the slab and the full 3-D solution for the second MOSFET is plotted in Fig. 5 as a function of the slab size. A slab with thickness 16 nm is necessary to bring the error below the 1% margin. This does not undermine the importance of the economic slab solution in the atomistic simulations, which can be used to study the doping-induced fluctuations after the proper scaling of the devices of interest. In many cases, the scaling can be done using 2-D simulations and the corresponding computing time is negligible compared to the time needed for the atomistic simulations.

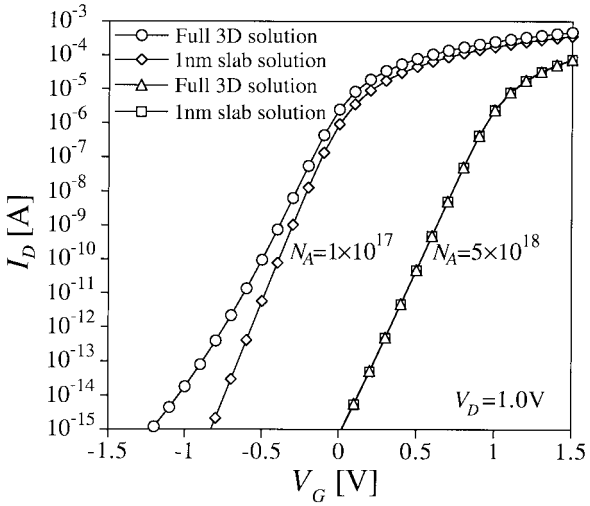


Fig. 4. I_D–V_G characteristics of two atomistic 50 × 50 nm MOSFET's with $t_{ox} = 3$ nm, $x_j = 7$ nm, and channel doping $N_A = 1 \times 10^{17}$ cm^{-3} and 5×10^{18} cm^{-3}, respectively, calculated at $V_D = 1$ V using 1-nm slab solution and a full 3-D solution.

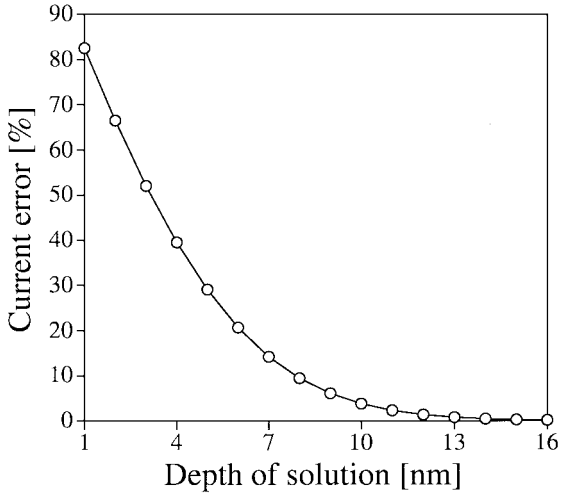


Fig. 5. Error in the current calculated using a slab solution of the current-continuity equation as a function of the slab thickness for a poorly scaled 50 × 50 nm MOSFET with $N_A = 1 \times 10^{17}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm. The applied voltages are $V_D = 1$ V and $V_G = 0.7$ V.

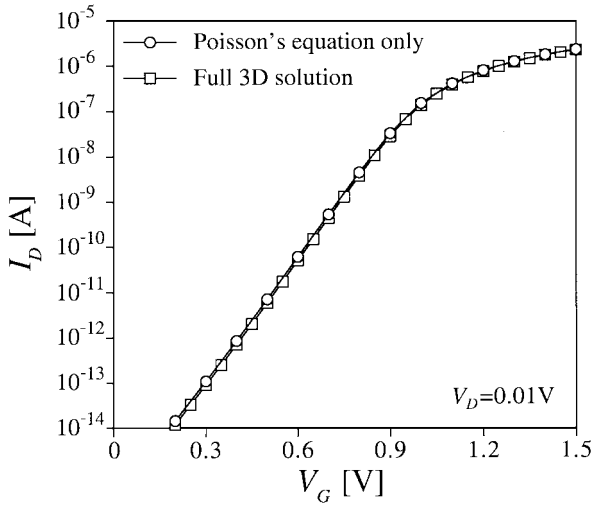


Fig. 6. I_D–V_G characteristics for a 50×50 nm MOSFET with $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm, calculated at $V_D = 10$ mV using a full 3-D self-consistent solution and a single Poisson solution.

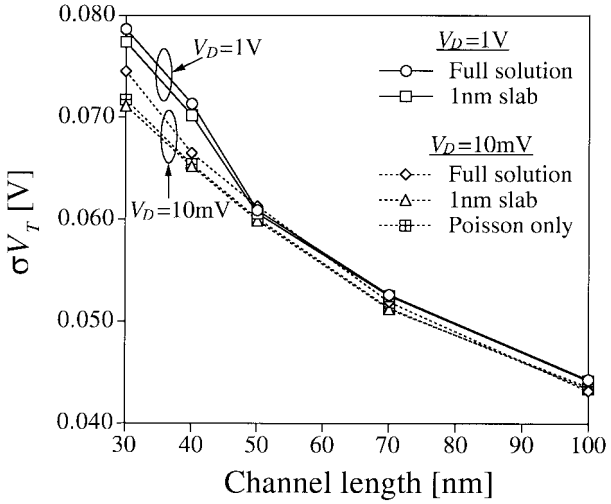


Fig. 7. Standard deviations in the threshold voltage σV_T, as a function of the channel length calculated using FSS, SSS, and PSO, at $V_D = 1$ V and $V_D = 10$ mV for MOSFET's with $W_{\text{eff}} = 50$ nm, $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm.

TABLE II
THRESHOLD VOLTAGE STANDARD DEVIATION σV_T CALCULATED USING FULL 3-D, SLAB, AND POISSON SOLUTION ONLY AT $V_D = 10$ mV

	Full 3D	1 nm Slab	Poisson solution only
σV_T [mV]	61.3	59.9	60.1

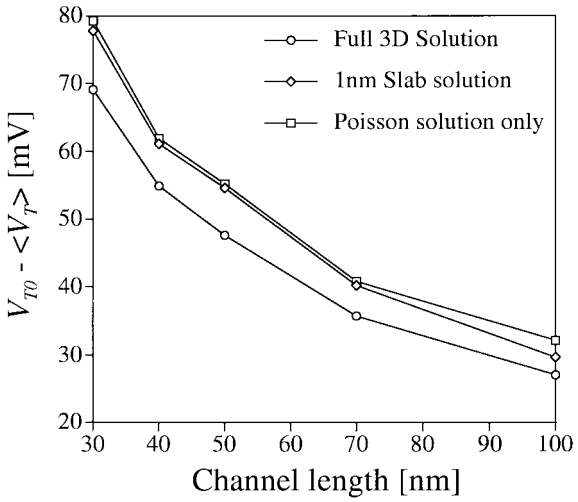


Fig. 8. The threshold voltage lowering, $V_{T0} - \langle V_T \rangle$, as a function of the effective channel length calculated using FSS, SSS, and PSO at $V_D = 10$ mV, for MOSFET's with $W_{\text{eff}} = 50$ nm, $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm.

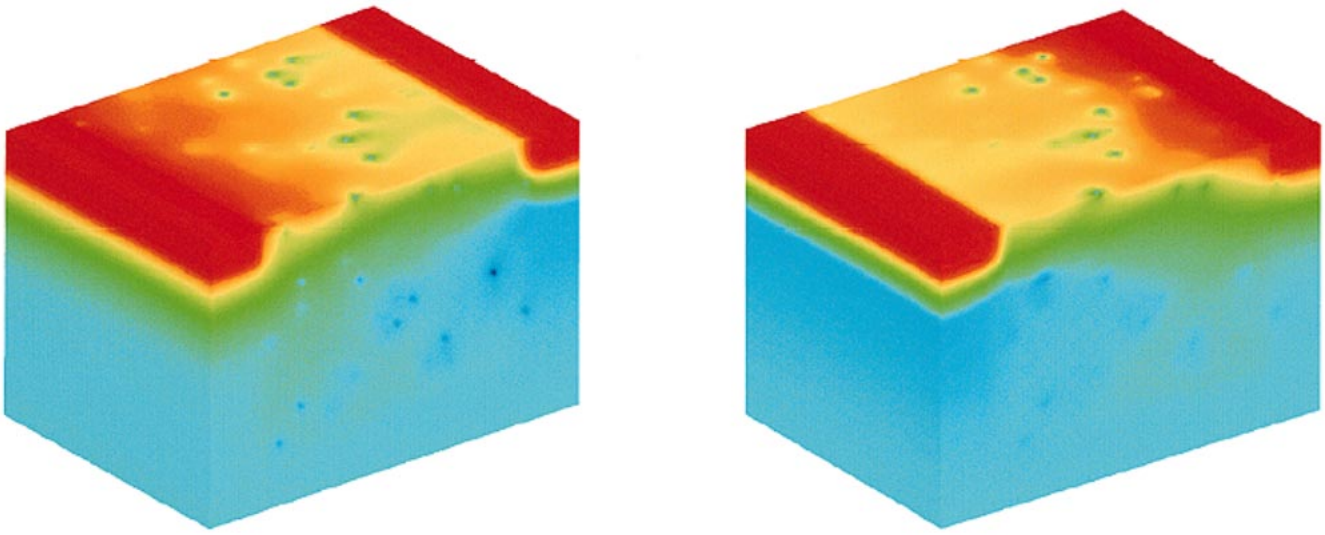
IV. SINGLE POISSON SOLUTION OPTION

At low drain voltage V_D, the current in the atomistic simulations can be estimated with sufficient accuracy by a single solution of the nonlinear Poisson equation. The solution for a particular gate voltage V_G is carried out for a zero-potential difference between the source and the drain. The carrier concentration obtained from this solution is used for calculating the resistance of the device and, hence, the current. This is done by solving the current-continuity equation in a drift-only-approximation $\nabla \cdot \mu_n n \nabla V = 0$, where V is the voltage driving the current, μ_n is the mobility, and n is the carrier concentration. Similar to Section III, the solution domain for a properly scaled MOSFET can be a thin slab extending from the Si/SiO_2 interface to several nanometers in the silicon. Neumann boundary conditions for V are applied at the top and bottom surfaces of the slab. At the source and drain contacts, $V = 0$ and $V = V_D$, respectively. The current is calculated by integrating the drift current density $J_n = \mu_n n \nabla V$ along an arbitrary cross section of the solution domain. The previously described BiCGSTAB solver is used to solve the modified current-continuity equation. The memory requirements for the single Poisson solution option are similar to the memory requirements for the slab self-consistent solution. The computing time, however, is equivalent to the computing time for a single Gummel iteration.

The I_D–V_G characteristics for a 50×50 nm MOSFET with doping in the channel region $N_A = 5 \times 10^{18}$ cm^{-3}, oxide thickness $t_{ox} = 3$ nm, and junction depth $x_j = 7$ nm, calculated at $V_D = 10$ mV using a full 3-D self-consistent solution and a single Poisson solution, are compared in Fig. 6. The standard deviations in the threshold voltage σV_T calculated at $V_D = 10$ mV using the full solution, 1-nm slab solution and Poisson solution only are compared in Table II for a sample of 200 devices. Although there is a small discrepancy in the subthreshold current, the agreement in the standard deviations between the full 3-D self-consistent solution and the single Poisson solution is remarkably good.

V. APPLICATIONS

The hierarchy in the atomistic simulation techniques described in the previous sections can be used to save computing time in studying various aspects of the fluctuations in MOSFET parameters induced by the random dopants and in the design of devices resistant to such fluctuations. One of the



(a) (b)

Fig. 9. Electron concentration at threshold voltage for a 50×50 nm MOSFET with $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm. (a) $V_D = 1$ V applied at the right source/drain contact ($VT = 0.67$ V) and (b) $V_D = 1$ V applied at the left source/drain contact ($V_T = 0.80$ V).

major and most frequently studied parameters affected by the fluctuations in number and position of the dopants is the threshold voltage [9]–[14]. The standard deviations in the threshold σV_T calculated using a full self-consistent solution (FSS), slab self-consistent solution (SSS), and Poisson solution only (PSO) are compared in Fig. 7 for a range of MOSFET's with channel width $W_{\text{eff}} = 50$ nm and different channel lengths. Similar to the previous examples, the device has doping concentration in the channel region $N_A = 5 \times 10^{18}$ cm^{-3}, oxide thickness $t_{ox} = 3$ nm, and junction depth $x_j = 7$ nm. The agreement between FSS and PSO at low drain voltage is remarkably good over the whole range of channel lengths. The high drain voltage increases σV_T but the difference from the results at low drain voltage is small for the properly scaled devices down to 50 nm. The discrepancy increases below 50 nm when the drain depletion region becomes comparable to the channel length and requires SSS.

The discreteness and randomness of the doping typically results in an average threshold voltage $\langle V_T \rangle$, which is lower than the corresponding threshold voltage V_{T0}, for continuous-charge simulations [10], [14]. The threshold-voltage-lowering $V_{T0} - \langle V_T \rangle$, as a function of the effective channel length, calculated using FSS, SSS, and PSO, is compared in Fig. 8 for the set of devices from the previous figure. In general, FSS predicts less threshold-voltage-lowering compared to SSS and PSO. The discrepancy increases at shorter channel lengths but remains within the 15% margin.

The above results lead to the conclusion that PSO can be used confidently to estimate both the lowering and fluctuations induced in the threshold voltage by random dopants in properly scaled MOSFET's. Conventional continuous charge simulators are recommended to optimize the initial device and suppress the short-channel effects in order to ensure applicability of the PSO.

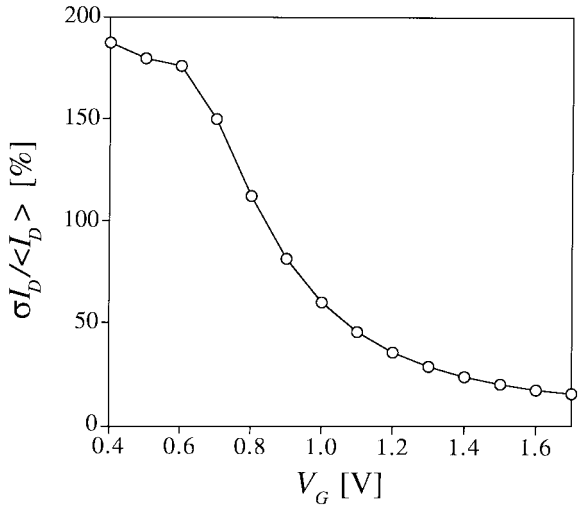


Fig. 10. Percentage drain current fluctuations as a function of the gate voltage calculated at $V_D = 1$ V for a 50×50 nm MOSFET with $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm.

A phenomenon which cannot be studied using PSO, but for which SSS or FSS is essential, is the asymmetry induced in the MOSFET characteristics by the random dopants at high drain voltage, pointed out in [10] but not studied in further detail. Fig. 9 illustrates the origin of this effect, comparing the electron concentrations at threshold voltage for a 50×50 nm MOSFET with 1 V applied first at one of the source/drain contacts and then at the second one. The device structure is the same as in the previous example. The corresponding values of the threshold voltage are $V_{T1} = 0.67$ V and $V_{T2} = 0.80$ V, respectively, giving rise to a difference in the threshold voltage $\Delta V_T = 0.13$ V. This is the worst case in a sample of 200 microscopically different MOSFET's. The strong asymmetry

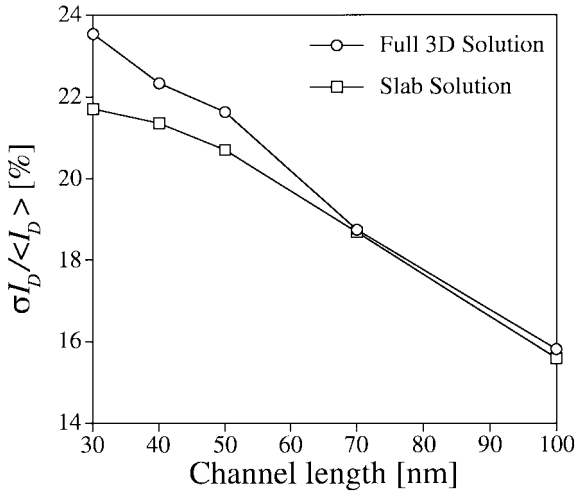


Fig. 11. Percentage fluctuation in the drain current as a function of the channel length, calculated using SSS and FSS at $V_G = (V_T + 0.7)$ V and $V_D = 1$ V for a MOSFET with $N_A = 5 \times 10^{18}$ cm^{-3}, $t_{ox} = 3$ nm, and $x_j = 7$ nm.

is related to the grouping of the dopants closer to one of the source/drain contacts. The average asymmetry for the whole sample is $\langle|\Delta V_T|\rangle = 32$ mV with standard deviation $\sigma_{\Delta V_T} = 25$ mV.

As pointed out in Section II, the drift-diffusion approach will underestimate the drain current in sub-0.1-μm MOSFET's, but SSS or FSS can be used to estimate the relative fluctuations in the drain current at normal working conditions. The percentage drain current fluctuations, for our example 50×50 nm MOSFET, are plotted in Fig. 10 as a function of the gate voltage for drain voltage $V_D = 1$ V. The fluctuations are more pronounced in the subthreshold region and near threshold. They reduce for gate voltages above the threshold, where the inversion layer charge more efficiently screens the charge of the random dopants. The percentage fluctuation in the drain current, calculated using SSS and FSS at $V_G = (V_T + 0.7)$ V and $V_D = 1$ V is plotted in Fig. 11 as a function of the channel length. As can be expected the results from SSS and FSS agree well for the properly scaled MOSFET's with channel length above 70 nm but some discrepancy is already apparent at the 50 nm device. The discrepancies however do not exceed 10% for the whole range of simulated devices.

VI. Conclusions

The need to simulate an ensemble of atomically different devices, instead of a single device with a continuous charge density, is inescapable as MOSFET's are scaled to deep submicron dimensions. Such simulations are extremely intensive in processor time and memory, requiring a 3-D solution domain with fine grain discretization. Large samples of microscopically different devices must be simulated for the statistical evaluation of the means and standard deviations of the MOSFET's parameters, effectively transforming the problem into a 4-D one.

To reduce the computational burden of the atomistic simulation we have developed a hierarchical simulation strategy. At high drain voltage the processor time and memory requirement can be reduced by restricting the solution of the current-continuity equation, during each Gummel cycle, to a slab whose thickness is comparable to that of the channel-inversion layer. At low drain voltage substantial savings can be made by solving the nonlinear Poisson equation only once, and calculating the current from the carrier concentration in the channel by solving the current continuity equation in a drift-only approximation.

The "Poisson solution only" method can be used with confidence at low drain voltages for evaluating the fluctuations and lowering induced by random dopants in the threshold voltage of properly scaled MOSFET's. Similarly, the slab self-consistent solution can be used with confidence for evaluating the threshold voltage asymmetry and the drain current fluctuations in properly scaled devices. If, however, the behavior of the device is dominated by DIBL effects, a full self-consistent atomistic solution is required.

References

[1] B. Hoeneisen and C. A. Mad, "Fundamental limitations in microelectronics-I, MOS technology," *Solid-State Electron.*, vol. 15, pp. 819–829, 1972.

[2] R. W. Keys, "Physical limits in digital electronics," *Proc. IEEE*, vol. 63, pp. 740–766. 1975.

[3] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 2216–2221, 1994.

[4] M. Steyaert, J. Bastos, R. Roovers, P. Kinget, W. Sansen, B. Graindourse, A. Pergot, and E. Janssens, "Threshold voltage mismatch in short-channel MOS transistors," *Electron. Lett*, vol. 30, pp. 1546–1548, 1994.

[5] J. T. Horstmann, U. Hilleringmann, and K. F. Goser, "Matching analysis of deposition defined 50-nm MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 299–306, 1997.

[6] C. G. Linnenbank, W. Weber, U. Kolmer, B. Holzapfl, S. Sauter, U. Achaper, R. Brederlow, S. Cyrusian, S. Kessel, R. Heinrich, E. Hoefig, G. Knobinger, A. Hesener, and R. Thewes, "What do matching results of medium area MOSFET's reveal for large area devices in typical analogue applications," in *Proc. ESSDERC'98*, G. Bakarani, M. Rudan, Eds., pp. 104–107.

[7] O. R. dit Buisson and G. Morin, "MOSFET matching in deep submicron technology," in *Proc. ESSDERC'96*, G. Bakarani, M. Rudan, Eds., pp. 731–734.

[8] J.-R. Zhou and D. K. Ferry, "Three-dimensional simulation of the effect of random dopant distribution on conductance for deep submicron devices," in *Proc. 3rd Int. Workshop Computational Electronics*, 1994, pp. 74–77.

[9] K. Nishiohara, N. Shiguo, and T. Wada, "Effects of mesoscopic fluctuations in dopant distributions on MOSFET threshold voltage," *IEEE Trans. Electron Devices*, vol. 39, pp. 634–639, 1992.

[10] H.-S. Wong and Y. Taur, "Three dimensional 'atomistic' simulation of discrete random dopant distribution effects in sub-0.1 μm MOSFET's," in *Proc. IEDM'93. Dig. Tech. Papers*, pp. 705–708.

[11] V. K. De, X. Tang, and D. J. Meindl, "Random MOSFET parameter fluctuation limits to gigascale integration (GSI)," in *Tech. Dig., VLSI Symp.'96*, pp. 198–199.

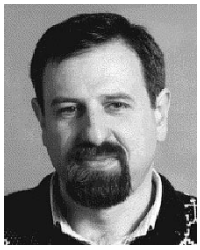
[12] P. A. Stolk, F. P. Widdershoven, and D. B. M. Klaassen, "Modeling statistical dopant fluctuations in MOS Transistors," *IEEE Trans. Electron Devices*, vol. 45, pp. 1960–1971, 1998.

[13] D. Vasileska, W. J. Gross, and D. K. Ferry, "Modeling of deep-submicrometer MOSFETs: Random impurity effects, threshold voltage shifts and gate capacitance attenuation," in Extended abstracts IWCE-6, Osaka, Japan, 1998, *IEEE Cat. No. 98EX116*, pp. 259–262.

[14] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 0.1 μm MOSFETs: A 3-D 'atomistic' simulation study," *IEEE Trans. Electron Devices*, vol. 45, pp. 2505–2513, 1998.

[15] M. Eisele, J. Berthold, R. Thewes, E. Wohlrabh, D. Schmitt-Landsiedel, and W. Weber, "Intra-die device parameter variations and their impact

on digital CMOS gates at low supply voltages," in *IEDM Tech Dig.*, 1995, pp. 67–70.
[16] D. Burnett, K. Erington, C. Subramanian, and K. Baker, "Implications of fundamental threshold voltage variations for high density SRAM and logic circuits," in *Tech. Dig. VLSI Simp.'94*, pp. 15–16.
[17] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub 50 nm MOSFETs: A 3-D 'atomistic' simulation study," *Nanotechnology*. In press.
[18] *The National Technology Road-Map for Semiconductors*. San Jose, CA: Semiconductor Ind. Assoc., 1997; revision.
[19] B. Meinerzhagen and W. L. Engl, "The influence of the thermal equilibrium approximation on the accuracy of classical two-dimensional numerical modeling of silicon submicrometer MOS transistors," *IEEE Trans. Electron Devices*, vol. 35, pp. 689–697, 1988.
[20] G. H. Gilmer, L. Palaz, C. Rafferty, and M. Jaraiz, "Multiscale modeling of the implantation and anealing of silicon devices," in *Simulation of Semiconductor Processes and Devices*, K. De Meyer, S. Biesemans, Eds. Vienna, Austria: Springer-Verlag, 1998, pp. 46–48.
[21] H. K. Gummel, "A self-consistent iterative scheme for one-dimensional steady state transistor calculations," *IEEE Trans. Electron Devices*, vol. 11, pp. 455–465, 1964
[22] A. Asenov, J. R. Barker, A. R. Brown, and G. L. Lee, "Scalable parallel 3-D finite element nonlinear Poisson solver," *J. Simulation Practice Theory*, vol. 4, pp. 155–168, 1996
[23] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Vienna, Austria: Springer-Verlag, 1984
[24] A. Asenov, A. R. Brown, and S. Roy, "Parallel semiconductor device simulation: from power to atomistic devices," in Extended abstracts IWCE-6, Osaka, Japan, 1998, *IEEE Cat. No. 98EX116*, pp. 58–61.



Asen Asenov (M'96) received the M.Sc. degree in solid state physics from Sofia University, Bulgaria, in 1979 and Ph.D. degree in physics from The Bulgarian Academy of Science in 1989.

He had ten years industrial experience as a head of the Process and Device Modeling Group in IME-Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. In 1989–1991 he was a Visiting Professor at the Physics Department, Technische Universität, Munich, Germany. He is currently Head of Department of Electronics and Electrical Engineering at the University of Glasgow, Glasgow, Scotland. As a leader of the Device Modeling Group and Academic Director of the Process and Device Simulation Centre, he also coordinates the development of 2-D and 3-D device simulators and their application in the design of FET's, SiGe MOSFET's, and IGBT's. He has over 130 publications in process and device modeling and simulation, semiconductor device physics, 'atomistic' effects in ultra-small devices, and parallel computing.

Andrew R. Brown received the B.Eng degree in electronics and electrical engineering from the University of Glasgow, Glasgow, Scotland, in 1992.

Since this time he has employed in the Electrical Engineering Department at the University of Glasgow working on the development of parallel 3-D simulators for semiconductor devices. He is currently developing a parallel 3-D 'atomistic' simulator to investigate random dopant induced parameter fluctuations in sub-0.1 micron MOSFET's. His previous work includes the simulation of IGBT's. His interests include high-performance parallel computing and device modeling and visualization.

John H. Davies received the Ph.D. degree from the University of Cambridge, Cambridge, U.K., in 1982 for theoretical work on the electronic properties of amorphous semiconductors.

He was a Research Fellow at Cornell University before coming to Glasgow University, Glasgow, Scotland, in 1986, and has since spent two periods of leave at Ohio State University, Columbus, and the University of California at Santa Barbara. Most of his research is centered on the physics of transport in III-V heterostructures. This has included the modeling of surfaces and gates, including the effect of stress from patterned surfaces and gates. He has been interested in the effect of discrete random donors for many years, and previous research showed their destructive effect on quantum transport in ballistic devices at low temperature. His other interests include the theory of resonant tunneling, conduction in lateral superlattices, and the calculation of magnetic fields in permanent-magnet motors.

Subhash Saini received the Ph.D. degree from the University of Southern California, Los Angeles.

He has held positions at University of California at Los Angeles, University of California at Berkeley, and Lawrence Livermore National Laboratory, Livermore. He has more than ten years experience of teaching physics at B.S. (Hons) and M.S. level. His research interests involve performance evaluation and modeling of new generation of CMOS-based processors and highly parallel computers. He has published over 80 technical papers in nuclear engineering, quantum scattering, nanotechnology, high-temperature materials, operating systems, computer architectures, and performance modeling of high-end computers. He has presented over 100 technical talks. He joined NAS in 1989 and he was named the NAS-NASA employee of the year in 1991. Currently, he is Manager of a department at NASA Ames Research Center which includes several groups such as information systems performance modeling; algorithms, architectures, and application; information power grid architectures; legacy codes modernization; higher level languages; nanotechnology; and device modeling.