

Hierarchical Model Predictive Control of Grid-Connected Cascaded Multilevel Inverter

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Abstract—This article presents a hierarchical finite-set model predictive control (MPC) scheme to enable autonomous operation and self-balancing cascaded multilevel inverter. The proposed approach is an alternative to MPC scheme based on a generic cost function, which in some applications is ill fit or challenging to design. The proposed controller has a hierarchical framework to eliminate the overall cost function optimization and associated weight factor design stage of the control objectives. The control formulation approach allows for multiobjective optimization with a cost-tolerance framework. The concept is well suited to simplify the control design stage of cascaded H-bridge inverters at the grid-edge with advanced functionality. The control scheme achieves active and reactive power control with switching event reduction while equalizing power draw from the independent voltage sources. The latter of these objectives is made possible by the proposed hierarchical approach to the control objective tracking. The control is modularized for each phase, making the system robust to unbalanced grid conditions. The concept is explained in depth in simulation, and then tested experimentally on hardware.

Index Terms—Cascaded multilevel inverter (CMI), model predictive control (MPC), smart inverters.

I. INTRODUCTION

MULTILEVEL converters are a long-studied and widely accepted class of power converters. When compared to two-level converter topologies, multilevel topologies exhibit improved harmonic content of the output voltage waveform, reducing either the necessary switching frequency or output filtering requirements, and reduced common-mode voltage [1], [2]. They are often proposed in high-power applications, as the increased number of series connected semiconductor switches increases the voltage rating of the converter [3].

Manuscript received March 14, 2020; revised May 20, 2020 and June 25, 2020; accepted July 23, 2020. Date of publication August 10, 2020; date of current version May 28, 2021. This work was supported by the Qatar National Research Fund (a member of the Qatar Foundation) (autonomous operation and self-balancing cascaded multilevel inverter) under Grant #NPRP 12S-0226-190158. The statement made herein is solely the responsibility of the authors. Recommended for publication by Associate Editor Josep Pou. (Corresponding author: Mohammad B. Shadmand.)

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Digital Object Identifier 10.1109/JESTPE.2020.3015128

Among these, the cascaded multilevel inverter (CMI) consists of series connected H-bridges, and was first proposed in [4]. The modularity of the CMI deems it more reliable and capable of fault-tolerant operation than other multilevel topologies such as the neutral point clamped inverter and flying capacitor inverter. The CMI topology has been proposed for a wide range of applications, including photovoltaic inverters [5], motor drives [6], and static VAR compensators [7]. Traditional control techniques for the CMI incorporate linear controllers and pulsewidth modulation (PWM) switching technique such as phase-shifted PWM, space-vector PWM, and subharmonic multilevel PWM [8], [9]. In general, linear controllers lack the fast dynamic response that can be realized with modern, computationally extensive control techniques. Furthermore, incorporating them into a multiobjective control system generally requires cascading control loops, which is challenging to design and increases complexity.

Model predictive control (MPC) is becoming a topic of greater interest in power electronics and has recently achieved adoption in industry [10], [11]. The subset known as finite-set MPC is the most intuitive implementation of MPC, as control actions are considered directly, and eliminates the need of a modulator [12]–[15]. The phrase “control action” here refers to either a specific sequence of gate signals applied to the semiconductor switches (referred to as optimal switching sequence MPC) or the space vector that results for a specific sequence of gate signals (referred to as optimal space vector MPC). Besides an intuitive implementation, MPC tends to work well as an inner control loop due to its fast dynamic response [16]–[18]. Finite-set MPC characteristics can be leveraged to tackle constrained multiobjective control problem challenges within the power electronics space [19]. Thus, finite-set MPC is a potential solution toward resilient power electronics at the grid-edge to enhance the power distribution system resiliency in a straightforward manner [20]. Modern power converters are commonly required to provide auxiliary services which requires implementation of multiobjective control schemes. As such, finite-set MPC is a promising solution toward grid-enhancing power converters with advance functionality.

Despite these benefits, there are challenges in the MPC formulation that have not been fully addressed [12], [21], [22]. In other words, what allows multiobjective MPC to boast its simplicity is what creates difficulty in the design stage. The cost function, while simple to implement, leaves its user to determine how they should weight the objectives in the cost function. Discussion in literature on how to design the weight

factors is limited to trial-and-error techniques for finding an optimal set-point [23], [24]. These techniques require the user to observe the tracking performance of each control objective and decide what the best behavior is. To be succinct, the optimal weight factor ratio of multiobjective MPC tends to be laborious to navigate and difficult to define, particularly for cost functions with more than two objectives. Additionally, a static weight factor ratio will likely not have optimal performance for all considerable scenarios [25], e.g., in a grid-connected inverter, the control object references should alter due to a grid-fault. The concept of an adaptive weight factor ratio for a power quality compensator was proposed in [26], where the weight factor of each control objective's cost in the overall cost function adapts to the predicted optimal error of each term. Still, such a control provides no guaranteed tracking performance of its objectives and requires normalizing its control objectives according to a predefined operating point. Thus, some of the difficulties that arise when implementing a multiobjective finite-set MPC stem from its use of a single cost function. Furthermore, conventional finite-set MPC with an overall cost function is not designed to drive any parameter error to fall below an acceptable tolerance. The designed weight factor ratios by themselves do not reveal nor confirm any tracking capability of the control; only through extensive tests can the control be evaluated which is a challenging design strategy. Any reported weight factor ratios may become unfit for a user who wants to emulate a controller under new conditions. Ultimately, it is desirable and simpler for end users to define their multiobjective controllers directly based on desired tracking performance of the objectives, while still being generally aware of tradeoffs associated with multiobjective optimization.

This article proposes a method to achieve multi-objective MPC without using an overall cost function for a CMI at the grid-edge. The proposed approaches enable users to design the controller according to acceptable tracking performance. This is achieved by addressing each control objective hierarchically instead of combining all control objectives in a single cost function, and the objectives are evaluated in sequence. Thus, the proposed control structure eliminates the need to design weight factors for a generic cost function. By ranking control objectives and defining an acceptable bound of error, the objectives are tracked in a descending fashion. Control actions that do not satisfy the error bound of an objective will be removed before considering subsequent control objectives. This will create stronger assurance of controller tracking for critical objectives, while still allowing for local minimization of less critical/slower dynamic control objectives.

The proposed concept is presented generally for finite-set MPC of N objectives, then described for the presented case study that enables resilient cascaded multilevel inverter at grid-edge. The proposed MPC approach is well-suited for CMI with advanced functionalities. The controller achieves active and reactive power injection with switching event minimization while simultaneously balancing the power drawn from the individual DC voltage sources. The represented DC sources could be battery cells connected to the grid through the proposed CMI. The latter of these control objectives is made

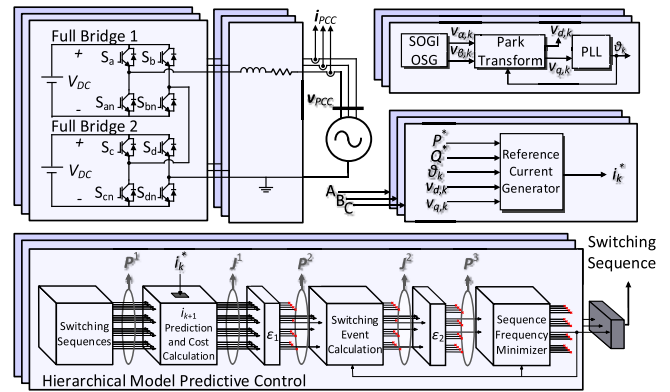


Fig. 1. Hierarchical MPC developed for grid-connected CMI.

possible by the proposed hierarchical approach to the control objective tracking, whereas traditional MPC requires complex logic external to the cost function [27], [28]. These approaches quickly become impractical as the number of cascaded bridges increase, as the number of switching sequences increase exponentially. Finally, the control is modularized for each phase, making the CMI robust to unbalanced grid conditions. Although it is beyond the scope of this article, the proposed control scheme can be integrated with energy management algorithms to optimize the power drawn from battery cells while considering current stresses on the battery cells during grid fast transients.

The remainder of this article is organized as follows. Section II explains the grid interactive CMI, the foundation of the predictive model, and reference generation for MPC cost function. Section III details the hierarchical MPC concept, and explains how it can be implemented on a controller with sequential logic. In Section IV, the concept is demonstrated for the presented case study in simulation, to investigate the control procedure in detail. In Section V, the control is implemented in a hardware experiment for one phase, where multiple transients are induced on the system. Finally, Section VI summarizes the findings.

II. SYSTEM DESCRIPTION

As mentioned in the introduction, the presented case study for the hierarchical MPC framework is a CMI at the grid-edge. Fig. 1 illustrates the CMI topology and summarizes the control scheme. A second-order generalized integrator (SOGI) phase-locked loop (PLL) detects the grid voltage angle [29]. The SOGI orthogonal signal generation technique is particularly beneficial for its inherent filtering of the grid voltage, making the reference current signal robust to grid voltage harmonics [30]. The reference current is assembled in the rotating reference (dq) frame, which is then converted to the reference grid current in stationary frame. The dq frame conversion is made possible by the orthogonal signal generation capability of the SOGI, where the original and quadrature signals are inputs to the Park transformation. The reference current is determined using equations for single-phase active and reactive power in

the dq frame:

$$P_k^* = \frac{1}{2}(v_{d,k}i_{d,k}^* + v_{q,k}i_{q,k}^*) \quad Q_k^* = \frac{1}{2}(v_{q,k}i_{d,k}^* - v_{d,k}i_{q,k}^*) \quad (1)$$

where P_k^* and Q_k^* are the active/reactive power set-points for the CMI. The subscript k indicates a discrete sampling instant. $v_{d,k}$ and $v_{q,k}$ are the grid's components in the rotating reference frame, and $i_{d,k}^*$ and $i_{q,k}^*$ are decoupled components of the reference current to be solved. This equation is rearranged to calculate the reference current components in the dq frame, and then converted to the original time-variant frame using the inverse Park equation

$$i_{d,k}^* = \frac{2(P_k^*v_{d,k} + Q_k^*v_{q,k})}{v_{d,k}^2 + v_{q,k}^2} \quad i_{q,k}^* = \frac{2(Q_k^*v_{d,k} - P_k^*v_{q,k})}{v_{d,k}^2 + v_{q,k}^2} \quad (2)$$

$$i_k^* = i_{d,k}^* \sin(\theta_k) + i_{q,k}^* \cos(\theta_k) \quad (3)$$

where θ_k is the grid angle detected by the PLL, and i_k^* is the time-variant reference current. For current control, the finite-set MPC evaluates each of the switching sequences or switching states, and compares it to the reference. The output current predictions derive from the AC-side KVL equation

$$v_{\text{inv}} = r(i) + L \frac{di}{dt} + v_g \quad (4)$$

where L and r are the filter inductance and equivalent series resistance (ESR), respectively. v_g and v_{inv} are the grid and inverter voltages, respectively. This equation is discretized by approximating the differential using forward Euler, assuming constant inductance, and is rearranged to create an explicit solution for the one-step ahead prediction of the output current

$$i_{k+1}^M = \left(1 - \frac{r}{L}T_s\right)i_k + \frac{T_s}{L}(v_{\text{inv},k+1}^M - v_{g,k}) \quad (5)$$

$M \in \mathbb{Z} : M \in [-2 \quad 2]$

where M is the output voltage level of the considered switching sequence; the applied output voltage is the output voltage level M multiplied by the DC link voltage V_{DC} . The associated cost term for injected current is defined as

$$\mathbf{J}^1 = |i_{k+1} - i_k^*| \quad (6)$$

where \mathbf{J}^1 is the cost vector of injected grid current. This will be explained more in Section III. The control also considers changes in the switches gate logic as a control objective to reduce the switching events and as a result the average switching frequency. The cost is defined as

$$\mathbf{J}^2 = \sum_{i=a,b,c,d} 2|S_{i,k+1} - S_{i,k}| \quad (7)$$

The gate logic for each switching sequence is provided in Table I. The summation in (7) is multiplied by two to account for the other switch in the leg (S_{an} and S_{bn}). There is a third control objective, referred to as sequence frequency minimization, but further discussion of it is left for Section III. The proposed sequence frequency minimization adds a unique feature to CMI via the proposed hierarchical MPC scheme that enables self-power balancing of its H-bridge cells, that is balances the power drawn from battery cells.

TABLE I
SWITCHING SEQUENCES FOR ONE PHASE OF FIVE-LEVEL CMI

Sw. Seq.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
S_a	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	1
S_{an}	1	1	1	0	0	0	1	1	1	0	1	0	0	0	1	0
S_b	0	0	1	0	1	1	0	1	1	1	0	0	0	1	1	0
S_{bn}	1	1	0	1	0	0	1	0	0	0	1	1	1	0	0	1
S_c	0	1	1	0	0	1	0	0	1	0	1	0	1	1	0	1
S_{cn}	1	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0
S_d	0	1	0	1	0	1	1	0	1	1	0	0	1	0	1	0
S_{dn}	1	0	1	0	1	0	0	1	0	0	1	1	0	1	0	1
M	0	0	0	0	0	0	-1	-1	-1	-1	1	1	1	1	-2	2

III. PROPOSED HIERARCHICAL PREDICTIVE CONTROL

Hierarchical MPC is first described in a conceptual way. To aid in understanding the concept, and to address a few exceptional cases of the control, we then describe how the control is actualized in a discrete controller.

A. Hierarchical Model Predictive Control: Conceptualized

The hierarchical predictive control paradigm is presented for N control objectives. The control is explained using two types of vectors, called cost vectors and argument vectors. Cost vectors are denoted with \mathbf{J} , as is standard in the field of convex optimization [31], [32]. The argument vectors are denoted as \mathbf{P} . For each control objective, there is an associated pair of cost and argument vectors. The rank of the vectors' associated objective is denoted by the vectors' superscript. For example, the cost and argument vectors associated with the primary objective are denoted by \mathbf{J}^1 and \mathbf{P}^1 , respectively. If a subscript i is specified, then the expression is referring to the i th element in the vector. \mathbf{J}_3^1 is referring to the third cost (cost of switching sequence three) of the primary objective. Each element has an associated switching sequence. Each objective is denoted by its rank within the hierarchy. As described earlier, switching sequences that are not projected to meet the specified cost tolerance are removed from the optimization set of the subsequent objective. This is denoted in the following equation:

$$\mathbf{P}^n = \{i : \mathbf{J}_i^{n-1} < \varepsilon_{n-1}\}. \quad (8)$$

Thus, \mathbf{P}^n contains the arguments of the optimization set for the subsequent objective n . Cost vectors $\mathbf{J}_{S \times 1}$ hold the projected cost of each switching sequence that remains in the optimization set. The value ε_{n-1} is the cost tolerance of the previous control objective (objective $n-1$). Each control objective, with the exception of the last control objective, will use a cost tolerance for removing candidate-switching sequences. Switching sequences are evaluated for each control objective according to the objective's \mathbf{P} vector. The \mathbf{P} vector of an objective details all the switching sequences that will have its cost measured for the objective

$$\mathbf{P}^N \subseteq \mathbf{P}^{N-1} \subseteq \dots \subseteq \mathbf{P}^2 \subseteq \mathbf{P}^1 \quad \mathbf{P}^1 = \{x \in \mathbb{N} | x \leq S\} \quad (9)$$

where S equals the number of possible switching sequences. For the CMI, this is equal to 4^H , where H is the number

of H-bridges in cascade [33]. Also shown in (9) is the time-invariant setting of \mathbf{P}^1 . Definitely, \mathbf{J}^1 will be computed for each possible switching sequence, as nothing else has allowed switching sequences to be excluded. This means \mathbf{P}^1 will hold a constant size, which is simply an array of incrementing natural numbers from 1 to S . From (9), we see the \mathbf{P} vectors may decrease in size to objective N , but are not guaranteed to. This reduction in the optimization set is dependent on the chosen cost tolerances. In general, hierarchical MPC cannot guarantee a consistent reduction in cost computations, but also cannot exceed that of a traditional finite-set MPC. This will be demonstrated in Section IV. Upon evaluation of all switching sequences with respect to each control objective, the controller will have determined a reduced optimization set, equal to \mathbf{P}^N . Again, there is no guarantee to the size of \mathbf{P}^N , only a guaranteed upper bound. However, since all sequences within are deemed sufficient for proceeding objective s , the control selects the sequence within this set which optimizes the N th objective

$$s_{k+1} = \arg \min\{\mathbf{J}^N\}. \quad (10)$$

Thus, for the lowest rank objective, a cost tolerance need not be defined.

B. Hierarchical Model Predictive Control: Actualized

For implementation in a microcontroller with sequential logic, Algorithm I outlines how the controller can be implemented. It is noted that the argument vector \mathbf{P}^1 is fixed, since all switching sequences will be evaluated for the primary objective. In block 1 of the algorithm, \mathbf{P}^2 is constructed, and is of varying length. The bottom two lines of block 1 suggest a scenario not yet considered: what if none of the switching sequences allow any of the cost to be less than its associated tolerance ε ? A switching decision must still be made. The most obvious workaround is to choose the switching sequence which minimizes the cost, despite the cost exceeding the defined bound. Effectively, this is what is done. However, it is possible to continue optimizing subordinate objectives if there are redundancies in the minimized cost. Redundant switching sequences are especially prevalent in the CMI topology [8]. As an example, let us consider the following scenario: at instant k , it is predicted that no switching sequence will allow the injected current to meet the defined tolerance. Additionally, when optimizing for grid current, it is determined that applying an output voltage level of 0 will minimize cost. For the five-level CMI, there are six switching sequences which can achieve this voltage level. Thus, these six switching sequences can be evaluated for subordinate objectives, while still ensuring minimization of cost in injected current. Such logic is described in Algorithm 2, which is nested in blocks one through $N - 1$ in Algorithm 1.

Algorithm 2 is written in for an arbitrary objective U , where $U \in [1, N - 1]$. Block 1 acts in a very similar way to block N of Algorithm 1. Essentially, objective U is being optimized with the optimization set developed from objective $U - 1$. If a redundant optimal sequence is found, the vector redundancies are filled with logic-high values in alignment

with the redundant sequences. The variable redundancy acts as a flag to trigger block two of the algorithm. If no redundant optimal sequences are detected, the control breaks out of Algorithm 2 and Algorithm 1 and returns the optimal sequence. However, if there are redundant optimal switching sequences with respect to objective U , the control moves to block two, which fills the argument vector \mathbf{P}^U with the detected redundant sequences. In this scenario, the control returns to Algorithm 1 to evaluate Objective $U + 1$.

For the case study implemented in this article, the primary, secondary, and tertiary objectives are (respectively): injected grid current, switching events, and a term referred to as sequence frequency. Sequence frequency is the frequency in which the controller selects a particular switching sequence. Applying the sequence frequency objective allows the controller to eliminate bias among redundant switching sequences. To better understand the purpose of this objective, we will introduce a traditional finite-set MPC for the presented case study. It optimizes injected grid current and minimizes switching events with the following cost function:

$$\mathbf{J} = |i_{k+1} - i_k^*| + \lambda \sum_{i=a,b,c,d} 2|S_{i,k+1} - S_{i,k}| \quad \lambda \ll 1$$

$$s_{k+1} = \arg \min(\mathbf{J}). \quad (11)$$

The weight factor applied to the switch minimization term is made sufficiently small so as not to affect the current objective, which only depends on the output voltage level M . The optimization procedure of such a control is similar to block N of Algorithm 1, where \mathbf{J} replaces \mathbf{J}^N , and \mathbf{P}^1 replaces \mathbf{P}^N . For implementation of this control, redundant switching sequences are ignored. That is, when there are two or more switching sequences that equally optimize the control objective(s), the control will consistently select only one of the sequences. If $\mathbf{P}^1 i$ and \mathbf{P}_{i+1}^1 minimize \mathbf{J} equally, the function will always return s_{k+1} as \mathbf{P}_i^1 . This is common for finite-set predictive control [19], [34]. For the traditional predictive control outlined by (11), consider the scenario where the previous switching sequence was switching sequence 16 ($M = 2$), and to optimize injected grid current, the controller will implement $M = 1$. There are four switching sequences to achieve this; two sequences apply positive voltage across cell one (sequences 12 and 13), the other two apply positive voltage across cell two (switching sequences 11 and 14). Considering both injected grid current and switching events in the cost function, the controller will always select the first switching sequence such that $M = 1$ (switching state 11) when the previous switching state was switching state 16, since $\mathbf{J}_{11} = \mathbf{J}_{12} = \mathbf{J}_{13} = \mathbf{J}_{14}$. Undue bias toward this switching sequence induces unequal power draw from the isolated DC sources, which has practical consequences such as uneven discharge rates of grid-connected battery storage systems. When applying switching events in the cost function, it cannot be said with certainty how the power draw characteristics will behave for traditional finite-set MPC, since this depends on the changes in the selected output voltage over time, which depends on the output filter, sampling frequency, and DC link voltages. However, without an objective to regulate the selection of redundant switching sequences, the power draw

characteristics are likely to be distinct for each source. This will be demonstrated in Section V.

For hierarchical MPC, applying an objective to remove such biases is simple. This objective is applied by creating a tertiary cost vector \mathbf{J}^3 and incrementing \mathbf{J}_i^3 each time the controller selects switching sequence i . Mitigation of bias among the possible switching sequences improves the equalization of power draw from the isolated DC sources. An objective such as this is difficult to apply directly in a traditional finite-set MPC, since the cost increases without bound. Over time, this objective would “dominate” the cost function, as its magnitude of the cost quickly exceeds that of all other objectives. With the hierarchical controller, this is impossible, as this objective can only be optimized once the superordinate objectives fall within their respective bounds.

Algorithm 1 HMPC, S Switching Sequences, N Objectives

Function $[s_{k+1}] = \text{HMPC}(\text{measurements})$

Initialization: sampling at T_s , Define $\varepsilon_1, \varepsilon_2, \dots, \varepsilon_{N-1}$

$\mathbf{J}^1 \leftarrow \mathbf{J}^2 \leftarrow \dots \leftarrow \mathbf{J}^N \leftarrow [0 \ 0 \ \dots \ 0]_{1 \times M}$, $\mathbf{P}^1 \leftarrow [1 \ 2 \ \dots \ M]_{1 \times S}$ $\mathbf{J}_{\text{opt}}^1 \leftarrow \mathbf{J}_{\text{opt}}^2 \leftarrow \dots \leftarrow \mathbf{J}_{\text{opt}}^N \leftarrow \infty$, $i \leftarrow 1$

1: Argument Reduction for Primary Objective

for each $x \in \mathbf{P}^1$ do

compute \mathbf{J}_x^1

if $\mathbf{J}_x^1 \leq \varepsilon_1$ then

$\mathbf{P}_i^2 \leftarrow x$, $++i$

end if, end for, reset i

if $\text{length}(\mathbf{P}^2) = 0$ then \rightarrow Optimize \mathbf{J}^1 (Algo. 2)

else \rightarrow descend ...

2: Argument Reduction for Secondary Objective

for each $x \in \mathbf{P}^2$ do

compute \mathbf{J}_x^2

if $\mathbf{J}_x^2 \leq \varepsilon_2$ then

$\mathbf{P}_i^3 \leftarrow x$, $++i$

end if, end for, reset i

if $\text{length}(\mathbf{P}^3) = 0$ then \rightarrow Optimize \mathbf{J}^2 (Algo. 2)

else \rightarrow descend ...

⋮

$N-1$: Argument Reduction for Objective $N-1$

for each $x \in \mathbf{P}^{N-1}$ do

compute \mathbf{J}_x^{N-1}

if $\mathbf{J}_x^{N-1} \leq \varepsilon_{N-1}$ then

$\mathbf{P}_i^N \leftarrow x$, $++i$

end if, end for, reset i

if $\text{length}(\mathbf{P}^N) = 0$ then \rightarrow Optimize \mathbf{J}^{N-1} (Algo. 2)

else \rightarrow descend ...

N : Optimization of N^{th} Objective

for each $x \in \mathbf{P}^N$ do

if $\mathbf{J}_x^N < \mathbf{J}_{\text{opt}}^N$ then

$s_{k+1} \leftarrow x$, $\mathbf{J}_{\text{opt}}^N \leftarrow \mathbf{J}_x^N$

end if, end for

end N hierarchical if statements, Return s_{k+1} , End function

While discussing this control, the feasibility of finite-set MPC (and the proposed HMPC) for alternative applications should be addressed. First, it should be established that the

Algorithm 2 Nested in Algorithm 1, Triggered If Cost Tolerance Cannot Be Met for Objective U

Initialization: $\text{redundancies} = [0 \ 0 \ \dots \ 0]_{1 \times S}$

1: Optimizing \mathbf{J}^U , Tracking Redundant Optimal Sequences

for each $x \in \mathbf{P}^{U-1}$ do

if $\mathbf{J}_x^U < \mathbf{J}_{\text{opt}}^U$ then

$s_{k+1} \leftarrow x$, $\text{redundancy} \leftarrow 0$, reset redundancies

elseif $\mathbf{J}_x^U = \mathbf{J}_{\text{opt}}^U$ then

$\text{redundancy} \leftarrow 1$, $\text{redundancies}_x = 1$

$\text{redundancies}_{s_{k+1}} \leftarrow 1$

end if, end for

2: Checking for Redundant Optimal Sequences

if $\text{redundancy} = 1$ then

for each $x \in \mathbf{P}^{U-1}$ do

if $\text{redundancies}_x = 1$ then

$\mathbf{P}_i^U \leftarrow \mathbf{P}_x^{U-1}$, $++i$

end if, end for

else break hierarchical if statements, Return s_{k+1} , End function

end if, End of Nested Algorithm

proposed HMPC can easily be expanded for CMI with a larger number of series-connected H-bridge modules. If there are N -series connected H-bridges, the possible control actions and maximum size of the argument vectors can be defined automatically from N . However, the number of possible controls actions to implement increases exponentially with N . In the selected application (with $N = 2$) there are 16 possible control actions. This can be easily implemented at a high controller sampling frequency. For instance, a sampling frequency of 50 kHz is used in the hardware experiment of Section V, and the sampling rate was limited primarily because of the analog-to-digital converters for sensed measurements. To consider a topology with 100 H-bridge modules ($N = 100$), there would be 4^{100} unique control actions. Needless to say, evaluating this number of control actions is not possible with a practical embedded system at a reasonable sampling frequency. This is inherent to any finite-set control, including traditional finite-set MPC. Mitigation of this issue for such applications would require a technique which carefully eliminates a substantial number of control actions without removing the benefits of finite-set MPC or introducing critical drawbacks, but further discussion is outside the scope of this work.

IV. ILLUSTRATION OF CONCEPT

The main objective of this section is the detailed analysis of the control procedure which is not feasible in the hardware implementation of the system. For instance, we cannot collect intermediate variables, for example, cost and argument vectors, in real time at each discrete instant while still implementing a practical controller sampling frequency. To overcome this, we first simulate the hardware experiment. The sampling frequency, filter size, and grid voltage are equal to that of the hardware experiment in Section V. In Section IV-A, the tracking of each objective is studied in depth. In Section IV-B,

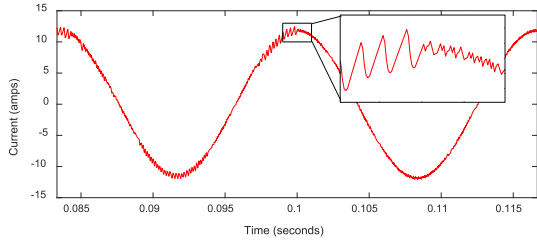


Fig. 2. Injected phase current. At $t = 0.1$ s, ε_1 is reduced from 0.8 to 0.3 A.

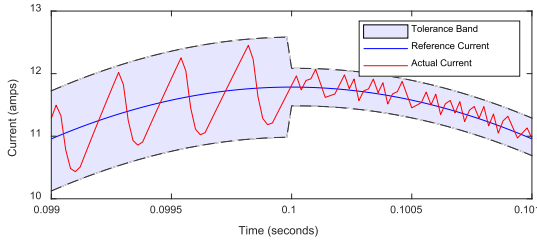


Fig. 3. Injected phase current, reference current, and tolerance band as ε_1 is reduced from 0.8 to 0.3 A.

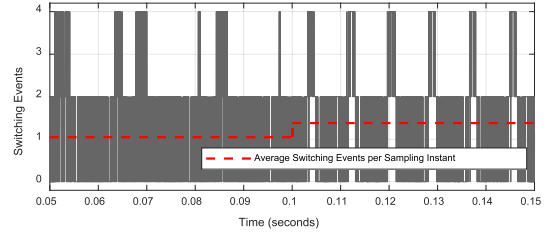


Fig. 4. Number of switching events as ε_1 is reduced from 0.8 to 0.3 A, and ε_2 increases from 3 to 5. These changes result in about a 30% increase in the average number of switching events per discrete sampling instant.

we examine the effect of model inductance error on current tracking.

A. Objective Tracking Analysis

Data are collected for one phase of the modular control. Fig. 2 shows the injected grid current for one phase during a step-change in cost tolerances of objective one and two. At $t = 0.1$ s, the cost tolerance of injected grid current is reduced from 0.8 to 0.3 A, while the cost tolerance of switching events is increased from 3 to 5. Fig. 3 shows the reference current, injected current, and cost tolerance bounds during this step change. An obvious reduction in current ripple about the peaks is observed, and the controller is able to maintain the current within this bound. Fig. 4 shows the number of switching events, changes in gate signal logic, during this transition. Since a relaxation of switching event error bound has been implemented, the average number of switching events per sampling instant increases by roughly 30%. Fig. 5 shows the better understand the decision making procedure of the hierarchical MPC. The same parameters are present that were shown in Fig. 3, but the next-state predictions at each discrete sampling instant. The next-state prediction of the selected switching sequence is highlighted for each instant. It is noted that there are only five next-state predictions per instant, yet some predictions are represented by a darker point. This demonstrates that there exist only five unique current predictions among the 16 possible switching sequences, one unique prediction for each possible output voltage level, and thus many predictions overlap. This agrees with Table I, showing each switching sequence and its output voltage level M . The instances in Fig. 3 occur before the transition in cost tolerance. Prior to $t = 0.09928$ s, we see the controller continues implementing $M = 2$, despite the fact that it is not optimizing the injected current objective. Since these control actions fall within the bounds of its cost tolerance,

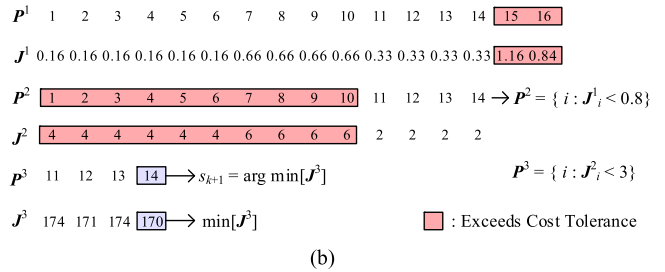
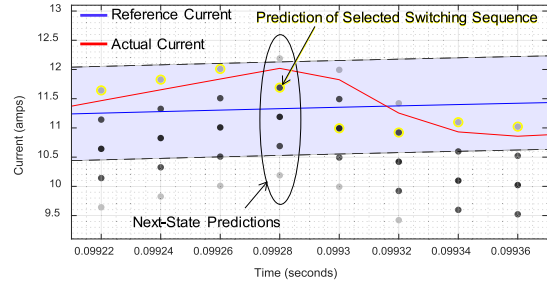


Fig. 5. (a) Injected phase current, reference current, tolerance band, and next-state current predictions for each discrete instant, evaluated with ε_1 equal to 0.8 A. The prediction of the selected switching sequence is highlighted. (b) Cost and argument vectors at instant $t = 0.09928$ s. Cost tolerance of objectives 1 and 2 are 0.8 A and 5 switching events, respectively.

switching sequences such that $M \in [0, 2]$, are still being considered as the controller moves to calculating switching event computations. With the cost tolerance of objective two set to three (switching events) switching sequences that require more than one bridge gate inversion are removed. From examining Table I, we see this will eliminate zero-voltage levels, but retains all sequences such that $M = 1$, as well as the previous switching state. Thus, switching sequences 11, 12, 13, 14, and 16 remain in the optimization set. From there, the controller selects the switching state that has been chosen the least. From this, we conclude the $M = 1$ switching sequences have been chosen more frequently at this point, thus, the control continues to implement switching sequence 16.

A transition in switching sequence occurs at $t = 0.09928$ s. We see that the presently implemented voltage level of two is no longer in the acceptable boundary. The cost and argument vectors at the end of this iteration are shown in Fig. 5. After computing J_1 , switching sequences 15 and 16 which produce output voltage levels of negative two and positive two, respectively, exceed ε_1 . Thus, P^2 has both sequences removed from the optimization set. However, since the currently selected

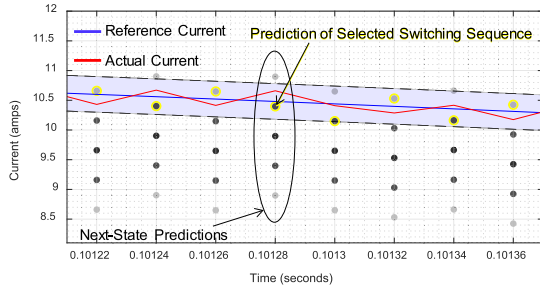
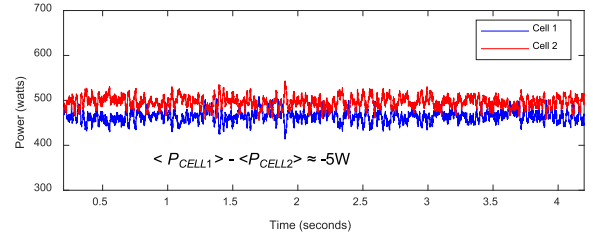


Fig. 6. Injected phase current, reference current, tolerance band, and next-state current predictions for each discrete instant, evaluated with ε_1 equal to 0.3 A. The prediction of the selected switching sequence is highlighted.

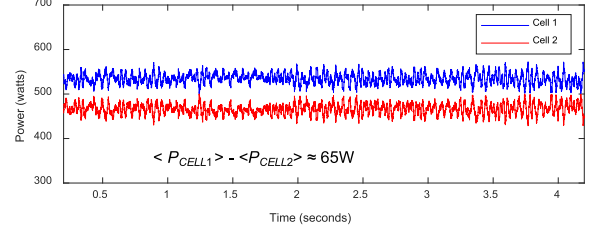
switching state is 16, and the switching event tolerance is three, all negative and zero output voltage levels are removed, as they require at least four gate signal transitions. The only switching sequences that remain in the set are those such that $M = 1$, thus \mathbf{P}^3 contains the 11 through 14. Finally, the controller selects among the reduced set according to the level that has been selected the least, which is switching state 14. Thus, the controller implements switching state 14 at $t = 0.0993$ s. It is noted that the size of the cost vectors do not change size; Fig. 5 only includes the cost vector elements that were computed.

In Fig. 6, the current, reference current, and reduced tolerance band ($\varepsilon_1 = 0.3$ A) are shown after $t = 0.1$ s with the next-state current predictions. It is clear that fewer voltage levels tend to fall within this error bound. In general, the argument vectors \mathbf{P}^2 and \mathbf{P}^3 will be smaller in this scenario. Thus, it will be more difficult to optimize their associated objectives. This is also evidenced in Fig. 7, which shows the power draw characteristics of the individual H-bridges for each set of cost tolerances. In Fig. 7(a), the larger cost tolerance for injected grid current induces greater equalization of power draw from the two sources, with a difference in power draw of roughly 5 W. The controller is better able to even the selection of switching sequences. Fig. 7(b) shows the power draw of each cell for the reduced ε_1 . The difference in power draw increases to 65 W, as a result of the size reduction in \mathbf{P}^3 . As will be shown in the hardware results, this deviation is far less than that of traditional MPC.

As discussed in Section III, hierarchical MPC does not guarantee a consistent reduction in iterative computation when compared to traditional finite-set MPC. However, hierarchical MPC will not exceed the computation of traditional MPC. To understand this, the iterative computations are directly tracked in Fig. 8. Here, a computation is considered an addition, subtraction, multiplication, division, or comparison. A comparison is done when searching for an arg min, or finding objectives which fall within their respective tolerances. This tracking is done for a high-level explanation of how computations differ for hierarchical MPC and not for a definitive comparison of feasible sampling frequencies; this would require an assumed architecture of the embedded system. Furthermore, computations are only considered for the optimization portion of the control (i.e., computations for reference



(a)



(b)

Fig. 7. Power injection from each of the isolated sources for (a) $\varepsilon_1 = 0.8$ A and (b) $\varepsilon_1 = 0.3$ A.

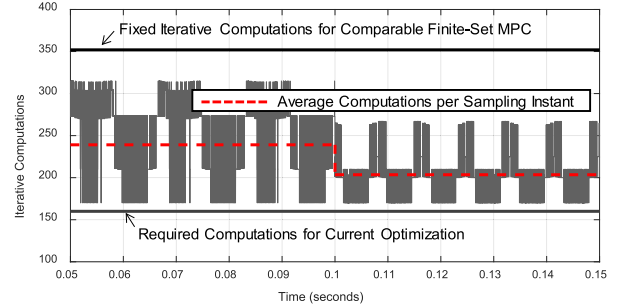


Fig. 8. Number of iterative computations as ε_1 is reduced from 0.8 to 0.3 A, and ε_2 increases from 3 to 5. These changes result in an average iterative computation count of roughly 239 to about 203.

signal generation are not included). Prior to the change in cost tolerances at $t = 0.1$ s, we see computation varies between 170 and 315, with an average of about 239. There is a fixed minimum number of computations associated with computing J^1 and P^2 . The remaining computations are dependent on the length of \mathbf{P}^2 and \mathbf{P}^3 . For larger tolerances, the length of succeeding argument vectors will increase, and iterative computation will increase accordingly. Thus, following the reduction in ε_1 at $t = 0.1$ s, we see a reduction in iterative computation. This is a result of \mathbf{P}^2 tending to be smaller, as the current optimization constraint has become more difficult to satisfy. It is noted that the comparable finite-set MPC has a fixed number of iterative computations of 352. For the selected error tolerances, the hierarchical MPC has a consistently reduced number of computations.

B. Effect of Model Parameter Error on Current Tracking

Accurate next-state current prediction is dependent on accurate estimation of the model parameters. For finite-set model predictive current control with an inductive filter, model inductance error is found to be much more critical than error

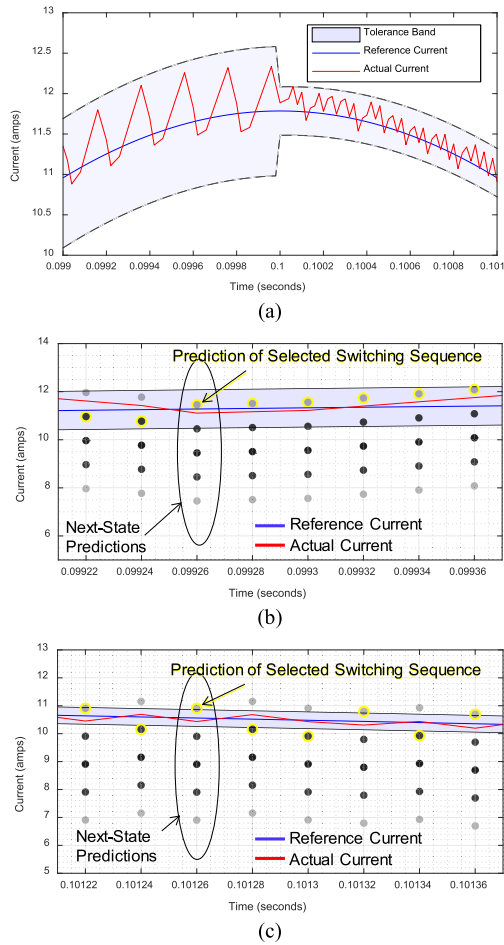


Fig. 9. Current tracking for negative 50% relative error in model inductance. (a) Injected phase current, reference current, and tolerance band as ε_1 is reduced from 0.8 to 0.3 A. (b) Injected phase current, reference current, tolerance band, and next-state current predictions for each discrete instant, evaluated with ε_1 equal to 0.8 A and (c) ε_1 equal to 0.3 A.

on the ESR of the filter [35]. Thus, we have restricted our focus to relative error on the model inductance.

First, a relative error of negative 50% is applied to the model inductance. That is, the inductance within the HMPC algorithm is half of the physical inductance. The same transient from subsection A is applied here; namely, ε_1 is reduced from 0.8 to 0.3 A, and ε_2 is increased from three to five at time $t = 0.1$ s. The injected current, reference current, and cost tolerance bounds are shown in Fig. 9(a). It is evident that the current is maintained well within the defined bound. In fact, the error magnitude appears lower on average than was seen without model inductance error. The reason the bound is maintained can be explained when looking back to (5) which computes the next-state current prediction for each output voltage level. With a reduced model inductance L , the prediction overestimates the change induced on the current from the estimated voltage across the filter. In Fig. 9(b), ε_1 is 0.8 A, and the difference in predicted currents for each output voltage level is around 1 A. The current predictions have “spread out,” from the model-aligned inductance from Fig. 6, where the predictions were roughly 0.5 A apart. Less output

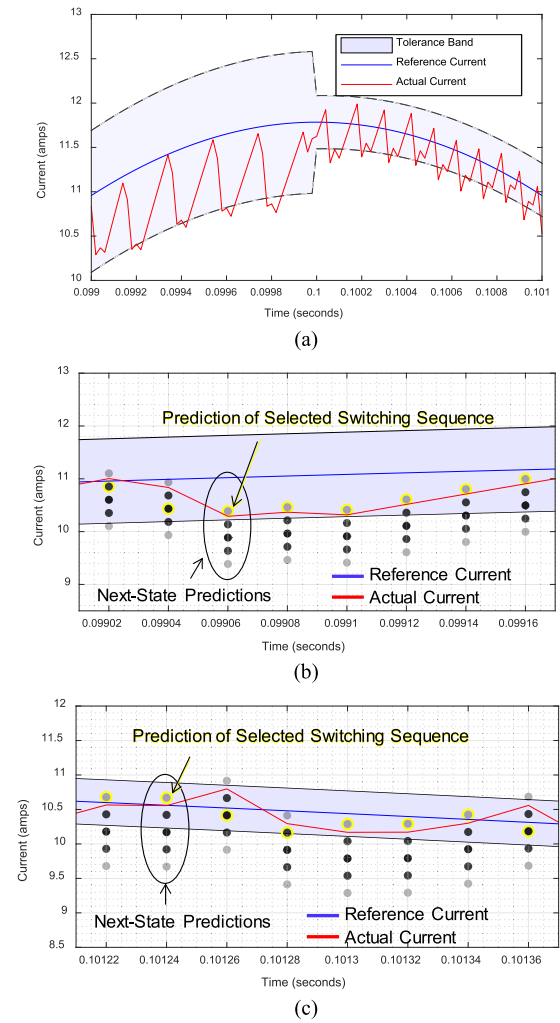


Fig. 10. Current tracking for 100% relative error in model inductance. (a) Injected phase current, reference current, and tolerance band as ε_1 is reduced from 0.8 to 0.3 A. (b) Injected phase current, reference current, tolerance band, and next-state current predictions for each discrete instant, evaluated with ε_1 equal to 0.8 A and (c) ε_1 equal to 0.3 A.

voltage levels are determined to be within the defined error tolerance bound, and the current stays well within the bound as a result. In Fig. 9(c), for most sampling instances, there is no output voltage level which satisfies the cost tolerance ε_1 . As a result, the control must select the output voltage which minimizes the current error magnitude. This allows the controller to maintain the defined boundary.

Next, a relative error of 100% is applied to the model inductance. This is considered a worst-case scenario. The inductance value in the controller is set to twice that of the physical filter inductance. The previous transient is again applied at $t = 0.1$ s, as shown in Fig. 10(a). Unlike the scenario of underestimated model inductance, the overestimated model inductance is unable to keep the current within the defined bound. With positive relative error on the model inductance, the control underestimates the change in inductor current. In Fig. 10(b), we see the current predictions closer together for each sampling instant. As a result, output voltage levels which would not normally reside within the acceptable boundary

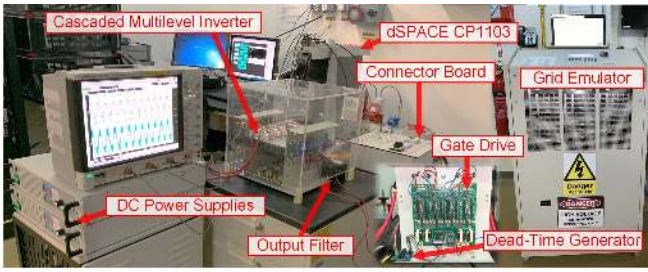


Fig. 11. Hardware setup for experimental validation of proposed hierarchical MPC scheme toward smart CMI.

TABLE II
SYSTEM SPECIFICATIONS

Parameter	Value
DC-link voltages	165V
Filter Inductance	2.5mH
Filter Resistance	0.2 Ω
Rated line-neutral Grid Voltage	120V _{RMS}
P^*	1kW
Q^* (normal grid condition)	0kVAR
Q^* (grid voltage sag)	0.25kVAR
Controller Sampling Frequency	50kHz
Imposed dead-time	1ms
ε_1 [Hierarchical MPC]	0.2A
ε_2 [Hierarchical MPC]	5 switching events
λ [Traditional MPC, governed by (10)]	1e-6
k_p (PR controller of PWM-based control)	0.1
k_r (PR controller of PWM-based control)	10

are kept within the optimization set for the secondary and tertiary objectives. Since there are more zero voltage switching sequences, they tend to be selected less frequently. As a result, the control tends to select switching sequences with lower voltage levels to satisfy the tertiary objective. Thus, near the peak of the reference current, the injected current tends to settle below the reference. In Fig. 10(c), the reduced cost tolerance boundary contains more voltage levels than was noted for reduced model inductance. Whereas reduced model inductance still allowed for the current to be constrained within the desired boundary set by ε_1 , the increased model inductance cannot. It is worth mentioning that this case study demonstrates a significant model parameter error as a worst-case scenario which is rarely considered in practice. This extreme model parameter error demonstrates the acceptable performance of the proposed controller.

V. RESULTS AND DISCUSSION

The proposed hierarchical MPC scheme is tested experimentally. For the case studies, a five-level CMI is tied to a 120 V_{LN} (RMS) grid. Table II details parameters of the testbed, shown in Fig. 11. DC power supplies provide the DC link voltages of the H-bridges, and a four-quadrant (power-bidirectional) grid emulator is tied to the output of the CMI. The control is implemented on a rapid control prototyping device, the dSPACE CP1103. The CP1103 has embedded analog-to-digital converters, and thus all measurements shown in this section come from stored values sensed/computed by

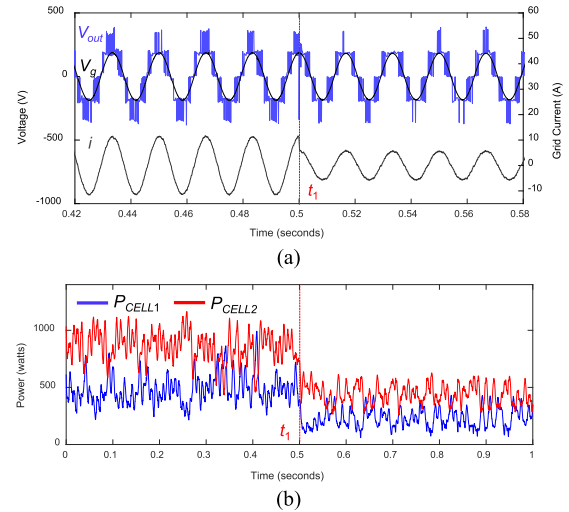


Fig. 12. Dynamic response of traditional finite-set MPC for reduction in power reference at t_1 from (a) output voltage, grid voltage, and output current and (b) power draw characteristics.

the CP1103. To store data in real time, the sampling rate of the collected measurements are 12.5 kHz (one fourth of the controller's sampling frequency). The cost tolerances ε_1 and ε_2 are set to 0.2 A and five switching events, respectively. When validating the control to system transients, its dynamic and steady-state response is compared to a comparable, traditional finite-set control scheme, and a standard PWM current control. In all three control schemes, the current reference is developed identically, which is described in Section II. In Section V-A, the control is compared to standard finite-set MPC. In Section V-B, the proposed control is compared to a current control scheme which uses a multilevel subharmonic PWM switching scheme, and the modulation signal is developed from a proportional-resonant (PR) control.

A. Comparison Against Traditional Finite-Set MPC

The standard model predictive current control implements the cost function and control action defined in (10). Its weight factor λ tied to switching event minimization is defined in Table II as 1e-6. It is noted that this is done so the control will only reduce switching events once the optimal output voltage level M is selected. It is expected that the control will select the same switching sequences for all λ less than 1e-4 but greater than 0. This statement is equivalent to saying it is expected that the cost difference of the current predictions between different voltage levels will always exceed 0.8 mA, as the greatest cost produced by the switching event term in J cannot exceed 8e-4. Thus, the designed cost function will behave in a similar fashion to the proposed hierarchical control, but does not include the sequence frequency objective.

Both the proposed control and finite-set MPC are tested for a step change in power reference, from 1 kW to 0.5 kW. In Fig. 12, the traditional finite-set MPC implements a reduced power reference at t_1 . Within a few samples, the control settles the current amplitude in alignment with the reduced power reference, as shown in Fig. 12(a). In Fig. 12(b),

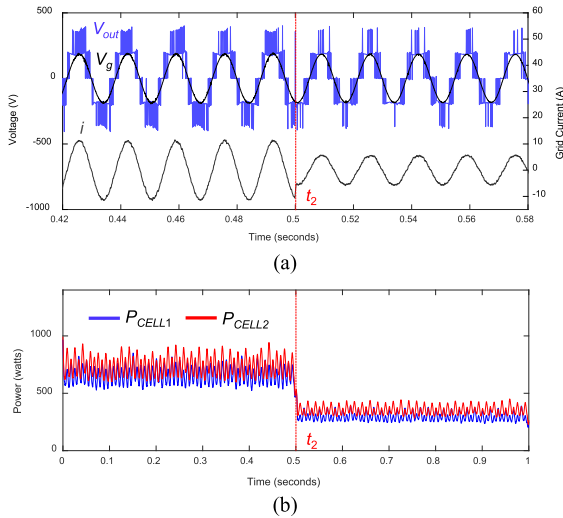


Fig. 13. Dynamic response of the proposed control for reduction in power reference at t_2 . (a) Output voltage, grid voltage, and output current. (b) Power draw characteristics.

the power-draw characteristics of each voltage source are shown. There is evident double-frequency power ripple. This is also evidenced on the DC-link voltages, which are used to compute the output voltage in Fig. 12(a). Furthermore, there is a notable distinction in power draw among the voltage sources. In particular, the voltage source of the lower H-bridge has notably larger power draw on average than that of the upper H-bridge. Without an objective to equalize the selection of switching sequences, the standard MPC selects only one switching sequence for each output voltage level. This distinction is dependent on how the switching sequences are defined and compared in the control algorithm, unlike the proposed control. In Fig. 13(a), the proposed control is placed under the same power reference reduction at t_2 . The control reduces the output current to the reduced reference current amplitude within a few sampling instants, as was seen with the traditional finite-set MPC. In Fig. 13(b), the power draw characteristics of each H-bridge are shown. The double-frequency power ripple that was seen in traditional finite-set MPC still occurs for the proposed control. However, there is only a slight distinction in power draw between the voltage sources. This was noted in Section IV, where implementing a small ε_1 created a slight distinction in power draw. Thus, the proposed control successfully retains the fast reference tracking of traditional finite-set MPC while substantially reducing the distinction in power draw characteristics.

Next, each control is tested for a sag in grid voltage. As noted in Table II, the reactive power reference (Q^*) is 0 under normal grid conditions. However, in the event of a significant grid voltage sag, the inverter injects 250VAR to support the grid voltage. In Fig. 14, the dynamic response of traditional finite-set MPC is shown for a 20% sag in grid voltage at t_3 . Shortly after t_3 , there is a notable adjustment in the output current. Specifically, the amplitude of the current has increased and lags the grid voltage. This suggests the current reference has been adjusted to enable reactive power

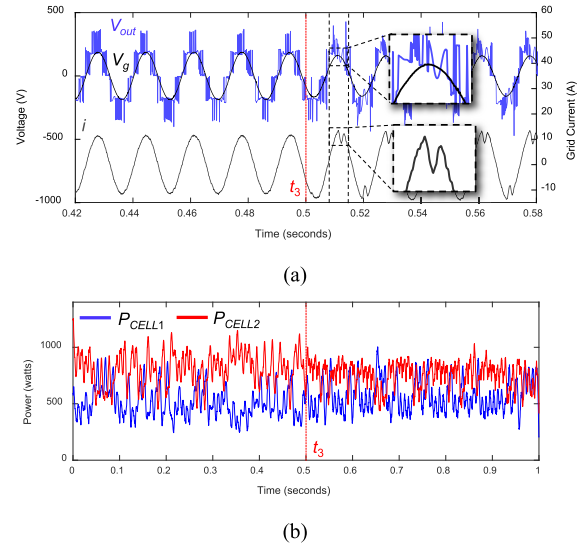


Fig. 14. Dynamic response of traditional finite-set MPC for 20% grid voltage sag at t_3 . (a) Output voltage, grid voltage, and output current. (b) Power draw characteristics.

injection. However, in Fig. 14(a), substantial distortion occurs at the current peaks. Furthermore, it is noted that the output voltage of the CMI falls below the grid voltage during this interval of current distortion. This voltage oscillation at the DC side is a result of the erratic and disparate power drawn from the voltage sources. In Fig. 14(b), the power draw characteristics of the finite-set MPC are shown. Not only is the power draw largely distinct for each voltage source, but there is notable fluctuations in the power drawn over time, marginalizing the stability of the DC-link voltages. This unregulated power draw is inherent to the finite-set MPC, making the traditional predictive control unable to reach the desired output current. The same grid voltage sag is applied to the proposed HMPC at t_4 . In Fig. 15(a), the current is noted to increase in amplitude and lag the grid voltage, as was noted in traditional finite-set MPC. However, the proposed HMPC does not experience the current distortion previously noted for the traditional finite-set MPC. In Fig. 15(b), there is a slight increase in overall power draw from the voltage sources, presumably caused by a slight reduction in efficiency from the increased current demand of the converter. However, stable and near-equal power draw characteristics are observed from the voltage sources, and thus the control is able to meet the demanded active and reactive power. The problem observed using the traditional finite-set MPC can be mitigated with increased DC-link capacitance. However, the stable and equalized power draw characteristics of proposed control helps to reduce the resultant voltage ripple across the DC-link, when compared to a traditional finite-set MPC scheme. With the proposed control, the sequence frequency objective can be applied to the control as J^3 , and thus the control tends to select redundant switching sequences more evenly. Furthermore, the proposed hierarchical approach mitigated the trial and error design stage of the weight factors of traditional MPC.

The total harmonic distortion of the grid current is found to be 3.75% when injecting 1 kW of active power at steady state.

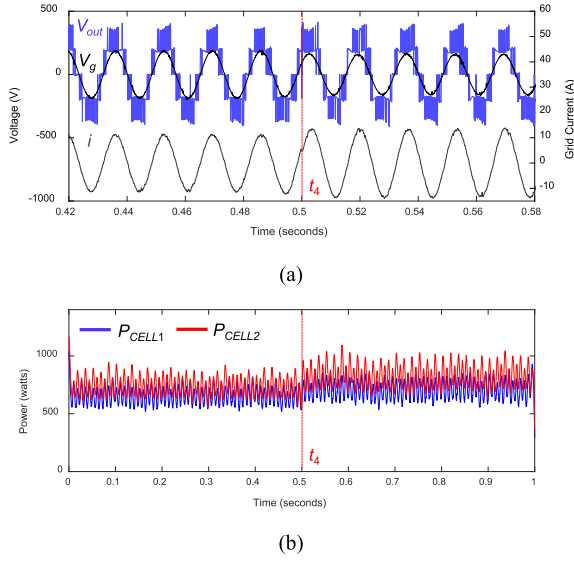


Fig. 15. Dynamic response of proposed control for 20% grid voltage sag at t_4 . (a) Output voltage, grid voltage, and output current. (b) Power draw characteristics.

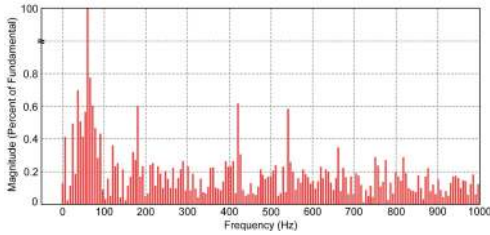


Fig. 16. FFT analysis of the proposed control scheme.

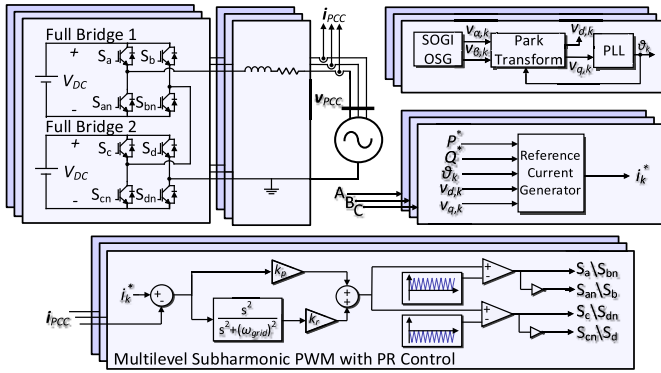


Fig. 17. Cascaded H-bridge topology and proportional-resonant-based current control with subharmonic PWM.

The distortion of the comparable finite-set MPC is computed as 3.78%, thus there is no notable distinction in the error of the injected grid current between the two strategies. An FFT analysis of the injected current for the proposed control scheme is provided in Fig. 16. What is most notable is the continuous nature of the harmonic content, which is inherent finite-set MPC, which operates with a variable switching frequency.

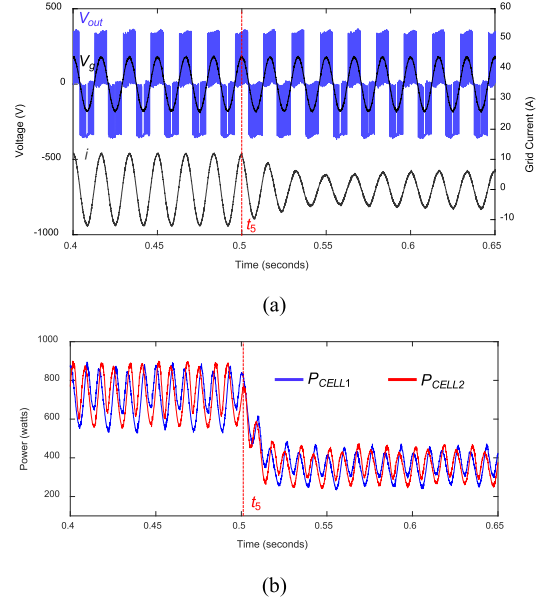


Fig. 18. PR-based current control with subharmonic PWM with a reduction in power reference at t_5 . (a) Output voltage, grid voltage, and output current. (b) Power draw characteristics.

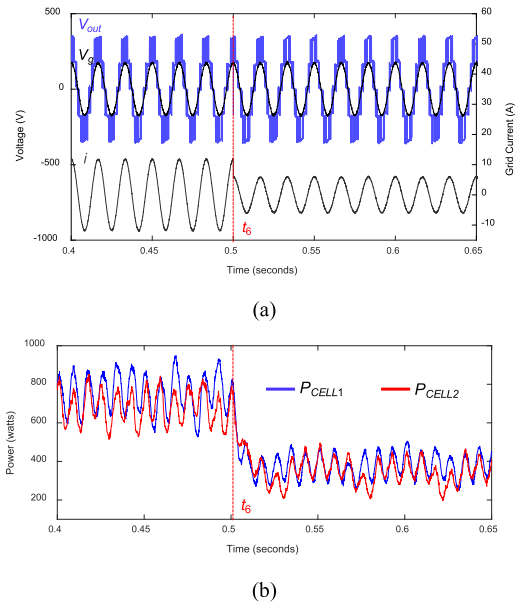


Fig. 19. Proposed hierarchical MPC with a reduction in power reference at t_6 . (a) Output voltage, grid voltage, and output current. (b) Power draw characteristics.

TABLE III
CONTROL COMPARISON AT 1-kW POWER INJECTION

Control Technique	Current THD	Settling time (P^* reduction)	$ \langle P_{CELL1} \rangle - \langle P_{CELL2} \rangle $	Control Design Effort
Proposed Control	3.75%	$\sim 160\mu s$	$\sim 65W$	Low
Traditional FS- MPC	3.78%	$\sim 160\mu s$	$\sim 325W$	Medium
PR current control	5.57%	$\sim 51ms$	$\sim 7W$	High

B. Comparison Against PR Current Control Scheme

The proposed control is also compared to a classical, PWM-based current control scheme for the CMI topology,

as shown in Fig. 17. The modulation technique is referred to as multilevel subharmonic PWM [9]. A proportional-resonant controller is used to provide a modulation signal that matches the grid frequency. The gains of the controller, k_p and k_r , were tuned to 0.1 and 10, respectively. There was a tradeoff when tuning the gains of transient response and power quality at steady state. The carrier signals are set to 20 kHz. Since finite-set MPC has a variable switching frequency, we could not ensure the switching frequencies of both control scheme were equal. In Fig. 18(a), the output current is tracked for a 50% reduction in reference power at t_5 . First, it is noted that the output voltage acts as a three-level switching scheme. The subharmonic PWM scheme operates each H-bridge with bipolar modulation. Thus, two cascaded H-bridges operate like a three-level inverter. The new reference current is tracked within a few grid cycles, or around 50 ms. In Fig. 18(b), it is noted that the power draw of each H-bridge is roughly equal. The issue of unequal power draw is not inherent to this control scheme, as neither H-bridge operate with a zero-voltage output level. In Fig. 19, the same transient is applied to the proposed hierarchical MPC at t_6 . In Fig. 19(a), the new reference current is tracked in under 200 μ s. The control applies negative output voltage during this time to drive the current down to the updated reference. This modulation signal of the PR-based control scheme is unable to reduce sufficiently fast to match the transient response of the proposed control. In Fig. 19(b), the power draw characteristics are shown for the proposed control. There is only a slight distinction between the power draw of the two H-bridges. This is because the tertiary objective equalizes the rate of selection of redundant switching sequences, which mitigates selection bias in standard finite-set MPC. Furthermore, the current THD of the PR-based control was computed as 5.84% at reduced power, while the proposed control produced current with 3.92% THD. Thus, the proposed control realizes significantly faster transient response and improved power quality when compared to the traditional control scheme, but is able to exhibit similar power draw characteristics that traditional finite-set MPC cannot. Table III documents the main findings of the results section. As noted in Section IV, the difference in power draw can be reduced further in the proposed control by increasing the current tolerance ε_1 . Thus, in summary as presented in Table III, the proposed hierarchical MPC is highly superior in power balancing feature comparing to traditional MPC. In comparison to PR current control, the proposed hierarchical MPC is highly superior in current THD and dynamic response measures. Finally, the proposed hierarchical can be implemented in a straightforward manner which highlight its low control design effort requirement comparing to traditional MPC and PR current control techniques. This is due to the fact that the proposed controller mitigated the control parameter tuning effort which is needed in PR current control and weight factor tuning effort which is needed in traditional MPC.

VI. CONCLUSION

This article presented a new approach within the scope of finite-set MPC framework for power electronic converters.

The presented predictive control approach does not include a generic cost function. Rather, control objectives are ranked and given a cost tolerance, and switching sequences that do not meet the specified cost tolerance are removed from the optimization set of all the subsequent objectives. Not only does this remove the need to select among the equivocal weight factor design procedures but it also allows for the implementation of nonstandard control objectives. The proposed hierarchical MPC is leveraged to enhance the operation of the cascaded multilevel converter at grid-edge with a self-power balancing feature. This is demonstrated with an incrementing cost objective referred to as sequence frequency, which equalizes the controller's selection of redundant switching sequences. Applying this objective is shown to improve equality in behavior, power draw, among the H-bridges in the CMI. The theoretical analysis and experimental results demonstrate the difference in power draw among the H-bridges is reduced by over 75% when evaluated against a comparable implementation of conventional MPC. When compared to a traditional PR-based control scheme, the proposed control scheme is shown to exhibit similar power draw characteristics, while maintaining superior dynamic response and power quality. Finally, the tuning stage is mitigated in the proposed control scheme which makes it superior to both PR-based control and conventional MPC schemes. Illustration of concept via simulation and hardware experiments verify the control's ability to track its respective P and Q set points in case of a grid-fault as a required feature for grid-supporting power converters in the future high penetrated grid with power converters. Finally, it is demonstrated that the proposed hierarchical MPC computational cost is significantly reduced comparing to the traditional MPC formulation.

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