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The precise measurement of a capacitance difference or ratio in a digital form is very important for capacitive sensors, for CMOS process characterization as well as for the realization of precise switched-capacitor data converters, amplifiers and other circuits utilizing ratioed capacitors. This thesis introduces design techniques for on-chip capacitor ratio testing and sensor readout that utilize sigma-delta modulation and integrate the sensor capacitors into the modulator. Several single-ended circuits are introduced, and the correlated-double-sampling (CDS) technique is used in the circuits to reduce the non-ideal effects of opamps. Several simple calibration schemes for clock-feedthrough cancellation are also introduced and discussed. A fully-differential implementation is also described and various common-mode feedback schemes are discussed and analyzed. Simulation and experimental results show that these circuits can provide extremely accurate results even in the presence of non-ideal circuit effects such as finite opamp gain, opamp input offset and noise, and clock-feedthrough effect from the switches.

To verify the effectiveness of the circuits and simulations, two prototype chips containing a single-ended realization and a fully-differential one were designed and fabricated in a 1.2 μm CMOS technology. Two off-chip mica capacitors were used in the test circuits, and the measured results show that very accurate results can be obtained using these circuit techniques even with off-chip noise coupling and large parasitic capacitances.

High-Accuracy Circuits for On-Chip Capacitor Ratio Testing and Sensor Readout

by

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Bo Wang, Author

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High-Accuracy Circuits for On-Chip Capacitor Ratio Testing and Sensor Readout

Chapter 1. Introduction

The precise measurement of a capacitance difference or ratio in a digital form is very important for capacitive sensors, for CMOS process characterization as well as for the realization of precise switched-capacitor (SC) data converters, amplifiers and other circuits utilizing ratioed capacitors. Capacitive sensors are widely used in automation of process and manufacturing industries, in experimental engineering, in non-manufacturing areas such as environmental control (air, noise, water), in cars and household machines, etc. The development of sensor technology made high sensitivity sensors available, which need high-accuracy sensor interfaces. On the other hand, in SC circuit design, it is often necessary to obtain information about capacitor matching on the chip since circuit performance usually depends on how good the matching is. Thus, the accurate measurement of on-chip capacitor matching is necessary for the correct characterization of process. In circuit design, it is very helpful in determining design approaches and performance. Capacitor matching errors as small as 0.1% or better [1] have been achieved in some processes. It is obvious that the accuracy of the measuring system needs to be better than that.

This thesis introduces design techniques for high-accuracy on-chip capacitor ratio testing and sensor interfaces that utilize sigma-delta modulation. Several single-ended circuits are introduced, and the correlated-double-sampling (CDS) technique is used in the circuits to reduce the non-ideal effects of opamps. Simple calibration schemes for clock-feedthrough cancellation are also introduced and discussed. A fully-differential implementation is also introduced and various common-mode feedback schemes are discussed and analyzed. Simulation results show that these circuits can provide extremely

accurate results even in the presence of non-ideal circuit effects such as finite opamp gain, opamp input offset and noise, and clock feedthrough effect from the switches. One single-ended and one fully-differential prototype have been developed and tested. The measurement results confirmed the highly accurate results obtained from the simulations.

1.1 Motivation

In high-performance SC circuit design, knowing the matching error of capacitors is usually required before the real design begins. For example, in SC filter design, the matching of capacitors affects the passband ripple, passband edge, stopband attenuation and other filter performance. In Nyquist-rate SC analog-to-digital (A/D) and digital-to-analog (D/A) converters, imperfect matching of capacitors causes integral nonlinearities (INL) and differential nonlinearities (DNL), and hence, generates harmonic distortions. The matching of capacitors then determines the best achievable signal-to-distortion ratio (SDR) without using calibration or dynamic matching techniques. Even in SC sigma-delta modulators, which are usually less sensitive to circuit imperfections, capacitor mismatch causes errors in realizing the noise transfer functions, and can greatly reduce the signal-to-noise ratio (SNR) in multi-stage modulators. Capacitor mismatch also causes gain errors in SC amplifiers. Hence, the accurate measurement of capacitor mismatches can help the designer to evaluate the potential of a certain circuit configuration to meet its goal or to decide if extra calibration or dynamic matching techniques are needed for a given specification.

The major advantages of capacitive sensors are high sensitivity, simplicity of construction, high frequency response, small size, and small mechanical loading effect [2]. Capacitive sensors are used in many applications, such as liquid-level gauge, pressure measurement, accelerometers, microflowmeters in medical industrial process control, shaft torque measurement, capacitive person detector, etc. Accurate sensor readout makes it

possible to achieve accurate control of processes, and to provide crucial information on the working condition of devices or machines, so that proper actions may be taken before problems occur. In some applications, extremely high accuracy is needed.

Normally, the mismatch between two matched capacitors with the same nominal values is obtained by measuring the ratio of the two capacitors and seeing how much it deviates from 1.0, or by measuring the ratio of the capacitance difference and the total capacitance. In sensor applications, usually one sensor capacitor is measured against a reference capacitor, or both sensor capacitors may change and the mismatch between the two capacitors is measured. The sensor is usually connected to an interface circuit so that the data can be collected and analyzed. It is advantageous if the sensor and the interface are integrated together, so that no external connections are needed, and the noise is reduced.

Oversampling sigma-delta modulation has been well known as a technique to achieve high resolution converters without requiring high-accuracy components. Over 18-bit accuracy A/D converters have been reported [3][4][5] without using expensive laser trimming or calibration processes. Higher accuracy may be achieved by using a high-order modulator or by increasing the oversampling ratio. Since for fixed capacitor measurements the signal is at DC, while the signal bandwidth for sensors is usually below 1 kHz, the oversampling technique is very suitable for signal conditioning. This thesis introduces design techniques for high-accuracy on-chip capacitor ratio testing and sensor readout, utilizing oversampling sigma-delta modulation. Several circuits have been developed and simulation results are presented. Experimental results for two IC implementations are also shown.

1.2 Thesis Organization

Chapter 2 introduces some characteristics of capacitor ratio measurements and capacitive sensor readouts. Some existing techniques for capacitor ratio measurement are discussed.

In Chapter 3, the fundamentals of oversampling delta-sigma modulation are briefly reviewed. Then the design of high-accuracy circuits for capacitor ratio testing and sensor readout utilizing sigma-delta modulation is presented. Several structures are introduced and analyzed. Simulations results are also shown.

In Chapter 4, some non-ideal circuit effects are discussed and analyzed. The influence of these non-ideal effects on high-accuracy sensor readout is also discussed and some solutions are presented.

Chapter 5 introduces a single-ended implementation suitable for fixed capacitor ratio testing or differential capacitive transducer readout. Design approaches to minimize non-ideal effects are presented. Simulation and measurement results obtained from the prototype are also shown.

In Chapter 6, a fully-differential implementation is presented. Existing and new common-mode feedback schemes are discussed and analyzed. Simulation and experimental results are also described.

Finally, Chapter 7 summarizes the work and suggests some future work for this research.

Chapter 2. Background: Capacitor Ratio Testing and Sensor Readout

In this chapter, a review of the characteristics of capacitive sensors is given. Following that, the limitations for high-accuracy capacitor ratio measurement are discussed. Existing techniques for capacitor ratio measurement and sensor readout are illustrated and analyzed.

2.1 Introduction to Capacitive Sensors

Accurate measurement of capacitor ratios is very important for capacitive sensor interfaces. The measurement for fixed capacitors can be performed measuring DC signals, while the continuous varying of sensor capacitors requires readout circuits that can work for a certain bandwidth. Thus, the technique for measuring on-chip capacitor mismatches which usually measures DC signals may not be suitable for capacitive sensors. On the other hand, usually sensor readout circuits can be used for fixed capacitor ratio testing. Next, structures and characteristics of capacitive sensors will be discussed.

A capacitive sensor is often called a capacitive transducer because it usually converts a signal from one physical form to a corresponding signal, which is the variation of capacitance here. In this thesis, we use both terms. A capacitive transducer provides a usable electrical output for a specified measurand. The term measurand stands for the quantity, property, or condition that is to be measured; for example, the pressure in a manifold, the roughness of a surface, or the number of parts on a conveyer [2]. The transducers can be divided into two categories: input transducer (physical signal to electric signal) and output transducer (electric signal to display or actuation). The trend, particularly in robotics, is toward using the term "sensor" to refer to the input transducer while "actuator" refers to the output transducer [6]. A capacitive transducer converts a change in the position of the electroconductive plates forming a capacitor, or a change of

the properties of a dielectric between the plates, into an electrical signal. An illustration is shown in Figure 2.1. The capacitance of such an element is written as follows

$$C = \frac{\varepsilon A}{d}, \tag{2.1}$$

where ε is the permittivity of the dielectric, A is the area and d is the distance between the plates. Alternation of any of the three physical parameters causes a change of the capacitance. For instance, the top plate can be displaced along the x- and y-axes, providing a signal proportional to the displacement. If ε is affected by temperature or moisture, the magnitude of C responds to these variables. The displacement of plates parallel to their planes gives the change of the overlapping area (A). It is usually used to measure big displacements (>1 mm). A shift in longitudinal position with a variation of d is typical for measurements of small displacements (<<1 mm). With mechanical elements linked to the moving plate or with a special substance placed between the plates, the element can be adapted for measuring displacement, size, proximity to a target, velocities, forces, accelerations, vibrations, sound intensity, pressure, and levels of liquid [2]. It is widely used in microelectronic sensors due to its simple structure and ease of microfabrication. Two recent examples are micromotors [7] and accelerometers [8].

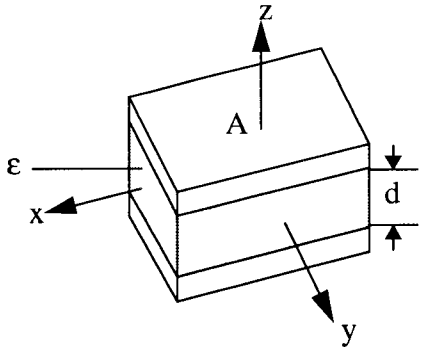
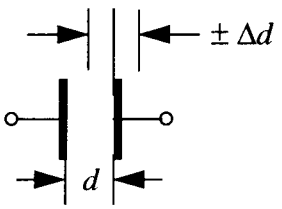
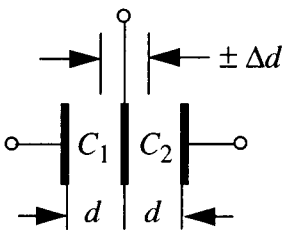
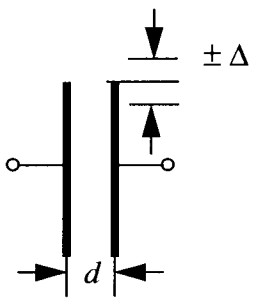
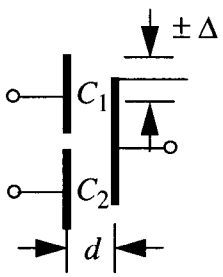


Figure 2.1: Model of capacitive element.

There are many different structures of capacitive transducers. For simplicity, only a few are illustrated in Table 2.1. The differential structures allow the reduction of the nonlinearity of the transfer characteristic and electrostatic force on the moving part. It is also helpful in the compensation for temperature drift [2].

Table 2.1: Structures of capacitive transducers.

Index	Variable Parameter	Structure	Capacitance
(a)	Gap d		$C = \frac{\varepsilon A}{d \pm \Delta d}$
(b)	Gap d for a differential scheme		$C_1 = \frac{\varepsilon A}{d \pm \frac{1}{2}\Delta d}$ $C_2 = \frac{\varepsilon A}{d \mp \frac{1}{2}\Delta d}$
(c)	Area A		$C = \frac{\varepsilon(A \pm \Delta A)}{d}$
(d)	Area A for a differential scheme		$C_1 = \frac{\varepsilon\left(A \pm \frac{1}{2}\Delta A\right)}{d}$ $C_2 = \frac{\varepsilon\left(A \mp \frac{1}{2}\Delta A\right)}{d}$

2.2 Limitations on High-Accuracy Capacitor Ratio Measurement

Capacitive transducers have many features which make them suitable for a wide range of applications. A capacitive transducer may have high sensitivity, wide bandwidth, small size and small mechanical loading effect. It can operate at high temperatures and it is insensitive to permanent fields, A capacitive transducer can have good linearity, repeatability, stability and resolution. However, a capacitive sensor/transducer itself does not provide any useful information without a readout interface which detects the change of capacitance and converts it into electric signals for measurement and processing. In order to get accurate representation of the measurand, both the capacitive transducer and the readout interface need to have high accuracy. Since the accuracy of the capacitive sensor is not the topic of this thesis, it is assumed that only the interface is the limiting component for high-accuracy capacitor ratio measurement.

The capacitive sensor may be separate, or the sensor and the interface may be together on the same chip. The development of silicon technologies has made possible the integration of microsensors and even micromotors with electronic circuits. A monolithic solution for a capacitive sensor and its interface is advantageous because it has no outside interconnects which usually introduce noise, and the cost can be greatly reduced. We will mainly address the case when the sensor is in a separate part, because then the sensor is usually more accurate, and the interface tends to have more noise because of the interconnections.

There are many factors that can reduce the accuracy of the sensor interface. There are also several dominant factors. The first one comes from the interconnects between the sensor and the interface circuit. The interconnects act as antennas and can pick up interference from the outside environment. Since the signal is also transmitted through the

interconnects, any noise pickup reduces the accuracy. By using shielded matching cables, the interference can be greatly reduced. But using cables does not solve the problem of parasitics; in fact, cables tend to generate more parasitic capacitance. The parasitic capacitance is 10 pF/cm for a typical shielded cable [9]. The parasitic capacitances associated with a cable are shown in Figure 2.2. Because of the shielding of the cable, C_{par} is greatly reduced [10]. However, C_{cable1} and C_{cable2} are usually of the same order as the sensor capacitor C_s and can usually cause errors in the measurement, unless the interface circuit is insensitive to parasitic capacitances.

The noise generated by the interface circuit may be the dominant factor in reducing the measurement accuracy. Since usually opamps and comparators are used as building blocks in the sensor interface, the noise generated by them affects the accuracy of the circuit. If only a single transistor is used, as in the floating gate test structure shown in the next section, the performance of the transistor and its parasitic gate capacitance limit the precision. In switched-capacitor implementations, the switches generate thermal noise and noise due to clock-feedthrough and charge injection [11], and that is usually the dominant noise source in the interface circuit. In order to achieve very high accuracy, the noise due

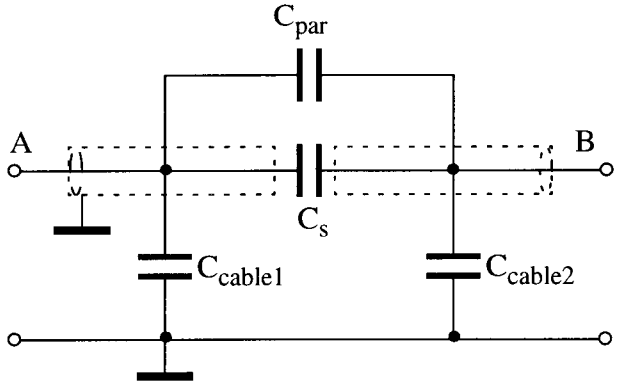


Figure 2.2: Cable parasitic capacitance.

to these components must be kept very low. This leads to larger area which increases the cost. The influence of the noise due to the opamps and switches in switched-capacitor realizations will be discussed and analyzed in Chapters 4 and 5.

The noise coupling to the interface circuit also affects the performance. In addition to the noise generated by the interface circuit itself, there might be noise coupled from various noise sources. One example is the power-supply-coupled noise. The power supply is usually noisy and if the designer is not careful enough, the noise from the power supply might greatly reduce the accuracy. The noise may also come from the substrate if the interface circuit is on a noisy substrate, such as in a big chip with a large amount of digital circuitry. For high-precision readout, the capacitively coupled interference should also be considered [12]. Between any pair of conductors there is a finite capacitance. The interference may come from the output path to the input path, or from the other path in a differential circuit.

In addition to the factors discussed above, some other effects also need to be considered. Magnetic field, for example, might cause interference. An induced electromotive force in the conductors due to the alternating magnetic field can create a spurious signal. The electric field from a close-by power generator may also cause a 60 Hz/50 Hz spurious signal. Shielding from electromagnetic fields is usually needed to reduce this interference. Last, but not the least, it should be noted that in order to get a high-accuracy readout, the test setup needs to be carefully designed so that noise coupling is minimized. The testing which involves human body interference may be the limiting factor too. Data averaging is necessary to minimize the short term random errors. Temperature control during the testing is also important since the capacitive sensor has a certain temperature coefficient. In Chapter 5, issues for high-precision testing are addressed and techniques for reducing the noise in the printed circuit board (PCB) are presented.

2.3 Existing Techniques for Capacitor Ratio Testing and Sensor Readout

The techniques for capacitor ratio measurements differ in various applications. Many results have been reported, and the accuracy of the measurement varied from 10^4 ppm to 35 ppm.

2.3.1. Direct Measurements

The immediate solution to measure capacitor ratios is to use capacitance meters. The ratio between two capacitors can be obtained by simply measuring the capacitances with the meter. This method is only suitable to measure discrete capacitors and when the capacitors to be measured are large capacitances, usually bigger than 10 pF. It is very sensitive to the parasitic capacitances due to the probes, and the parasitic capacitance strongly depends on the length of capacitor leads and where the probes are connected to the leads. Hence, large random errors exist and in order to get a precise result, a lot of data are needed for averaging. Usually, an LCR bridge is used for direct measurement since it provides a balance and reduces the effect of parasitics [13]. Capacitor bridges can also be used [14]. The accuracy of direct capacitor measurements is normally limited to 0.1% and calibration is usually needed [13].

The direct measurement method is not well suited for small on-chip capacitor measurement when the parasitic capacitance due to the leads or probes is much larger than the tested capacitors.

2.3.2. Floating Gate Technique

The floating gate technique [15] was introduced as a method for capacitor ratio measurement in a DC parametric test environment. Figure 2.3 shows the structure. C_1 and C_2 are the tested capacitors, M_1 is a PMOS transistor and I is a DC current source. C_{par} is

the parasitic capacitance at the gate of the MOSFET. V_{in} is a DC voltage source and C_1 and C_2 form a voltage divider. M_1 is configured as a source follower and the output V_{out} is monitored. Assuming that the voltages at the gate and source of M_1 are big enough so that M_1 is in its saturated strong inversion region, the current-voltage (*I-V*) characteristics of M_1 can be approximated by the following equation [15]

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{SG} - |V_T|)^2(1 + \lambda V_{SD}) \cdot \tag{2.2}$$

Here, μ_n, C_{ox}, W, L and λ may be considered fixed for a given transistor M_1. V_{GS} is the gate voltage and V_{DS} is the voltage across the drain and source. V_T is the threshold voltage and it may vary when V_{DS} changes. To show the relationship between V_{GS} and V_{DS}, Eq. (2.2) can be rewritten as

$$V_{SG} = V_S - V_G = \sqrt{\frac{2I}{\mu_n C_{ox}\frac{W}{L}(1 + \lambda V_{SD})}} + |V_T| \text{ , and} \tag{2.3}$$

$$V_S = V_G + \sqrt{\frac{2I}{\mu_n C_{ox}\frac{W}{L}(1 + \lambda V_{SD})}} + |V_T| \cdot \tag{2.4}$$

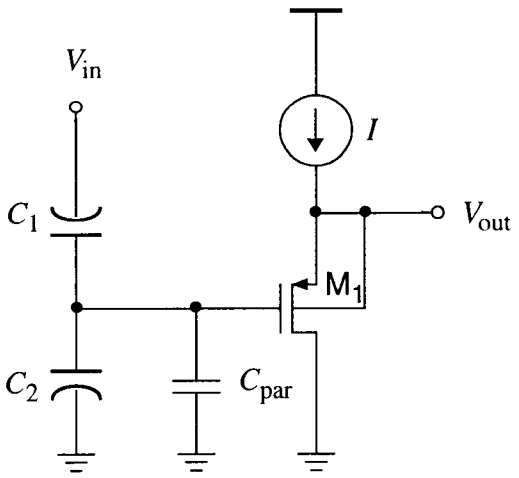


Figure 2.3: Floating gate capacitance measurement technique.

For the circuit shown in Figure 2.3, Eq. (2.4) becomes

$$V_{out} = \frac{C_1}{C_1 + C_2} V_{in} + \sqrt{\frac{2I}{\mu_n C_{ox} \frac{W}{L}(1 + \lambda V_{out})}} + |V_T| , \qquad (2.5)$$

where C_{par} is ignored. If the length L of M_1 is large, λ is very small and may be ignored for simplicity. Also V_T may be considered as constant if the variation of V_{SD} is small. Then it can be see that there is a linear relationship between V_{out} and V_{in}, and the slope is $C_1/(C_1+C_2)$. The capacitor ratio can be measured by applying at least two different input voltages and obtaining the slope of the output characteristic.

The accuracy of the floating gate method is usually around 0.1% [15] because of some fundamental limitations. One problem is the leakage current through the gate of the PMOS transistor. The leakage current can cause error in the voltage divider and may greatly reduce the readout accuracy. The leakage current can be reduced by using small size transistors. Another one is the effect of C_{par}, which makes the effective C_2 bigger and generates systematic error. To make C_{par} smaller, the top plates of the capacitors should be connected to the gate. The third limitation is the channel modulation effect of the MOS transistor. As shown in Eq. (2.5), non-zero λ causes a nonlinear factor and it causes the slope to become nonlinear. By increasing L, λ may become smaller, but this also increases C_{par}. One way to reduce this channel modulation effect is to reduce the change of V_{out} by applying smaller current I. But then the accuracy of reading the output voltage will be reduced. The fourth limitation is the voltage-dependent characteristics of the capacitors because the two capacitors are biased in opposite polarity. Thus, this method is only suitable for measuring low voltage-coefficient capacitors. The variation of V_T due to the change of V_{out} is also a limiting factor. Another limitation is that Eq. (2.5) is only an approximation and the actual characteristic differs in different bias conditions. That limits the accuracy fundamentally.

The basic floating gate method can be modified to a so-called double-slope algorithm [15]. In fact, it can be regarded as the floating gate method with a calibration scheme to cancel the systematic errors. By switching the location of C_1 and C_2, two different slopes (S_1 and S_2) are obtained, each corresponding to a different capacitor ratio. The capacitor ratio can be calculated from the following equation

$$2\frac{S_1 - S_2}{S_1 + S_2} = 2\frac{C_1 - C_2}{C_1 + C_2} = \frac{\Delta C}{C}, \tag{2.6}$$

where $C = (C_1 + C_2)/2$ is the nominal value of two matched capacitors and ΔC is their difference. Hence, this method is suitable for measuring capacitor mismatches. It was reported in [15] that by taking 144 observations, the measured standard deviation was 50 parts per million (ppm).

2.3.3. Capacitor Ratio Represented by Charge-to-Voltage and A/D Binary Codes

This technique [16] uses an A/D to represent the capacitor ratio. The reference input to an A/D is related to the sum of two capacitances, while the signal input to the A/D is proportional to one capacitor. The block diagram is shown in Figure 2.4. It is designed for

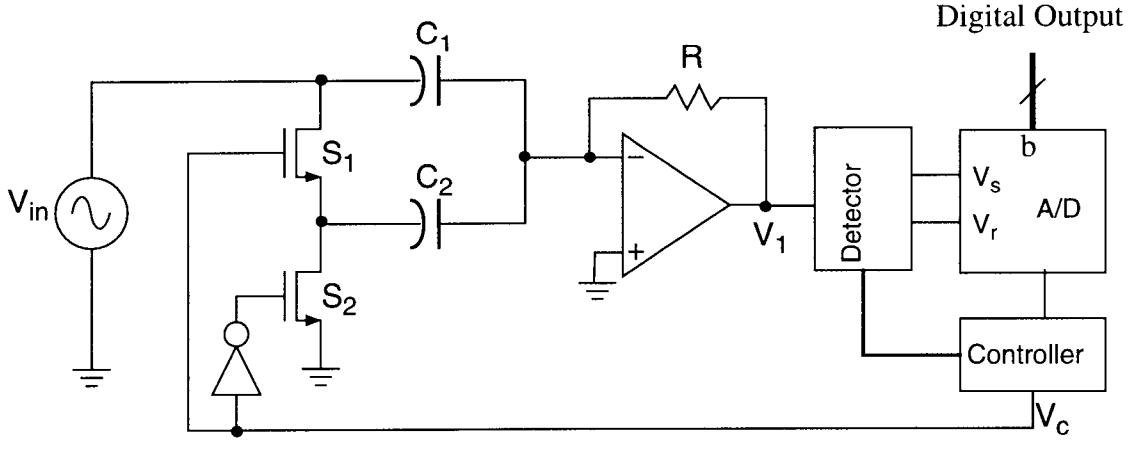


Figure 2.4: Block diagram of the circuit using A/D to represent the capacitor ratio.

the differential capacitive transducers as shown in Table 2.1(b) and (d). The first stage is the capacitance-to-voltage (C/V) converter. When the controller output voltage V_c is high, both C_1 and C_2 are connected to V_{in} and the opamp output is

$$V_1 = -s(C_1 + C_2)RV_{in} . \tag{2.7}$$

On the other hand, when V_c is low, only C_1 is connected to V_{in} and the opamp output becomes

$$V_1 = -sC_1RV_{in} . \tag{2.8}$$

The detector converts the opamp output to a DC voltage. When V_c is high, the detector output is sampled-and-held and connected to the reference input of a n-bit A/D converter. When V_c is low, the sampled-and-held detector output is connected to the signal pin of the A/D converter as the DC input voltage. Thus, the A/D converter binary output b is appoximately

$$b \approx \frac{-C_1RV_{in}}{-(C_1 + C_2)RV_{in}} \cdot 2^n = \frac{C_1}{C_1 + C_2} \cdot 2^n . \tag{2.9}$$

Hence, the output binary data of the A/D is directly proportional to the capacitor ratio. Rearranging Eq. (2.9), the following equation is obtained

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{2C_1}{C_1 + C_2} - 1 \approx \frac{b}{2^{n-1}} - 1 . \tag{2.10}$$

From Table 2.1(b), it can be derived that

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{\Delta d}{2d} . \tag{2.11}$$

and from Table 2.1(d), a similar equation can also be derived:

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{\Delta A}{2A} . \tag{2.12}$$

Thus, there is a linear relationship between the displacement in length or area and the A/D

output binary code. The method shown in Figure 2.4 is then suitable for use in differential capacitive transducers similar to those shown in Table 2.1(b) and (d).

The measurement accuracy strongly depends on the accuracy of the C/V converter, of the detector, and of the sample-and-hold circuit. The effects of several error sources were discussed in [17]. The accuracy of the A/D should be chosen so that it is better than the desired accuracy of the measurement. A 16-bit A/D converter was used in the discrete realization. The measured standard deviation was 0.21 fF for 6 pF capacitors, which is equivalent to a relative error of 35×10^{-6} (35 ppm).

Another approach to realize the C/V converter is to use SC circuitry. A simple C/V converter may be just a SC amplifier, as depicted in Figure 2.5. The input to the amplifier is a DC signal, and the output is given by

$$V_{out} = -\frac{C_2}{C_1} V_{in}. \tag{2.13}$$

Therefore, by measuring the output voltage, the capacitor ratio C_2/C_1 can be determined.

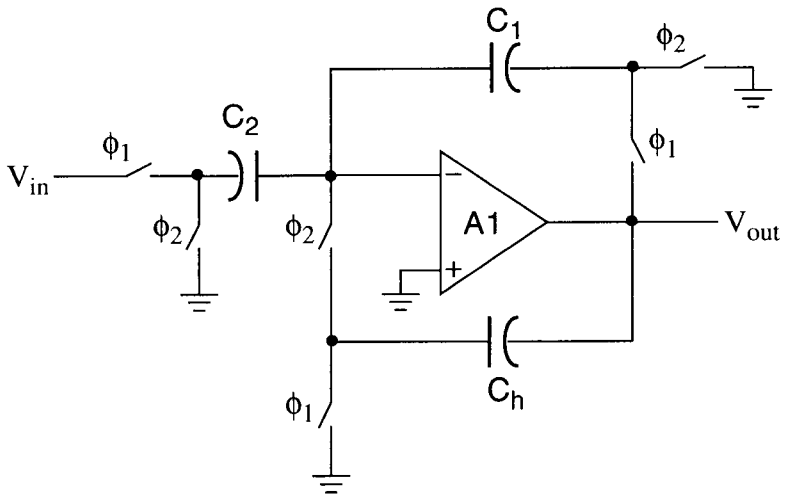


Figure 2.5: A SC amplifier with gain and offset compensation.

This structure is stray insensitive and allows the tested capacitors to be off-chip. The accuracy of the readout is also insensitive to some non-ideal effects of the opamp, such as 1/f noise, input offset voltage and finite-gain effect.

SC integrators are another alternative to realize the C/V converter. Figure 2.6 illustrates an example [18]. The transfer function can be derived as the following

$$H(z) = \frac{V_{out}}{V_{in}} = \frac{C_2}{C_1 - (1 - z^{-1})C_f} . \tag{2.14}$$

Hence, in steady state, $C_2 / C_1 = V_{out}/V_{in}$.

From Eq. (2.13) and Eq. (2.14), it can be seen that the SC C/V converters can be used for capacitor mismatch measurement or for capacitive sensors, where C_1 is a reference capacitor and C_2 is the sensor capacitor. By using gain-and-offset compensation schemes, the accuracy of SC C/V converters can be as good as 80 dB (100 ppm). An A/D converter is usually needed for data analysis and processing. One of the main limitations on the

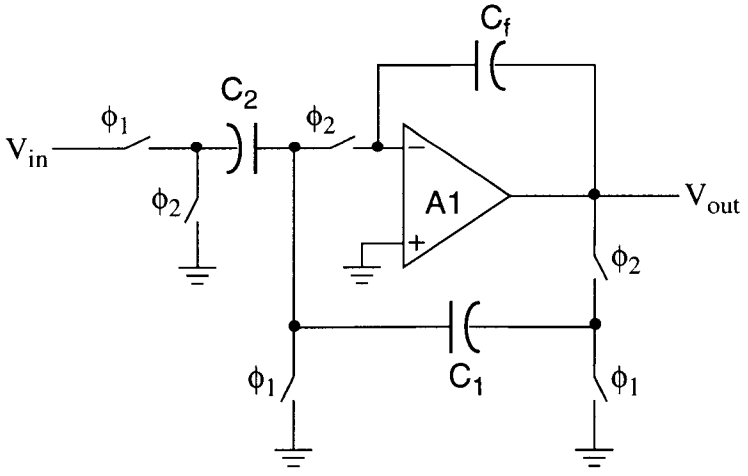


Figure 2.6: A SC integrator for capacitor ratio testing.

accuracy of the SC realization is the clock-feedthrough effect which will be discussed in detail in Chapter 4.

2.3.4. Measurement Based on Capacitance-to-Frequency Conversion

The capacitor ratio can also be measured by incorporating the tested capacitors in a oscillator and measure the output frequency or period. This technique can be regarded as capacitance-to-frequency conversion. A switched-capacitor relaxation oscillator was introduced by Martin [19] and is shown in Figure 2.7. The oscillation frequency is given by

$$f_o = \frac{C_2}{C_1}\frac{f_{clk}}{4} \quad . \tag{2.15}$$

where f_{clk} is the clock frequency and $V_{dd} = V_{ss}$ is assumed. Hence, the capacitor ratio C_2/C_1 can be obtained by measuring the oscillating frequency f_{out}. The circuit is insensitive to stray capacitances so that C_1 and C_2 can be off-chip and large parasitic due to the shielding cable can be allowed. However, the above equation is based on the assumption that $C_2 >> C_1$ [19]. Thus, this circuit can be used only when $C_2 >> C_1$,

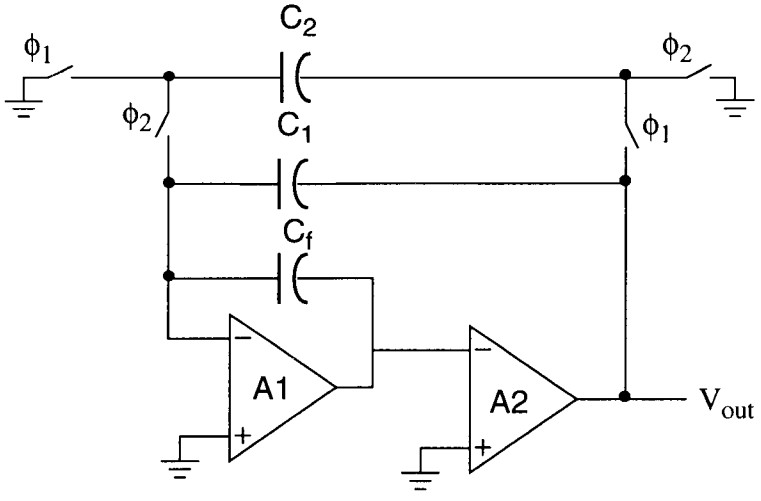


Figure 2.7: A SC stray insensitive relaxation oscillator.

otherwise, the accuracy will be greatly reduced. It is not suitable for measuring the differential capacitive transducers shown early in this chapter because the capacitors C_1 and C_2 in this circuit do not have a common node. The oscillator shown in Figure 2.7 can be modified and the switched capacitor C_2 replaced by a resistor, as shown in Figure 2.8. C_1 and C_2 are the two capacitors tested and C_{off} is the parasitic capacitance. When "select" outputs of the microcontroller are 0, the NAND gates are disabled and the oscillator has a period T_{off} [20], where

$$T_{off} = 4RC_{off}. \tag{2.16}$$

When the NAND gate associated with C_1 is selected, the period becomes

$$T_1 = 4R(C_{off} + C_1) = 4RC_1 + T_{off}. \tag{2.17}$$

When the NAND gate associated with C_2 is selected, the period is

$$T_2 = 4R(C_{off} + C_2) = 4RC_2 + T_{off}. \tag{2.18}$$

From Eq. (2.17) and Eq. (2.18), it can be shown that

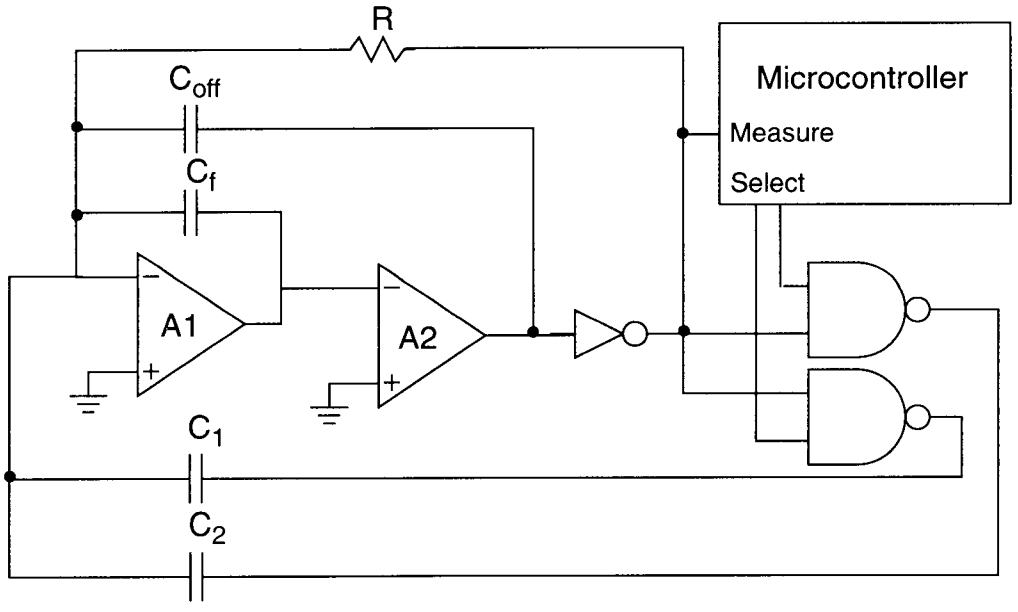


Figure 2.8: Modified Martin oscillator with microcontroller.

$$\frac{C_2}{C_1} = \frac{T_2 - T_{off}}{T_1 - T_{off}} \cdot \qquad (2.19)$$

The microcontroller is used to select the different capacitors. It also measures the period and calculates the capacitor ratio according to Eq. (2.19). One drawback of this scheme is that it requires all three measurements to be performed in exactly the same way. This means that the total parasitic capacitance as seen from A1 must not change during the measurements. This problem can be solved by using the so-called double-sided multiplexing scheme. In order to get an accurate measurement of the period, averaging of a large number of oscillator periods is needed. Measured standard deviation was 50 aF for a 2 pF capacitor and the total measurement time was 300 ms in [20].

2.3.5. Techniques Based on Charge Balancing

This technique converts the capacitance of the sensor into a charge, and uses successive approximation to achieve charge balancing. It combines the conditioning circuit and the A/D converter, and the output is similar to that of a regular successive approximation A/D converter.

Figure 2.9 shows the simplified diagram of an capacitive sensor interface using a sample/hold circuit and a charge balancing A/D converter [21]. The first stage is just a SC amplifier which provides an output charge $Q(x) = -V_r C(x)$, where $C(x)$ is the capacitive sensor and V_r is the reference voltage. Q_c is used to compensate for the DC charge in $Q(x)$ due to any constant offset in $C(x)$. Assuming that (say) a change of pressure causes $C(x)$ to increase by $\Delta C(x)$, then during each clock cycle a negative charge $Q = Q(x) - Q_c = -V_r \Delta C(x)$ is transferred to C_f and causes the integrator output V_{out} to increase. When the integrator output goes from negative to positive, ϕ_c changes from 0 to 1 and a positive charge $Q_r = V_r C_r$ flows to C_f and make V_{out} negative again. This process repeats for 2^n clock cycles

(duration of the hold state) and the counter output number becomes m at the end of the hold state. Then it can be derived [21] that

$$\frac{m}{2^n} = m_1 2^{-1} + m_2 2^{-2} + \ldots + m_n 2^{-n} = \frac{\Delta C(x)}{C_r} . \tag{2.20}$$

Thus, there is a linear relationship between the variance of sensor capacitance and the digital number. However, a lookup table is needed to get a linear relationship between the digital number and the measurand when the sensor capacitance does not change linearly as the pressure changes.

Another scheme for capacitive sensor measurement is shown in Figure 2.10 [22]. Its operation relies on the charge redistribution and balancing. A preamp is placed before the comparator to help detect small voltage difference. The switching sequence starts with grounding all the nodes, and the capacitors are discharged. The DAC output is also set to ground. Then the switch S_3 is closed and S_1 is switched to V_{ref}. So the total charge at the top plate of the capacitors is $-V_{ref}C_s$. Next, S_3 is opened, and subsequently C_s is connected

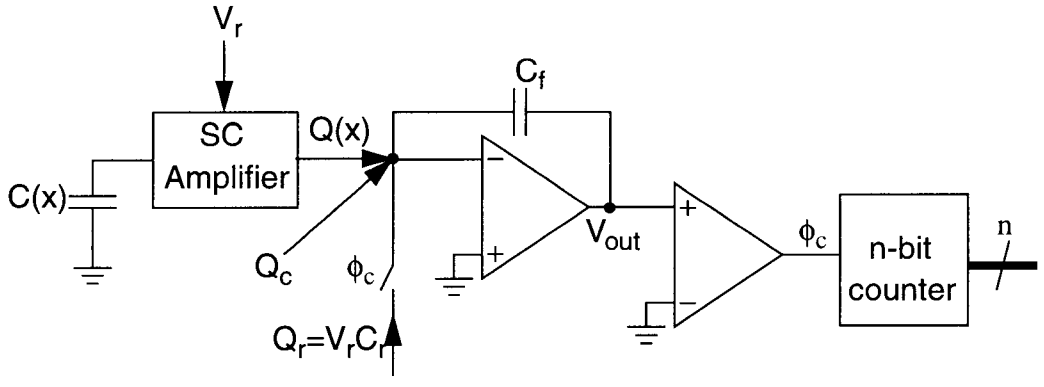


Figure 2.9: A capacitive pressure sensor interface.

to ground and V_{ref} is applied to C_r. This causes the charge redistribution between C_s and C_r, and V_x changes from 0 to

$$V_x = \frac{C_r - C_s}{C_s + C_r + C_p}. \tag{2.21}$$

Then the successive approximation (SAR) process begins and the operation is the same as for a SAR A/D converter. Hence, at the end of the conversion, V_x is close to 0 and the output voltage of the DAC becomes

$$V_{DAC} = \frac{C_s - C_r}{C_c} V_{ref}. \tag{2.22}$$

Since V_{DAC} is the analog representation of the digital data, the digital data has the same relationship scaled with V_{ref}. This technique can be used to measure capacitance difference between C_s and C_r, and it can also be used for capacitor ratio testing where C_s is the sensor capacitor and C_c is the reference capacitor. C_r can be regarded as an offset capacitor which compensates for the constant part of the sensor capacitor C_s.

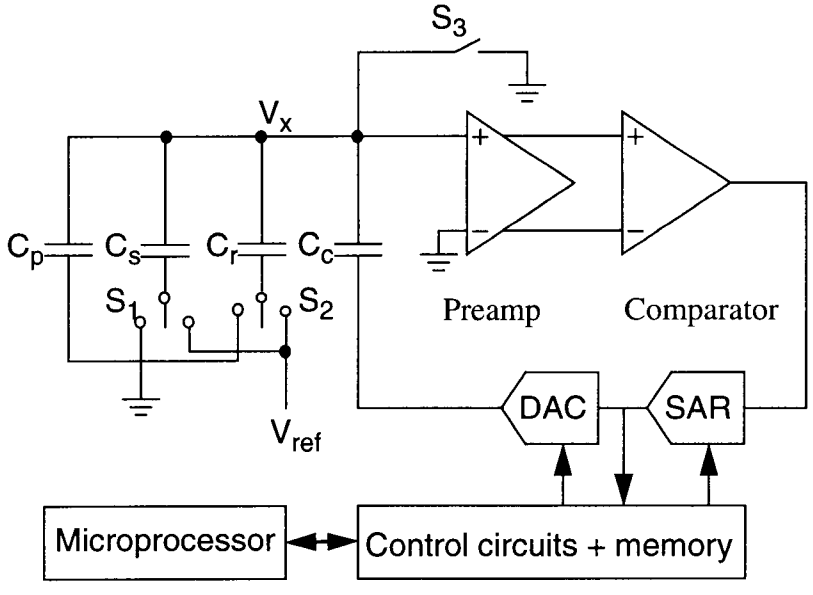


Figure 2.10:Charge-redistribution capacitance difference detection topology.

By using analog calibration, the effect of clock feedthrough due to S_3 and thermal noise of S_3 can be reduced [22]. During the power-up period, the error due to the clock feedthrough of S_3 and input offset of the preamp is measured and stored in the memory. Then during the measurement period, the output of the DAC is preset to the error voltage instead of ground and by doing this the error is removed from the final output data. A digital calibration scheme was introduced [23] to cancel the input offset and $1/f$ noise of the preamp. The kT/C noise of the switch S_3 can also be reduced by averaging the data. Capacitance resolution of 31 aF out of 100 fF capacitors was achieved using the digital calibration technique [23].

2.4 Conclusions

Capacitive sensors are widely used in industry, as well as in environmental control and consumer products. Usually sensor interfaces are needed to convert the physical variations into electric form so that the variations can be accurately observed. In the past, various interface circuits have been introduced to provide capacitor ratio or difference measurement. However, the accuracy of most of the interface circuits is limited by the noise from the circuit components, and demand for higher accuracy requires new techniques. Oversampling sigma-delta modulation has been well known to be effective in achieving high-resolution A/D converters under low frequency range. By using oversampling, the sensitivity to noise from circuit components, as well as the errors due to component matches can be greatly reduced. This leads to the design of interface circuits that utilize oversampling sigma-delta modulation to achieve very high accuracy in capacitive sensor interface circuits.

Chapter 3. Capacitor Ratio Readout Circuits Using Oversampling Delta-Sigma Modulation

In the last chapter, various techniques for capacitor ratio or difference measurement have been discussed. Some techniques are only good for fixed capacitor ratio measurement, and some are suitable for capacitive sensor interfaces where the sensor capacitors vary continuously. This chapter introduces new techniques for very high-accuracy capacitor ratio measurements. Utilizing oversampling delta-sigma modulation, several new structures with 1-bit digital output are presented. They are suitable for both on-chip capacitor mismatch testing or capacitive sensor readout. Some background of oversampling delta-sigma modulation is reviewed first. Then the SC realization of the delta-sigma modulator is briefly discussed. That is followed by the introduction of new structures for capacitor ratio measurements based on first-order modulation. Structures based on higher-order modulations are also presented and simulation results in SWITCAP2 are shown.

3.1 Oversampling Delta-Sigma Modulation: Background

Oversampling delta-sigma modulation has become popular in recent years because it avoids many of the difficulties encountered with conventional methods for analog-to-digital (A/D) and digital-to-analog (D/A) conversion. Oversampling A/D converters can use very simple and high-tolerance analog components and achieve high-resolution representation of relatively low-frequency analog signals. In instrumentation applications such as the sensor interfaces, the band of interest is usually at low frequencies, thus by incorporating delta-sigma modulation into the sensor interfaces very high-accuracy interface circuit can be obtained. Here, the basic principle is discussed as a background for the new structures proposed for capacitor ratio measurements. More description and analysis on the theory and design of delta-sigma data converters can be found in [24][25].

3.1.1. Quantization and Oversampling

Quantization of amplitude and sampling in time are at the heart of all A/D converters [25]. Periodic sampling at rates more than twice of the signal bandwidth need not introduce distortion, but quantization does. Usually a smart sensor interface needs to provide digital output for calibration, analysis and control, and many interface circuits use A/D converters. Quantization noise is one of the dominant noise sources in A/D converters.

The most commonly used quantization is uniform quantization, which has equal quantization steps denoted as Δ. An example is shown in Figure 3.1(a), where the

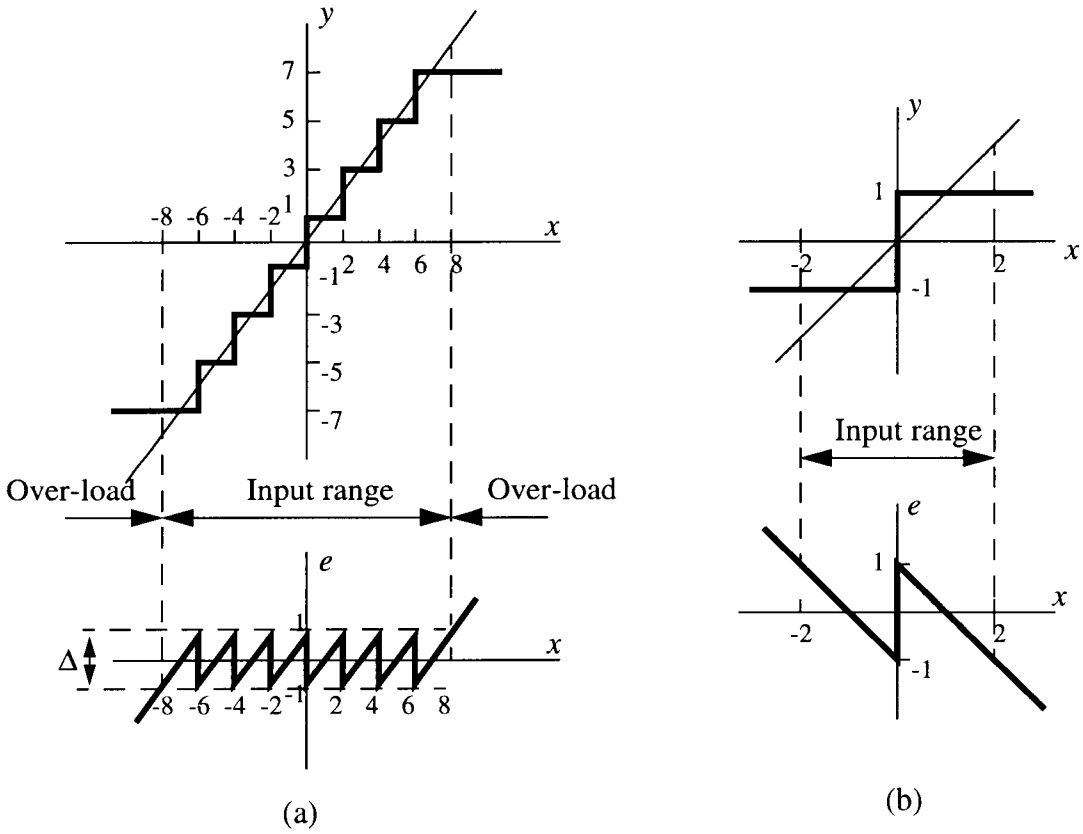


Figure 3.1: (a) An example of uniform multi-level quantization characteristic. (b) Single-bit quantization.

continuous amplitude signal x is rounded off to 8 discrete levels and e is the quantization error. It is useful to represent the quantized signal y by

$$y = Gx + e, \tag{3.1}$$

where the gain G is the slope of the straight line that passes through the center of the quantization characteristic. Other non-ideal effects, such as DC offset and non-linear gain error, can be taken into account in Eq. (3.1). The above consideration remains applicable to a 1-bit quantizer, as illustrated in Figure 3.1(b), but in this case the choice of gain G is arbitrary.

If there are total 2^n quantization levels, we talk about an n-bit quantization. For example, the one shown in Figure 3.1(a) is a 3-bit quantizer. If the range of the output amplitude is normalized to ± 1, the quantization step, or the value of the least-significant-bit (LSB) is then given by $\Delta = 2/(2^n - 1)$. The error e is completely defined by the input, but if the input changes randomly between samples by amounts comparable to or greater than Δ, and without saturating the quantizer, then e can be regarded as a random variable uniformly distributed in the range $\pm\Delta/2$. Under these assumptions, the quantization error e can be treated as white noise, and its mean-square value, i.e. the power of the quantization error is given by

$$\sigma_e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}. \tag{3.2}$$

As can be shown by simple calculation, the peak signal-to-noise ratio (SNR) of an ideal n-bit linear quantizer with a full-scale sine-wave input is approximately $6n$ dB.

In conventional Nyquist rate ADCs or DACs, higher resolution is achieved by using smaller step sizes (i.e. increasing n) which requires precisely matched analog components.

As a result, the practical limit with current (untrimmed) circuit techniques is about 14 bits of resolution. Trimmed circuits can achieve 16 or more bits of resolution, but are expensive.

Oversampling [25] is simply the process of sampling faster than the Nyquist criterion requires. If the signal occupies the band from DC to f_B and the sampling rate is f_s, the oversampling ratio (OSR) R is defined as $R = f_s/(2f_B)$. For quantizers with broadband quantization noise, oversampling reduces the amount of in-band quantization noise. Oversampling also eases the anti-alias filter design, since a wide transition band is created by the increased separation between the signal band and its first alias. Oversampling also reduces the sensitivity of circuit performance to wideband noise sources, such as the thermal noise of the switches and opamps in SC circuits. This allows the conversion to be much more accurate than the resolution of the quantizer. Specifically, each octave increase in the OSR results an increase in resolution of 3 dB (0.5 bit). As the next Section will show, delta-sigma modulation improves significantly this trade-off.

3.1.2. First-Order Delta-Sigma Modulator

A more efficient oversampling quantizer is the delta-sigma modulator. Figure 3.2 shows a first-order delta-sigma ($\Delta\Sigma$) modulator with a single-bit quantizer. The loop performs two operations: subtraction of the feedback signal from the output through the DAC (delta) and accumulation of the difference (sigma). The modulator has four major building blocks: the subtractor, the integrator, the quantizer and the 1-bit DAC. Assuming that the modulator is stable, the operation may be briefly described as follows: for the integrator output to be bounded, the DC component (or the low-frequency components) of the DAC output must be very close to the input signal, due to the high gain of the integrator at low frequencies. Hence, the 1-bit output is a good digital representation of the analog input signal at low frequencies. For input signals very close to DC, the gain of the integrator

is extremely high, thus, the baseband components of the feedback signal will be nearly the same as the input signal, and the first-order modulator will provide very high resolution.

Assuming that the gain of the quantizer is 1, the z-domain description of the modulator is

$$V(z) = z^{-1}U(z) + (1 - z^{-1})E(z), \tag{3.3}$$

where V is a discrete-time binary-valued signal, U is a discrete-time continuous-amplitude signal and E is the quantization error [26]. According to Eq. (3.3), the quantization error is frequency-shaped by the function $H(z) = 1 - z^{-1}$. $H(z)$ is called the noise transfer function (NTF) which, in this example, has a zero at DC and thus suppresses the quantization noise in the vicinity of DC.

Assuming that E is white with total power of σ_e^2, the in-band noise power for the first-order modulator is given by

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^2 d\omega = \frac{\sigma_e^2 \pi^2}{3R^3}, \tag{3.4}$$

where $\sigma_e^2 = \frac{\Delta^2}{12} = \frac{1}{3}$ if e is uniformly distributed in $[-1, 1]$. Eq. (3.4) indicates that an octave increase in R will increase the SNR by 9 dB. In principle, the in-band quantization noise can be made as small as desired, simply by making R large enough. Generally, the

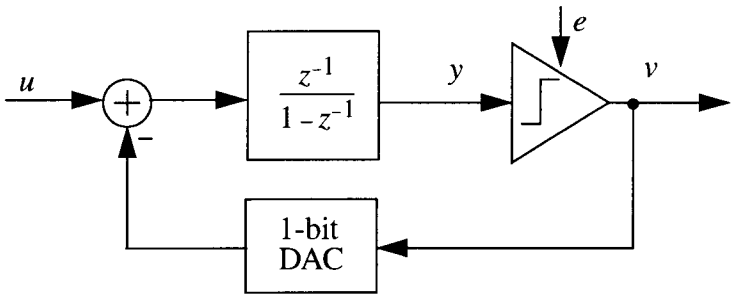


Figure 3.2: A first-order delta-sigma modulator.

resolution of a delta-sigma converter can be improved by clocking faster, and not by using larger, more sensitive analog circuitry.

The primary disadvantage of first-order ΔΣ modulators is that a high oversampling ratio is needed to achieve high resolution. For example, if we want 16-bit resolution, the oversampling ratio must be about 1500. Except for very low-frequency applications, a high oversampling ratio leads to a high sampling frequency and thus to difficulties in implementation. As the next Section will show, the oversampling ratio required to achieve a given resolution can be made smaller if higher-order ΔΣ modulators are used. Another disadvantage of first-order ΔΣ modulators is the presence of idle tones in the modulator output caused by limit cycles, especially when the input is a DC signal [27]-[29]. To ease this problem, several methods may be used, such as using multi-bit DAC feedback [30], chaotic modulation [31]-[33], or adding a dither signal [34][35].

3.1.3. Higher-Order Delta-Sigma Modulators

A general model of a delta-sigma modulator with one quantizer is shown in Figure 3.3. The modulator shown consists of three blocks: a loop filter, a quantizer and a

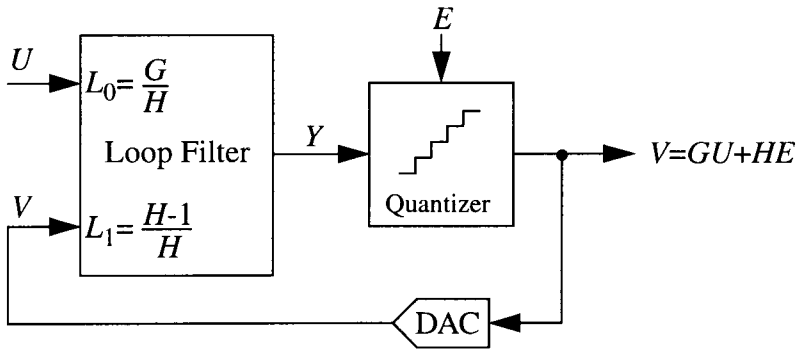


Figure 3.3: A general model of a delta-sigma modulator with one quantizer.

feedback DAC. Modeling the quantizer with $V = Y + E$, the output of the modulator becomes

$$V(z) = G(z)U(z) + H(z)E(z) , \tag{3.5}$$

where $G(z)$ and $H(z)$ are the signal transfer function (STF) and noise transfer function (NTF) of the modulator, respectively. To achieve spectral separation between signal and noise, the magnitude of STF must be close to 1 in the band of interest whereas the NTF must be close to 0.

One of the simplest higher-order delta-sigma modulator is the double-loop, or second-order, delta-sigma modulator [36]. A general structure is illustrated in Figure 3.4 [37]. The signal transfer function *G(z)* and the noise transfer function *H(z)* of this modulator are

$$G(z) = \frac{z}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)},$$

and (3.6)

$$H(z) = \frac{z^2 + (-2 + \alpha + \beta)z + (1 - \beta)}{z^2 + (-1 + \alpha + \beta + \gamma)z + (1 - \beta - \gamma)}. \tag{3.7}$$

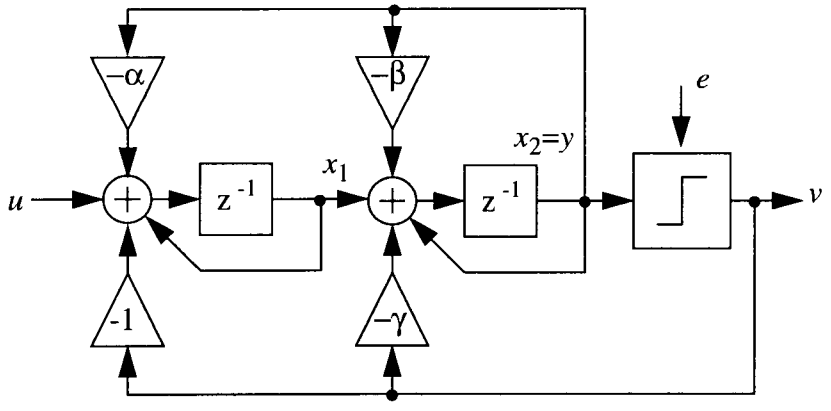


Figure 3.4: A general second-order delta-sigma modulator.

In the most common case, $(\alpha, \beta, \gamma) = (0, 0, 1)$, $G(z) = z^{-2}$ and $H(z) = (1 - z^{-1})^2$. This modulator will be referred to as MOD2. Other structures can also be used to realize MOD2 and some realizations will be described later in this chapter. Assuming that E is a white noise with power of σ_e^2, the noise power in the band of interest is

$$N_0^2 = \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} |H(e^{j\omega})|^2 d\omega \approx \frac{\sigma_e^2}{\pi}\int_0^{\frac{\pi}{R}} \omega^4 d\omega = \frac{\sigma_e^2 \pi^4}{5R^5}, \tag{3.8}$$

and thus an octave (factor of two) increase in R will increase the SNR by 15 dB, which, compared with the first-order modulator, is a 6 dB/octave improvement.

Even higher order modulators can be designed by employing higher-order NTFs. Also, the positions of the zeros in high-order NTFs need not to be all at DC, and can be optimized to further reduce the noise power in the band of interest. Some of the loop filter coefficients can be chosen to distribute the zeros around DC to optimize the in-band NTF response [38]. Cascaded architectures or modulators using multibit internal DAC can also be used [24].

When deriving the signal and noise transfer functions, the quantizer operation was modeled by the relation $v = y + e$. This is often called the linear model. The linear model allows the quantizer, a nonlinear system, to be treated as a linear system with independent inputs y and e. Note that e and y are in reality functionally related and therefore not completely independent. For linear systems with stable transfer functions, the output and the internal states are bounded if the input is bounded. However, the same cannot be said for delta-sigma modulators with stable signal and noise transfer functions, because e is not a real input— e is derived from y, in a nonlinear way. It is possible for $G(z)$ and $H(z)$ to be stable and yet result in a modulator with unbounded internal states. For a first-order modulator, it is easy to show [39] that if $|u| \leq 1$, where the input u is normalized to the

reference voltage, then the state y is bounded with $|e| \leq 1$. But for higher-order modulators, the stability issue is much more complicated and the limit on the input u becomes smaller for stable operation [24]. It should be noted that for a single-bit quantizer, the output can be represented by $v = ky + e$, where the quantizer gain k is unknown. An empirical approach to model the gain of a singe-bit quantizer is given in [40]. It is very useful for designing stable second-order modulators and also cascaded modulators.

3.2 SC Realization of Delta-Sigma Modulators

The delta-sigma modulators can be realized using SC circuits. Figure 3.5 illustrates a SC realization for the first-order delta-sigma modulator shown in Figure 3.2. The integrator with the transfer function of $\frac{z^{-1}}{1-z^{-1}}$ is realized by one opamp, two capacitors and 4 switches; the DAC by two voltage references and two extra switches; and the quantizer by a simple comparator and a D flip flop [41]. The analog circuitry appears to be quite trivial. By rearranging the clock phases controlling the switches, the integrator with transfer function $-\frac{1}{1-z^{-1}}$ can also be realized. However, the loop must contain at least one delay T.

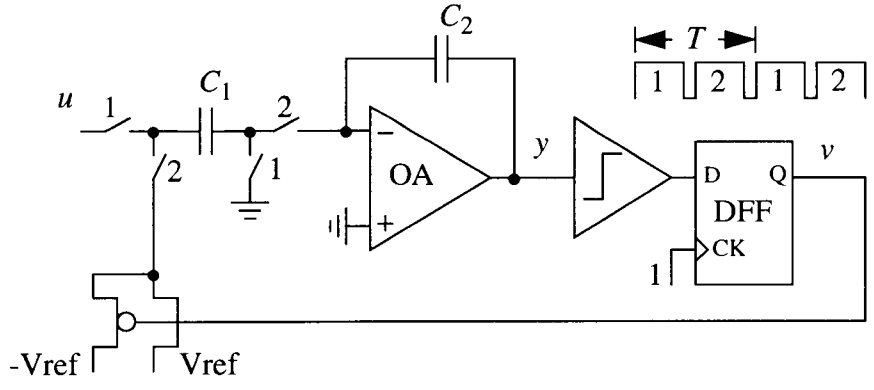


Figure 3.5: A switched-capacitor implementation of a first-order modulator.

SC integrators can be cascaded to realize high-order delta-sigma modulators, but care should be taken to insure that the integrator outputs are bounded and also the opamp outputs do not saturate. This leads to the necessity of adding a gain factor to the integrator to scale the integrator outputs, so that the opamps are operating in their linear region.

3.3 Basic Structures for Capacitor Ratio Measurement

Based on oversampling delta-sigma modulation, high-accuracy circuits for capacitor ratio measurement can be designed. The following part of this Section introduces three structures which can be used in different applications.

3.3.1. Structure Based on a Delta-Sigma Modulator

Figure 3.6 shows a SC delta-sigma modulator that is often used in oversampling A/D converters. C_1 is usually called the sampling capacitor and C_2 is called the DAC feedback capacitor. If C_1, C_2 and C_f are all equal, the noise transfer function of this modulator is $H(z) = 1 - z^{-1}$, and the signal transfer function is $G(z) = z^{-1}$. Hence it realizes the first-order shaping of the quantization noise. On the other hand, if input u is

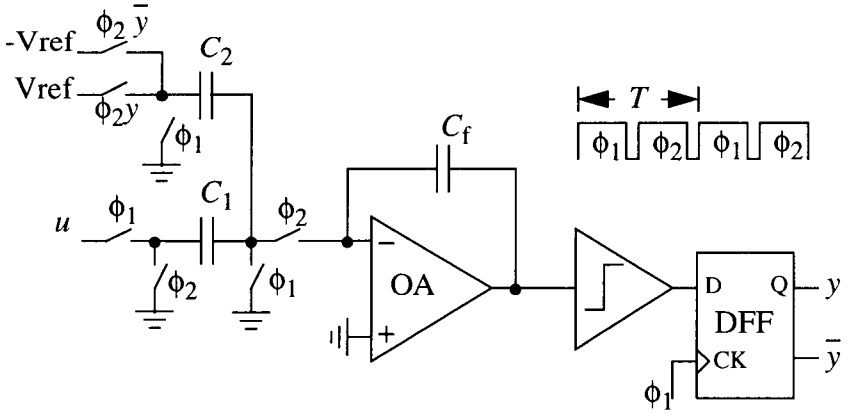


Figure 3.6: A SC first-order delta-sigma modulator for capacitor ratio measurement.

connected to the reference voltage V_{ref}, then C_1 can be a capacitor to be measured and C_2 the reference capacitor. Assuming that the modulator is stable, which means that the integrator output must be bounded, the average charge which flows from C_1 and C_2 to C_f is close to 0 (charge balance). Suppose that the total number of clock cycles is N, then the total charge from C_1 is $-NV_{ref}C_1$, while the charge from C_2 is $-(N-n)V_{ref}C_2 + nC_2V_{ref}$, where n is the number of clock cycles when y is "1". If the average of the charges is approximately 0, the following relationship is obtained

$$C_1 + \left(1 - \frac{2n}{N}\right)C_2 \approx 0\,, \tag{3.9}$$

where n/N is the average of v. If n/N is replaced by a new variable y_{ave}, the above equation can be rewritten as

$$\frac{C_1}{C_2} \approx 2y_{ave} - 1. \tag{3.10}$$

As Eq. (3.10) shows, the ratio of two capacitors C_1 and C_2 can be obtained by simply averaging the digital output data.

An alternative way to measure the capacitor ratio C_1/C_2 is using spectral analysis. For a traditional delta-sigma modulator, the input is u, and usually $C_1 = C_2 = C$. The charge flow from the input signal is uC, and the charge from the feedback path is either $V_{ref}C$ or $-V_{ref}C$, depending on the level of digital output y. The performance can be evaluated by measuring the signal and noise power in the output spectrum. Suppose u is a sinewave with amplitude V_m, then the normalized signal power is $(V_m/V_{ref})^2/2$. If in Figure 3.6, u is connected to V_{ref}, C_1 is the tested capacitor and C_2 is the reference capacitor, then the charge from the input signal is $V_{ref}C_1$ and the charge from the feedback path is either $V_{ref}C_2$ or $-V_{ref}C_2$, depending on y. This is equivalent to a regular modulator with input $u = V_{ref}C_1/C_2$ and the sampling and feedback capacitors equal to C_2. Now in the output spectrum, the normalized signal power becomes

$$\left(\frac{V_{ref}C_1}{V_{ref}C_2}\right)^2/2 = \left(\frac{C_1}{C_2}\right)^2/2. \tag{3.11}$$

Hence, by measuring the signal power and the noise power in the band of interest, the capacitor ratio can be obtained.

It should be noted that $C_2 > C_1$ is required so the equivalent input voltage $u = V_{ref}C_1/C_2$ is less than V_{ref}. As stated in earlier Section, when higher-order modulator is used, u must much smaller than V_{ref}, otherwise the modulator is not stable. For second-order modulators, u may be as large as $0.6V_{ref}$ and the modulator will still be stable [24]. Then $C_1 < 0.6C_2$ must hold for the maximum value of C_1. Therefore, this structure is only suitable for sensor applications where C_1 is the sensor capacitor and C_2 the reference capacitor, and C_2 is larger than C_1. It is not suitable for capacitor mismatch measurement where C_1 is very close to C_2 or even larger than C_2.

3.3.2. Structure for Differential Capacitive Displacement Sensor or Capacitor Mismatch Measurement

The differential capacitive sensor structure shown in Table 2.1(b) has been widely used because it reduces the nonlinearity of the transducer characteristic [17]. The relationship between the capacitor ratio and the displacement can be written as

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{\Delta d}{2d}, \tag{3.12}$$

where d is the distance between the center plate and the left plate or the right plate when there is no pressure applied; Δd is the displacement of the center plate, as shown in Table 2.1(b). Since d is fixed, Eq. (3.12) reflects that the capacitor ratio is a linear function of the displacement. To obtain a linear readout of the displacement, the interface circuit should then provide a linear readout proportional to $\frac{C_1 - C_2}{C_1 + C_2}$.

In Eq. (3.11), the DAC feedback capacitor C_2 is in the denominator of the capacitor ratio. It suggests that if C_1 and C_2 are both used in the DAC feedback loop, $(C_1 + C_2)$ will be in the denominator of the output formula. The circuit diagram of the structure is shown in Figure 3.7 [42]. In this circuit, C_1 and C_2 are used both as sampling capacitors and DAC feedback capacitors. The operation can be described as follows. Suppose y = "1". During the clock period when ϕ_1 is high, C_1 is disconnected from the input reference voltage and C_2 is discharged to ground. There is no charge delivered to the capacitor C_f so the integrator output remains unchanged. Next, at the next clock phase, ϕ_2 goes high, and a positive charge equal to $V_{ref}C_2$ is delivered to C_f. This causes the output voltage of the integrator to decrease by $V_{ref}C_2 / C_f$. If the integrator output voltage is below zero, y becomes "0" and now C_2 is disconnected from the input V_{ref}. Then during the clock phase when ϕ_1 is high, C_1 is charged to V_{ref}. When ϕ_2 goes high, C_1 is discharged between ground and the virtual ground, and a negative charge equal to $-V_{ref}C_1$ is delivered to C_f. The integrator output is then increased. The output waveform of the integrator is shown in Figure 3.8. The voltage

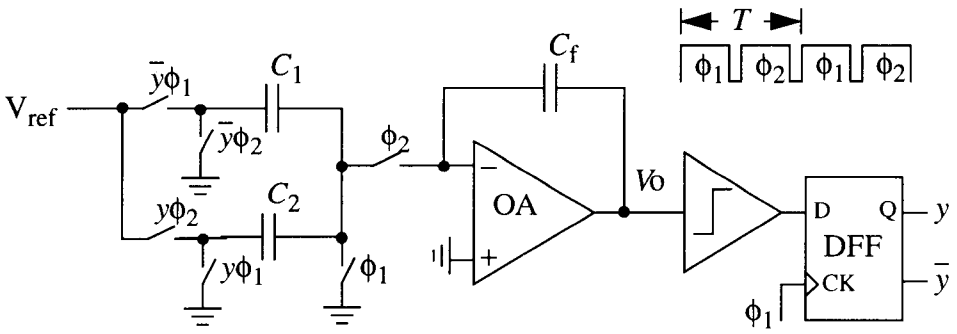


Figure 3.7: A first-order circuit for differential capacitive displacement sensors or capacitor mismatch measurement.

V_o varies around ground, and its average is close to zero. The negative feedback tends to make the average charge from C_1 and C_2 to be 0, and the following equation can be derived

$$nC_2V_{ref} - (N-n)C_1V_{ref} \approx 0, \tag{3.13}$$

where N is the number of clock cycles and n is the number of clock cycles when y is "1". Then the relationship between the capacitance ratio and the average of output data y becomes

$$\frac{C_2}{C_1 + C_2} \approx y_{ave}, \text{ and} \tag{3.14}$$

$$\frac{C_1 - C_2}{C_1 + C_2} \approx 1-2y_{ave}, \tag{3.15}$$

where y_{ave} is the average of the output binary data. Clearly, y_{ave} is a linear function of the displacement according to Eq. (3.12) and Eq. (3.15). Hence this structure is suitable for measuring the displacement without calibration for nonlinearity. As Eq. (2.6) shows, this structure can also be used for on-chip capacitor mismatch measurement. There are no limitations on the value of the capacitors in the measurement. Thus, C_1 can be equal to C_2 ($y_{ave} = 0.5$), or much smaller than C_2 ($y_{ave} \approx 1$).

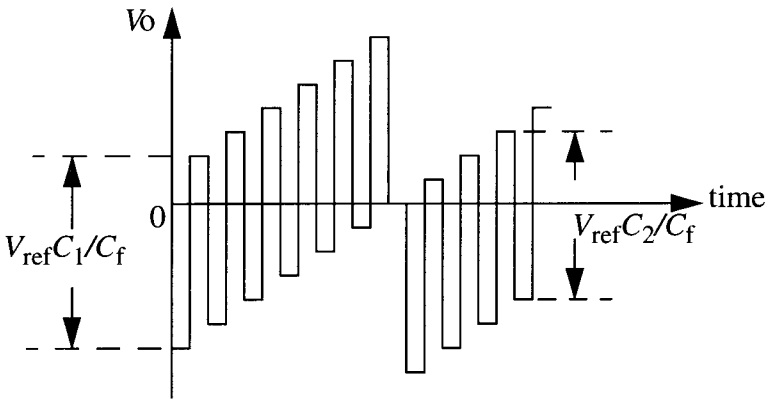


Figure 3.8: Output waveform of the integrator in the circuit for capacitive displacement sensor readout.

The capacitor ratio can also be obtained from the output spectrum. From Eq. (3.13), it can be see that this structure is equivalent to a SC delta-sigma modulator with a DC input equal to $\frac{C_1 - C_2}{C_1 + C_2} V_{ref}$ and with the sampling capacitor and the DAC feedback capacitor both equal to $(C_1+C_2)/2$. Hence, in the output spectrum, the normalized signal power is $\left(\frac{C_1 - C_2}{C_1 + C_2}\right)^2 / 2$. Hence, by measuring the normalized signal power and the in-band noise power in the output spectrum, the capacitor ratio can obtained.

It should be noted that this structure does not provide a linear readout when C_1 and C_2 are not in a differential configuration. For example, C_1 may be the sensor capacitor as shown in Table 2.1(a) and C_2 is a capacitor with fixed capacitance. Suppose that

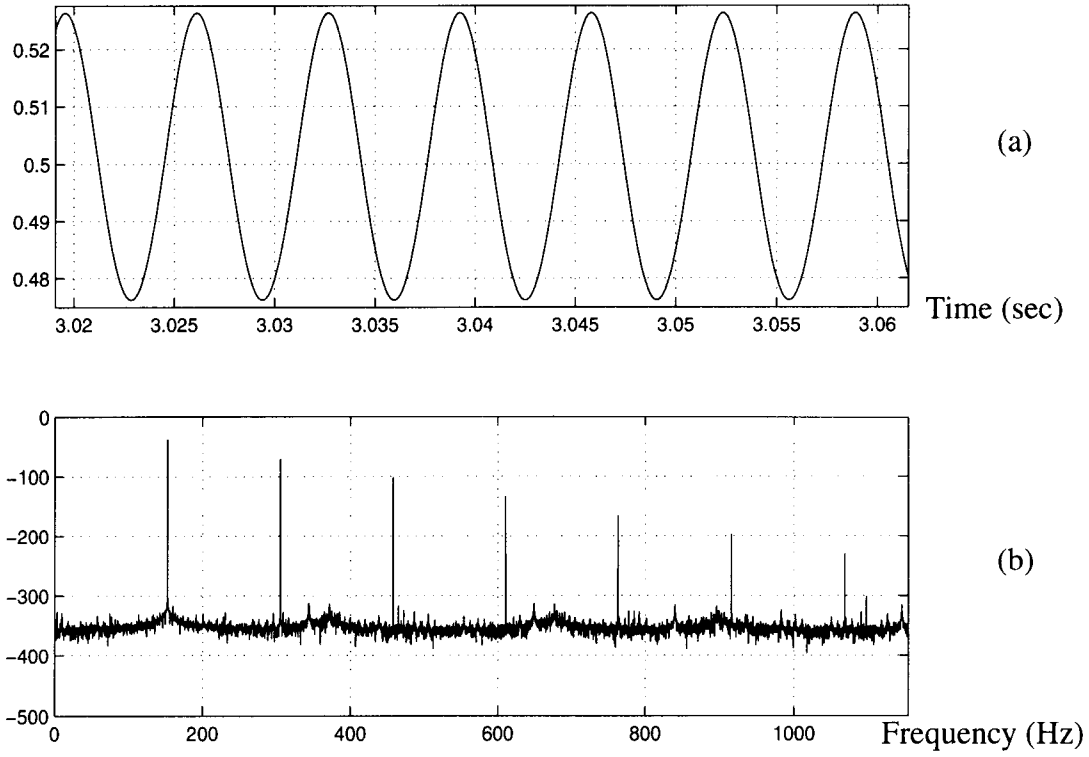


Figure 3.9: (a) Plot of the output y_{ave} in time domain.
(b) Plot of the output y_{ave} in frequency domain.

$C_1 = C_2(1 + k\sin(\omega t))$, where the nominal value of C_1 is C_2, and the variation of C_1 has a sinewave pattern. Then Eq. (3.14) becomes

$$\frac{C_2}{C_1 + C_2} = \frac{1}{2 + k\sin(\omega t)} \approx y_{ave}. \tag{3.16}$$

The function and the frequency components in the output are plotted in Figure 3.9. Here, instead of getting a single-tone sinewave at the output, harmonics exist even when the variation of C_1 contains only one frequency component.

3.3.3. Four-Phase Structure for Capacitor Ratio Measurement

Another structure for capacitive sensor readout or mismatch measurement is introduced in this Section. It is useful in capacitive sensor applications where the variation of the sensor capacitor is measured against a reference capacitor. Figure 3.10 illustrates the diagram of this structure which needs four non-overlapping clock phases for its operation.

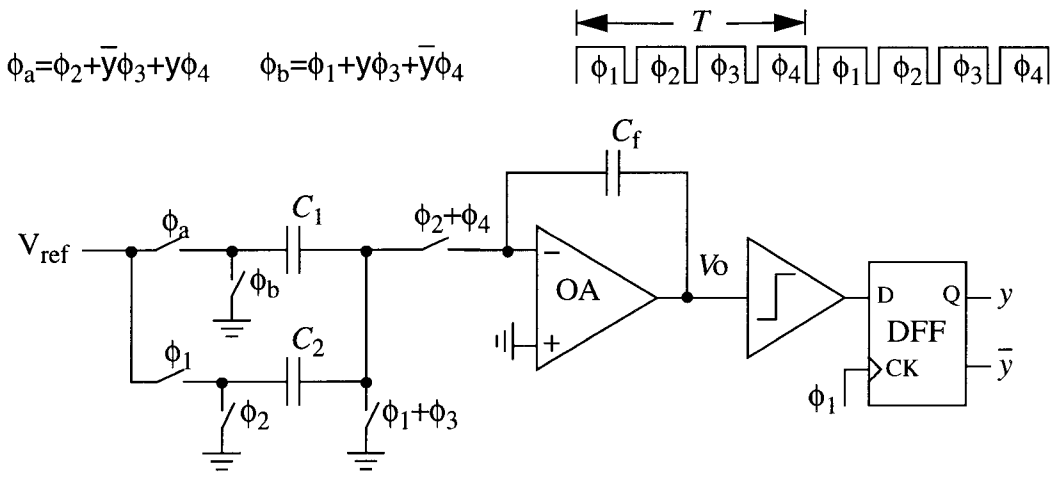


Figure 3.10:A four-phase structure for capacitor sensor readout.

In this structure, the operation is a little different from the previous introduced structures. C_1 is used in both the sampling and DAC feedback paths while C_2 is only used in the sampling phase. During the period when ϕ_1 is high, C_1 is charged to V_{ref} and C_2 is discharged to ground. At the next phase when ϕ_2 is high, a positive charge delivered by C_2 and a negative charge delivered by C_1 is transferred into the integrator feedback capacitor C_f, causing the output of the integrator to change by $V_{ref}(C_1 - C_2)/C_f$. Then, when ϕ_3 is high, C_1 is charged to V_{ref} or discharged to ground, depends on whether y is "0" or "1". During the interval when ϕ_4 is high, a negative charge equal to $-V_{ref}C_1$ is delivered to C_f when $y = 0$. If $y = 1$, a positive charge $V_{ref}C_1$ is transferred to C_f. So, basically, C_1 is acting as a DAC feedback capacitor during phase 3 and phase 4. The output waveform of the integrator is depicted in Figure 3.11. The average charge delivered to C_f is close to 0 after many clock cycles, thanks to the negative feedback through C_1. Hence, the following equation is obtained

$$N(C_2 - C_1)V_{ref} + (N - n)C_1V_{ref} - nC_1V_{ref} \approx 0, \tag{3.17}$$

where the definitions of N and n are the same as before. The relationship between the

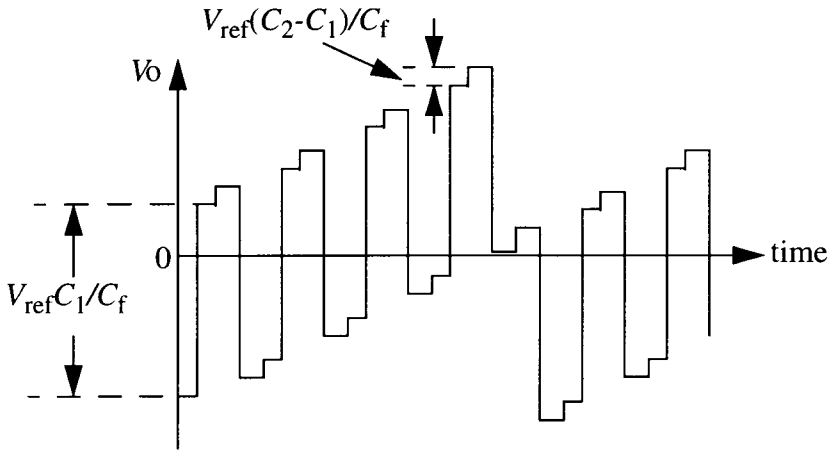


Figure 3.11:Output waveform of the integrator in the four- phase circuit.

capacitor ratio and the binary data average y_{ave} is derived from Eq. (3.17) as

$$\frac{C_2}{C_1} \approx 2y_{ave}. \tag{3.18}$$

The capacitor ratio is directly proportional to the average of binary output. It provides a linear readout of capacitance variation when C_1 is a reference capacitor and C_2 varies continuously. It can be seen from Eq. (3.18) that the range of capacitance variation is $0< C_2 < 2C_1$, since y_{ave} can vary from 0 to 1. Hence, this structure is also suitable for fixed capacitance measurement such as on-chip capacitor mismatch measurement.

Again, from the output spectrum, the capacitor ratio can be measured. In Figure 3.10, C_1 is the DAC feedback capacitor and the signal charge is $V_{ref}(C_1\text{-}C_2)$ during each clock cycle. Hence, this structure can be regarded as a regular modulator with a DC input equal to $V_{ref}(C_1\text{-}C_2)/C_1$ and a sampling capacitor equal to C_1. Then in the output spectrum, the normalized signal power is $\left(\frac{C_1 - C_2}{C_1}\right)^2/2$.

3.4 Second-Order Structures

The structures introduced in the previous Section are all based on first-order modulation with single-bit quantizers. As explained earlier in Section 3.1.2, a first-order modulator with single-bit quantizer needs a very high oversampling ratio to achieve high resolution, which limits the achievable bandwidth of the input signal. The first-order modulator also suffers from idle tones. One solution is to use multibit quantizers. As shown in Eq. (3.2), the quantization error σ_e^2 is reduced because the quantization step Δ in a multibit quantizer is smaller. However, the linearity of the DAC in the feedback loop becomes a limiting factor of the performance. Various techniques have been introduced to reduce non-linearities of the DAC in the band of interest [43]. However, the complexity of the circuit is greatly increased.

Another solution is to use high-order modulators, as discussed in Section 3.1.3. For an oversampling ratio of 256, the maximum achievable SNR for first-order, second-order and third-order modulator modulators is 72 dB, 102 dB and 132 dB, respectively [24]. Here, second-order modulators are preferable because they are easy to make stable and their realization is much easier than of third-order modulators. Since in capacitive sensor applications the band of interest is normally around a few kHz, for an oversampling ratio of 256 the sampling frequency makes the SC implementation still reasonable. With careful design, a second-order modulator can easily provide 16-bit accuracy. The possibility of idle tones is also greatly reduced.

3.4.1. Design of Second-Order Modulators

A possible realization of a second-order modulator is shown in Figure 3.12. It consists of two cascaded delayed integrators, and is a simplified structure of the one shown in Figure 3.4. Several scale factors have been added to reduce the swing of each integrator so that the outputs are within the linear range of the opamps in the integrators. Now the

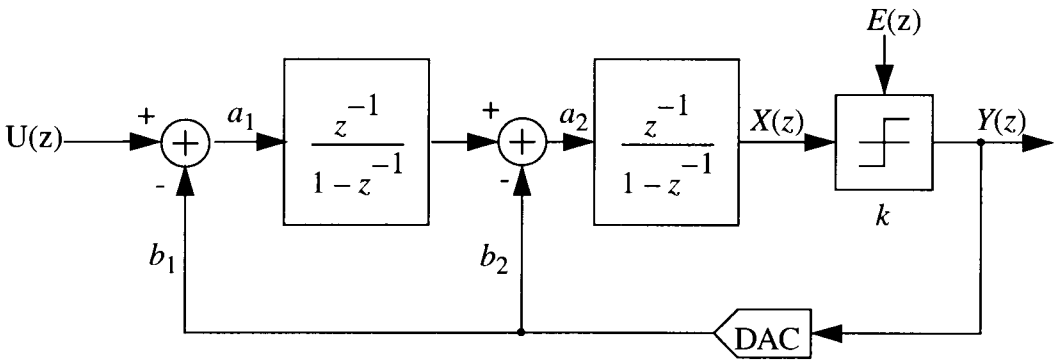


Figure 3.12:A realization of the second-order modulator.

performance of the modulator depends on how these factors are chosen. The output of the quantizer is given by

$$\left(a_1(U(z)-b_1Y(z))\frac{z^{-1}}{1-z^{-1}}-b_2Y(z)\right)\frac{a_2z^{-1}}{1-z^{-1}}k+E(z)\;=\;Y(z), \qquad (3.19)$$

where the transfer function of the quantizer is modeled as $Y(z) = kX(z) + E(z)$, k is the gain of the quantizer and $E(z)$ is the quantization error in the z domain.

The quantizer gain k is hard to derive by numerical analysis but can be modeled empirically by simulations. It can be assumed that the effective closed-loop gain is forced by the feedback to be unity, and then $k = 1/a_1a_2b_1$ [40]. As is well known, the closed-loop gain of the general model with unity negative feedback shown in Figure 3.13 is $\frac{A}{1+A}$. When A is very large, the closed-loop gain is approximately 1. The gain of the modulator shown in Figure 3.12 to the input signal can also be assumed to be 1 at low frequencies. It is based on the fact that the integrators have very large gain at low frequencies and it will be shown later that the subsequent analytical results compare well with simulation results.

It can be shown that k must be equal to $\frac{1}{a_1a_2b_1}$ for the loop gain to be unity [44]. Substituting $k = \frac{1}{a_1a_2b_1}$ in Eq. (3.19) and comparing it with the second-order modulator relation

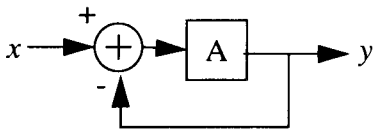


Figure 3.13:A general model for a gain block with unity negative feedback.

$$Y(z) = U(z)z^{-2} + (1-z^{-1})^2 E(z), \tag{3.20}$$

then $b_2 = 2a_1b_1$ and $b_1 = 1$ are obtained. Choosing $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$ and $b_2 = \frac{1}{2}$, simulations show that the outputs of the integrators are less than 0.8 of the full scale for input values up to 0.6 of full scale. When the input signal is small, $a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$ and $b_2 = 1$ can also be used without causing the integrator output to exceed the linear range of the opamps. All these coefficients are simple and the modulator is easy to implement in SC circuits.

The second-stage integrator can be replaced by a bilinear stage and the DAC feedback loop to the second stage integrator can be eliminated, as shown in Figure 3.14. The output now becomes

$$\left(a_1(U(z)-b_1Y(z))\frac{z^{-1}}{1-z^{-1}}\right)\frac{a_2-b_2z^{-1}}{1-z^{-1}}k + E(z) = Y(z). \tag{3.21}$$

Using the same empirical approach, the quantizer gain is $k = \frac{1}{a_1b_1b_2}$. Replacing k by

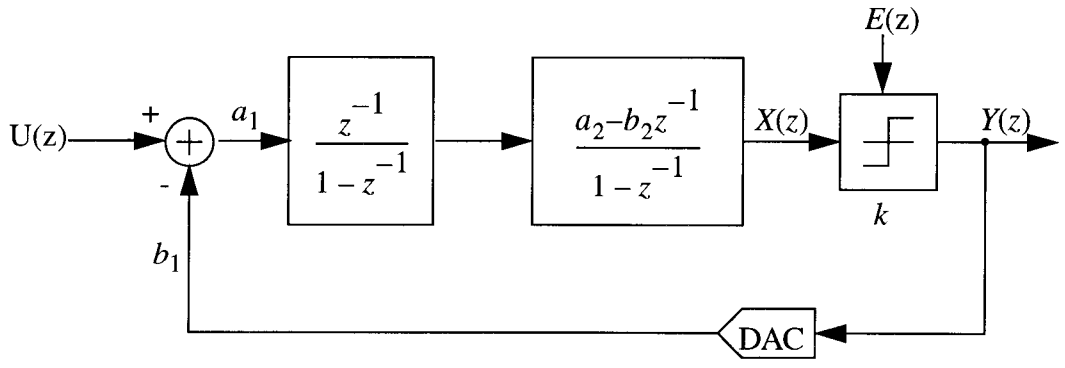


Figure 3.14:Another realization of the second-order modulator.

$\frac{1}{a_1 b_1 b_2}$ in Eq. (3.21), it can be rewritten as

$$\frac{\frac{a_2}{b_1 b_2} z - \frac{1}{b_1}}{(z-1)^2 + \left(\frac{a_2}{b_2} z - 1\right)} U(z) + \frac{(z-1)^2}{(z-1)^2 + \left(\frac{a_2}{b_2} z - 1\right)} E(z) = Y(z) \ . \qquad (3.22)$$

It can be seen from Eq. (3.22) that if the denominators on the left side equal z^2, the noise transfer function becomes $(1 - z^{-1})^2$, which realizes the second-order modulation. Now $a_2 = 2b_2$ is obtained and the signal transfer function is $G(z) = (2z^{-1} - z^{-2})/b_1$. The choice of a_1 and a_2 is arbitrary but they should be chosen so that the outputs of the integrators are in their linear range.

The modulators shown in Figure 3.12 and Figure 3.14 have been simulated in Matlab using ideal components. We call the modulator in Figure 3.12 "mod1" and the other one in Figure 3.14 "mod2". In the simulations, $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$ and $b_2 = \frac{1}{2}$ were used for mod1, and $a_1 = \frac{1}{4}$, $a_2 = \frac{1}{2}$, $b_1 = 1$ and $b_2 = \frac{1}{4}$ were used in mod2. The input signal was the same in two modulators. The simulated output spectra are shown in Figure 3.15. The solid line refers to mod1 and the broken line refers to mod2. It can be observed that the quantization error increases 40 dB when the frequency increases by 20 dB. In Eq. (3.8), the quantization noise power in a second-order modulator is proportional to ω^4, which means that when the frequency is 10 times (20 dB) higher, the quantization noise power is 10^4 (40 dB) larger. Hence, the simulation results verify that mod1 and mod2 are two realizations of second-order delta-sigma modulation.

The simulated signal-to-noise (SNR) performance shown in Figure 3.16 also shows that mod1 and mod2 achieve the same performance as a regular second-order modulator. The peak SNR is around 103 dB which is the same as stated earlier this Section for second-order modulators. It can be seen from Figure 3.16 that mod2 has almost the same SNR

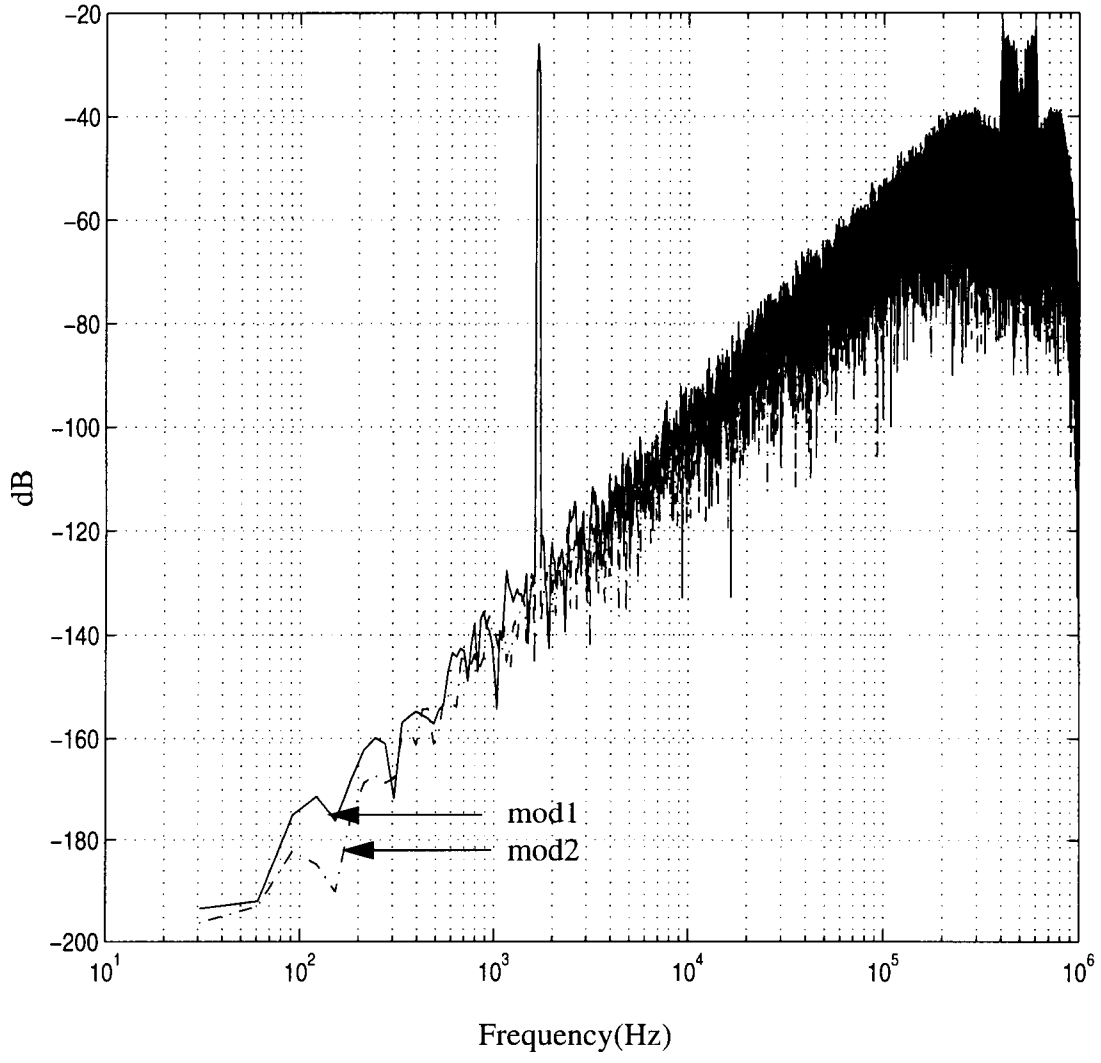


Figure 3.15:Output spectra of mod1 and mod2.

performance as mod1. In subsequent implementations of high-order structures for capacitor ratio testing and sensor readout, the configuration of mod2 will be used.

3.4.2. Second-Order Structures for Capacitor Ratio Testing and Sensor Readout

Based on the mod2 structure shown in Figure 3.14, second-order structures can be designed for the sensor readout circuits shown in Figures 3.6, 3.7 and 3.10. This is straightforward, and one example is shown in Figure 3.17. The second stage realizes the transfer function

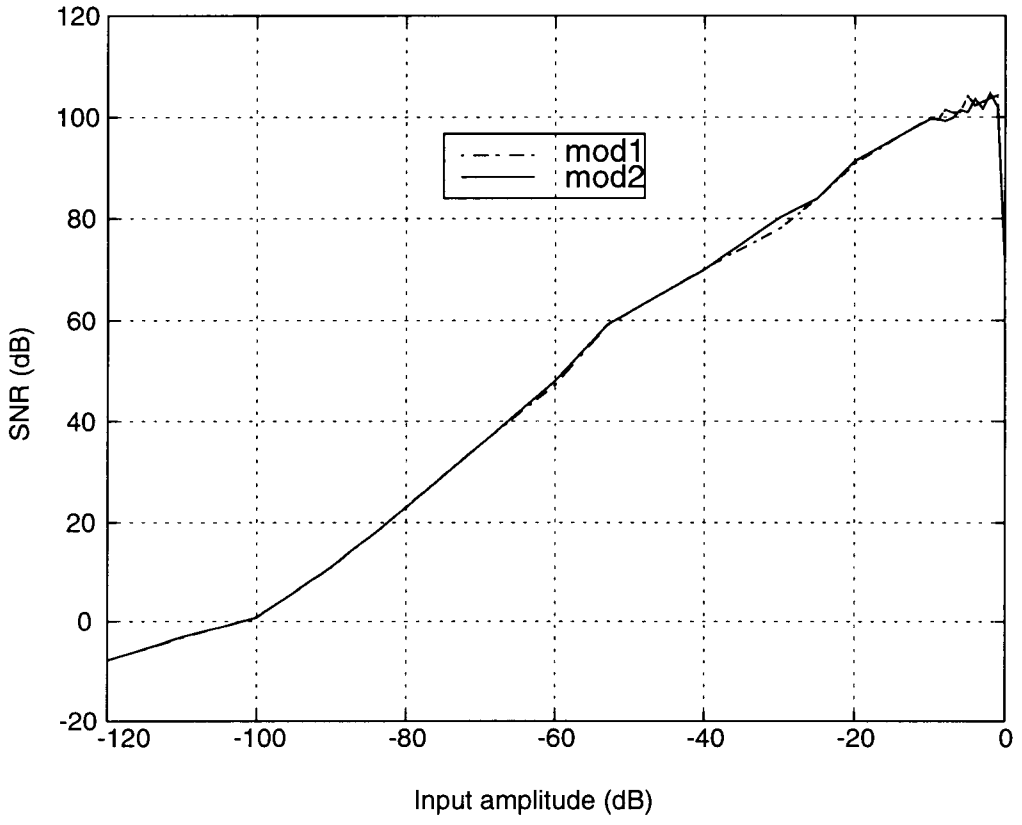


Figure 3.16:Simulated SNR for different input levels,
0 dB refers to full scale.

$$H(z) = -\frac{a_2 - b_2 z^{-1}}{1 - z^{-1}}, \tag{3.23}$$

where $a_2 = 2b_2$ is realized by the ratio of the two capacitors C_3 and C_4. $a_2 = \frac{1}{2}$ is also determined by a capacitor ratio. From Eq. (3.22), it can be seen the noise transfer function is mainly determined by $a_2 = 2b_2$. Hence, by designing the second stage as shown, the second-order modulation is assured, as long as the rest of design makes the circuit stable. There is a negative sign in Eq. (3.23), as opposed to the realization shown in Figure 3.14, which should be compensated in the first stage to keep the feedback negative. That is why in the first stage, the clock phases for the sensor capacitors C_1 and C_2 are interchanged, compared to those in Figure 3.7. The resulting output formula is now

$$\frac{C_1}{C_1 + C_2} \approx y_{ave}, \text{ and} \tag{3.24}$$

$$\frac{C_2 - C_1}{C_1 + C_2} \approx 1 - 2y_{ave}. \tag{3.25}$$

The same second stage can be applied to the structures in Figures 3.6, 3.7 and 3.10, and again, because of the negative sign in the circuit implementation, the clock

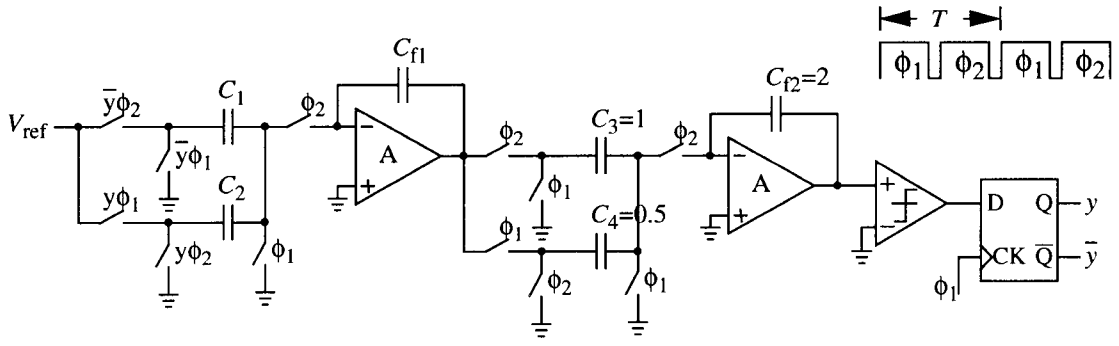


Figure 3.17:A second-order structure for capacitor ratio measurement.

phases in the first stage should be changed. For the four-phase structure, ϕ_2 in Figure 3.17 should be replaced by ϕ_4. Here, the other second-order structures are not shown.

3.5 Simulation of SC Realizations and Data Processing for Capacitor Ratio Readout

To verify the validity of the previous discussions and the functionality of the circuit realizations, the first-order and second-order SC circuits were simulated extensively in SWITCAP2, a SC circuit simulator which uses simplified models for switches, capacitors and opamps. In the simulations presented in this Section, all the circuit components were assumed to be ideal so that the functionality of these circuits could be quickly verified.

As discussed earlier in Section 3.3, the input capacitor ratio C_1/C_2 can be obtained in two different ways. One is using the spectral analysis and calculate the signal power in the output spectrum. The other way is using data averaging in time domain. No matter which method is used, the data are always truncated because of the limitations on the CPU and memory of the computers utilized. For the same reason, since an ideal lowpass filter requires infinite number of coefficients, which is not realistic, the coefficients are always truncated and the resulting frequency response is a "smeared" version of the ideal one. When the truncated data is simply averaged in the time domain, the equivalent in frequency domain is a crude lowpass filtering, and the number of coefficients in the lowpass filter is the same as the numbers in the data. Because of the so-called *Gibbs phenomenon*, the resulting lowpass filter has slow transition band and ripples in passband and stopband [45]. Increasing the number of the data (or coefficients) can make the transition band sharper but the ripples in the passband and stopband remain the same. The easiest solution to the problem generated by truncation is the window method. The simple truncation is equivalent to using a rectangular window which has large sidelobes. By tapering the window smoothly to zero as with Hanning or Blackman windows, the sidelobes can be greatly reduced so that

the resulting lowpass filter has larger attenuation in the stopband. The windows with smaller sidelobes yield better approximations at a discontinuity of the ideal response [45]. The penalty paid is the relatively slower transition band. Hanning window was used in our simulations and testing, since it provides relatively small sidelobes and the transition band is not significantly widened.

The circuit shown in Figure 3.17 has been simulated in SWITCAP2, using ideal switches, opamps and comparator. Figure 3.18 shows the simulation results when the capacitances of C_1 and C_2 are fixed. The estimation error is defined as $|C_2 - C_{2T}|/C_{nom}$, where C_{2T} is the capacitance of C_2 obtained from the simulation and C_{nom} is the nominal capacitance of C_1 and C_2. In the simulation, C_1 was 10.5 pF and C_2 was 9.5 pF, and C_{nom} is 10 pF. In Figure 3.18(a), the estimation is carried out by simply averaging the data, and in Figure 3.18(b) the Hanning window was used before the averaging of data. In this simulation, the length of the Hanning window is the same as that of the data. For instance, when the total number of data used in the averaging is 512, the length of the Hanning window used is also 512. It can be seen that by using Hanning window, for the same estimation accuracy, the number of data needed for averaging is greatly reduced.

When C_1, C_2 or both of them are varying, the variance of capacitance can be obtained from the output spectrum. However, the circuit show in Figure 3.17 is only suitable when C_1 and C_2 change differentially as illustrated in Table 2.1(b) and (d). Figure 3.19 shows the simulated output spectra of the circuit shown in Figure 3.17. In Figure 3.19(a), C_1 is fixed to be 10 pF and C_2 is assumed to vary around 10 pF. The variation of C_2 contains a sinewave signal and the range of the variation is 1 pF. The distortion is obvious which validates previous discussions in Section 3.3.2. In

Figure 3.21(b), both C_1 and C_2 vary and the change of capacitance has a differential signal which contain a single-tone sinewave. The range of variation is again 1 pF. It can be seen

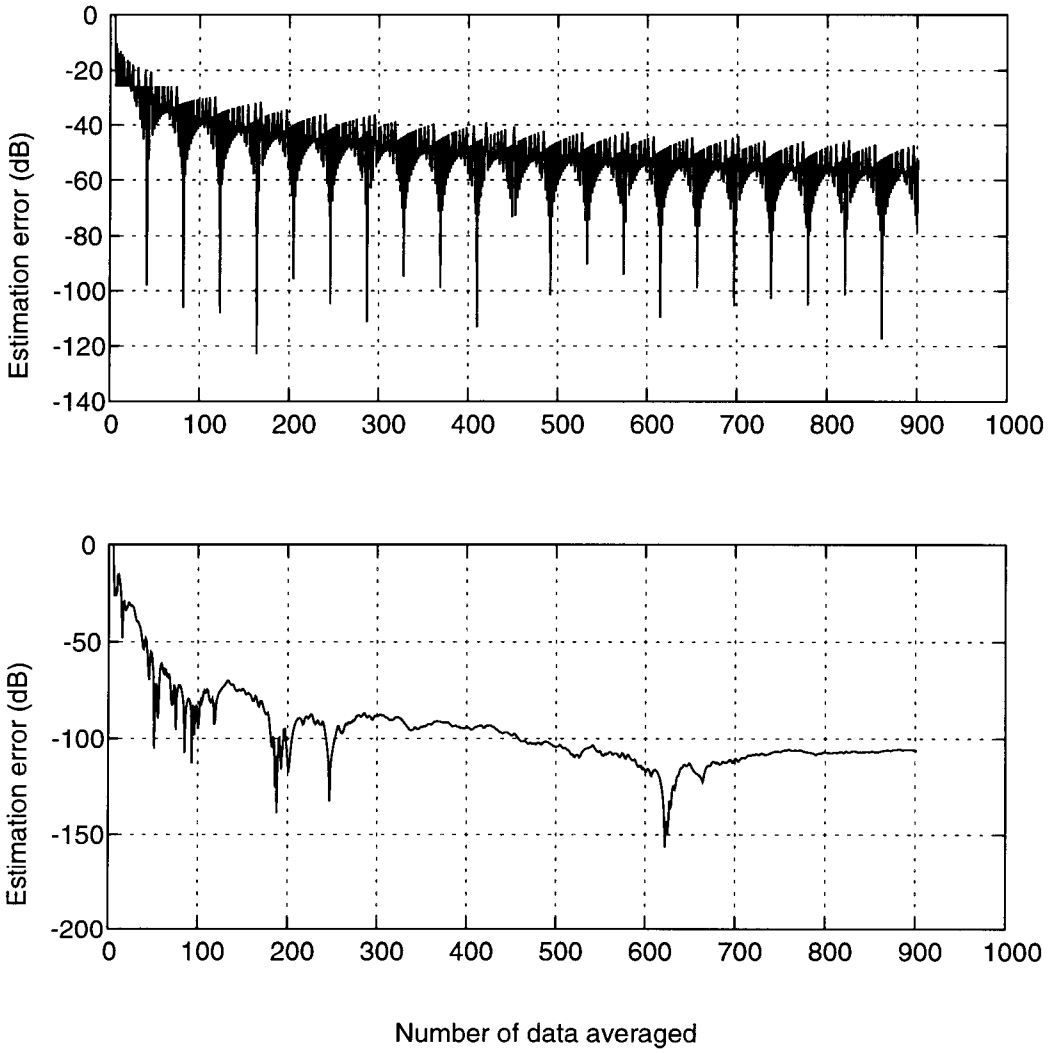


Figure 3.18:Estimation errors of fixed capacitor ratio of the circuit in Figure 3.17: (a) Rectangular window used;
(b) Hanning window used.

that the distortion is much smaller when C_1 and C_2 vary differentially. Therefore, the circuit shown in Figure 3.17 is suitable for either fixed capacitor ratio measurement or differential capacitive sensor readout.

When C_1 is fixed and C_2 is varying continuously, as in some sensor applications, the four-phase circuit shown in Figure 3.10 can be used. The average of its output is

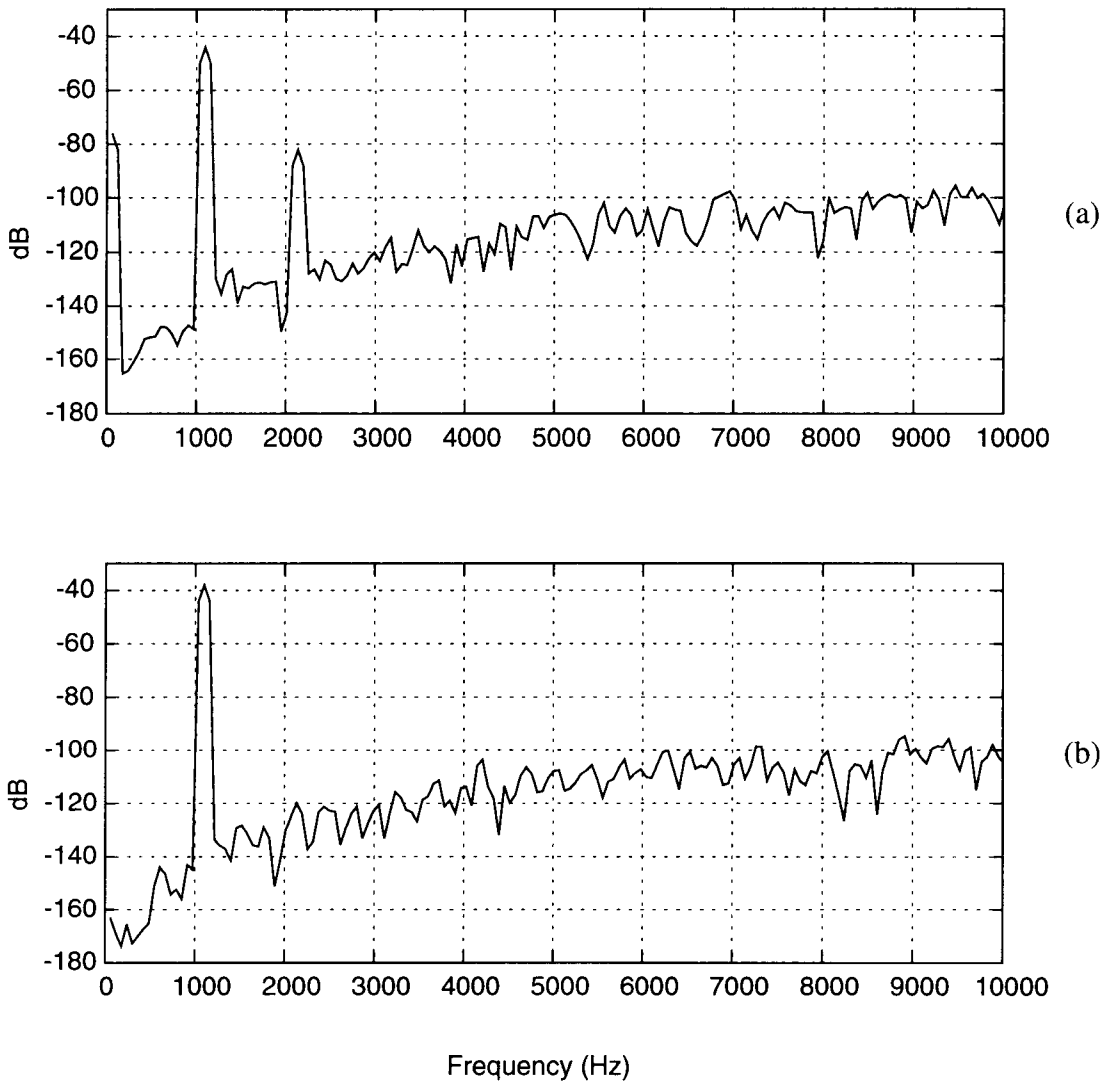


Figure 3.19:Simulated output spectra of the circuit in Figure 3.17:
(a) C_1 is fixed and C_2 varies; (b) C_1 and C_2 vary differentially.

directly proportional to the capacitor ratio C_2/C_1. The estimation error from Switcap simulation for the second-order four-phase circuit is depicted in Figure 3.20. Again Hanning window was used when data were averaged. In the simulation, C_1 is assumed to be the reference capacitor with capacitance of 10 pF and C_2 is the tested capacitor with capacitance of 10.5 pF. The estimation error is defined as $|C_2 - C_{2T}|/C_1$, where C_{2T} is the capacitance of C_2 obtained from the simulation. It can be observed from this figure that when the number of data used for averaging is larger than 600, the lowpass filter characteristic is very close to an ideal one. The estimation error is approximately -110 dB when more than 600 data are averaged, which corresponds to a resolution of 31 aF for a 10 pF capacitor (0.003%).

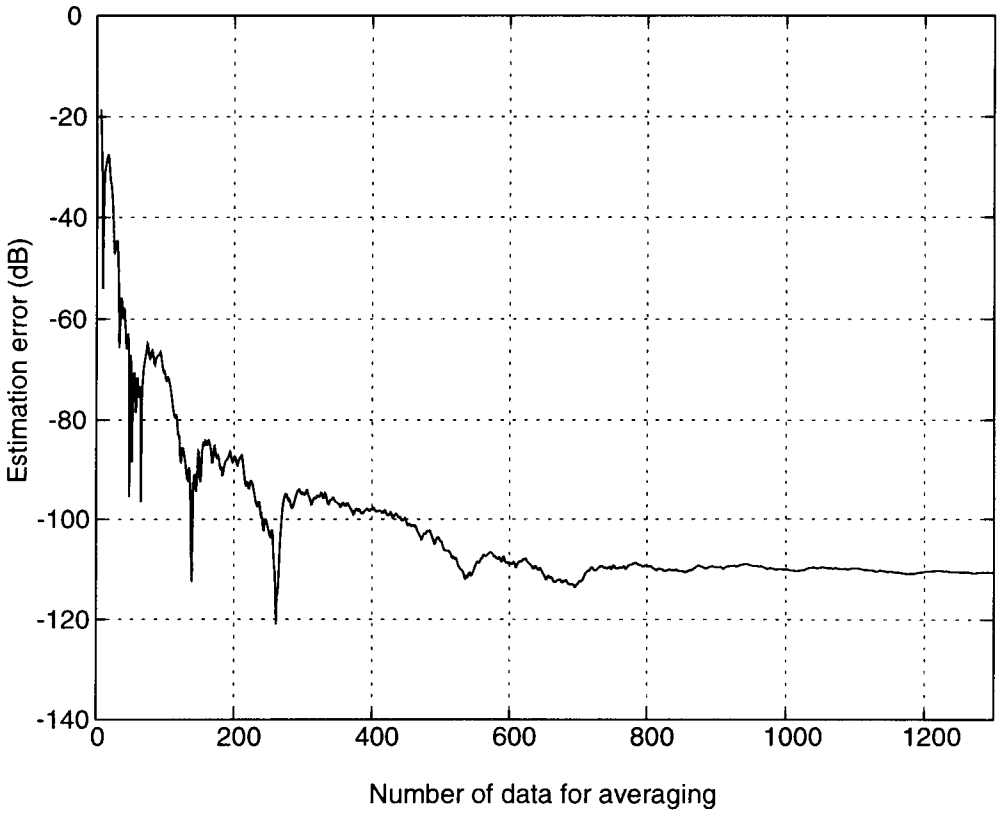


Figure 3.20:Estimation error of fixed capacitor ratio of the second-order four-phase circuit.

Figure 3.21 shows the simulated output spectra of the second-order four-phase circuit. In the simulation, C_2 is assumed to vary around 10 pF and its variation contains a single-tone sinewave signal. It can be seen that the output has good linearity as predicted earlier.

3.6 Conclusions

By utilizing oversampling delta-sigma technique, different structures for high-accuracy capacitor ratio testing and sensor readout can be designed. Several new structures have been proposed for different applications. These new structures combine the sensor capacitors with the input branch of the delta-sigma modulator, and hence are able to provide high-resolution digital output without the requirements of accurate component

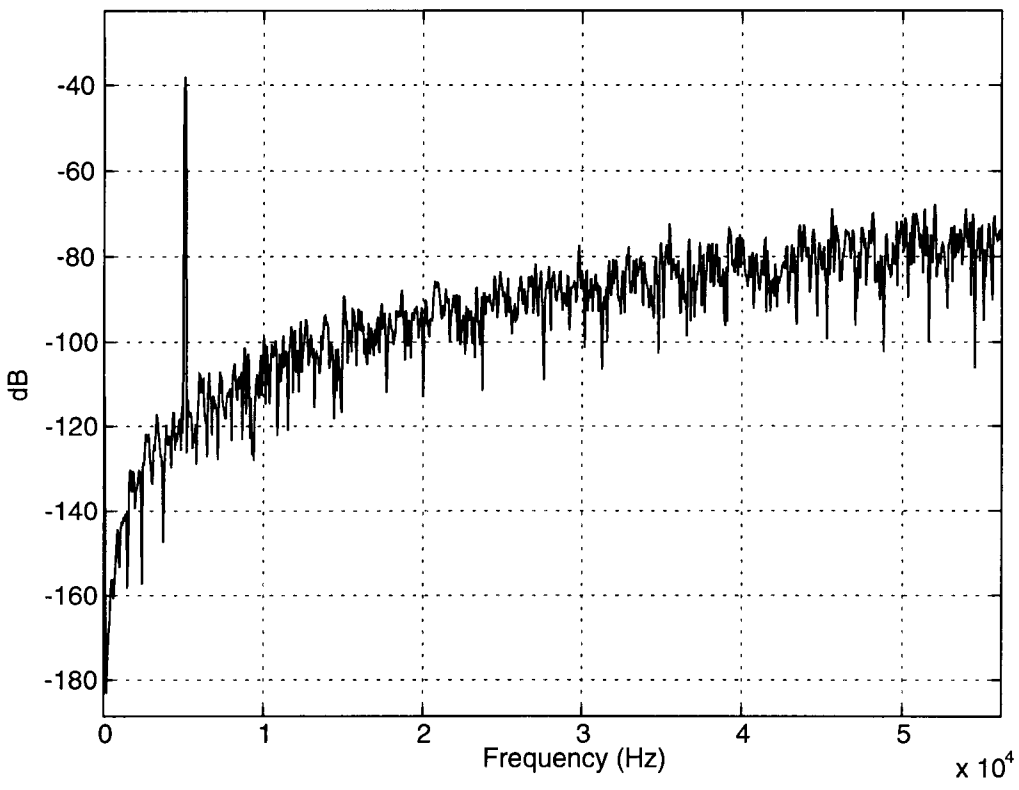


Figure 3.21:Simulated output spectra of the second-order four-phase circuit.

matching and high-performance components. SWITCAP2 simulations have been performed using ideal components, and the simulation results proved the functionality of the introduced structures and predicted that very high accuracy can be obtained.

Chapter 4. Non-Ideal Effects in Switched-Capacitor Sensor Interface Circuits

In Chapter 3, several switched-capacitor circuits have been introduced for accurate capacitor ratio measurement. Switcap simulation results showed that high accuracy can be achieved. However, since only simple models for circuit components were used in Switcap, in the actual circuit the performance is likely to be affected by the non-idealities of real components. In this Chapter, the effects of circuit non-idealities are analyzed and some solutions for their elimination are discussed.

4.1 Effect of Finite Gain and Input Offset of the Opamp

The opamp is a very popular building block in analog circuits and is widely used in signal processing. In analog delta-sigma modulators, opamps are often used to realize the integrators, which are the main blocks in the modulator, as shown in Chapter 3. The transfer function of the integrator is determined by the capacitor ratios, as well as the characteristics of the opamp. Since the integrators are used to realize the noise-shaping transfer function, errors in the transfer function of the integrator causes a deviation from ideal noise shaping and hence may cause an increase of quantization noise in the band of interest.

An ideal opamp should have infinite gain and zero offset voltage. However, a real opamp has finite DC gain, finite bandwidth and nonzero input offset voltage. This causes errors in the integrator transfer function, as will be discussed next. A typical non-inverting switched-capacitor integrator is shown in Figure 4.1, where the opamp is assumed to have a finite DC gain of A and an input offset of V_{os}. First, ignoring V_{os}, the z-domain transfer function of this integrator can be derived as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2 + \frac{C_1 + C_2}{A}} \cdot \frac{z^{-1}}{1 - \frac{C_2 + C_2/A}{C_2 + (C_1 + C_2)/A} z^{-1}} . \qquad (4.1)$$

Here the pole of the integrator transfer function is no longer at DC ($z_p = 1$), as in the transfer function of an ideal integrator. Instead, the pole of this non-ideal integrator is at

$$z_p = \frac{C_2 + C_2/A}{C_2 + (C_1 + C_2)/A} . \tag{4.2}$$

The pole is on the positive real axis and is less than 1. As also shown in Eq. (4.1), there is also a gain error in the transfer function of the non-ideal integrator. When V_{os} is considered, the integrator output is $V_{out}(z) = H(z)(V_{in}(z) + V_{os}(z))$. Hence, from the integrator output point of view, the input offset voltage of the opamp has the same effect as the offset voltage at the input.

Since usually the gain of the opamp A is much larger than 1, Eq. (4.1) can approximated by

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2}\left(1 - \frac{1 + C_1/C_2}{A}\right) \cdot \frac{z^{-1}}{1 - \left(1 - \frac{C_1}{AC_2}\right)z^{-1}} . \tag{4.3}$$

If $C_2 = 2C_1$, the extra gain factor is $1 - \frac{3}{2A}$ and the pole is at $z_p = 1 - \frac{1}{2A}$. Assuming A = 1000, then the finite gain causes a gain error of 0.15% and pole error of 0.005. This will affect the noise transfer function and causes noise leakage in the band of interest.

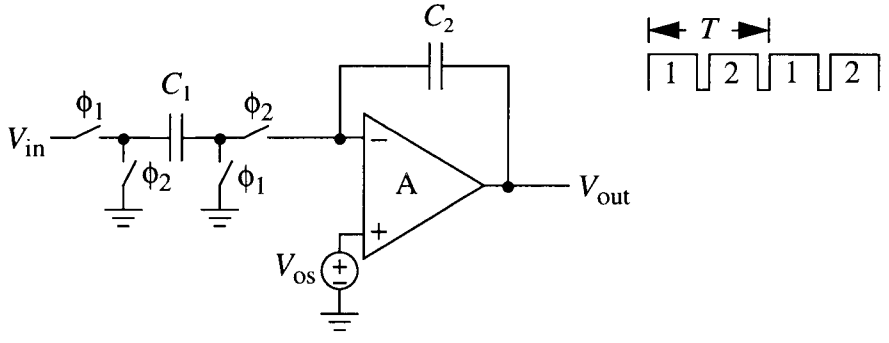


Figure 4.1: A switched-capacitor integrator.

For the circuit of Figure 3.5, the noise transfer function can be derived when the integrator is not ideal. Using the integrator transfer function shown in Eq. (4.3) and assuming $C_2 = 2C_1$ and $A = 1000$, the noise transfer function is

$$H(z) = \frac{1 - 0.9995z^{-1}}{1 - 0.001z^{-1}}, \tag{4.4}$$

and the signal transfer function is

$$G(z) = \frac{0.9985z^{-1}}{1 - 0.001z^{-1}}. \tag{4.5}$$

Figure 4.2 shows the plots of several noise transfer functions at low frequencies for the first-order delta-sigma modulator shown in Figure 3.5 with and without finite-gain

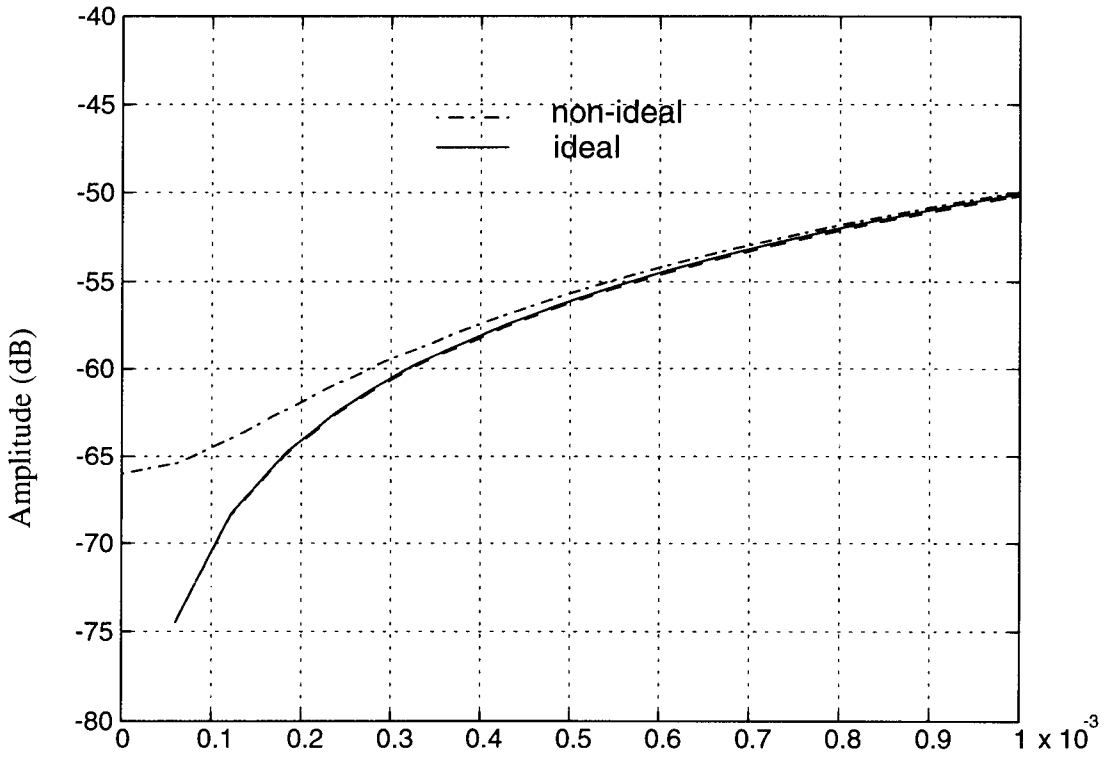


Figure 4.2: Noise transfer function plots for a first-order delta-sigma modulator.

effect of the opamp. Again $C_2 = 2C_1$ and $A = 1000$ are assumed. On the abscissa, "1" is equivalent to half of the sampling frequency. The solid line refers to an ideal first-order function $1 - z^{-1}$ and the dash-dot line refers to the non-ideal function shown in Eq. (4.4). The conclusions which can be drawn from Figure 4.2 are the following:

1. The finite-gain effect of the opamp reduces the attenuation of the quantization noise in the first-order lowpass delta-sigma modulator. This effect gets worse when the oversampling ratio is very high.

2. At low frequencies, the denominator in Eq. (4.4) is very close to 1 so Eq. (4.4) can be approximated by $1 - 0.9995 \cdot z^{-1}$. The error is due to the finite gain of the opamp which causes the deviation of the pole from 1 in the integrator transfer function of Eq. (4.3).

3. For the first-order modulator, the extra quantization noise (noise leakage) caused by the finite gain of the opamp depends on both the oversampling ratio and the gain of the opamp. The noise leakage is negligible if the opamp gain is larger than half of the oversampling ratio.

Notice that in Eq. (4.5) the signal transfer function is not unity. It can be approximated by just a constant 0.9985. This is due to the extra gain factor in Eq. (4.3) caused by the finite gain of the opamp. This gain error is usually tolerable in most applications. However, it will affect the cancellation of quantization noise in cascaded modulators when the noise cancellation is performed using an ideal noise transfer function in the digital filter.

The same analysis applies to the second-order modulator shown in Figure 3.12 with $a_1 = \frac{1}{2}$, $a_2 = \frac{1}{2}$, $b_1 = b_2 = 1$. The following noise transfer function is obtained

$$H(z) \approx \frac{(z-0.9995)^2}{z^2-0.002z} \cdot \tag{4.6}$$

The variation of the amplitude in the denominator is small (less than 0.04 dB) so the noise transfer function becomes $(1-0.9995\cdot z^{-1})^2$ or in a more general form $1-1/(2A)\cdot z^{-1})^2$, where A is the opamp gain. The amplitude response of the noise transfer function when A = 1000 is plotted in Figure 4.3. It can be seen that for OSR less than 1000, the difference between the ideal one and non-ideal one is smaller than the first order modulator but is larger than that in Figure 4.2 when OSR is larger than 1000. Therefore, if the second-order modulator needs an oversampling ratio of over 1024 to realize a large SNR, the gain of the opamp needs to be increased.

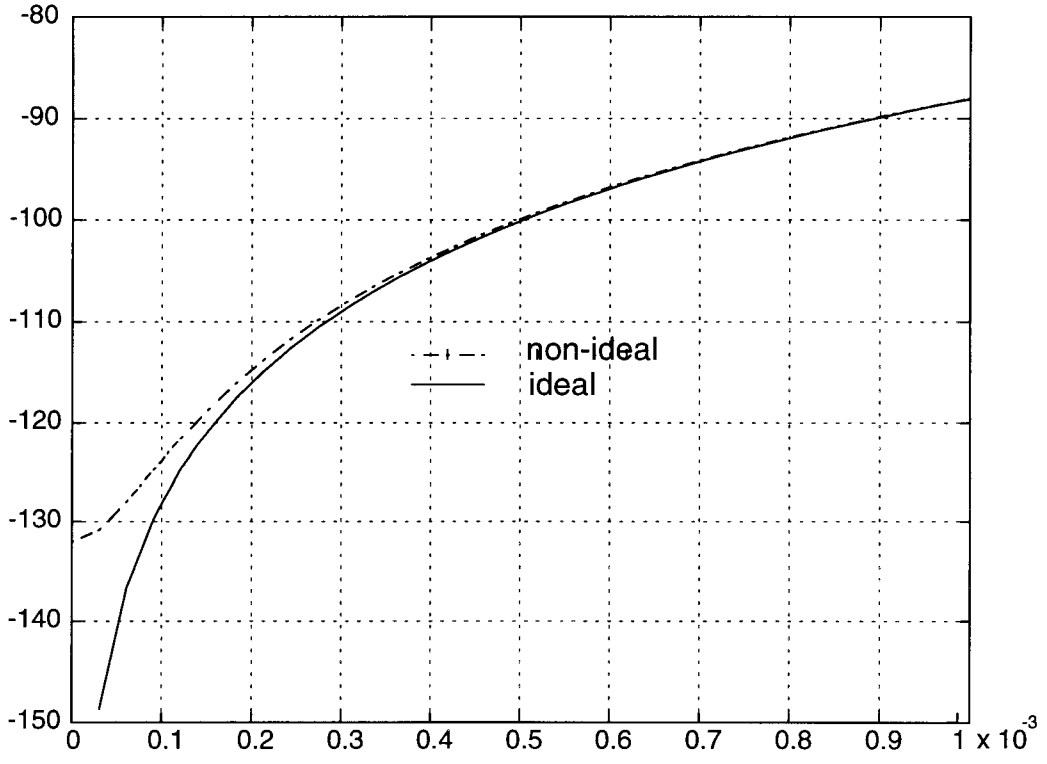


Figure 4.3: Noise transfer function plots for a second-order delta-sigma modulator.

It is straightforward to expect that by designing a high-gain opamp, the problem discussed above can be solved. This can only be achieved when the sampling frequency is not very high and at the cost of larger area and power consumption. However, if the bandwidth of the opamp is high, it is extremely hard to obtain a large gain for a standard CMOS process. Another alternative is to use correlated double sampling (CDS) techniques [46]. By holding the error voltage in the capacitors, and cancelling it later, the effective gain of the opamp can be increased. CDS technique can also be used to cancel the offset voltage.

4.2 Effect of Capacitor Mismatches

Another non-ideal circuit effect which also affects the noise transfer function is the mismatch of capacitors in SC delta-sigma modulators. Because of process variations, the capacitance varies at different locations, hence the capacitor ratio deviates from the designed value. In SC delta-sigma modulators, the realization of the signal and noise transfer functions relies on the ratio of capacitors. Hence, capacitor mismatches can cause deviation from an ideal noise transfer function. Suppose that the variation of capacitor ratio C_1/C_2 is δ and that the opamp gain is infinite. The integrator transfer function shown in Eq. (4.3) then becomes

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2}(1+\delta)\cdot\frac{z^{-1}}{1-z^{-1}}. \tag{4.7}$$

The value of δ depends on the process and the layout of the capacitors, and δ is a random number since the variation of the process is random.

Since the matching error in the realization of capacitor ratios only causes a gain error in the integrator transfer function and does not generate the pole deviation, it can be expected that the matching error of capacitors only causes a gain error in the signal transfer function in the first-order modulator. For higher-order modulators, the discussion is more complicated since there are more capacitors and the capacitor mismatches are random.

However, since the mismatch of capacitors does not cause pole error in the integrator, in the noise transfer function the numerator is the same as if there were no mismatch, and only the denominator is affected. The effect of capacitor mismatches can be empirically studied by Monte-Carlo simulations where capacitors can be deliberately mismatched within a certain range and the distribution of SNR due to capacitor mismatches is obtained.

Assuming that the standard deviation of the capacitor matching error is 0.3% (1 sigma) and the distribution of the error is Gaussian, the simulated SNR distribution of a second-order modulator is shown in Figure 4.4. The oversampling ratio of the modulator is 256 and the total number of simulations is 300. It can be observed that the distribution of the SNR is also Gaussian and the worst-case SNR is larger than 97 dB when the peak- to-peak capacitor matching error (6 sigma) is 1.8%.

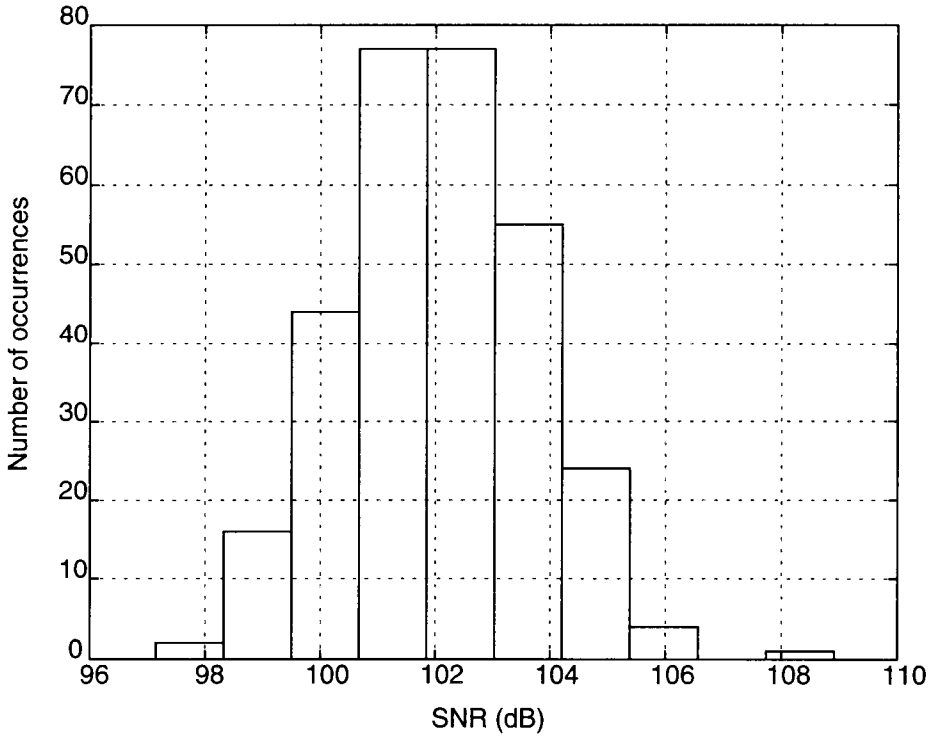


Figure 4.4: Monte-Carlo simulation for capacitor mismatches in a second-order delta-sigma modulator.

The matching error can be reduced by careful layout of the capacitors. There are some matching techniques in the layout [47] which can provide matching of capacitor as good as 0.1%. Then the error due to the matching error of capacitors may be negligible for the single-loop single-stage modulator as illustrated in Figure 3.12. However, it can still cause significant noise leakage in a high-resolution cascaded modulator.

4.3 Thermal Noise in SC Integrators

Thermal noise is perhaps the most fundamental error source in many switched-capacitor circuits. High-performance modulators can be designed so that the quantization noise is very small, but in actual realization the performance is often limited by the circuit noise, mainly the thermal noise due to the switches and opamps in the SC integrators.

4.3.1. Thermal Noise of the Switches

For the integrator shown in Figure 4.1, the switches can be represented by ideal switches associated with resistance, as illustrated in Figure 4.5. The noise power spectrum for a resistor is $4kTR\Delta f$ and the total noise power on the capacitor when $\phi_1 = 1$ can be found by evaluating the following integral

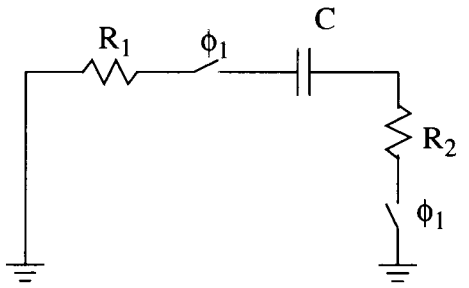


Figure 4.5: Equivalent switched-capacitor circuit for noise analysis.

$$e_T^2 = \int_0^\infty \frac{4kT(R_1 + R_2)}{1 + [2\pi f(R_1 + R_2)C]^2} df = \frac{kT}{C}, \tag{4.8}$$

assuming that the noise voltages generated by R_1 and R_2 are not correlated. Notice that the noise contribution of two resistors is equivalent to that of just one resistor. It should be pointed out that although the capacitor is noiseless, the resulting noise on the capacitor which is generated by the resistors is determined by the capacitor. The noise is often called the *kT/C* noise.

The noise bandwidth of the resistor in the *RC* network can be calculated as $f_n = \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{1}{4RC}$. When the sampling frequency f_s is larger than twice of f_n, the spectral density of the sampled noise can be regarded as

$$S(f) = \frac{1}{f_n}\frac{kT}{C} = 4RC\frac{kT}{C} = 4RkT, \tag{4.9}$$

up to f_n and 0 from f_n to $f_s/2$, which has the same spectral density as the noise of the resistor. However, because of settling time requirement, the *RC* constant is usually small and f_s is smaller than f_n. Hence noise will be aliased back to the band from 0 to $f_s/2$. Assuming that $\alpha = f_n/f_s$ and α is much larger than 1, then the noise spectral density is

$$S(f) \approx \frac{1}{f_n}\frac{kT}{C} \cdot 2\alpha = \frac{1}{f_n}\frac{kT}{C} \cdot 2\frac{f_n}{f_s} = \frac{2}{f_s}\frac{kT}{C}. \tag{4.10}$$

Since the capacitor is sampled and discharged in $\phi_1 = 1$ and $\phi_2 = 1$, the thermal noise is sampled twice in one clock period which results in a spectral density

$$S(f) = \frac{4}{f_s}\frac{kT}{C}. \tag{4.11}$$

Again the noise stored in the capacitor can be represented by the equivalent noise at the input and hence it reduces the dynamic range of the input signal.

Usually, in high-resolution delta-sigma data converters, the quantization noise is greatly reduced by using higher-order modulators or multi-bit quantizers, and the *kT/C* noise becomes the dominant noise source. Therefore, care must be taken in choosing the minimum input capacitors. For a given SNR and OSR, the total in-band noise power is $10^{(-SNR/10)}$ (dB), assuming the signal power is 0 dB. Then according to Eq. (4.11), the input capacitor should be larger than $2kT/(OSR*10^{(-SNR/10)})$. For example, if the desired SNR is 96 dB and OSR = 64, the input capacitor C should be at least 0.52 pF.

4.3.2. Thermal Noise of the Opamp

The thermal noise of the opamp is analyzed in [48]. For a single MOSFET transistor, the gate-referred noise is given by [49]

$$\overline{v_n^2} = \frac{8}{3} \cdot \frac{kT}{g_m} \cdot \Delta f . \tag{4.12}$$

Usually the opamp has very large gain and the input devices are the dominant noise sources. Hence the input-referred noise can be determined by the noise of the input devices and the bandwidth of the opamp. For a two-stage opamp with one dominant pole, the opamp unity gain bandwidth is often related to the Miller capacitor and is given by

$$f_{UGB} = \frac{g_m}{C_m}, \tag{4.13}$$

where g_m is the transconductance of the input device and C_m is the Miller compensation capacitor. The opamp thermal noise can then be approximated by

$$\overline{v_n^2} = \frac{8}{3} \cdot \frac{kT}{g_m} \cdot \frac{g_m}{C_m} = \frac{8}{3} \cdot \frac{kT}{C_m} . \tag{4.14}$$

Again, the noise is only determined by a capacitor [50]. The noise bandwidth is

$$f_n = \frac{g_m}{C_m} \cdot \frac{\pi}{2} . \tag{4.15}$$

Since the noise bandwidth of the opamp is often larger than the sampling frequency, noise is aliased from high frequency into the band from 0 to $f_s/2$. The higher the opamp bandwidth, the larger amount of the noise will get aliased [49].

4.4 Clock Feedthrough and Charge Injection

The switches in SC circuits are realized either by NMOS or PMOS devices, or by transmission gates. A clock signal is applied to the gate of the MOS transistor and turns it on and off alternately. When the transistor is used as a switch, it operates in its linear region and has nonzero on-resistance. In addition, MOS switches exhibit charge feedthrough and charge injection. Clock feedthrough is caused by the overlap capacitances between the gate and source or drain terminals, and charge injection is generated by the channel charge stored when the device is on [51]. The charge due to clock feedthrough for a NMOS transistor can be expressed as

$$Q_{cf} = -C_{ov}(V_{DD} - V_{in}), \tag{4.16}$$

where C_{ov} is the input voltage, C_{ov} is the overlap capacitor, V_{in} is the input voltage and the voltage of the control signal is V_{DD}. When the device is in its strong inversion region, the channel charge can be expressed as

$$Q_{ch} = -WLC_{ox}(V_{GS} - V_{TH}) = -WLC_{ox}(V_{DD} - V_{in} - V_{TH}). \tag{4.17}$$

where W, L are the width and length of the NMOS transistor, respectively, V_{GS} is the gate-source voltage, V_{TH} is the threshold voltage, and C_{ox} is the oxide capacitance per unit area. It can be seen from Eq. (4.16) and Eq. (4.17) that when the input V_{in} varies, the error charges due to either clock feedthrough or charge injection are signal dependent. This will cause distortions. However, in our circuits the input is connected to a DC signal, and the error due to charge injection and feedthrough only cause offset errors.

As a first-order approximation, the MOS switch can be modeled as a network containing an ideal switch, a resistor and some parasitic capacitors, as shown in Figure 4.7(a). C_{ov1} and C_{ov2} are the overlap capacitors from the gate to source and gate to the drain, respectively. The charge injection is represented by C_{gs}, C_{gd} and V_C. V_C is equal to V_{DD} - V_{in} - V_{TH}. C_{gs} and C_{gd} are the equivalent capacitors which represent the amount of channel charge flows to node 1 and 2, respectively. $C_{gs} + C_{gd} = WLC_{ox}$. C_s and C_d are the parasitics to ground and may affect the channel charge distribution, as will be shown later.

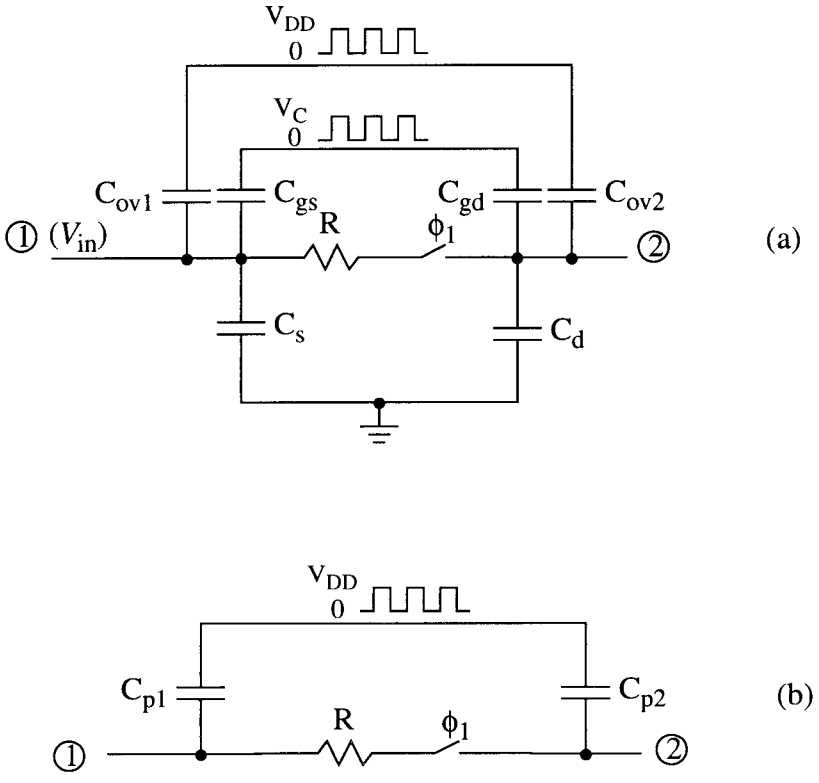


Figure 4.6: The models for clock feedthrough and charge injection of a NMOS switch: (a) a general model; (b) a simplified model when the input is DC.

This model can be further simplified by using two capacitors $C_{g1} = C_{ov1}+C_{gs}(V_{DD} - V_{in} - V_{TH})/(V_{DD} - V_{in})$, and $C_{g2} = C_{ov2}+C_{gd}(V_{DD} - V_{in} - V_{TH})/(V_{DD} - V_{in})$ to replace those four capacitors, as shown in Figure 4.6(b). Node 1 or node 2 is connected to an input signal and the control voltage across the capacitors is $(V_{DD} - V_{in})$. The charge stored in C_{g1} and C_{g2} when the switch is "on" is the sum of Q_{cf} and Q_{ch} in Eq. (4.16) and Eq. (4.17). Hence, this simplified model represents both clock feedthrough and charge injection. The model can also be applied to PMOS where the polarity of the clock is inverted and the threshold voltage is negative.

Usually, one side of the switch is connected to a noncritical low-impedance node such as the input or ground. Then only the capacitor which is not connected to the low impedance node contributes error charge to the circuit when the switch is turned off. The capacitor connected to the low impedance node is discharged between that node and ground when the switch is turned off. Therefore, the charge doesn't enter the circuit.

Figure 4.7 shows the simplified circuit of the SC integrator in Figure 4.1 using the NMOS switch model in Figure 4.6(a). For simplicity, only the transition when ϕ_1 changes from high to low is illustrated.

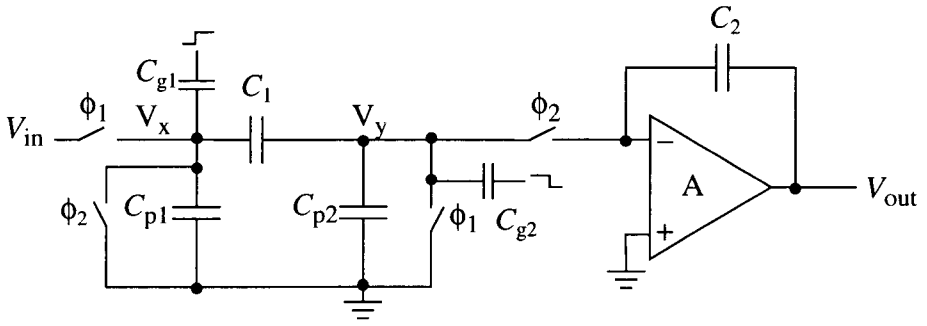


Figure 4.7: The model for clock feedthrough and charge injection analysis in an integrator.

Assume that the voltage that controls the switches is either high (V_{DD}) or low (0), and that the input and ground have low impedance. Note that in Figure 4.7(b), the parasitic capacitors of the switches associated with the input and ground terminals were eliminated because the charge flow to those terminals do not contribute error voltages. When ϕ_1 is high, C_{g1} is charged to (V_{DD} - V_{in}), C_{g2} is charged to V_{DD}, C_{p1} is charged to V_{in}, C_{p2} is discharged to ground, and C_1 is charged to V_{in}. When ϕ_2 goes high, the charges are redistributed, and by using nodal analysis, the following equations can be obtained

$$(V_x + V_{DD} - V_{in})C_{g1} + (V_x - V_{in})C_{p1} + (V_x - V_y - V_{in})C_1 = 0, \text{ and} \qquad (4.18)$$

$$(V_y + V_{DD})C_{g1} + V_y C_{p2} + (V_y - V_x + V_{in})C_1 = 0. \qquad (4.19)$$

Solving for V_x and V_y results in the following

$$V_x - V_y = V_{in} - V_{DD}\left(\frac{C_{g1}+C_{g2}}{C_p+C_{g1}} + \frac{C_1\dfrac{C_{g1}+C_{g2}}{C_p+C_{g1}} + C_{g2}}{C_p + C_{g1} + C_1\left(1+\dfrac{C_p+C_{g2}}{C_p+C_{g1}}\right)}\left(1+\frac{C_p+C_{g2}}{C_p+C_{g1}}\right)\right), \qquad (4.20)$$

where $C_p = C_{p1} = C_{p2}$ is assumed. Here, $C_{g1} = C_{ov} + C_{gs}(V_{DD} - V_{in} - V_{TH})/V_{DD}$ and $C_{g2} = C_{ov} + C_{gs}(V_{DD} - V_{TH})/V_{DD}$. In sensor interface applications where C_1 is usually off-chip, or has a large on-chip structure, C_p is usually much larger than C_{g1} or C_{g2}. Then Eq. (4.20) can be simplified to

$$V_x - V_y \approx V_{in} - V_{DD}\left(\frac{C_{g1}+C_{g2}}{C_p} + 2\frac{C_1\dfrac{C_{g1}+C_{g2}}{C_p} + C_{g2}}{C_p + 2C_1}\right). \qquad (4.21)$$

Now the charge stored in C_1 is no longer $C_1 V_{in}$ and the error charge is

$$C_1(V_x - V_y) - C_1 V_{in} \approx C_1 V_{DD}\left(\frac{C_{g1}+C_{g2}}{C_p} + 2\frac{C_1\dfrac{C_{g1}+C_{g2}}{C_p} + C_{g2}}{C_p + 2C_1}\right). \qquad (4.22)$$

Some conclusions can be drawn from Eq. (4.22):

1. The error charge is determined by the "high" voltage of the clock signal, usually V_{DD}. The higher V_{DD}, the larger the error;

2. The parasitic capacitance C_p also affects the error. The error is smaller if C_p is larger;

3. The error also depends on the sensor or tested capacitor C_1;

4. C_{g1} and C_{g2} should be made as small as possible to reduce the error. This requires minimum size of the switch, as small as the settling requirement allows.

The exact calculation of C_{g1} and C_{g2} is usually complicated, since the amount of charge injection to the drain and source side depends on the load on each side, as well as on the slope of the clock. Assuming that the load condition is the same on both side of the switch, then

$$C_{g1} = C_{ov} + \frac{1}{2}WLC_{ox}(V_{DD} - V_{in} - V_{TH})/(V_{DD} - V_{in}), \text{ and} \qquad (4.23)$$

$$C_{g2} = C_{ov} + \frac{1}{2}WLC_{ox}(V_{DD} - V_{TH})/V_{DD}. \qquad (4.24)$$

The error due to charge injection and clock feedthrough effect can be reduced by using calibration, or by realizing the circuit in a fully-differential configuration, as will be shown in Chapters 5 and 6.

4.5 Flicker Noise

Flicker noise exists in both bipolar and MOSFET devices. In a MOSFET device, it is caused by traps associated with contamination and crystal defects. The noise of a MOSFET transistor can be modeled as an equivalent gate-referred voltage source and its spectral density is

$$S(f) = \frac{K}{WL}\frac{1}{f}. \tag{4.25}$$

Since the noise spectral density has a $1/f$ frequency dependence, the flicker noise is often called the $1/f$ noise. It is the dominant noise source for the opamp at low frequencies, and hence it might be the limiting factor in the sensor interface circuit, where the bandwidth of the signal is usually from DC to a few kHz. As Eq. (4.25) shows, the $1/f$ noise can be made smaller by increasing the size of the input transistors. For the opamp, the input pair is usually the dominant noise source, and the size of these transistors can be increased to minimize $1/f$ noise. However, the size increase makes the area larger and may reduces the bandwidth because of the parasitics associated with larger transistors.

In some state-of-the-art CMOS processes, K in Eq. (4.25) for a PMOS transistor is much smaller than for an NMOS transistor. If PMOS transistors are used as input devices, $1/f$ noise may not be a problem when the input transistors are properly sized [52]. However, in a lot of processes, care needs to be taken to reduce this noise. Fortunately, several techniques have been reported to solve this problem. One technique is the chopper-stabilization method which modulates the inputs of an opamp [53]. Another technique is the CDS technique which is briefly discussed in Sec. 4.1. CDS is very effective in canceling low-frequency noise. Moreover, it can also reduce the finite gain effect of the opamp. Hence it is used in the implementations of the single-ended and fully-differential sensor interface circuits, as will be shown in Chapters 5 and 6.

Chapter 5. Design and Implementation of Single-Ended Circuits

In this chapter, the design of two single-ended circuits for capacitive sensor readout or capacitor ratio measurement is described. Two calibration schemes are proposed to cancel the effects of clock feedthrough and charge injection. A single-ended circuit which uses two clock phases and provides a linear output for differential capacitive sensors was implemented. From the test chip, the measured standard deviation of the tested capacitors is less than 100 aF for a clock frequency of 500 kHz.

5.1 Design of a High-Accuracy Two-Phase Circuit

The schematic of a second-order circuit for capacitor ratio testing and sensor readout has been described in Chapter 3 and its functionality has also been verified using SWITCAP2. The simulation result showed that a capacitance resolution as small as 0.1 fF for 10 pF capacitors could be achieved. However, it should be noted that in the simulations the circuit's non-ideal effects haven't been included.

As discussed in Chapter 4, circuit non-idealities such as the input offset and finite gain of the opamp, clock feedthrough and charge injection can greatly reduce the accuracy of the circuit. By using techniques such as CDS and self-calibration, these non-ideal effects can be greatly reduced.

5.1.1. CDS Circuit Design

As mentioned earlier in Section 4.1, CDS technique can be used in SC circuits to cancel the opamp's input offset and increase the effective gain of the opamp. The way CDS technique usually works is that the error voltage due to the finite gain and input offset of the opamp is stored in one or more capacitors during one clock phase, and then the error voltage will be subtracted in another clock phase [46]. A simple CDS circuit for the two-

phase circuit shown in Figure 3.17 can be realized by adding an extra capacitor C_h and some switches, as shown in Figure 5.1. For simplicity, only the first-stage integrator is shown. When ϕ_1 is high, C_h samples the opamp input voltage V_{in}, which contains the error due to finite gain and input offset. Then, when ϕ_2 is high, C_h is floating and the voltage across C_h remains unchanged. Therefore, V_g becomes the virtual ground and it is given by

$$V_g = V_{in}(n) - V_{in}(n-1), \tag{5.1}$$

where n refers to the nth clock cycle. In order to find out how V_g changes, it is necessary to examine the input and output voltages of the opamp in the integrator shown in Figure 5.1.

The output waveform when the values of C_1 and C_2 are nearly the same was shown in Figure 3.8, and the input waveform is depicted in Figure 5.2, assuming that the gain of the opamp is A and the input offset is V_{os}. It is clear that the change of V_{in} depends on the level of y. It can be derived from Eq. (5.1) and Figure 5.2 that V_g is either

$$V_g = \frac{V_{ref}}{A}\frac{C_2}{C_f}, \tag{5.2}$$

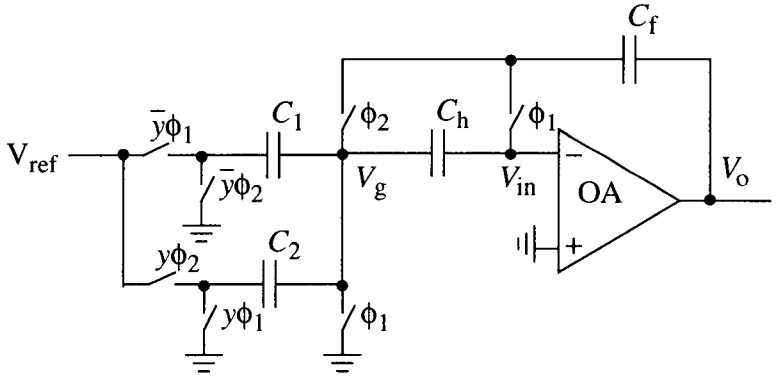


Figure 5.1: A simple CDS structure.

when $y = 1$, or

$$V_g = -\frac{V_{ref}}{A}\frac{C_1}{C_f}, \tag{5.3}$$

when $y = 0$. From Eq. (5.2) and Eq. (5.3), it can be seen that while V_g is still dependent on the gain of the opamp, V_{os} has been eliminated in V_g due to the differentiation in Eq. (5.1). It should be noted that since the $1/f$ noise of the opamp is at low frequencies, its variation between two adjacent clock cycles is also small. Therefore, it is greatly attenuated in V_g according Eq. (5.1).

Figure 5.3 shows the improved CDS circuit used to reduce the dependence of V_g on A. Capacitors C_{h1} and C_{h2} are used to store V_{in} when $y = 1$ and $y = 0$, respectively. The change of V_{in} is as before, but now V_g becomes

$$V_g = \frac{V_{ref}}{A}\frac{C_1 - C_2}{C_f}, \tag{5.4}$$

when $y = 1$, or

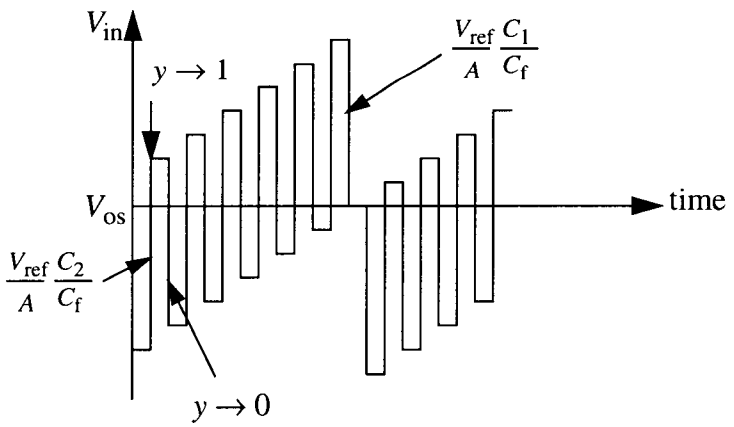


Figure 5.2: The opamp input voltage of the first-order two-phase circuit.

$$V_g = \frac{V_{ref}}{A}\frac{C_2 - C_1}{C_f}, \tag{5.5}$$

when $y = 0$. Comparing Eq. (5.4) and Eq. (5.5) with Eq. (5.2) and Eq. (5.3), it can be seen that V_g is greatly reduced when the difference between the tested capacitors C_1 and C_2 is small.

To verify the effectiveness of the discussed CDS schemes, the second-order circuit shown in Figure 3.17 has been simulated in SWITCAP2 first without using CDS, then using the simple scheme in Figure 5.1 and finally using the scheme in Figure 5.3. In the simulations, the opamp was assumed to have an input offset of 5 mV and a finite gain of 1000, and C_1 and C_2 were 10.5 pF and 10 pF, respectively. The simulation results are shown in Figure 5.4. The estimation error is again defined as $|C_2 - C_{2T}|/C_{nom}$, the same as in Chapter 3. It is obvious that by using CDS, the error due to the opamp input offset was drastically reduced. The simulation results also indicates that the CDS scheme shown in Figure 5.3 improves the measurement accuracy by approximately 5 dB, compared to the simple CDS scheme.

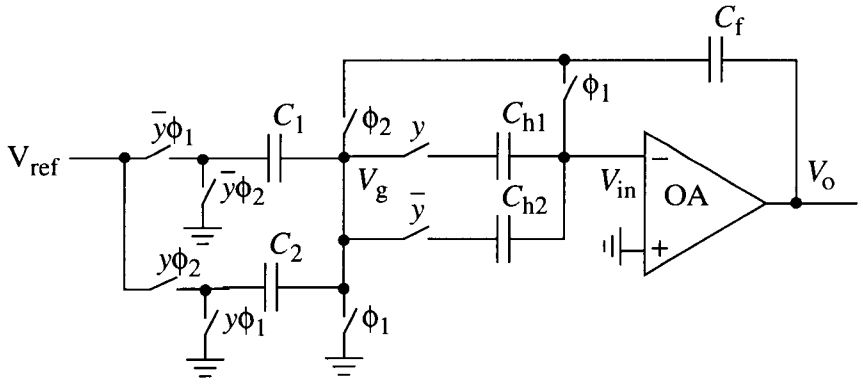


Figure 5.3: The improved CDS circuit for the two-phase circuit.

The error due to opamp finite-gain and input offset in the second stage of the circuit shown in Figure 3.17 is greatly reduced by the inverse transfer function of the first-stage integrator, which is a first-order noise-shaping function. Therefore, CDS is only needed for the first stage.

5.1.2. Calibrations for Clock Feedthrough and Charge Injection

The simulation results shown in Figure 5.4 ignored the non-ideal effect of the switches. However, when the capacitors are around 10 pF, for fast settling, the switch sizes must be much larger than the minimum size. Therefore, the clock feedthrough and charge injection of the switches can't be ignored.

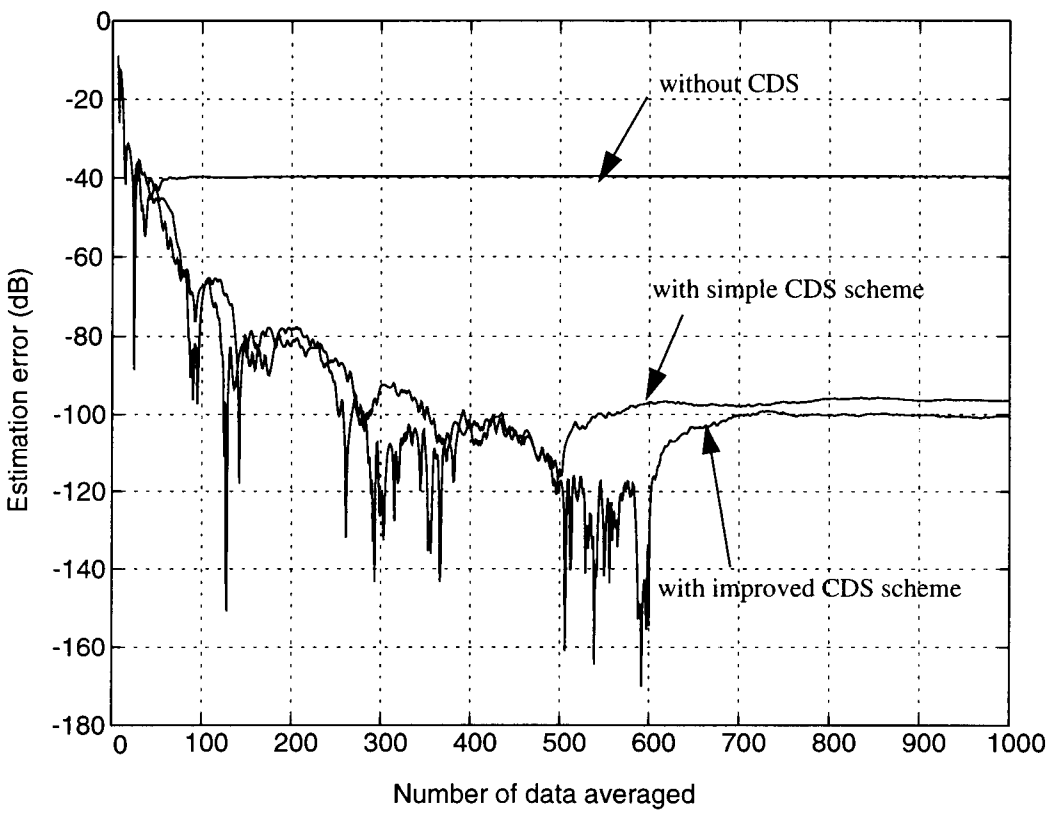


Figure 5.4: Simulation results for the two-phase circuit with non-ideal opamps.

Figure 5.5 illustrates the input stage of the second-order circuit shown earlier in Figure 3.17. It has been shown in Section 4.4 that when one side of the switch is connected to a low impedance node, the clock feedthrough and charge injection may be modeled as a capacitor C_g with a voltage step (V_{DD} - V_{in}). Therefore, in Figure 5.5, all the switches except S_6 can be replaced by an ideal switch and a capacitor C_g with a voltage step source. From Eq. (4.16) and Eq. (4.17), the amount of charge injected into C_1 when S_1 is turned off can be approximately written as

$$Q_{err} = -(V_{DD} - V_{ref})C_g = -(V_{DD} - V_{ref})k\left(C_{ov} + C_{gd}\frac{V_{DD} - V_{in} - V_{TH}}{V_{DD} - V_{ref}}\right) \quad (5.6)$$

where k represents the fraction of the charge in S_1 transferred from S_1 to C_1, (1-k) is the fraction that enters the parasitic capacitance at node 1 and C_{gd} is the equivalent capacitance that represents the charge injection from S_1. When C_1 is fixed, k and C_{gd} are also fixed because the voltage across C_1 is always V_{ref} before S_1 is turned off. Therefore, the charge from S_1 to C_1 is also fixed. For the same reason, when S_2 is turned off the error charge from S_2 to C_1 is also fixed. S_5 and S_6 also cause charge injection to C_1. When S_5 is turned off, the extra charge due to clock feedthrough and charge injection of S_5 is

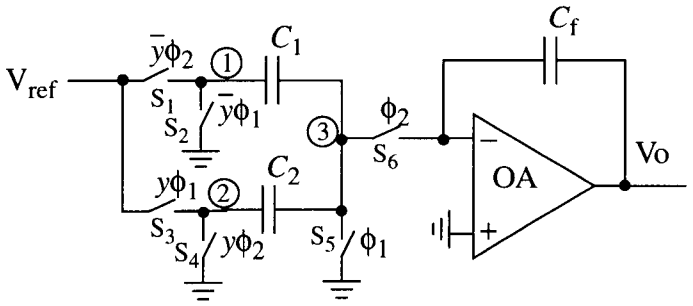


Figure 5.5: The input stage.

distributed between C_1, C_2 and the parasitic capacitance at node 3. Again, because the load condition is the same when y is "0" and when y is "1", the charge injected to C_1 is fixed. For S_6, the load condition on the right side changes because the opamp output varies. However, because the output voltage is close to random and the average is 0, it can be assumed that the average load for S_6 is also fixed, and therefore the charge injection from S_6 to C_1 is also fixed.

For C_2, the switches that contribute to charge injection are S_3 through S_6. For a constant C_2, the injected charge due to those switches is also fixed. It should be noted that the charge injection to C_1 can cause errors in the output only when y is "0" because the charge stored in C_1 is transferred to C_f when y is "0". For C_2, the injected charge causes an error only when y is "1". However, the injected charge from S_6 to C_f causes an offset error in each clock cycle at the output when y is either "1" or "0". Therefore, the charge balancing equation in Eq. (3.13) can be expressed as the following

$$n(C_2V_{ref}+Q_2)-(N-n)(C_1V_{ref}+Q_1)+NQ_f\approx 0\,, \tag{5.7}$$

where Q_1, Q_2 and Q_3 are the error charges stored in C_1, C_2 and C_f, respectively.

The average of the binary data y becomes

$$y_{ave}\approx\frac{C_1V_{ref}+Q_1+Q_f}{C_2V_{ref}+C_1V_{ref}+Q_2+Q_1}=\frac{C_1}{C_1+C_2}\cdot\frac{1+\dfrac{Q_1-Q_f}{C_1V_{ref}}}{1+\dfrac{Q_2+Q_1}{C_2V_{ref}+C_1V_{ref}}}\,. \tag{5.8}$$

Comparing Eq. (5.8) with Eq. (3.14), it can be seen that y_{ave} contains a constant gain error, assuming that C_1 and C_2 are fixed. The error is due to the clock feedthrough and charge injection of the switches. Reducing the control voltage for the switches can reduce the error. However, if the settling time remains the same, reducing the control voltage leads to larger switches, which increases C_g and may increase the error in y_{ave}.

The output error due to clock feedthrough and charge injections can be cancelled by using calibration. In Eq. (5.8), when $C_1 = C_2$, the average of y is equal to

$$y_{ave} \approx \frac{1}{2} \cdot \frac{1 + \frac{Q_1 - Q_f}{C_1 V_{ref}}}{1 + \frac{Q_2 + Q_1}{C_2 V_{ref} + C_1 V_{ref}}} \quad . \tag{5.9}$$

Ideally, y is 0.5 when there is no clock feedthrough and charge injection. If the output is measured when C_1 and C_2 are equal, the gain error can be obtained. Hence, when $C_1 \neq C_2$, the gain error can be cancelled by dividing Eq. (5.8) by Eq. (5.9), and the following is obtained

$$\frac{C_1}{C_1 + C_2} \approx \frac{y_{ave}}{2y'_{ave}} \quad , \tag{5.10}$$

where y_{ave} and y'_{ave} are the average values of y when $C_1 \neq C_2$ and $C_1 = C_2$, respectively. Hence, the capacitor ratio C_2 / C_1 can be derived as

$$\frac{C_2}{C_1} \approx \frac{2y'_{ave}}{y_{ave}} - 1 \quad . \tag{5.11}$$

The calibration scheme is illustrated in Figure 5.6. For simplicity, only the first stage is shown. The measurement is divided into two steps. First, the signal ϕ_{cal} is set to "1", and capacitor C_2 is disconnected. C_1 is used whether y is "0" or "1", and this is equivalent to the case when $C_2 = C_1$. Therefore, y'_{ave} in Eq. (5.10) is obtained. Next, ϕ_{cal} is set to "0" so $\overline{\phi}_{cal}$ is "1". Now the circuit is in its normal measuring mode, and y_{ave} is obtained. The capacitor ratio can be measured using Eq. (5.11), and the error due to clock feedthrough and charge injection is cancelled.

Another calibration scheme is depicted in Figure 5.7. The measurement is again divided into two steps. First, the signal ϕ_{cal} is set to "0". The circuit is in the normal measuring mode and y_{ave} is obtained. Then ϕ_{cal} is set to "1" and the positions of C_2 and C_1

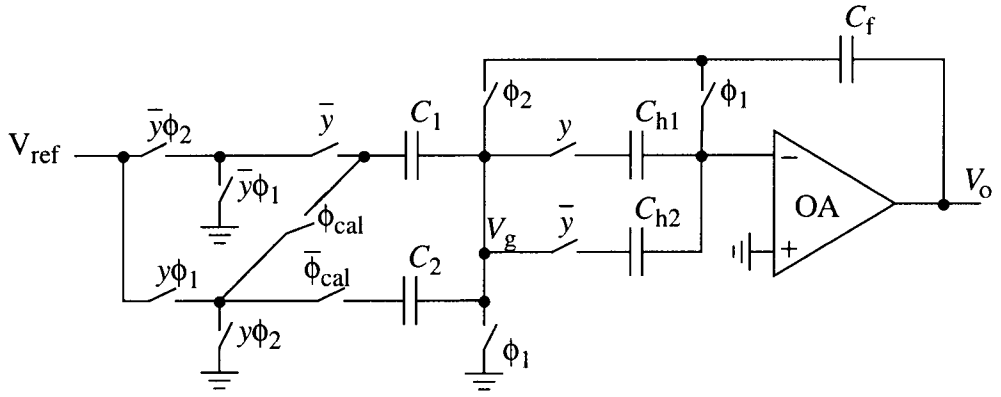


Figure 5.6: A calibration scheme (#1) to cancel the error due to clock feedthrough and charge injection.

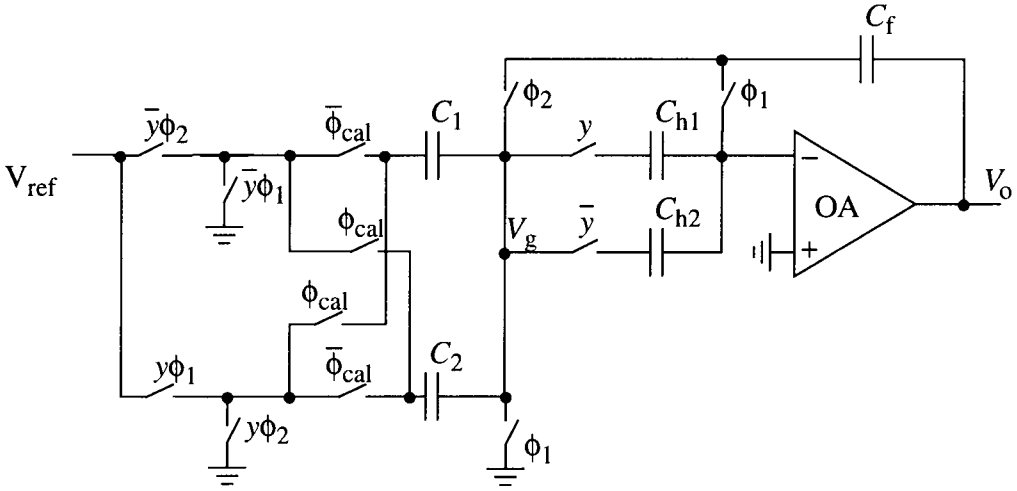


Figure 5.7: Another calibration scheme(#2) to cancel the error due to clock feedthrough and charge injection.

are exchanged. The average of y is now y'_{ave}. From Eq. (5.7), when ϕ_{cal} is "0", it can be shown that

$$\frac{C_1}{C_1+C_2} \approx y_{ave} + y_{ave}\frac{Q_2+Q_1}{(C_2+C_1)V_{ref}} - \frac{Q_1-Q_f}{(C_2+C_1)V_{ref}}. \tag{5.12}$$

When ϕ_{cal} is "1", Eq. (5.12) becomes

$$\frac{C_2}{C_1+C_2} \approx y'_{ave} + y'_{ave}\frac{Q_2+Q_1}{(C_2+C_1)V_{ref}} - \frac{Q_1-Q_f}{(C_2+C_1)V_{ref}} \quad . \tag{5.13}$$

When Eq. (5.12) is subtracted from Eq. (5.13), it results in

$$\frac{C_1-C_2}{C_1+C_2} \approx (y_{ave}-y'_{ave}) + (y_{ave}-y'_{ave})\frac{Q_2+Q_1}{(C_2+C_1)V_{ref}} \approx (y_{ave}-y'_{ave}) \quad . \tag{5.14}$$

Hence, the capacitor ratio can be obtained by subtracting the two measured averages, and the error due to clock feedthrough and charge injection is cancelled.

The validity of the above discussions and the proposed calibration schemes has been verified by SWITCAP2 simulations. Figure 5.8 shows the simulation results with the

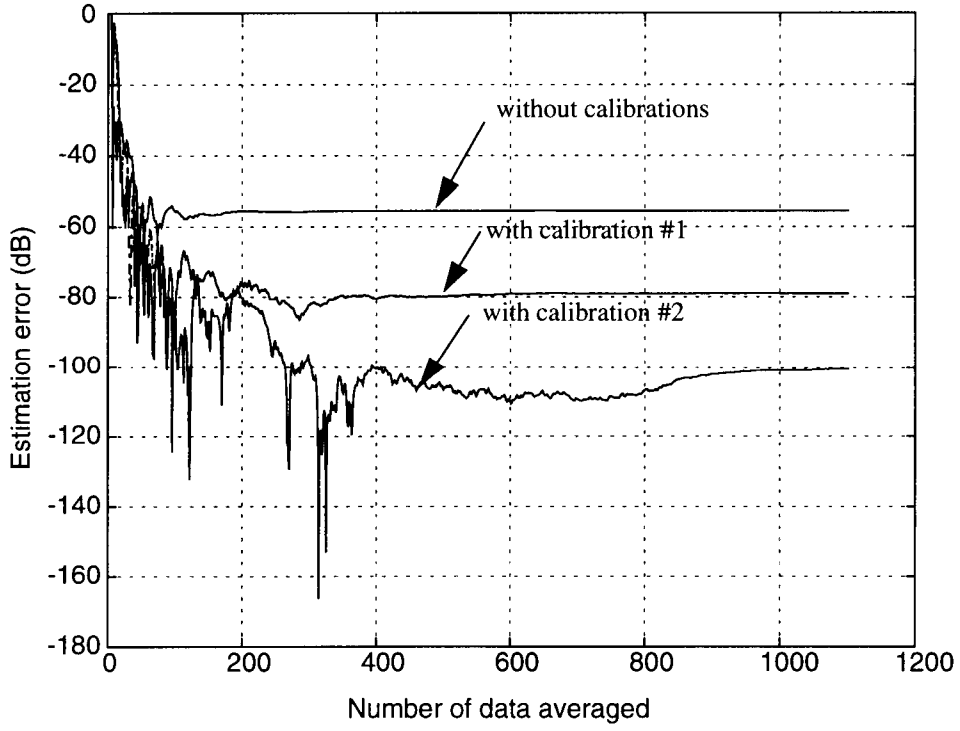


Figure 5.8: Simulation results for the two-phase circuit with clock- feedthrough effect and charge injections.

non-ideal NMOS switch model in SWITCAP2 [54]. In the simulations, C_1 = 10.5 pF and C_2 = 10 pF was assumed. The effect of calibration is obvious. It can be seen that calibration scheme #2 provides better cancellation of the error due to clock feedthrough and charge injection. This is because (as shown in Figure 5.6), only C_1 is charged and discharged when ϕ_{cal} is "1" and this is different from the case when C_1 and C_2 are both used. Therefore, the error terms in Eq. (5.8) and Eq. (5.9) are not equal, and the cancellation shown in Eq. (5.10) still has an error left. By contrast, in Figure 5.6, the errors due to clock feedthrough and charge injection are almost the same when ϕ_{cal} is "0" and ϕ_{cal} is "1", so the cancellation is more effective.

Figure 5.9 shows the simulated estimation error for different values of C_2 for the second-order circuit shown in Figure 3.17, with the first stage replaced by the circuit shown

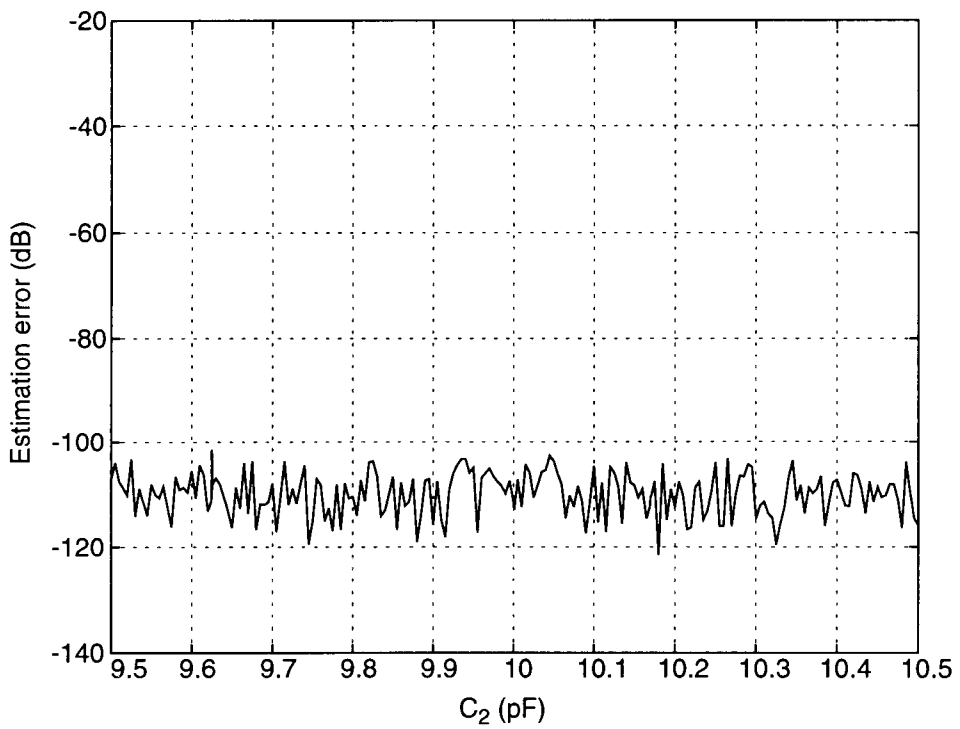


Figure 5.9: Simulated estimation error vs. C_2 for the two-phase circuit shown in Figure 5.7.

in Figure 5.7. It can be seen that even when non-ideal opamps are used, the estimation error is below -100 dB, which corresponds to a resolution of 100 fF for 10 pF capacitors.

5.2 Design of a High-Accuracy Four-Phase Circuit

5.2.1. CDS Circuit Design

For the four-phase circuit shown in Figure 3.10, the finite gain and input offset of the opamp can also reduce the accuracy of the circuit. Since the output of the opamp is similar to that in Figure 3.8 when C_1 and C_2 are nearly equal, the CDS scheme shown in Figure 5.7 can be used also for the four-phase circuit. A SWITCAP2 simulation result is shown in Figure 5.10, assuming that the opamp has a DC gain of 60 dB and a 5 mV input

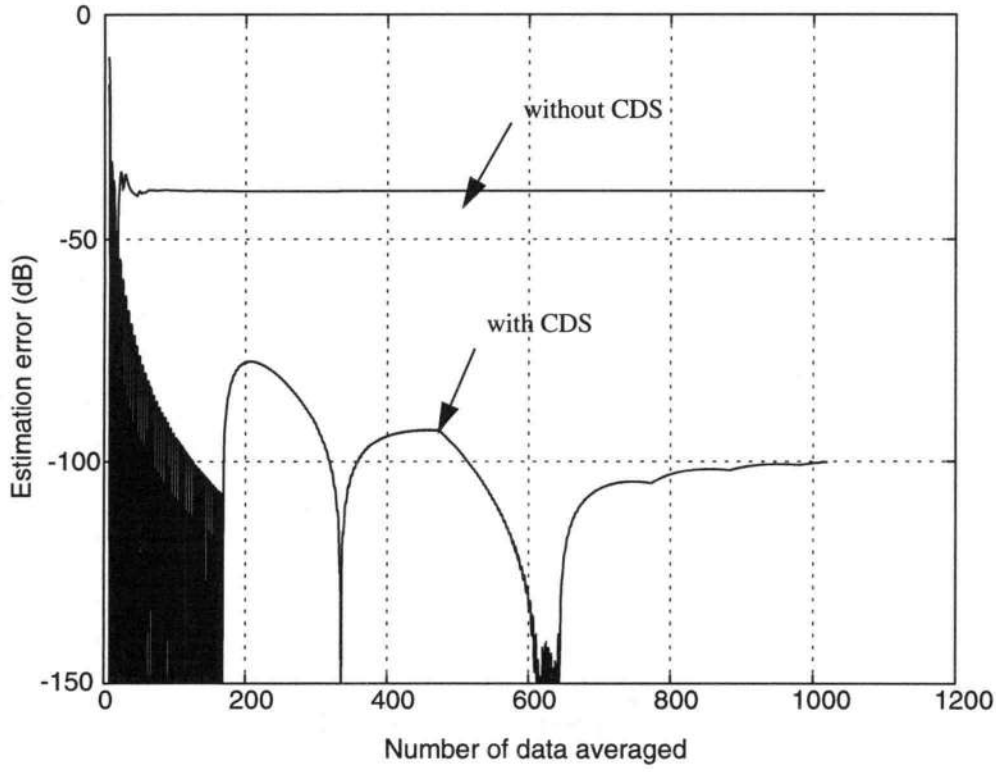


Figure 5.10:Simulation results for the four-phase circuit with non-ideal opamps.

offset. It shows that by using CDS, the error due to finite gain and input offset of the opamp is greatly reduced.

5.2.2. Calibration for Clock Feedthrough and Charge Injection

Figure 5.11 shows the complete schematic of the four-phase circuit with calibration. During the period when ϕ_c is "0", the circuit is in the normal measurement mode and the operation is the same as discussed in Chapter 3. Then when ϕ_c is "1", the circuit is in its calibration mode, and C_1 is disconnected from the reference voltage V_{ref} when ϕ_1 is high. Next, when ϕ_2 is high, C_2 is also disconnected from V_{ref}, so ideally, at the end of ϕ_2 = "1", there is no charge delivered to C_{f1} and the average of the output data y should be 0.5. This is equivalent to the case when $C_1 = C_2$. But due to clock feedthrough and charge injection, the net charge delivered to C_{f1} is not zero, and the average of output y is no longer 0.5. The principle of calibration is very similar to the two-phase circuit in Figure 5.6. Basically, the error is stored in the calibration phase and cancelled later in the

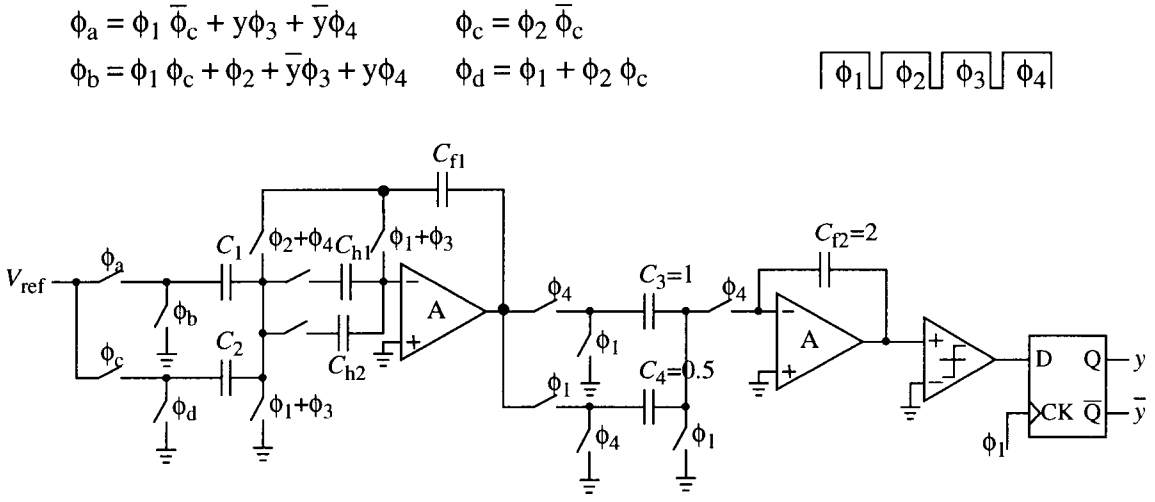


Figure 5.11:Schematic of the four-phase circuit with calibration.

measurement phase. If the error is considered as an offset in the output, then during the calibration phase the average of y can be represented by

$$y'_{ave} \approx 0.5 + y_{err}\,, \tag{5.15}$$

where y_{err} is the error due to clock feedthrough and charge injection. During the measurement phase when ϕ_c = "0", the average of y becomes

$$y_{ave} \approx \frac{C_2}{2C_1} + y_{err}\,, \tag{5.16}$$

assuming the error remains the same. Therefore, the capacitor ratio is

$$\frac{C_2}{C_1} \approx 2(y_{ave} - y'_{ave} + 0.5). \tag{5.17}$$

The simulation results after calibration are shown in Figure 5.12 for different values of C_2.

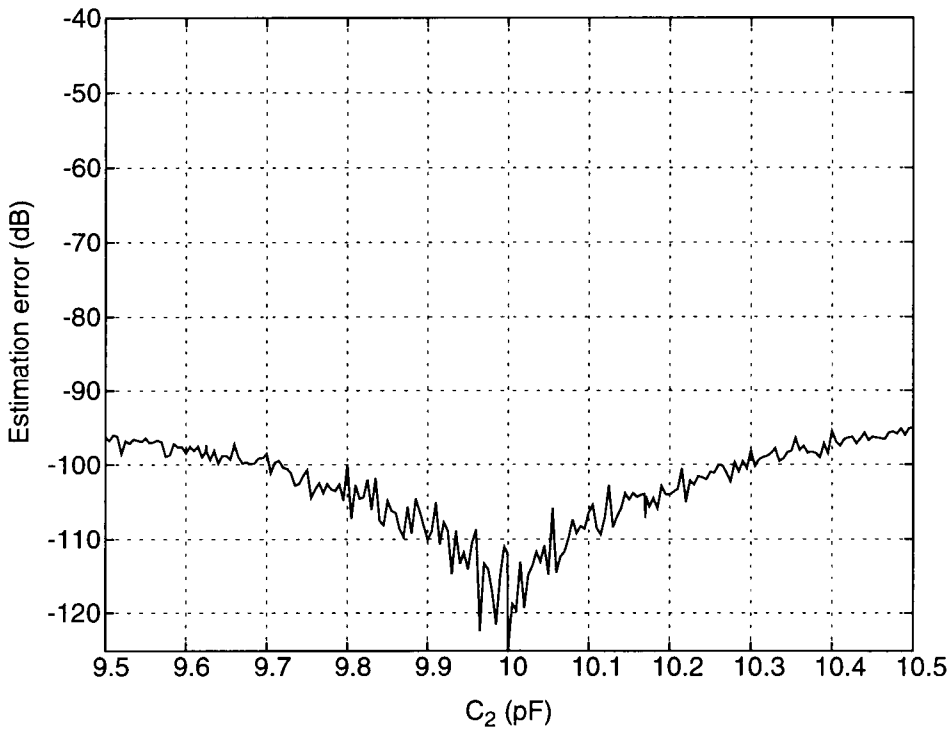


Figure 5.12:Simulated estimation error vs. C_2 for the four-phase circuit.

It can be seen that after calibration the error becomes larger when C_2 is further off from its nominal value 10 pF. This indicates that the calibration is more effective when C_1 and C_2 are close. This is because the switches in the four-phase circuit are on-and-off more often than in the two-phase circuit in one clock period, hence generating more clock feedthrough and charge injection. Furthermore, the calibration assumes that the error terms in Eq. (5.15) and Eq. (5.16) are equal, but when the difference between C_1 and C_2 becomes bigger, the load for the switches changes, and hence the distribution of error charges to C_1 and C_2 changes. Hence, the difference between the error term in Eq. (5.15) and Eq. (5.16) becomes bigger, and the calibration is less effective.

5.3 Implementation of the Two-Phase Circuits

As shown in Section 5.1 and Figure 3.17, the two-phase circuits with different calibration schemes can be realized by using switches, capacitors, opamps, a comparator and some digital blocks.

The switches are realized by CMOS transmission gates. To minimize the clock feedthrough and charge injection from the switches, all the transistors for the switches have minimum channel length: 1.2 μm. The width of the transistors should also be chosen to be the minimum size that the settling requirement allows.

The tested capacitors are the only input capacitors, and (as shown in Section 4.3.1) the thermal noise of the switches is determined by the values of input capacitors. The tested capacitors have a nominal value of C = 10 pF each, and the input referred noise due to the input switches is

$$P_{thermal} = 10 \cdot \log 10\left(\frac{k \cdot T}{OSR} \cdot \frac{4}{C}\right) \quad \text{dB.} \tag{5.18}$$

For OSR = 512, the noise level is below -114 dB. Hence, the noise contribution from the

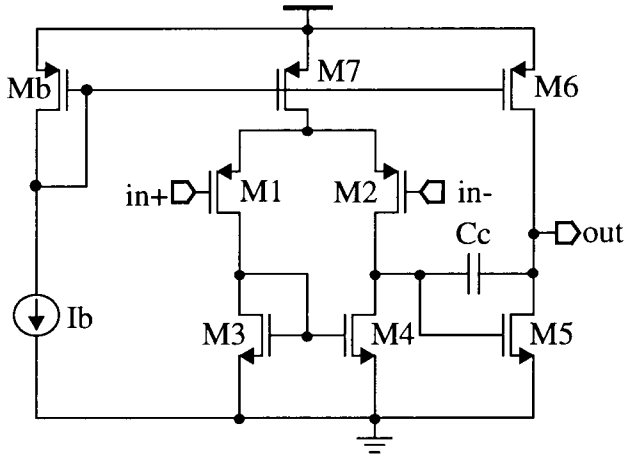


Figure 5.13:The two-stage opamp used in the two-phase implementation.

switches is negligible for a desired estimation error of -100 dB. Since the thermal noise from the second stage is first-order shaped, the input capacitors for the second stage can be smaller. The minimum capacitance was chosen to be 1 pF.

Since CDS is used, the opamp does not need high gain and low input offset. A regular two-stage architecture was chosen for the opamp, because it is fairly easy to design and a DC gain of 60 dB can easily be achieved. Figure 5.13 shows the schematic of the single-ended opamp and Table 5.1 summarizes the simulated performance of the opamp using a 1.2 μm Hspice Level 28 model. The opamp also has a large output range which is

Table 5.1: Simulated performance of the two-stage opamp.

DC gain (dB)	Unit-Gain Bandwidth (MHz)	Phase Margin (degree)	Slew Rate (V/μs)
62	15	70	15

needed since the input capacitors can be as big as 10 pF each, and hence the variation of the opamp output can be large. The same type of opamp is used in both the first and second stages.

The comparator used in the single-ended implementation is a dynamic comparator, as shown in Figure 5.14 [24]. Since the comparator appears after the second integrator, the non-idealities associated with it are shaped the same way as the quantization noise. However, there are still design issues such as metastability and hysteresis to observe. By resetting the comparator when clk is low, the hysteresis issue is solved.

The digital blocks include a non-overlapping two-phase clock generator, a *D* flip-flop and some logic gates used to generates the control signal for the input switches shown in Figure 3.17.

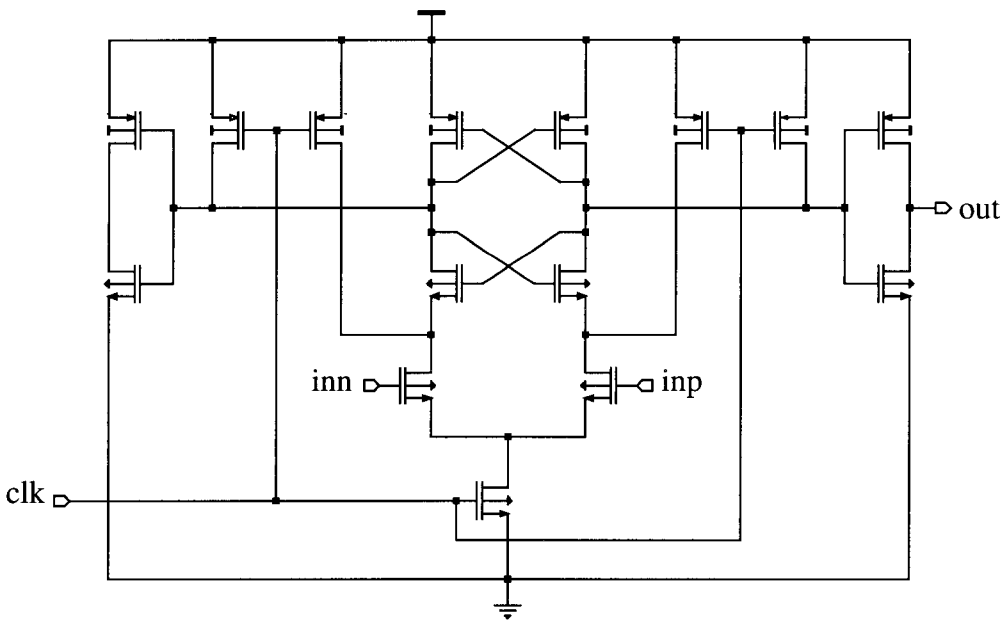


Figure 5.14:The dynamic comparator.

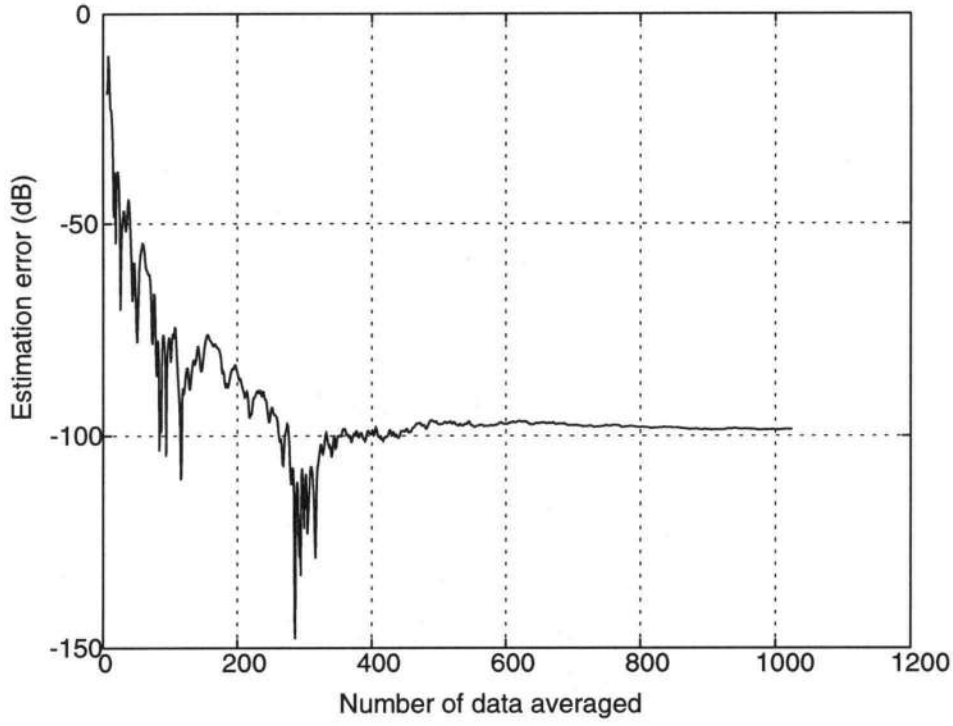


Figure 5.15:Hspice simulation result for the single-ended two- phase implementation.

Figure 5.15 shows the Hspice simulation result for the second-order two-phase circuit using the calibration scheme shown in Figure 5.7. C_1 = 10 pF and C_2 = 9.5 pF were assumed in the simulation. The clock frequency was 1 MHz. The simulation result indicates that when over 1000 data are averaged, the estimation error after calibration is close to -100 dB, which is equivalent to a resolution of about 100 fF.

5.4 Experimental Results

The single-ended two-phase circuit was fabricated in the Orbit 1.2 μm double-metal double-poly process. Figure 5.16 shows the microphotograph of the prototype chip. An extra opamp (Opampt) was also included on the chip for test purpose. The die size is 2 mm x 2 mm. The tested capacitors C_1 and C_2 are off-chip. The test setup is shown in

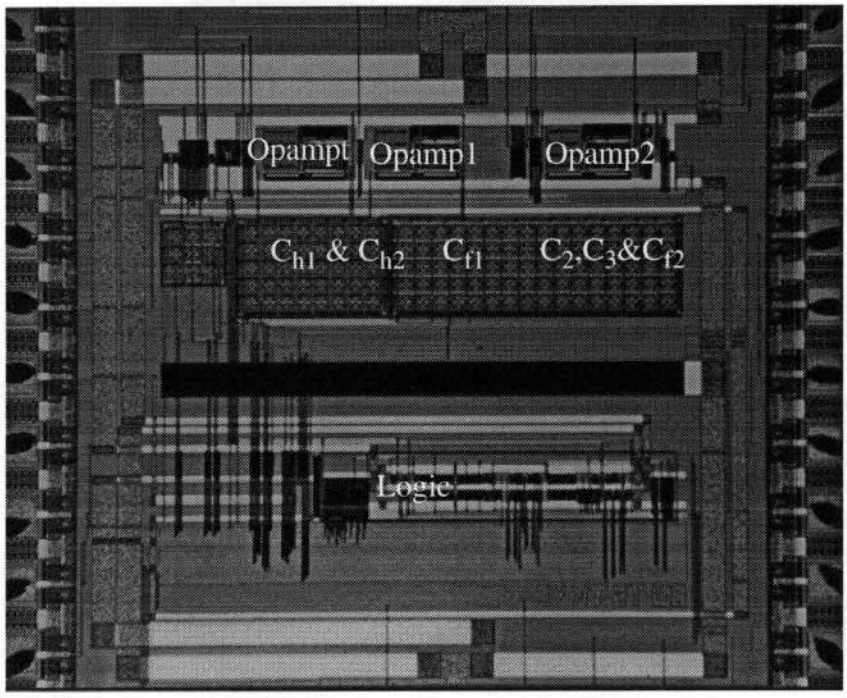


Figure 5.16:Die photograph of the single-ended implementation.

Figure 5.17. The blocks inside the dotted line are on the test board. It should be mentioned that since the desired resolution of capacitance is very high, the PCB board was designed so that the noise from the circuit board is minimized. All the critical signal paths have bypass capacitors connected to a ground plane to reduce noise coupling from the power supply. In addition, the analog and the digital blocks have separate power supplies.

In the testing, C_1 and C_2 were mica capacitors with small temperature coefficient. They were first measured off the board with a HP LCR meter, and C_1 was found around 11 pF and $C_2 \approx 10$ pF. The clock was set to 500 kHz. The output data y were read into the Next workstation [55] and processed in Matlab.

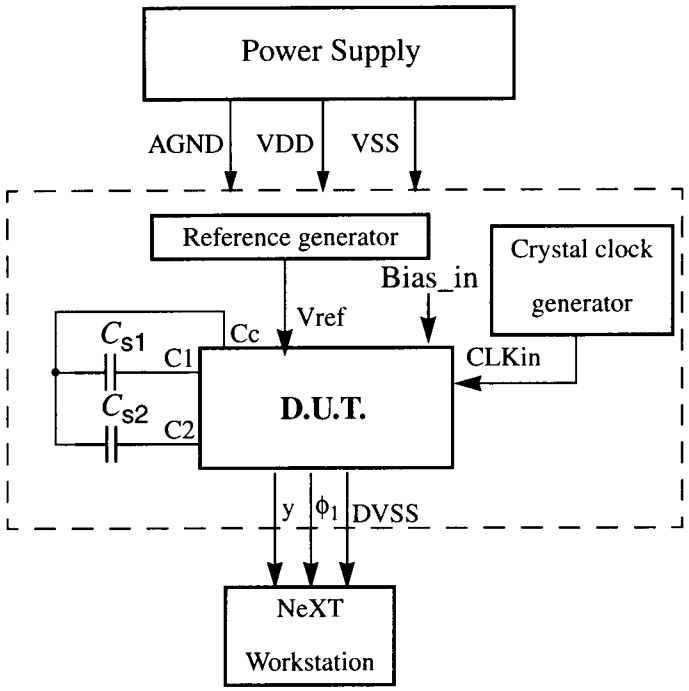


Figure 5.17:Test setup for the single-ended chip.

In the simulations, the accuracy of readout was obtained by comparing the simulation results with the real value of a capacitor or capacitor ratio. However, in the testing, the real value of the measurand is unknown, and it is difficult to obtain the absolute value. A more meaningful term to characterize the accuracy is "repeatability".

The *repeatability* is measured by the agreement between successive results obtained with the same method, under the same conditions and in a short time interval [6]. Quantitatively the repeatability is the minimum value that exceeds, with a specified probability, the absolute value of the difference between two successive readings obtained under the specified conditions. If not stated, it is assumed that the probability level is 95%. The repeatability can be characterized by measuring the standard deviation σ of many

repeated measurements. It is known that the probability that the absolute value of the difference between two successive readings is within 3σ is more than 99%.

The standard deviation of the capacitance ratio $(C_1 - C_2)/(C_1 + C_2)$ from a typical set of 40 measurements was calculated. Figure 5.18 shows the measured standard deviation of C_2 for different lengths of data averaged. It can be seen that when 4096 data are averaged, the standard deviation is close to $\sigma = 0.09$ fF. The equivalent resolution is $3\sigma = 0.27$ fF.

It should be noted that the term "repeatability" should not be mixed with "reproducibility". The *reproducibility* is also related to the degree of coincidence between

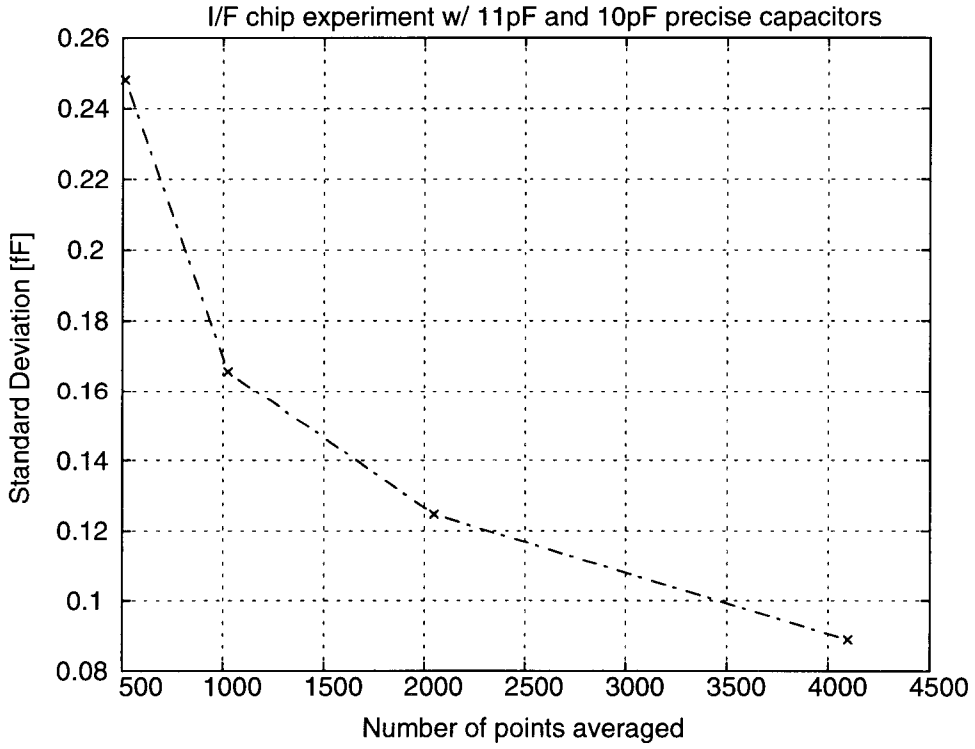


Figure 5.18:Standard deviation from 40 measurements for the single-ended test chip.

successive readings when the same quantity is measured with a given method, but in this case for a long-term set of measurements, or with measurements carried out by different people or performed with different instruments, or in different laboratories. For example, the standard deviation when 4096 data are averaged can vary from time to time. The measurements have been repeated many times during different days and the standard deviation when 4096 data were averaged varied between 0.06 fF to 0.15 fF.

Figure 5.19 shows the output spectrum of the single-ended test chip with 65,536 FFT points. The Hanning window was used before the FFT was performed. The signal is at DC and equal to $(C_1 - C_2)/(C_1 + C_2)$, which is approximately -26.3 dB. The noise-

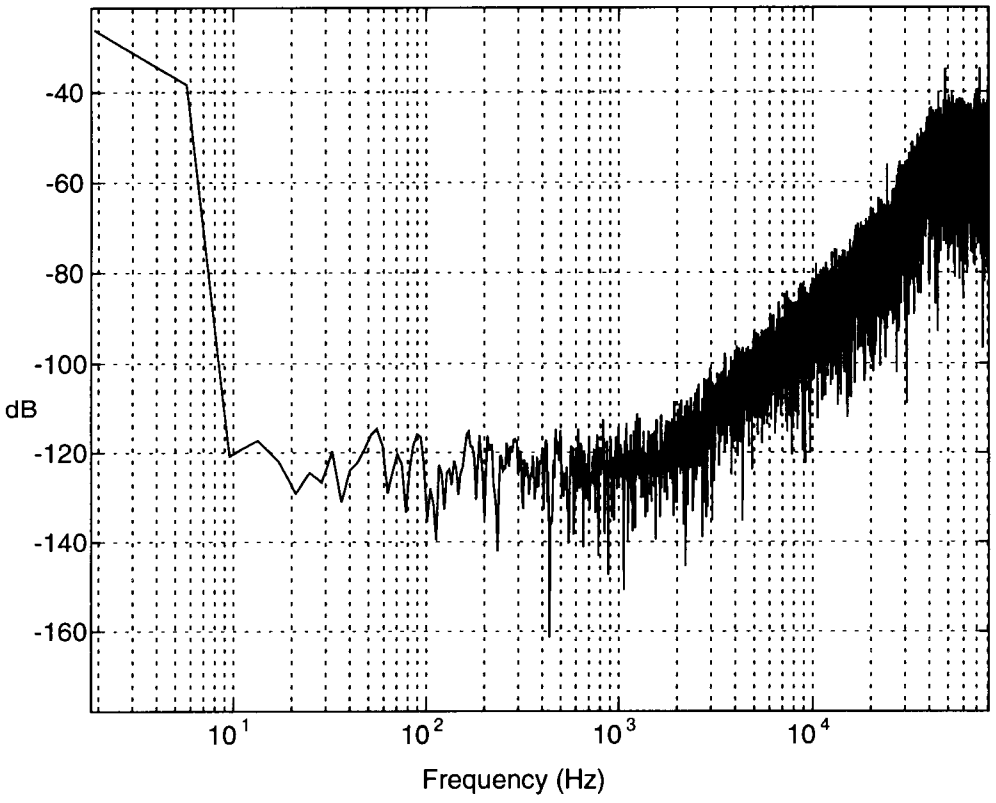


Figure 5.19:Output spectrum of the single-ended test chip.

shaping effect can be observed. The $1/f$ noise is not obvious in the output since CDS was used.

The measurement results were worse than the those obtained by simulations. One possible reason is that in simulations the noise coupled from the substrate was not considered. Another reason may due to the noise coupling from the outside. Due to the limitation of facilities in the lab, the data were acquired to the Next workstation, which is very noisy and was directly connected to the test board. Since single-ended circuits have poor noise rejection, the extra noise coupled to the test chip may limit the achievable resolution.

5.5 Conclusions

The use of CDS to reduce the sensitivity of readout accuracy on the non-idealities of the opamp was discussed. Various calibration schemes for clock feedthrough and charge injection cancellation have been presented. The implementation of single-ended circuits for capacitor ratio testing and for sensor readout were described. The test results for the integrated realization of a two-phase circuit verified the simulation results.

Chapter 6. A Fully-Differential Implementation

In Chapter 3, several structures for capacitor ratio testing and sensor readout have been introduced, and in Chapter 5 a single-ended implementation for fixed capacitor ratio testing and differential sensor readout was presented. In this chapter, a fully-differential implementation is described. New common-mode compensation schemes are introduced and implemented to cancel the large common-mode signal from the input capacitors. The area of the test chip is 2 mm by 2 mm, and the measured standard deviation of the capacitors is less than 20 aF for a clock frequency of 1.5 MHz.

6.1 Design Motivation and Goal

As shown in previous chapters, single-ended circuitry is sensitive to clock feedthrough effect, and calibration is usually needed to minimize the error generated by clock feedthrough and charge injection. However, calibration does not cancel random noise in the circuit which may dominate in high-accuracy applications. Another solution to minimize the clock-feedthrough effect is to realize the circuit in a fully-differential form. Because of its symmetric structure, the error due to charge injection and clock feedthrough only causes a common-mode charge error and is effectively rejected. For the same reason, the effects of other noise sources which appear as common-mode signal to the circuit are also greatly reduced. Hence, the fully-differential structure has larger rejection of noise coupled from power supply and the substrate, which is usually the limiting factor on the performance for single-ended circuits. In addition to noise reduction, the signal amplitude is also doubled in a fully-differential architecture, which further increases the dynamic range of the circuit. Hence, fully-differential realizations of the sensor interface circuits discussed in Chapter 3 are needed in order to obtain very high accuracy.

In many industrial applications, floating capacitive sensors are widely used. In automation applications, the requirement for the accuracy of capacitive sensor and its interface is very high. Usually a differential capacitive sensor is needed to get better sensitivity. The goal of this design is to realize a sensor interface circuit in a fully-differential structure. The structure and characteristics of the capacitive sensor is the same as shown in Chapter 5. The requirement for the resolution is better than 0.1 fF for 10 pF capacitors, which was specified in an industrial application.

6.2 Common-Mode Feedback in Fully-Differential Circuits

As discussed in Section 6.1 the fully-differential structure has many advantages over the single-ended one. However, it has some drawbacks too. One drawback is the increased circuit complexity caused by the added symmetric circuitry, and another drawback is that a common-mode feedback circuit is usually needed for a fully-differential circuit.

Figure 6.1 shows a typical non-inverting fully-differential SC integrator. For simplicity, all capacitors are assumed to have the same value *C*. Assuming that the input signal contains a small common-mode voltage and there is no compensation for the common-mode signal, this circuit performs as an integrator for both the differential signal

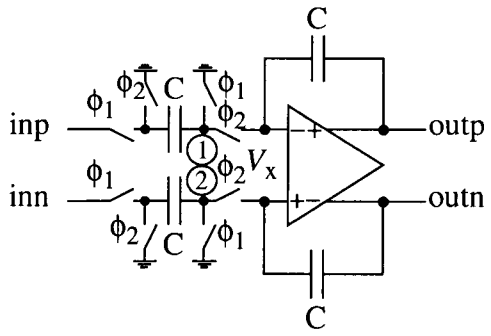


Figure 6.1: A fully-differential SC integrator.

V(inp) - V(inn) and the common-mode signal (V(inp) + V(inn))/2. When the integrator is used in a feedback application, the applied feedback usually determines the differential signal voltages, but does not affect the common-mode voltages. If the input common-mode signal is non-zero and constant, the opamp output common-mode voltage is the integrated value of the DC input common-mode voltage, and hence the opamp outputs will go to rails and saturate. Therefore, the desired integration function for the differential signal no longer exists. This is not a problem for the single-ended circuit, where there is no common-mode signal and the feedback takes care of the stability of the integrator. For the differential circuit, even when there is no common-mode signal from the input, due to non-ideal effects such as charge injection of the switches and leakage current, common-mode voltage will still be built up at the inputs and outputs of the opamp and will eventually saturate the opamp outputs. Since the integrator is a major building block in delta-sigma modulators and the sensor interface circuits, a common-mode feedback circuit is usually required to maintain a stable integration function for the differential signal.

There are various circuit topologies for common-mode compensation. They can be divided into the following three categories: output common-mode feedback, input common-mode feedback, and feedback for both input and output common-mode voltages. They are discussed in Sections 6.2.1 to 6.2.3.

6.2.1. Output Common-Mode Feedback Compensation

The purpose of the output common-mode feedback circuit is to sense the common-mode voltage at the opamp output and use it to stabilize the opamp output common-mode voltage itself. An example is illustrated in Figure 6.2. There are two typical approaches to design the common-mode feedback (CMFB) block: continuous-time approach [56] and SC approach [57]. In steady state, the CMFB circuit forces the output common-mode voltage to be close to the applied reference voltage V_{cmr} due to the negative feedback. Hence, the

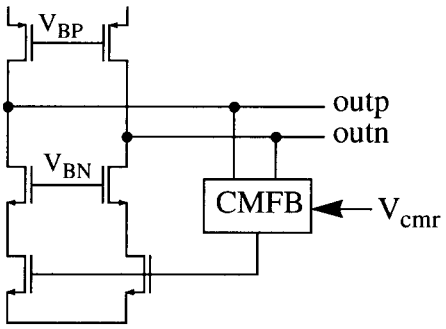


Figure 6.2: An example of output common-mode feedback.

differential output swing is maximized and the next stage receives only a very small common-mode voltage.

It is interesting to examine the input common-mode voltage of the opamp in Figure 6.1 when the output common-mode voltage is fixed. In Figure 6.1, assuming that the input has a common-mode voltage *Vcmi*, that the common-mode voltage at the opamp input is *Vx*, and that under steady-state conditions the output common-mode voltage *Vcmo* is 0, the relationship between *Vx* and *Vcmi* can be derived as the following

$$(Vcmi - Vx) = Vx(1 - z^{-1}) . \qquad (6.1)$$

When the input common-mode voltage *Vcmi* is fixed, in steady state *Vx* is almost fixed and hence $Vx(1 - z^{-1}) \approx 0$. It can then be easily observed from Eq. (6.1) that $Vx \approx Vcmi$. Hence, although the output common-mode voltage is fixed, the input of the opamp still tracks the common-mode voltage of the input signal. Also as shown in Eq. (6.1), this effect does not depend on the ratio of the feedback capacitor and the sampling capacitor. Therefore, this approach is only suitable for applications where the input common-mode voltage is relatively small so it does not exceed the input common-mode range of the opamp. However, in capacitive sensor interfaces or capacitor mismatch measurements, the signal of interest is usually the capacitance difference of two capacitors and it may be

much smaller than the nominal value of the capacitors. Thus, using the sensor capacitors as the sampling capacitors, as proposed in Chapter 3, will force the opamp out of its input common-mode range and into saturation.

One possible solution for this problem is depicted in Figure 6.3. We assume that the opamp has output common-mode feedback so the outputs contain only differential signals. In steady state, when ϕ_2 is high, the left plates of input capacitors are connected together and their voltage is equal to the common-mode input voltage. Therefore, the opamp input common-mode voltage Vx is 0, and the input common-mode voltage is moved from the opamp input to the common node of the input capacitors. This solution has a major drawback: it is sensitive to parasitic capacitance mismatch at nodes $v1$ and $v2$. The capacitance mismatch causes the change of some common-mode signal into differential signal and hence generates error in the differential outputs. Therefore, the parasitic capacitances at nodes $v1$ and $v2$ need to match accurately. When the input capacitors are off-chip sensors, they are usually connected by long cables, which make it very difficult to match the parasitic capacitances. Also due to change of environment, the parasitic capacitances can change. Therefore, for high-accuracy interface circuits, this scheme may not be a practical solution. Furthermore, this method can't be used for differential

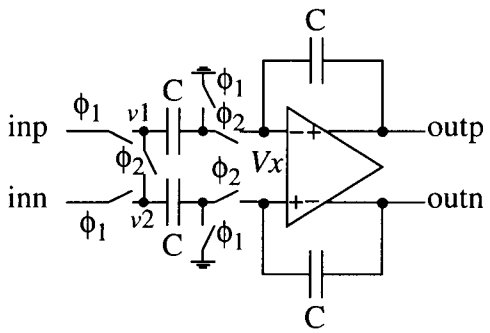


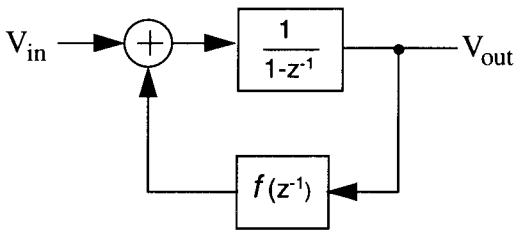
Figure 6.3: A simple input common-mode cancellation scheme.

capacitive sensor interfaces, where the two capacitors have only 3 terminals with one common plate.

Therefore, other common-mode compensation techniques should be considered. Since the input signal contains a large common-mode component, input common-mode compensation may be useful.

6.2.2. Input Common-Mode Feedback Compensation

Figure 6.4 shows the block diagram of a scheme to compensate the input common-mode signal. For simplicity, only the common-mode signal path is illustrated so V_{in} refers to the input common-mode signal and V_{out} is the output common-mode signal. The transfer function in the signal path is just a delay-free integration function, the same as the one used in sensor interface circuits. The feedback path is represented by a function $f(z^{-1})$. The idea of this common-mode compensation scheme is to sense the output common-mode voltage and then use it to compensate the input common-mode voltage. Under steady-state conditions, the common-mode signal from the input is equal to the negative of the signal from the feedback path. Now the integrator in Figure 6.1 has both common-mode and differential feedback from the output.



$$V_{out} = \frac{1}{1-z^{-1}}\left[V_{in} + f(z^{-1})V_{out}\right]$$

$$V_{out} = \frac{V_{in}}{1-z^{-1}-f(z^{-1})}$$

Figure 6.4: Block diagram of a new input common-mode compensation scheme.

The criteria for choosing a transfer function $f(z^{-1})$ are the following: the chosen function must provide negative feedback for the common-mode signal, it should not affect the operation for differential signal, and it must be stable. A simple choice is $f(z^{-1}) = -Fz^{-1}$. Then the closed-loop gain for the common-mode feedback path is

$$L(z) = \frac{V_{out}}{V_{in}} = \frac{z}{z + (F - 1)} . \tag{6.2}$$

In order to make this feedback stable, the pole of the function shown in Eq. (6.2) should be inside the unit circle [45][49]. Hence the value of F should be between 0 and 2.

Since this scheme uses the output common-mode voltage to compensate the input common-mode voltage, the regular output common-mode feedback is not needed. The function shown in Eq. (6.2) can be realized by switched-capacitor circuits, as shown in Figure 6.5. The circuit consists of a SC amplifier with offset and gain compensations [46]. The inputs to the amplifier are from the integrator shown in Figure 6.1 and the output nodes 1 and 2 are also connected to the nodes 1 and 2 in Figure 6.1, respectively. The output of the amplifier V_{cm} can be derived as

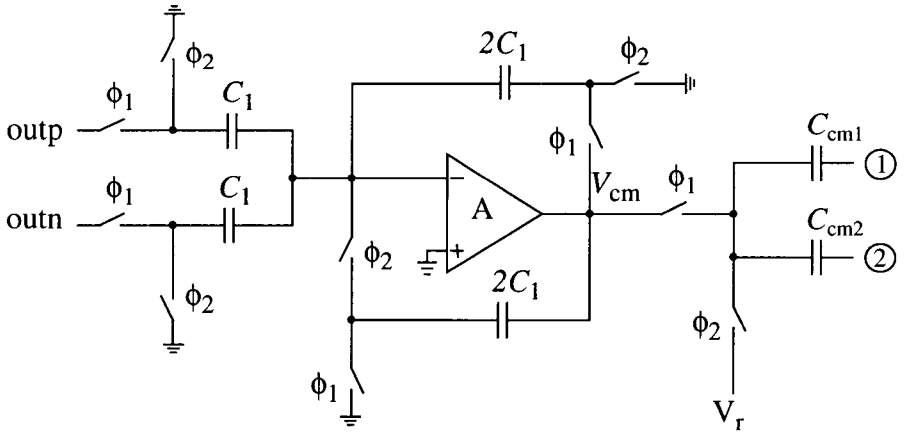


Figure 6.5: Switched-capacitor realizations of the feedback function.

$$V_{cm}(z) = \frac{Voutp(z) + Voutn(z)}{2} \cdot z^{-1} . \tag{6.3}$$

Hence, the output voltage of the amplifier is equal to the delayed output common-mode voltage of the integrator. When ϕ_1 is high, the capacitors C_{cm1} and C_{cm2} are charged to V_{cm}. When ϕ_2 is high, V_r is connected to both capacitors C_{cm1} and C_{cm2} ($C_{cm1} = C_{cm2} = C_{cm}$), and charges equal to $C_{cm}(V_r - V_{cm})$ are transferred back to the integrator. Therefore, $f(z^{-1}) = -\frac{C_{cm}}{C} z^{-1}$ is realized, where C is the feedback capacitor in Figure 6.3. Assuming the feedback loop is stable so that the common-mode signal from the input signal becomes equal to the common-mode signal from the feedback,

$$C_{cm}(V_r(z) - V_{cm}(z)) = V_{cmi}(z)C \tag{6.4}$$

results, where V_{cmi} is the input common-mode voltage, V_r is a reference voltage, and V_{cm} is the output common-mode voltage. If $C_{cm} = C$ and $V_r = V_{cmi}$, then $V_{cm} = 0$, so the net common-mode input signal to the integrator is zero. This scheme is very useful in the capacitor readout circuits discussed earlier, where the input is a reference voltage V_r, and hence the same reference can be used as V_r to cancel the input common-mode signal.

In Figure 6.4, $f(z^{-1}) = -\frac{k_1 z^{-1}}{1 - k_2 z^{-1}}$ ($k_2 \geq 0$) can also be used. The closed-loop gain is then

$$L(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{z(z - k_2)}{z^2 + (k_1 - k_2 - 1)z + k_2} . \tag{6.5}$$

Again, the poles of the loop transfer function should be inside the unit circle so that the feedback loop is stable. Therefore, the choice of k_1 and k_2 is limited by the following conditions: $0 \leq k_2 < 1$ and $-2\sqrt{k_2} < k_1 - k_2 - 1 < 2\sqrt{k_2}$. The range of k_1 can be derived to be

$$k_2 - 2\sqrt{k_2} + 1 < k_1 < k_2 + 2\sqrt{k_2} + 1 . \tag{6.6}$$

$f(z^{-1}) = \dfrac{k_1 z^{-1}}{1 - k_2 z^{-1}}$ can be realized by a lossy SC integrator, as shown in Figure 6.6. If only the common-mode signal is considered, the common-mode transfer function of the integrator can be derived as

$$f(z) = -\frac{2C_1/(C_2 + C_3)}{1 - C_2/(C_2 + C_3) \cdot z^{-1}} . \tag{6.7}$$

Therefore, $k_1 = 2C_1/(C_2 + C_3)$ and $k_2 = C_2/(C_2 + C_3)$. If $C_1 = C$ and $C_2 = C_3 = C$, then $k_1 = 1$ and $k_2 = 0.5$. Again, the output of the integrator is fed back to the integrator in Figure 6.1 through capacitors C_{cm1} and C_{cm2}, since the nodes 1 and 2 are connected to the nodes 1 and 2 in Figure 6.1, respectively.

6.2.3. Input and Output Common-Mode Compensation

This new compensation scheme combines the output common-mode feedback discussed in Section 6.2.1 with a new input common-mode compensation technique. For a fully-differential circuit such as an amplifier and an integrator, the output common-mode feedback stabilizes the output common-mode voltage, and the input common-mode

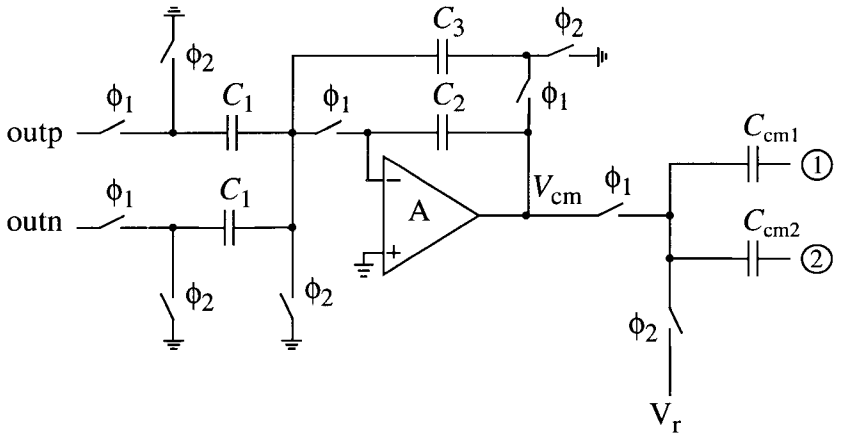


Figure 6.6: A new input common-mode feedback circuit using a lossy SC integrator.

compensation allows the input common-mode voltage of the opamp to be independent of the common-mode voltage of the input signal.

Figure 6.7(a) shows the schematic of the new input common-mode compensation scheme. The purpose is to automatically sense the amount of input common-mode charge and feed it back to the same path as the input signal, but with a negative sign. Hence, the total input common-mode charge entering the integrator is zero. In Figure 6.7(a), the input nodes 1 and 2 are connected to an integrator similar to the one in Figure 6.1 except that the two grounding switches controlled by ϕ_1 are eliminated, as illustrated in Figure 6.7(b). When ϕ_1 is high, nodes 1 and 2 are shorted to the virtual ground node V_g of the circuit in

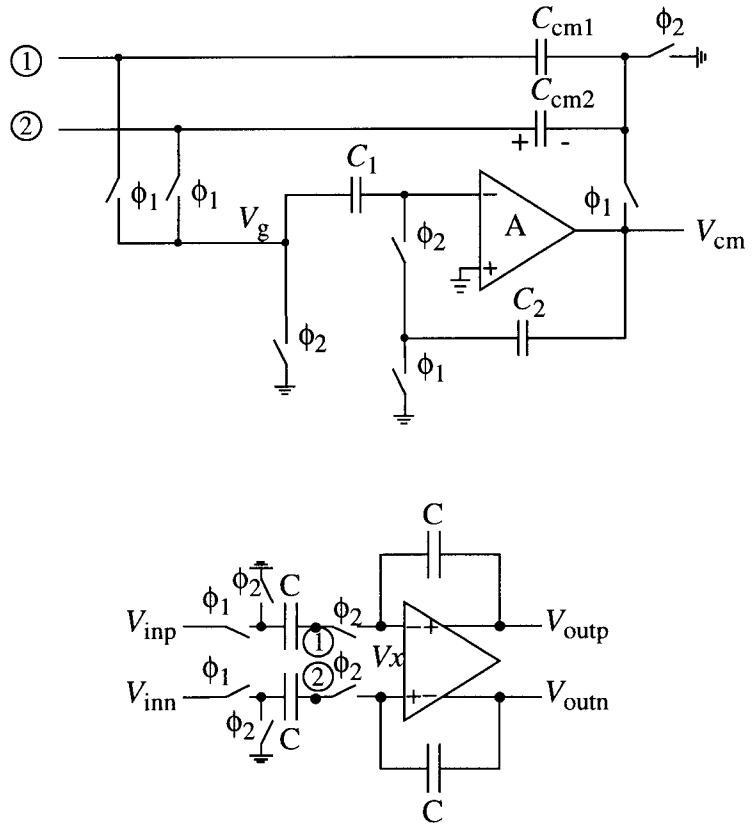


Figure 6.7: A new compensation scheme to cancel the input common-mode signal: (a) circuit diagram; (b) modified SC integrator.

Figure 6.7(a), and the input capacitors C in Figure 6.7(b) are charged to V_{inp} and V_{inn}, respectively. The charges stored in these two capacitors contain both common-mode and differential signals. At the same time, the same amount of charges are transferred to both C_{cm1} and C_{cm2} and the opamp output voltage V_{cm} becomes

$$V_{cm} = -(V_{inp} + V_{inn}) \cdot \frac{C}{C_{cm1} + C_{cm2}} = -V_{cmi} \cdot \frac{2C}{C_{cm1} + C_{cm2}}, \qquad (6.8)$$

where V_{cmi} is the input common-mode voltage. Assuming that C_{cm1} and C_{cm2} are equal, it can be seen from Eq. (6.8) that the charge stored in C_{cm1} or C_{cm2} ($-V_{cm}C_{cm1}$) is equal to the common-mode charge $V_{cmi}C$ stored in the sampling capacitors C in Figure 6.7(b).

When ϕ_2 is high, the sampling capacitors C, C_{cm1} and C_{cm2} are discharged between ground and the virtual ground. The total common-mode charge entering the integrator is then $-V_{cm}C_{cm1} - V_{cmi}C = V_{cmi}C - V_{cmi}C = 0$. Hence, the common-mode signal is cancelled by using the circuit in Figure 6.7(a). From Eq. (6.8), it can be seen that V_{cm} is not a function of the differential signal, and therefore the compensation does not affect the differential operation. In the same clock phase, capacitor C_1 stores the error voltage at the opamp input so that node V_g can serve as the virtual ground when ϕ_1 is high. C_2 provides feedback and holds V_{cm} for the opamp when ϕ_2 is high.

6.3 Design and Simulation of the Differential Structures

6.3.1. The Fully-Differential Structure

The same type of modulator used in the single-ended realization can also be used for the differential structure. For illustration, the diagram of the modulator is redrawn in Figure 6.8. It is again based on the modulator shown in Figure 3.14. The schematic of the fully-differential realization is shown in Figure 6.9. The first stage is based on the single-ended structure shown in Figure 3.6 and it contains three blocks: the integrator, the DAC

feedback branch and the common-mode feedback circuit. The differential input signal is generated by the capacitance difference of two tested capacitors, C_{s1} and C_{s2}. The integrator realizes the function $z^{-1}/(1-z^{-1})$. The effect of opamp finite gain and offset is compensated by using CDS technique through C_{h1} and C_{h2} [58][59]. The DAC feedback is provided by C_{dac1}, C_{dac2}, some logic control and switches. C_{dac1} and C_{dac2} are equal, and C_{f1} was chosen to be four times as large as C_{dac1} to realize the 0.25 scaling factor.

The circuit shown in Figure 6.7(a) can be used as the CMFB block in Figure 6.9. Then, due to the charge balancing operation described in Chapter 3, the following relation holds

$$(C_{s1} - C_{s2})(V_{ref} + V_{x2} - V_{x1})N - 2nC_{dac}V_{ref} + 2(N-n)C_{dac}V_{ref} \approx 0, \quad (6.9)$$

where N is the total number of the binary outputs y, n is total number of the binary outputs when y is high, $C_{dac} = C_{dac1} = C_{dac2}$, and V_{x1} and V_{x2} are the common-mode voltages at nodes 1 and 2 when ϕ_1 is high and when ϕ_2 is high, respectively. Here it is assumed that the differential error voltages at nodes 1 and 2 are cancelled by CDS. Now, from Eq. (6.9), the ratio between the tested capacitors and the reference capacitor can be derived as

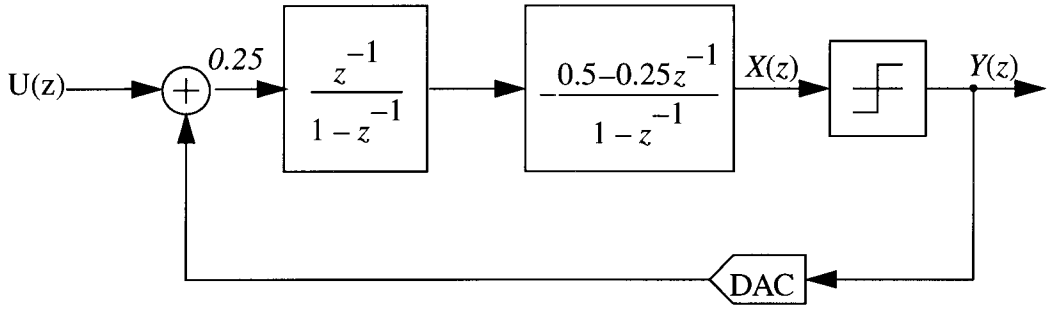


Figure 6.8: The diagram of the second-order modulator used in the fully-differential realization.

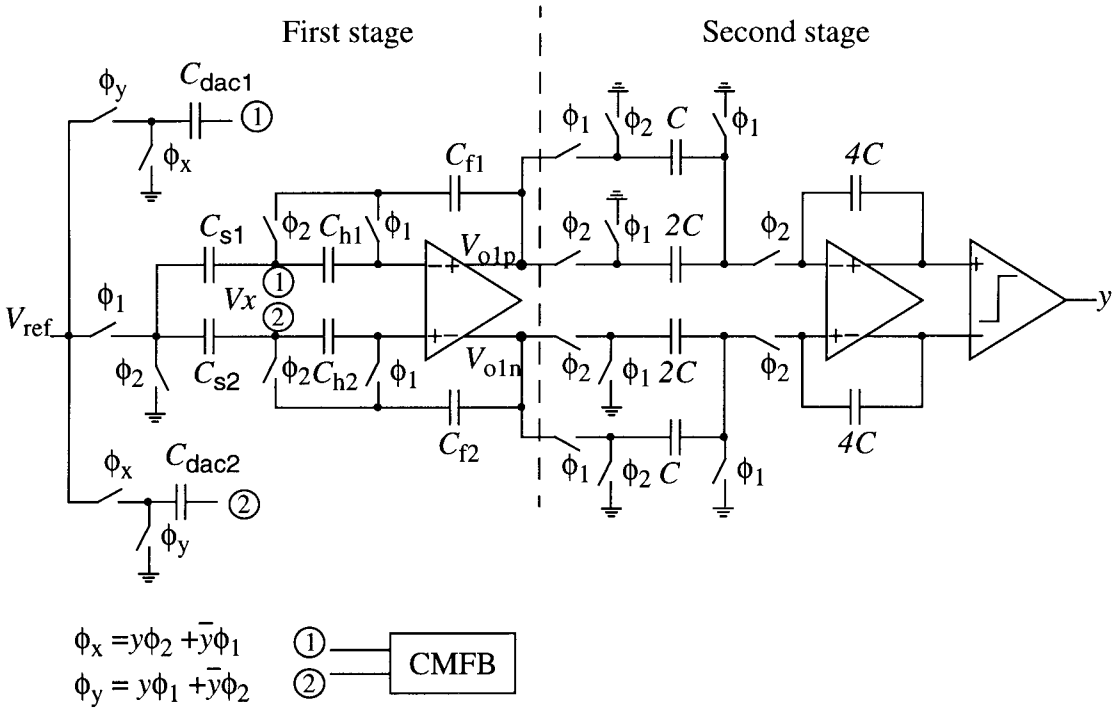


Figure 6.9: The fully-differential circuit for capacitor ratio testing and sensor readout.

$$\frac{C_{s1} - C_{s2}}{2C_{dac}} \approx \frac{V_{ref}}{V_{ref} + V_{x2} - V_{x1}}(2y_{ave} - 1). \tag{6.10}$$

Usually, V_{x1} and V_{x2} are not equal but much smaller V_{ref} since the common-mode from the input is compensated. However, for high-accuracy measurement, V_{x1} and V_{x2} can cause gain errors and limit the accuracy.

6.3.2. The Pseudo-Differential Structure

As shown in Eq. (6.10), for the fully-differential circuit in Figure 6.9, the readout of the capacitor ratio is affected by the common-mode voltage at the virtual ground. An effective solution for this problem is to use the pseudo-differential structure, as shown in Figure 6.10. The difference between this pseudo-differential structure and the fully-

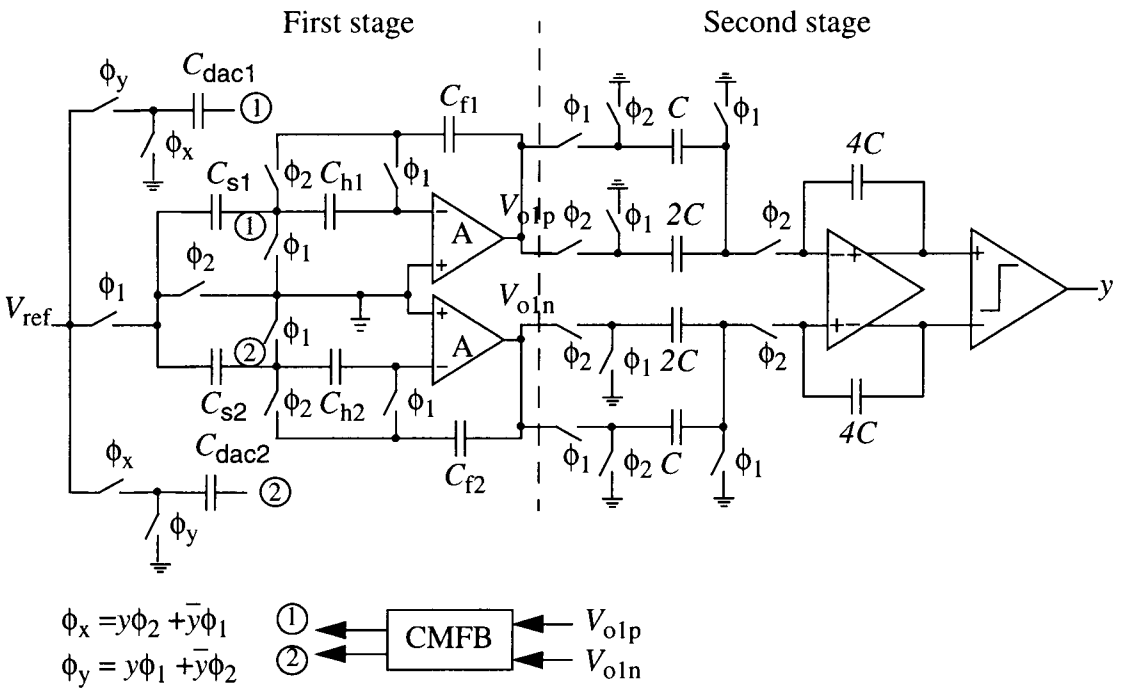


Figure 6.10:The pseudo-differential structure.

differential structure in Figure 6.9 is in the first stage integrator. Instead of using a fully-differential opamp, two single-ended opamps are used and connected in a symmetric way. Their positive inputs are connected to analog ground. The high gain of the opamps forces the negative input terminals to be virtual grounds, assuming the input offset voltage is zero. Again, the CDS technique is utilized with C_{h1} and C_{h2} storing the error voltages due to the finite gain and input offset of the opamps. Hence, the voltages at node 1 and node 2 are very close to ground and the problem with the input common-mode voltage is no longer present.

Now, the input common-mode signal can easily make the opamp outputs go to the rail, if it is not properly compensated. The input common-mode signal can be compensated using the circuits in Figure 6.5 or Figure 6.6. A regular SC or continuous-time output common-mode feedback circuit can be used for the fully-differential opamp in the second stage.

6.3.3. Simulation of the Differential Circuits

To verify the fully-differential and pseudo-differential structures with different common-mode compensation schemes, the circuits shown in Figure 6.9 and Figure 6.10 have been simulated in Hspice. In the simulations, C_{s1} =10.5 pF and C_{s2} = 9.5 pF were assumed, the power supply was 5 V, and V_{ref} was 5 V as well. Hence, the common-mode capacitance is 10 pF, which is ten times as large as the differential one (1 pF). In Figure 6.7(a), to prevent the large common-mode signal to saturate the opamp output, C_{cm1} and C_{cm2} were set to be 15 pF each so that the opamp output is still in the linear range. In Figure 6.5 and Figure 6.6, V_r was connected to V_{ref}, and C_{cm1} and C_{cm2} were set to 10 pF each.

The simulated input common-mode voltage for first-stage integrator in Figure 6.9 is shown in Figure 6.11. As can be seen from Figure 6.11, the input common-mode

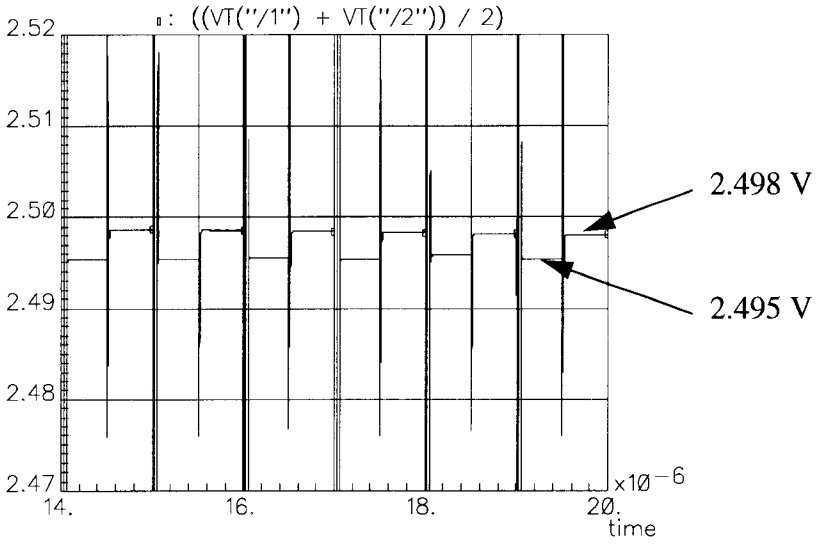


Figure 6.11:Common-mode voltage at nodes 1 and 2 in the first-stage integrator of the fully-differential circuit in Figure 6.9.

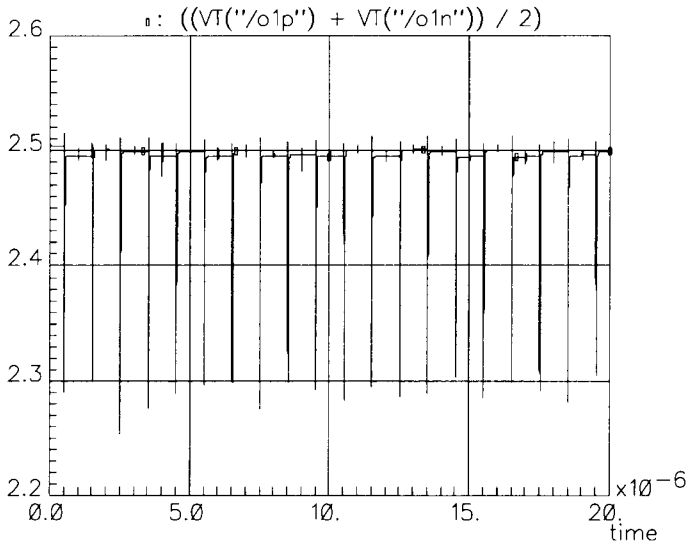
voltages at nodes 1 and 2 are very close to the analog ground, which is 2.5 V. However, as discussed earlier, the variation of the input common-mode voltage at node 1 and 2 in Figure 6.7 can cause gain error in the capacitor ratio readout. Although the variation may be in the mV range, it still limits the accuracy to around 60 dB, as will be shown later.

Figure 6.12 (a) and (b) illustrate the output common-mode voltages of the circuit of Figure 6.10 using the amplifier and lossy integrator in the CMFB circuit. In both cases, the output common-mode voltages were greatly suppressed and the variation of output common-mode voltage is around a few mVs. As can be observed from Figure 6.12, the output common-mode voltages are close to 2.5 V. This is because in Figure 6.5 and Figure 6.6, C_{cm1} and C_{cm2} were set to be 10 pF each, the same as the common-mode value of the tested capacitors. In reality, the tested capacitor may be off-chip and C_{cm1} and C_{cm2} could be on-chip capacitors, and it is very difficult to match them. Hence, it is necessary to check how the output common-mode voltage changes when C_{cm1} and C_{cm2} are not exactly 10 pF. The output common-mode voltage should be small so that the opamp outputs can have a large dynamic range. The simulated waveforms are shown in Figure 6.13. It can be seen that the CMFB circuit using the lossy integrator has better control over the output common-mode voltage. This can be explained from the following equation

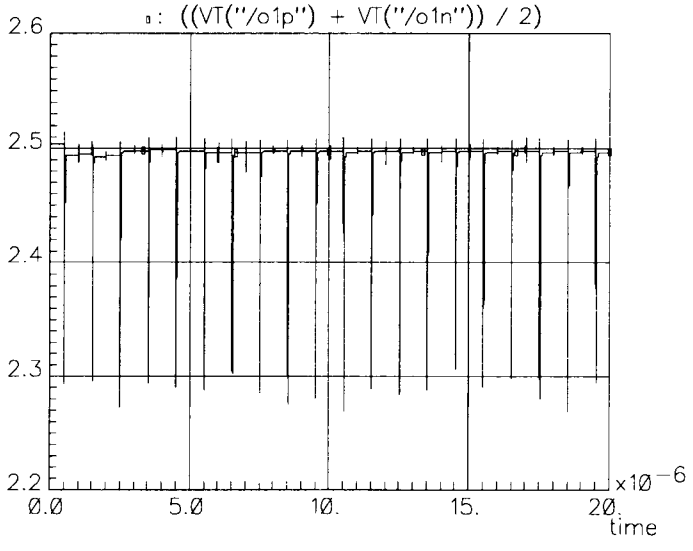
$$V_{cmo} = \frac{V_r \cdot (10 - C_{cm})}{kC_{cm}}, \tag{6.11}$$

where V_{cmo} is the output common-mode voltage of the first stage integrator in Figure 6.10, k is the DC gain of the lossy integrator or the amplifier, and $C_{cm} = C_{cm1} = C_{cm2}$ is assumed. Eq. (6.11) indicates that when C_{cm} is not equal to 10 pF, V_{cmo} is inversely proportional to k. To reduce the variation of V_{cmo} when C_{cm} is not equal to 10 pF, k needs to be as large as possible. However, the stability requirement limits the range of k that can be selected. In Section 6.2.2, it has been shown that the lossy integrator allows larger range of k so that the variation of V_{cmo} can be smaller.

The capacitor ratio can also be derived from the binary output data in the simulations. Table 6.1 lists some simulation results for the fully-differential and pseudo-



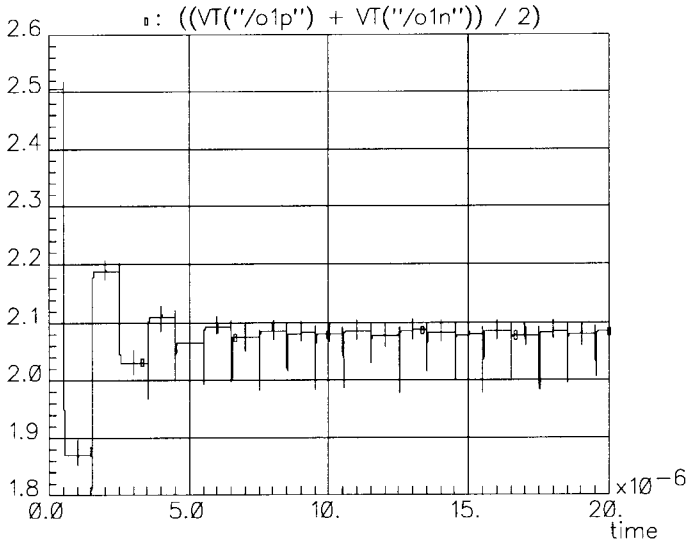
(a)



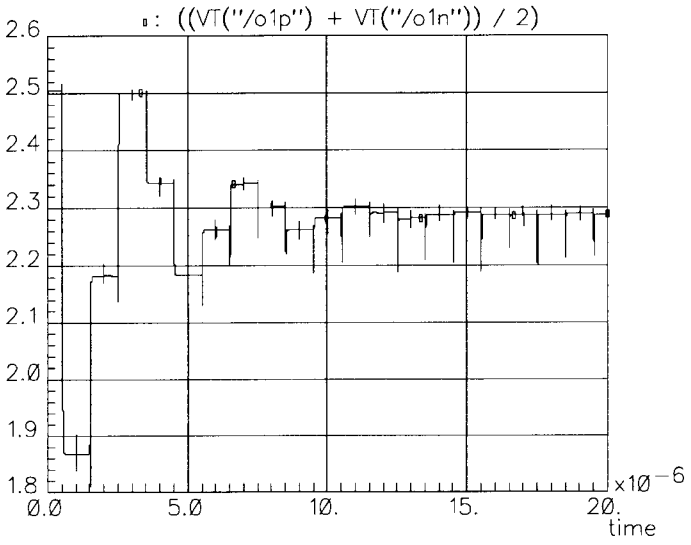
(b)

Figure 6.12:Output common-mode voltages in the first-stage integrator of the pseudo-differential circuit in Figure 6.10: (a) CMFB using an amplifier; (b) CMFB using a lossy integrator.

differential circuits and for different C_{s1} and C_{s2}. The effect of the gain factor can be seen from the simulation results for the fully-differential circuit in Figure 6.9.



(a)



(b)

Figure 6.13:Output common-mode voltages in the first-stage integrator of the pseudo-differential circuit when $C_{cm1} = C_{cm2} = 12$ pF:
(a) CMFB using an SC amplifier;
(b) CMFB using a lossy integrator.

6.4 Circuit Implementation

The pseudo-differential circuit shown in Figure 6.10 was chosen in the IC implementation and it provided good results which met the design goal. The CMFB circuit with SC amplifier was used in the implementation because it can effectively stabilize the output common-mode voltage. The integrator version of CMFB was developed after the IC implementation.

6.4.1. Design of Operational Amplifiers

The opamp is perhaps the most important building block in the differential readout circuit. Any non-idealities such as finite gain, $1/f$ noise, input offset, thermal noise, as well as non-linear settling may cause serious deterioration of the readout accuracy. However, since correlated double sampling was used, the effect of $1/f$ noise, input offset and finite gain was greatly reduced and made minor noise contribution.

Figure 6.14 shows the schematic of the single-ended opamp used for the first-stage integrator in Figure 6.10. Basically, it has the same architecture as the one used in the single-ended implementation. Instead of using the simple Miller compensation, a transistor biased in the triode region was added in series with the Miller capacitor. This realizes a zero which can cancel the non-dominant pole [50][56]. The bias circuit generates the control

Table 6.1: Simulation results for the fully-differential and pseudo-differential circuits.

C_{s1}, C_{s2} (pF)	C_{s1} - C_{s2} (pF)	$(C_{s1} - C_{s2})_{simulated}$ (pF)	
		Fully-differential	Pseudo-differential
10.5, 9.5	1	1.006358	1.000027
9.5, 10.5	-1	-1.006358	-1.000024

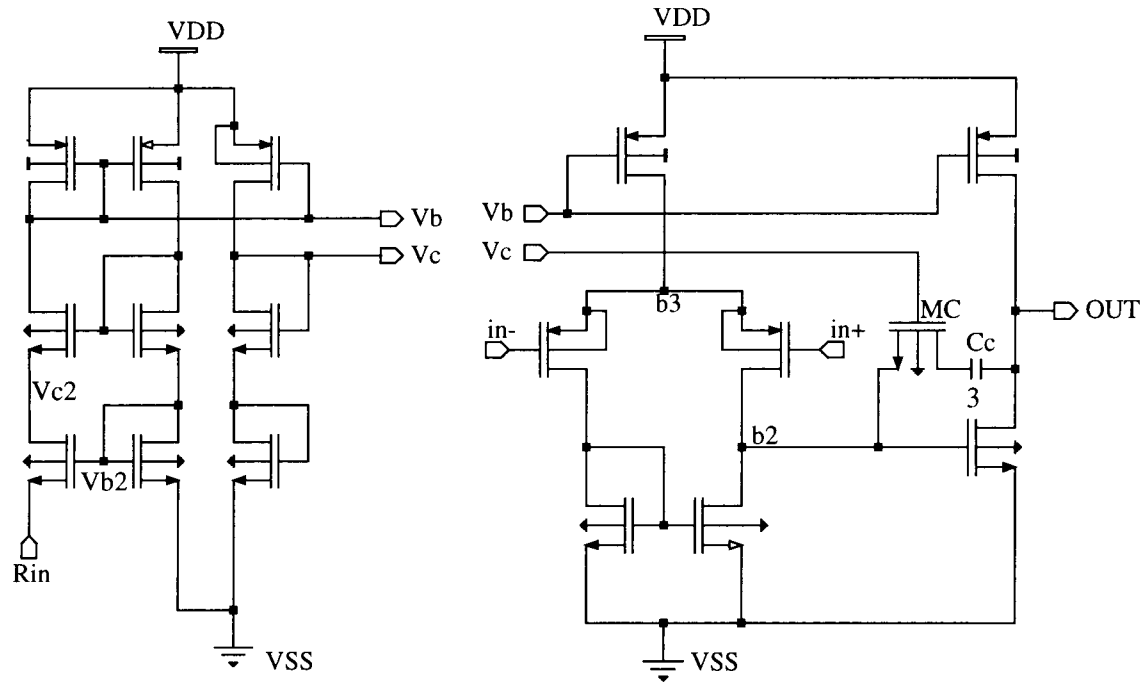


Figure 6.14:Two-stage opamp and the bias circuit.

voltage for the transistor used for compensation, as well as the bias voltage for the current source. The pin Rin is connected to an external resistor which to a first-order approximation makes the transistor transconductance independent of power-supply voltage as well as process and temperature variations [56].

The opamp was realized in a 1.2 μm CMOS process. Table 6.2 lists the simulated performance of the opamp obtained using an Hspice Level 28 model. The load capacitance

Table 6.2: Simulated performance of the single-ended opamp.

DC gain (dB)	Unit-Gain Bandwidth (MHz)	Phase Margin (degree)	Slew Rate (V/μs)	Input -Referred Noise (nV/$\sqrt{Hz}$)
75	25	75	20	20

was 20 pF. Simulations showed a 14-bit settling accuracy in 200 ns. This allows the opamp to operate at a clock frequency of over 1 MHz. Since the oversampling ratio is over 512, the contribution of the opamp thermal noise is very small.

The second-stage integrator uses a folded-cascode fully-differential opamp, as shown in Figure 6.15. The bias circuit is shown in Figure 6.16. It provides the voltages V_{p1}, V_{p2} and V_{n2} that supply the cascoded current sources in Figure 6.15. It also provides the reference voltage V_{cmr} for the SC common-mode feedback circuit, which is shown in Figure 6.17. The simulated performance of the opamp is summarized in Table 6.3.

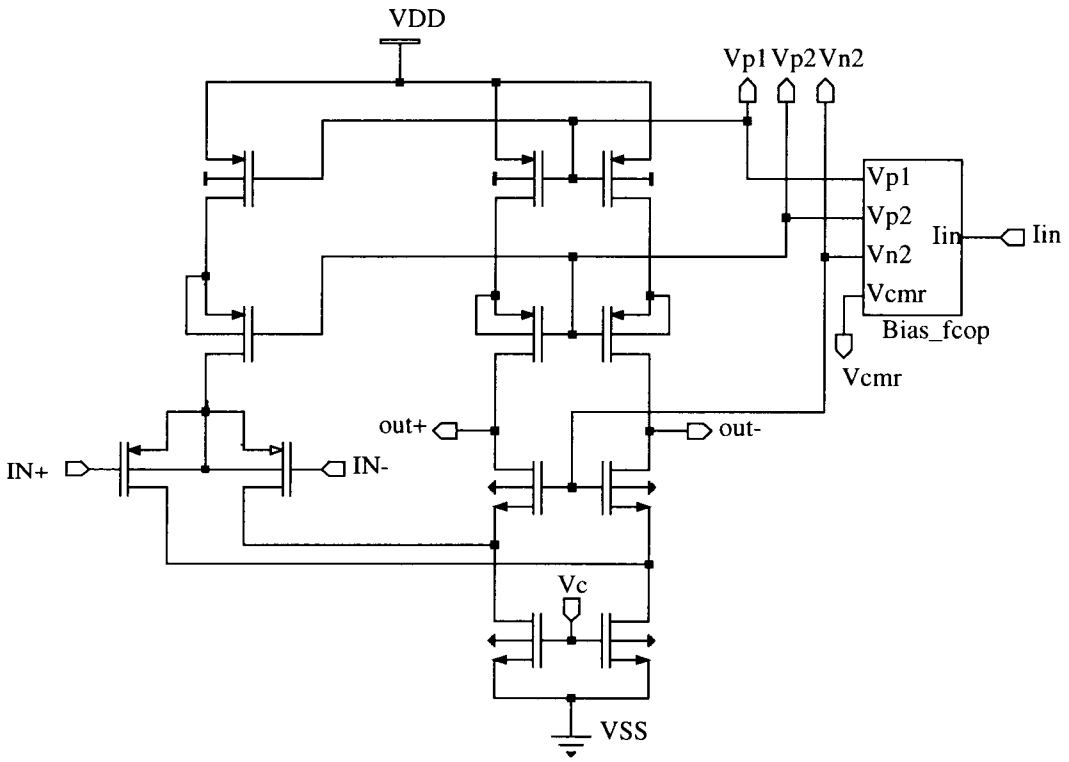


Figure 6.15:The differential opamp with the bias circuit.

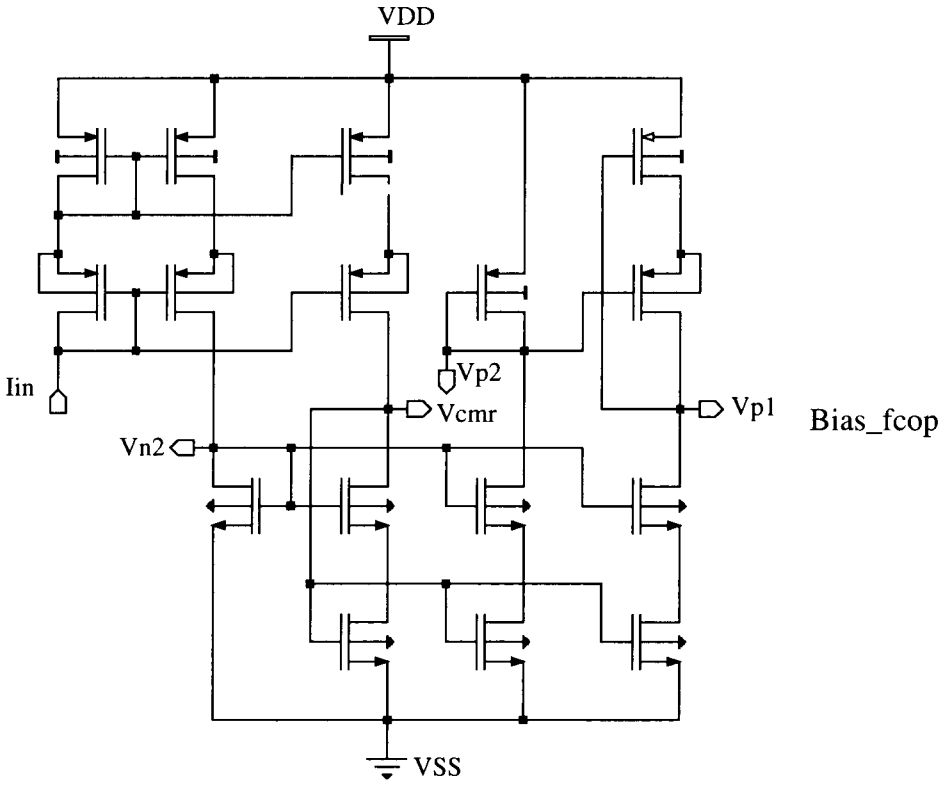


Figure 6.16:The bias circuit for the differential opamp.

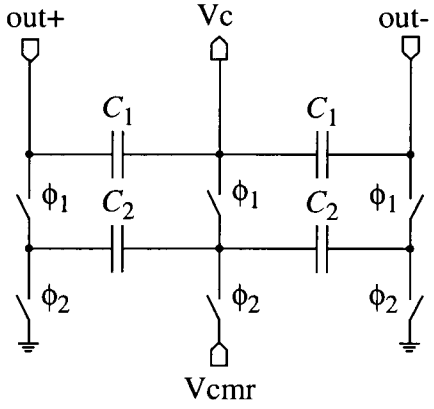


Figure 6.17:Common-mode feedback circuit.

Table 6.3: Simulated performance of the differential opamp.

DC gain (dB)	Unit-Gain Bandwidth (MHz)	Phase Margin (degree)	Slew Rate (V/μs)
80	30	75	25

6.4.2. Clock Generator, Comparator and Other Components

The clock generator with delay control is shown Figure 6.18. Vdelay is the control voltage that can change the duration of the non-overlapping interval between clock phases ϕ_1 and ϕ_2. Two transmission gates were also added to adjust the slopes of the rising and falling edges of the clock signals so that the crossings of ϕ_1 and ϕ_{1b}, ϕ_2 and ϕ_{2b} are symmetrical. Therefore, when a switch is realized by the transmission gate with equal-size PMOS and NMOS transistors, the charge injections of the PMOS and NMOS may cancel each other and the total charge injection is minimized.

The comparator and the *D* flip-flop are the same as the ones used in the single-ended implementation.

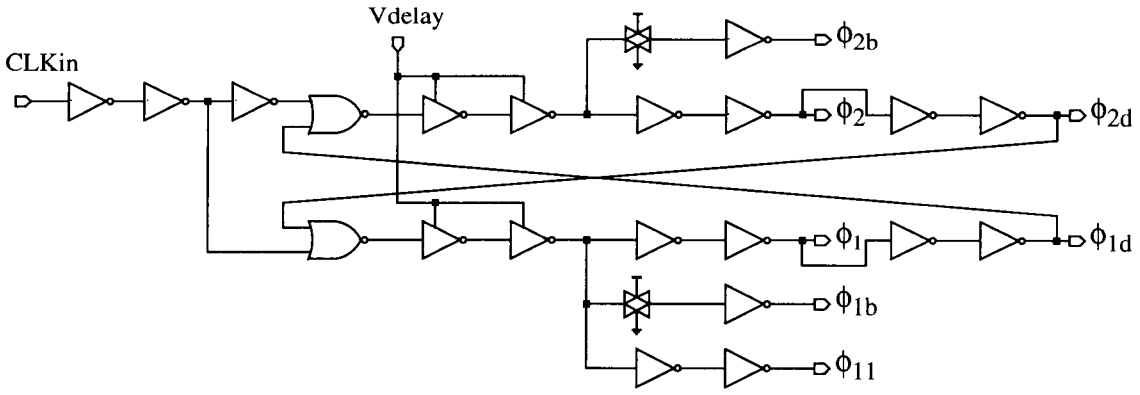


Figure 6.18:Clock generator.

The DAC feedback capacitors C_{dac1} and C_{dac2} in Figure 6.10 were realized by poly-poly capacitors, and $C_{dac1} = C_{dac2} = 2$ pF were used. Since the input capacitors C_{s1} and C_{s2} have a nominal value of 10 pF, the input-referred thermal noise is dominated by the switches associated with the DAC feedback. The inband input-referred thermal noise power can be approximated as

$$P_{thermal} = 10 \cdot \log 10\left(\frac{k \cdot T}{OSR} \cdot \frac{4}{C_{dac1}}\right) \text{ dB.} \qquad (6.12)$$

For $OSR = 512$, at room temperature, Eq. (6.12) gives a noise level of -108 dB. Hence this circuit can have a large dynamic range.

6.4.3. The Top-Level Schematic and Simulations

Figure 6.19 show the top-level schematic of the implemented readout circuit. The sensor capacitors C_{s1} and C_{s2} were two external capacitors and are not shown in the schematic. They were connected later for testing to the three pins C1, C2, Cc. Notice that at the inputs, some switches were realized by a small size NMOS transistor in parallel with a larger transmission gate which is turned off a little before the NMOS transistor. The transmission gate has much larger size so that its RC time constant is small and the settling is fast, but it generates larger clock feedthrough and charge injection when it is turned off. However, the added NMOS can help with fine settling and conducts the extra charge due to clock feedthrough and charge injection of the transmission gate to ground, when the transmission gate is cut off. The NMOS switch generates very little charge error when it is turned off because of its minimum size.

The circuit shown in Figure 6.5 was implemented as the common-feedback block in the first-stage integrator. In order to monitor the output common-mode voltage of the integrator, the output of the opamp was brought to a pin Vcm1 which causes to an extra 10 pF capacitive load. Suppose C_{cm1} and C_{cm2} in Figure 6.5 are 10 pF each, then the

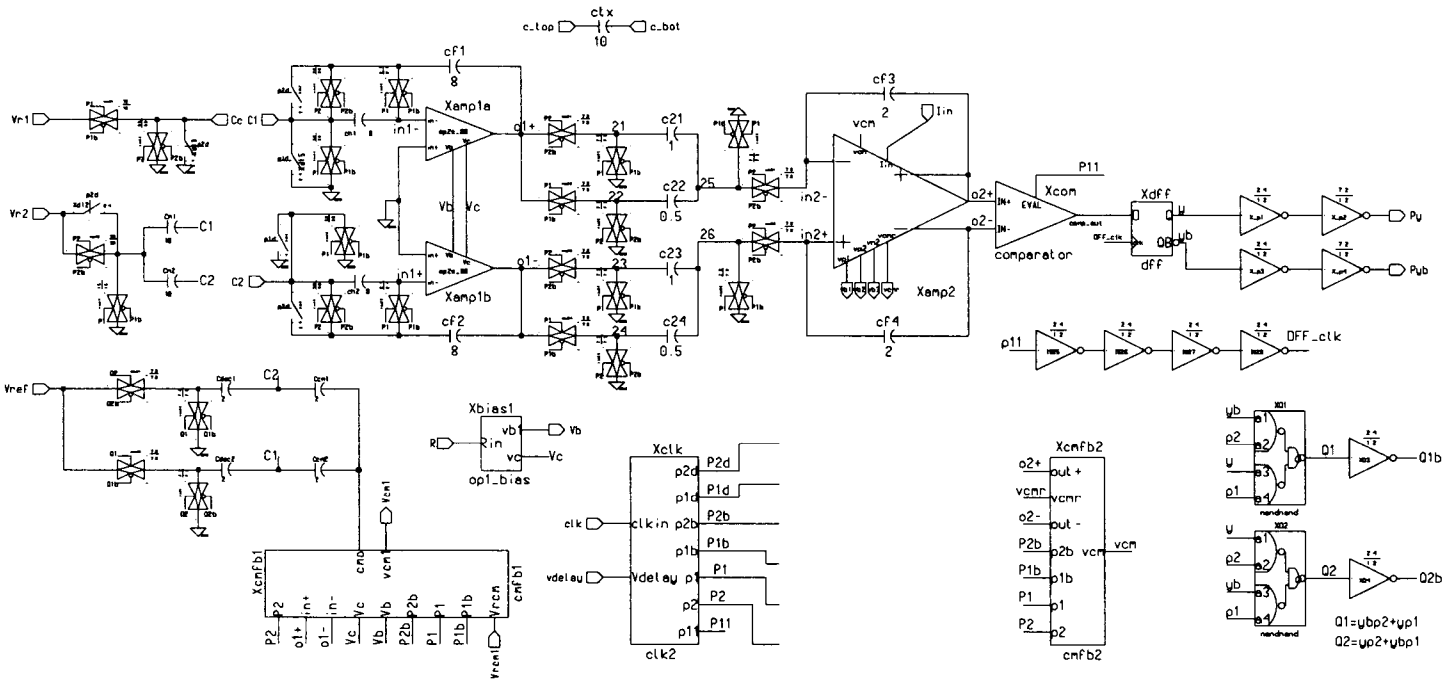


Figure 6.19:Schematic of the differential implementation.

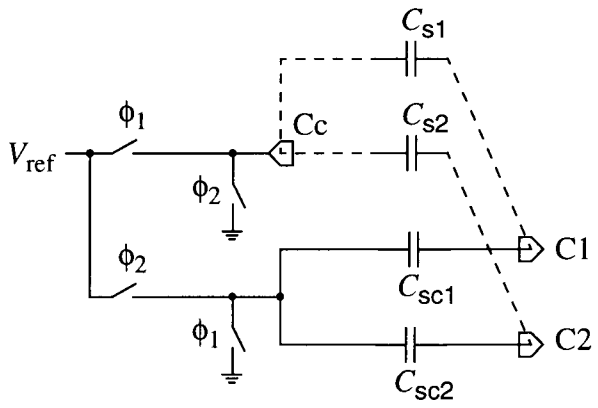


Figure 6.20:The connection of the two added capacitors for coarse common-mode compensation.

capacitive load of the opamp is more than 30 pF and opamp may become unstable. The solution is to reduce the common-mode signal from the two tested capacitors so that C_{cm1} and C_{cm2} can be reduced. Two extra on-chip capacitors were added to compensate the majority of the common-mode signal from the tested capacitors C_{s1} and C_{s2}. Assuming that the nominal value of C_{s1} and C_{s2} is 10 pF and the design value of the two capacitors is also 10 pF, the input common-mode signal is zero and the output common-mode voltage will be very small. The connection of the two on-chip capacitors as well as C_{s1} and C_{s2} are illustrated in Figure 6.20. Usually, the absolute capacitance error of poly-poly capacitors is less than 20% of the nominal value, so C_{cm1} and C_{cm2} were designed as 2 pF each. Now the capacitive load of the opamp is greatly reduced and opamp is still stable when driving the pin. It should also be noted, that in Figure 6.5, V_r can be connected to ground since the output of the opamp can provide the voltage to compensate the reduced input common-mode signal.

The Hspice simulation result is shown in Figure 6.21. It can be seen that without calibration, the estimation error is less than -100 dB when over 800 data are averaged. Therefore, the resolution of this differential circuit is better than $10^{(-100/20)}*10$ pF = 0.1 fF.

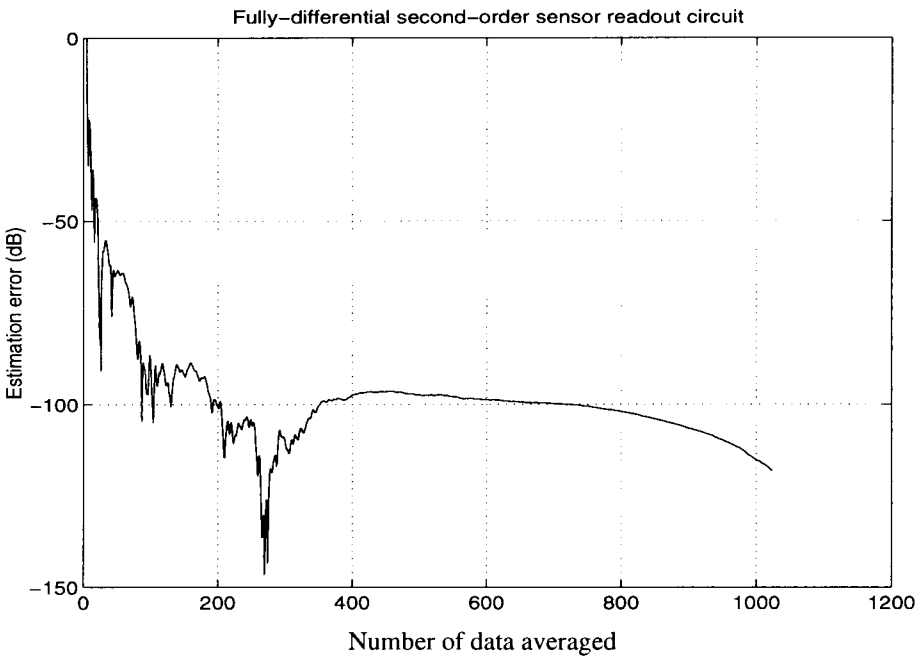


Figure 6.21:Hspice simulation result for the differential implementation.

6.5 Experimental Results

The design was fabricated in the Orbit 1.2 μm double-metal/double-poly process. Figure 6.22 shows the microphotograph of the prototype chip. The die size is 2 mm x 2 mm. The pinout of the chip and the test setup are shown in Figure 6.23. The blocks inside the dotted line are on the test board.

In the test setup, the control voltages Vdelay, Vrcm1 were connected to analog ground AGND. The CMT pins are for testing of the comparator and they were not connected during the test. The tested capacitors C_{s1} and C_{s2} were mica capacitors with a nominal value of 10 pF. They were first measured off board with a HP LCR meter, and C_{s1} was found around 11 pF and $C_{s2} \approx 10$ pF. The clock signal for the chip was provided by an on-board crystal oscillator with added dividers which generated different clock frequencies. The reference voltage was generated by a LM317 which has a large ripple

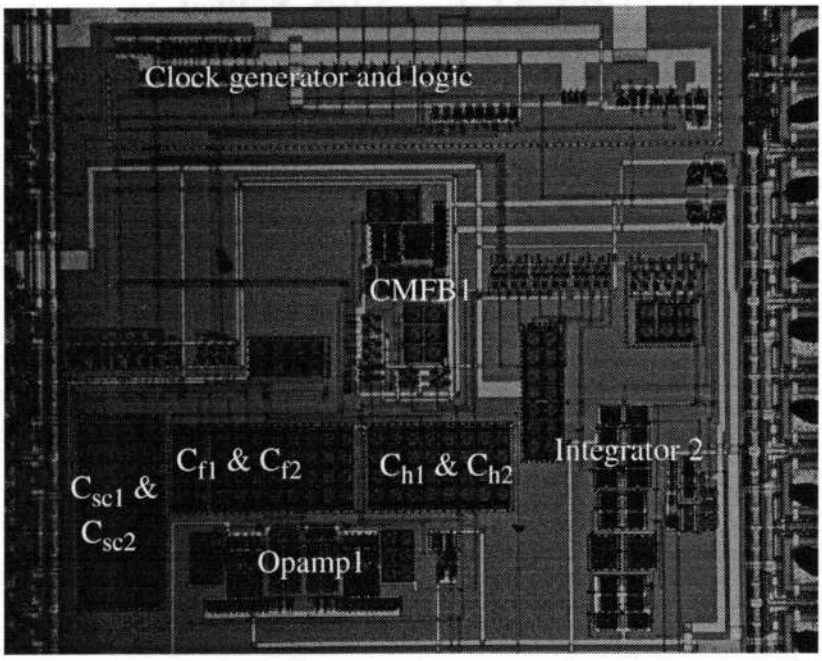


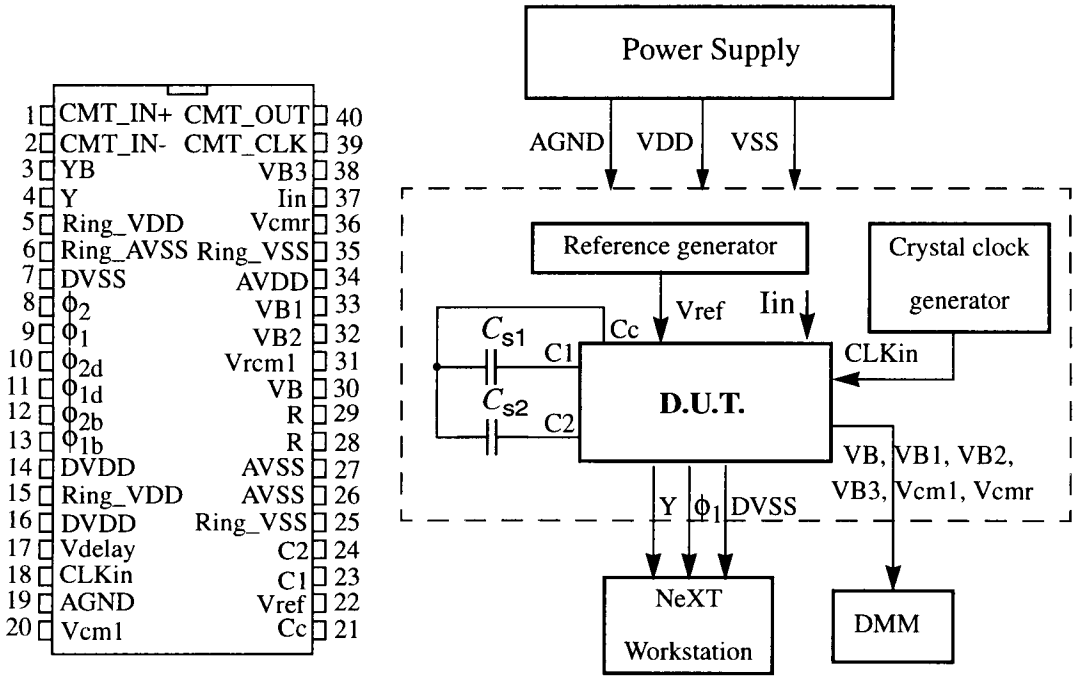
Figure 6.22:Die photograph of the differential implementation.

rejection and a wide output range starting from 1.2 V [60]. The output binary data were read into the Next workstation through the RS232 cable and stored in a file. The bias voltages and the output common-mode voltage of the first stage integrator were monitored by the DMM.

With CLKin set to 1.5 MHz, the output data were acquired and processed in Matlab and the standard deviation of the capacitance ratio $(C_{s1} - C_{s2})/2C_{dac}$ from a typical 40 measurements was calculated. Assuming that the DAC feedback capacitors were 2 pF in the realization, the standard deviation of $(C_{s1} - C_{s2})$ can also be derived, as shown in Figure 6.24. The mean value of $(C_{s1} - C_{s2})$ was 1.0048 pF. When more than 4000 data were averaged in each measurement, the standard deviation σ was better than 0.02 fF. Hence, the resolution of the circuit is better than $3\sigma = 0.06$ fF. When only 1000 data were averaged, the standard deviation was 0.04 fF, and the resolution was 0.12 fF. Compared with the

simulation result shown in Figure 6.21, the test result was close but a little worse. The increased noise may be caused by noise coupling on the circuit board, as well as from the environment.

The standard deviation can also be obtained from the output spectrum. Figure 6.25 depicted the overall spectrum of the output binary data Y with 65536 points. The Hanning window was used before FFT was performed. The desired signal $(C_{s1} - C_{s2})/2C_{dac}$ is at DC. In the output spectrum, the signal power is -12 dBV which corresponds to $(C_{s1} - C_{s2}) \approx$ 1.0051 pF. The total noise power (σ^2) for 100 Hz bandwidth is -114 dBV. Hence, the SNR is above 100 dB and the standard deviation is $\sigma \approx 0.014$ aF.



(a) (b)

Figure 6.23:Pinout and test setup for the differential chip:
(a) Pinout; (b) Test setup.

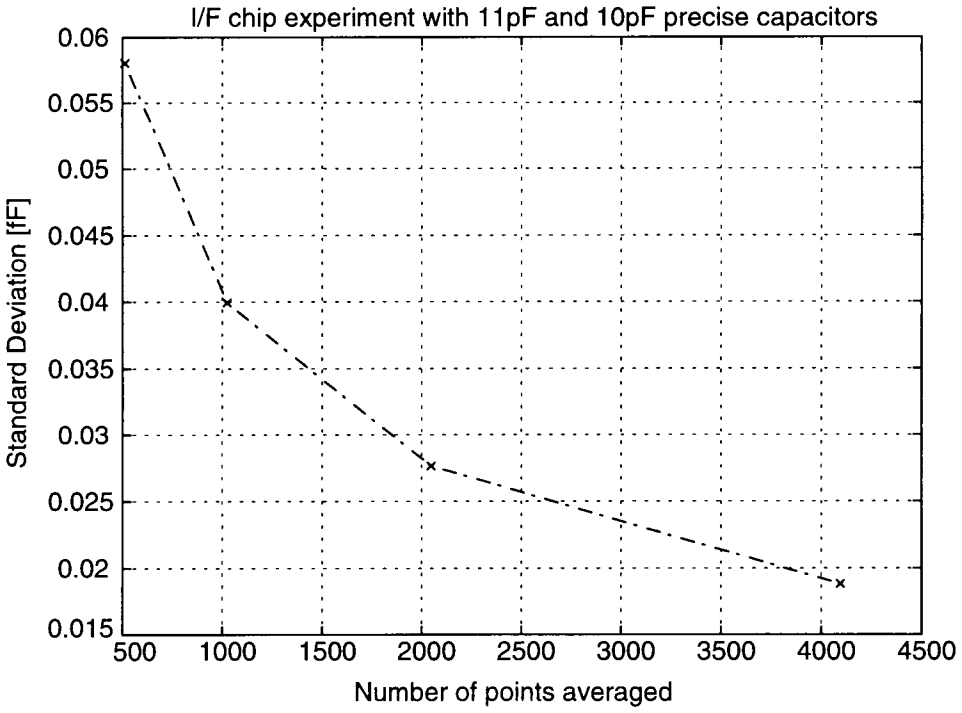


Figure 6.24:Standard deviation from 40 measurements.

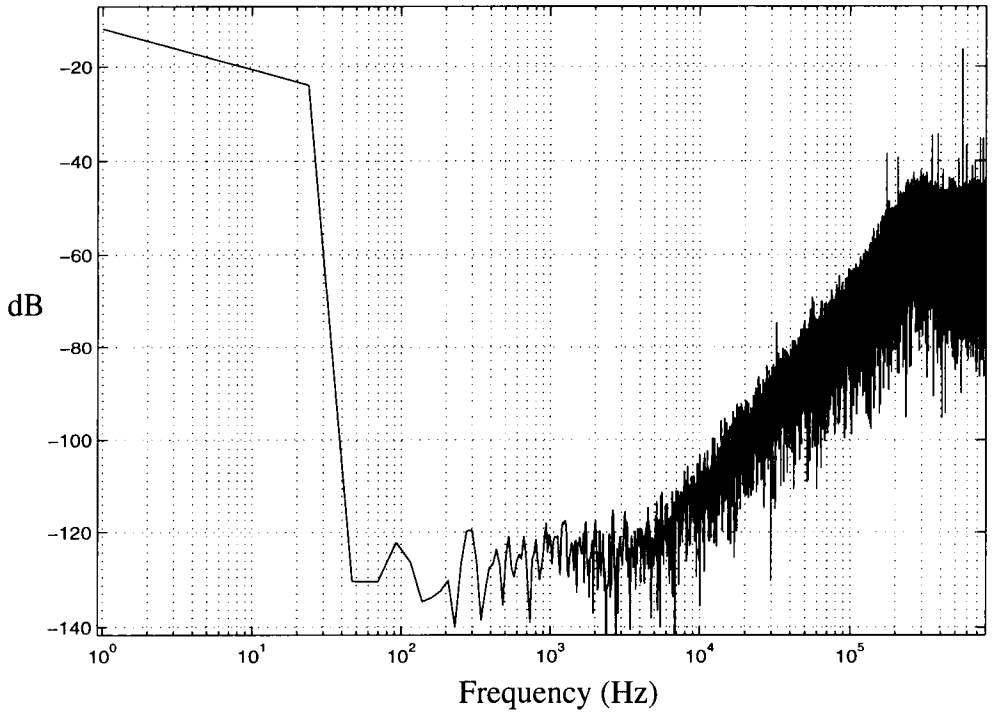


Figure 6.25:Measured power spectrum of the output binary data.

The measurements have been repeated in the lab at different times and for different test chips. Figure 6.26 shows the measured standard deviations for 22 measurements. In each measurement, the standard deviation was obtained from 40 short-term measurements. The number of data points used for estimating the capacitance was 2048 and 4096 for the top and bottom curves, respectively. The measured standard deviations from time to time and from chip to chip varied between 17.5 aF and 32 aF when 4096 data were used for estimation of the capacitance. This shows that the test results have good reproducibility.

In the testing, it was assumed that C_{dac} was 2 pF in the implementation. However, because of process variations, C_{dac} can be off as much as 20%. Hence, although the standard deviation of $(C_{s1} - C_{s2})/2C_{dac}$ was accurate, the standard deviation of $(C_{s1} - C_{s2})$

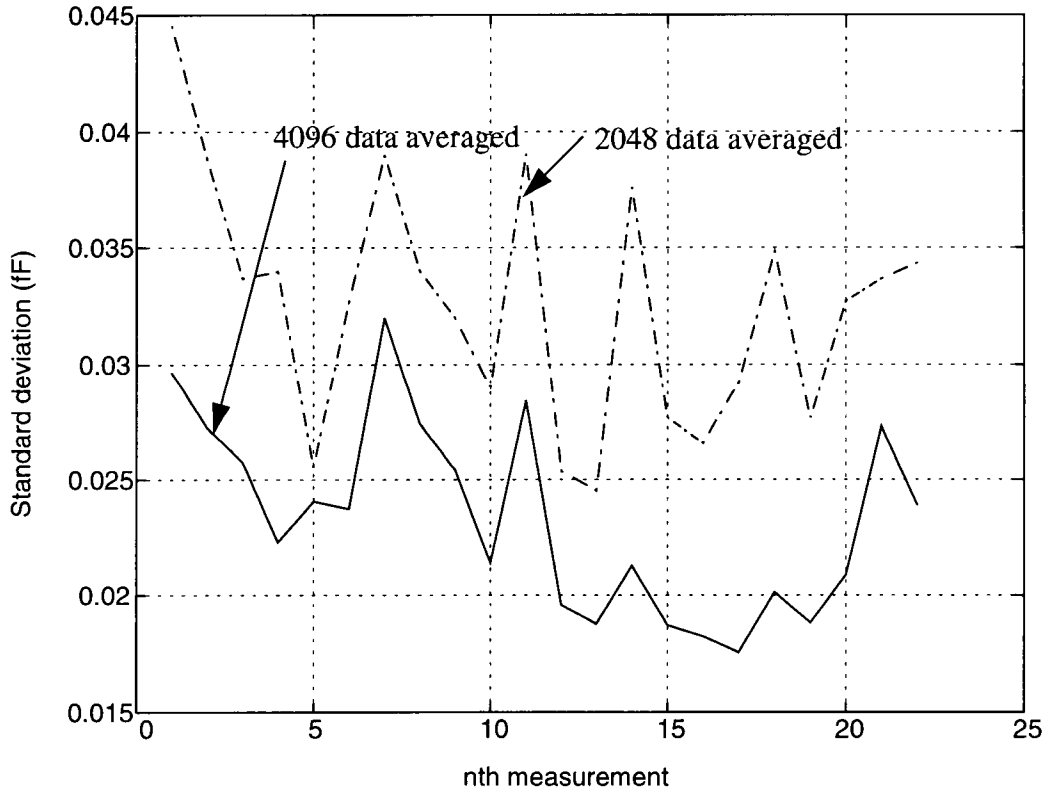


Figure 6.26:Standard deviations from different measurements.

might be off by 20%. For example, in Figure 6.24, when 1000 data were averaged, the real standard deviation would be between 0.032 fF to 0.048 fF.

Table 6.4 shows the comparison between some existing interface circuits for capacitor ratio testing and the single-ended and differential circuits realized in this research using delta-sigma modulation. It can be seen that the proposed single-ended and differential

Table 6.4: Comparison of earlier results and results using the proposed circuits.

Circuit	Output	Hardware Complexity	Accuracy	Measurement time
Floating Gate [15]	analog	simple but accurate ADC needed for post-processing	σ = 50 ppm	time needed to measure the output voltage
A/D based [16]	digital	16-bit ADC used	σ = 35 ppm	conversion time of ADC
Oscillator [20]	digital	Microprocessor needed	σ = 25 ppm	100 msec
Charge-redistribution [23]	digital	Microprocessor, accurate SAR ADC, and memory needed,	σ < 167 ppm	120 µsec
Proposed single-ended circuit	digital	Second-order SC circuit	σ < 10 ppm	4 msec
Proposed differential circuit	digital	Second-order SC circuit	σ < 2 ppm	2.7 msec

circuits have advantages over the existing interface circuits. They require less circuit complexity and are insensitive to non-ideal circuit effects, such as the input offset and finite-gain effect of the opamps, which usually require extra calibration time in other interface circuits. The proposed circuits can also be implemented on the same chip together with capacitive sensors so that the circuits can be smaller and more robust. The speed of the proposed circuits is also reasonably fast, suitable for most sensor applications.

It should be noted that because the new common-mode feedback circuit shown in Figure 6.5 was implemented, the test chip can not only measure the capacitor ratio (C_{s1} - C_{s2})/2C_{dac}, but also estimate the absolute value of C_{dac}. When C_{sc1} and C_{sc2} in Figure 6.20 were added in the implementation, under steady state conditions, Eq. (6.4) becomes

$$C_{cm}(V_r - V_{cm1}) = V_{ref}(C - C_{sc}), \tag{6.13}$$

where $C_{sc} = C_{sc1} = C_{sc2}$. In the implementation, V_{cm1} is the V_{cm} in Figure 6.5, $V_r = 0$, and $C = 10$ pF. C_{cm} and C_{sc} were designed to be 2 pF and 10 pF, respectively. Since the ratio of C_{cm} and C_{sc} can be implemented relatively accurately, the following can be derived from Eq. (6.13):

$$\frac{C}{C_{cm}} = \frac{C_{sc}}{C_{cm}} - \frac{V_{cm}}{V_{ref}} \approx 5 - \frac{V_{cm}}{V_{ref}}, \tag{6.14}$$

Therefore, if we change V_{ref} and monitor V_{cm1}, the ratio between the external capacitor and internal capacitor can be estimated.

Figure 6.27 shows the variations of V_{cm1} when V_{ref} was changed for all the test chips. The absolute value of C_{cm} can be estimated by measuring the slope of these curves, and Table 6.5 shows the results. It can be seen the absolute error is less than 3% for the process in which the chips were implemented. Since C_{dac1} and C_{dac2} were designed to be the same as C_{cm1} and C_{cm2}, and on-chip capacitor matching is usually better than 1%, it is

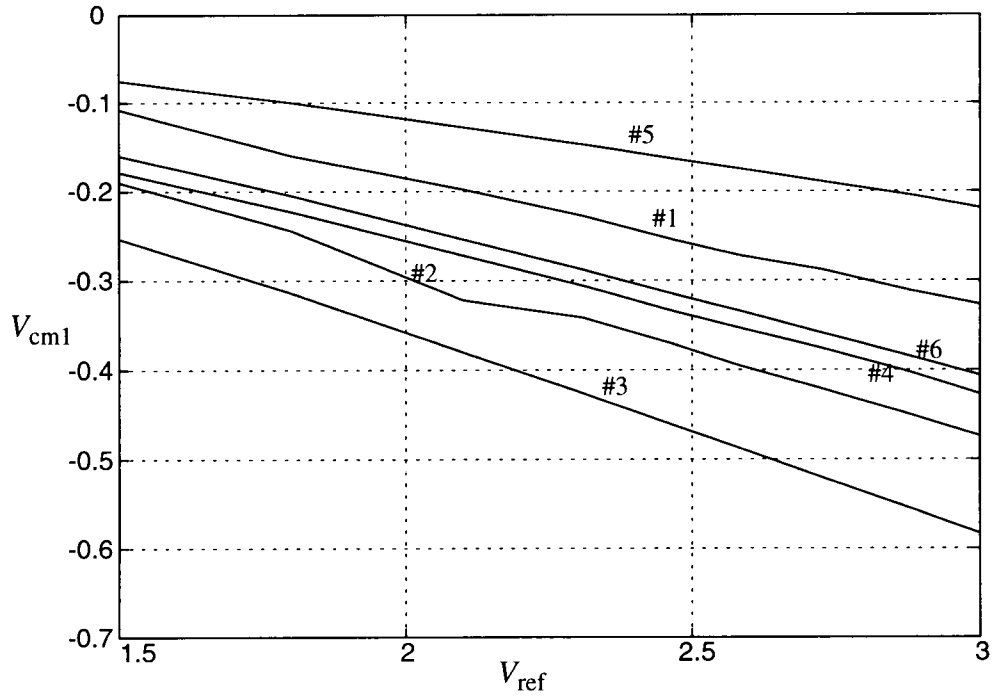


Figure 6.27:V_{cm1} vs. V_{ref} for 6 test chips.

expected that C_{dac1} and C_{dac2} were around 2 pF in the chips, and the absolute error was less than 4%.

6.6 Conclusions

Different schemes of common-mode compensation for fully-differential SC circuits have been analyzed and discussed in this chapter. A differential structure and a pseudo-differential structure were presented and compared. The pseudo-differential

Table 6.5: Estimated capacitance of C_{cm} for the test chips.

	#1	#2	#3	#4	#5	#6
C_{cm} (pF)	1.94	1.93	1.92	1.94	1.96	1.94

implementation of the circuit for capacitor ratio readout was described, and test results were presented. The measured performance shows that high-resolution measurement of capacitance can be obtained using the pseudo-differential circuit.

Chapter 7. Summary and Future Work

7.1 Summary

New techniques for high-accuracy capacitor ratio testing and sensor readout were proposed in this dissertation. Even in the presence of circuit non-idealities, using the proposed techniques, the circuits introduced can provide highly accurate readout of capacitor ratios or difference. The following topics were included:

1. The introduction of various capacitive sensor structures and their characteristics, the limiting factors in realizing highly accurate interface circuits, and some existing circuit techniques for capacitor ratio measurement.

2. Brief introduction of oversampling delta-sigma modulation, and how different circuit structures for capacitor ratio test and sensor readout can be developed using delta-sigma modulation.

3. Analysis of the effects of opamp non-idealities, clock feedthrough and charge injection from the switches, and kT/C noise in SC capacitive sensor interface circuits.

4. Use of correlated-double-sampling techniques to reduce the effects of some opamp non-idealities, and the design of different calibration schemes to cancel the clock feedthrough and charge injection of the switches.

5. Introduction and analysis of new common-mode feedback techniques for fully-differential circuits with large input common-mode input.

The prototype chip implementing a single-ended circuit described in this dissertation provides a readout of capacitor ratio, and its accuracy was higher than any other interface circuit reported to date. The prototype chip of the differential implementation verified the effectiveness of a proposed common-mode feedback scheme, and provided even better resolution than the single-ended chip.

7.2 Future Work

The proposed two-phase circuits have been shown to be useful for high-accuracy differential capacitive sensor interfaces, as well as for on-chip capacitor matching measurements. It would be interesting to use the single-ended circuits in a test structure to characterize process variations. For example, they can be used in a digital process to measure the mismatch of capacitors of different types, such as MOSFET capacitors, sandwich capacitors and poly-poly capacitors. Even the absolute value of capacitors can be measured, when one capacitor is on chip and another one is off chip.

The single-ended and differential structures can be further integrated with capacitive sensors, such as accelerometers and capacitive pressure sensors.

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