High-Aspect-Ratio Through Silicon Vias (TSVs) for High-Frequency Application Fabricated by Magnetic Assembly of Gold-Coated Nickel Wires

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***Abstract*—In this paper we demonstrate a novel manufacturing technology for high-aspect-ratio vertical interconnects for high-frequency applications. This novel approach is based on magnetic self-assembly of pre-fabricated nickel wires that are subsequently insulated with a thermosetting polymer. The high-frequency performance of the through silicon vias (TSVs) is enhanced by depositing a gold layer on the outer surface of the nickel wires and by reducing capacitive parasitics through a low-k polymer liner. As compared to conventional TSV designs, this novel concept offers a more compact design and a simpler, potentially more cost-effective manufacturing process. Moreover, this fabrication concept is very versatile and adaptable to many different applications such as interposer, MEMS, or millimeter wave applications. For evaluation purposes, coplanar waveguides (CPW) with incorporated TSV interconnections were fabricated and characterized. The experimental results reveal a high bandwidth from DC to 86 GHz and an insertion loss of less than 0.53 dB per single TSV interconnection for frequencies up to 75 GHz.**

***Index Terms*—RF signal transmission, skin effect, vertical interconnection, wafer scale integration, through silicon via (TSV).**

I. INTRODUCTION

DURING the past decades, hybrid integration of integrated circuits and micro electromechanical system (MEMS) technology has emerged as one of the most promising approaches in the pursuit of miniaturization and improved performance of microsystems. Hybrid integration does not only rely on pure miniaturization but also achieves more compact integration by merging different functionalities into one device. Especially three-dimensional integrated System in Package (3D-SiP) solutions, which are based on vertical chip stacking, are a general trend in many integration approaches. Not only can 3D-SiPs decrease costs by reducing the volume and weight of the package, they also improve system performance through enhanced signal transmission speed and lower power consumption which is of importance for various demanding applications [1], [2].

The key feature of 3D integration is vertical electrical interconnections which are called through silicon vias (TSVs). They serve the purpose of connecting different layers of a die-stack directly through the substrate. Typical dimensions of TSVs are in the range of 5 to 150 µm for the diameter and 20 to 200 µm for the via length. The utilization of TSVs enables an efficient interconnection technique, which leads to a more compact chip design and packaging as compared to conventional wire bonding techniques. Thus, the path lengths of the metal connections can be reduced, resulting in lower capacitive, resistive, and inductive parasitics of the vias [3]. Already, the first commercially available devices such as MEMS inertial sensors, MEMS microphones, CMOS imagers, and power LEDs successfully incorporate TSV technology [4]–[6].

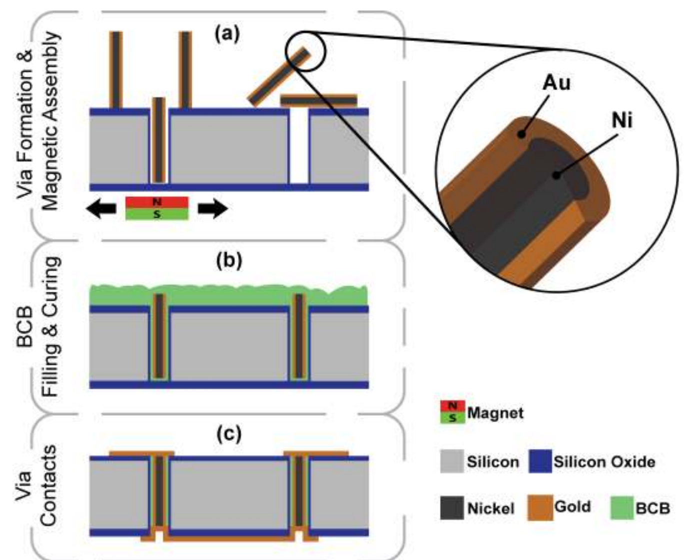

Fig. 1. The TSV fabrication process: (a) Formation of via holes by DRIE and automatic magnetic assembly of gold-coated nickel wires. (b) Application of benzocyclobutene (BCB) as insulation layer and curing under vacuum. (c) Removing excess BCB and opening of the vias on back side as well as deposition and patterning of the transmission lines.

In the field of millimeter wave applications, however, the development of high-performance TSV interconnections has been lagging behind and has become a bottleneck in circuit performance [7]. Important circuit characteristics such as delay times, impedance matching, and power losses are directly determined by the parasitic impedance of the metal interconnects. Thus, using very highly conductive materials such as copper or gold and low-k insulation materials is beneficial for high-frequency signal transmissions. In addition, the integration of multifunctional systems often demands a very high density of I/O connections. A variety of related research topics are currently under intensive investigation, such

as coplanar waveguide (CPW) transition by electromagnetic coupling [8], stacking of waveguide chips by gold bump bonding [9], microstrip transitions by copper TSVs [10], coaxial copper TSVs [11], copper TSV with polymer liner by laser ablation [12], [13], and high current Cu-Cu area-array interconnections [14]. Conventional TSV concepts use electroplated copper as conductive material and a layer of silicon oxide or silicon nitride as insulator [7], [10], [15]–[17]. However, the manufacturing of copper-plated high-aspect-ratio TSVs has proven to be very challenging [4], [15], [16], [18]. Thus, the achievable aspect ratio is limited, creating a trade-off between smaller via diameters and longer vias. In order to keep the via diameter small, most fabrication methods resort to thinning down the wafer substrate to a feasible thickness for the TSV. The process of thinning down the substrates causes a considerable increase of fabrication cost and poses the additional difficulty of handling thin substrates.

In recently published work by the authors, a fabrication concept for high-aspect-ratio TSVs was presented [19]–[21]. Fig. 1 shows the fabrication concept, consisting of the via formation and magnetic assembly in step (a), BCB filling and curing in step (b), and substrate polishing and formation of the via contacts in step (c). With this technology, through silicon vias with lengths of up to 465 µm and with very high aspect ratios of 24 have been demonstrated [19].

In this work, we extended this concept to implement and characterize high-frequency TSVs. We present high-aspect-ratio TSVs with superior high-frequency performance, fabricated using magnetic self-assembly of gold-coated nickel wires. Low losses are achieved by using gold-coated nickel wires as the conductive core and the low-k polymer benzocyclobutene (BCB) as insulation. High-aspect-ratio TSVs are achieved by magnetic self-assembly of the gold-coated nickel wires into the via holes. This process eliminates the need for complicated metallization processes or wafer thinning, making it a very fast and cost-effective fabrication process.

II. TSVs for High-Frequency Applications

Since the length of the metal interconnections and their parasitic impedances are two of the major concerns for high-frequency applications, there are strong requirements on TSVs in both dimension and electrical performance. Due to the skin effect, the resistance of a conductive TSV core increases for increasing frequencies. The skin effect causes the flow of alternating current in a conductor to be confined to a small volume close to the surface of the conductor. The confinement is dependent on the frequency of the alternating current and can be described by the skin depth. In Equation (1), the definition of the skin depth δ is given in relation to the specific electrical resistivity ρ, the angular frequency ω, and the magnetic permeability μ. The skin depth decreases for higher frequencies, causing the effective electrical resistance of the conductor to increase.

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \quad (1)$$

The concept of magnetically self-assembled TSVs is based on pre-fabricated nickel wires [21]. For high-frequency applications, however, ferromagnetic materials such as nickel or iron provide poorer conductivity as compared to gold or copper due to their low skin depth values. In order to improve the high-frequency capabilities of these TSVs, special nickel wires with a gold-cladding were fabricated that combine the ferromagnetic properties of nickel, needed for the magnetic self-assembly process, and the high electrical conductivity of gold. Due to the skin effect, the current density is greatest at the outermost region of the conductor. Thus, the skin effect can be utilized to confine most of the current to the gold cladding of the wires, which results in an improvement of the high-frequency conductivity and thus reduces of the signal losses [22]. The thickness of the gold layer is determined by the skin depth at the targeted operating frequency of 75 GHz which is 0.29 µm. To ensure good high-frequency performance, a gold layer with a thickness of 1.5 µm was deposited on the nickel wires. For the low frequency range the nickel offers a reasonably good conductance and, thus, ensures a very high bandwidth.

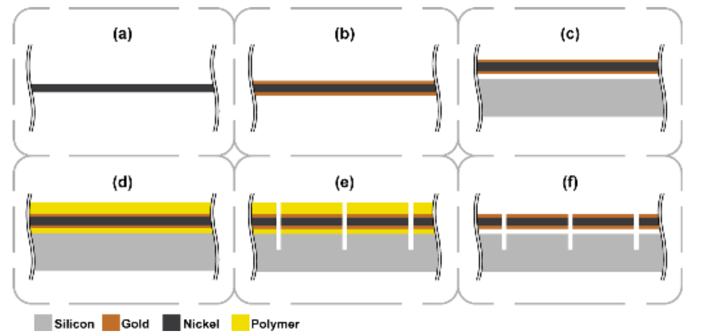

Fig. 2. Via core fabrication: (a) 35 µm diameter nickel wire. (b) Electroplating 1.5 µm gold layer. (c) Fixation of gold-coated nickel wires to a silicon substrate. (d) Embedding the wires in a polymer matrix. (e) Cutting the wires into 350 µm long rods using a wafer dicer. (f) Dissolving the polymer matrix and collecting the via cores.

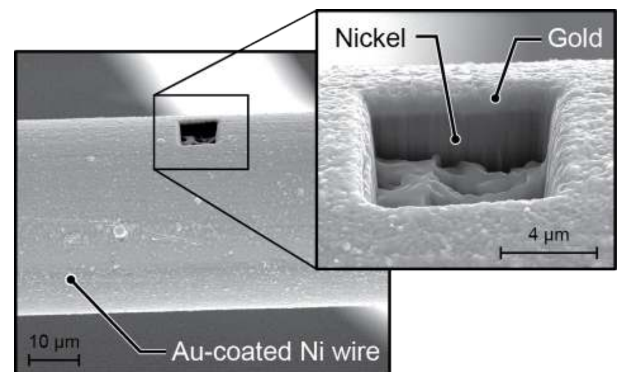

Fig. 3. SEM image of a gold-coated nickel wire. Inset: Cross-section of the Ni/Au interface, generated by focused ion beam (FIB) milling.

In order to minimize the substrate losses, a high-resistivity silicon (HRS) substrate was used. The substrate as well as the insulation material play an important role for the parasitic capacitances. The most commonly used insulator materials are thin layers of silicon oxide or silicon nitride on the via walls [7], [10], [15]–[17]. While these materials provide good elec-

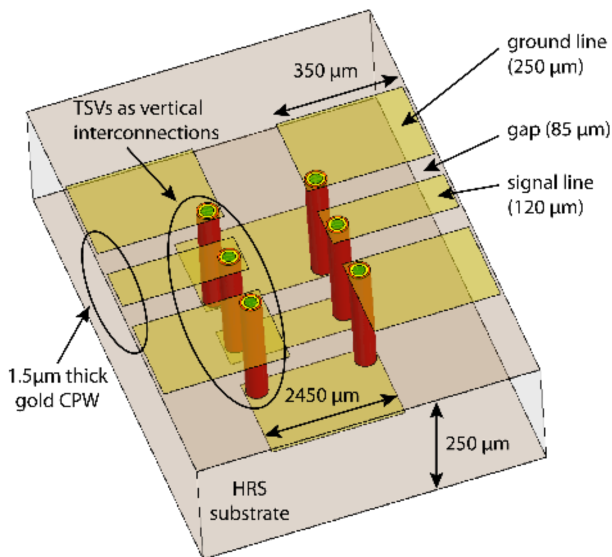

Fig. 4. Characterization structure consisting of oplanar waveguide (CPW) transmission lines incorporating the gold-coated nickel wire TSV concept (configuration (c) in Fig. 5) as vertical interconnections.

trical insulation, their relative permittivities are comparably high, which contributes to high parasitic capacitances. In this approach the low-k dielectric benzocyclobutene (BCB) with a dielectric constant of 2.65 at 20 GHz [23] was utilized instead. BCB also exhibits a low Young's modulus which allows it to act as a mechanical buffer for stresses that are induced by mismatch in coefficient of thermal expansion (CTE) between the metal core and the substrate.

A. Via Core Fabrication

The fabrication of the conductive via cores is performed prior to the magnetic assembly of the TSVs. It consists of two main steps: First a layer of gold is deposited on the surface of a nickel wire, and second the wire is cut into many rods. Fig. 2 shows the via core fabrication in detail. In this experiment, wires made of Nickel 270 with a purity of 99.97 % and a diameter of 35 µm were used. An electroplating process, with the electroplating agent Aurotron H 200 (Atotech GmbH, Germany), was chosen to deposit a uniform layer of gold on the outer surface of the wire. The native oxide on the surface of the nickel was removed by a short 10% HCl dip prior to the plating. Fig. 3 shows an SEM picture of the resulting gold-coated nickel wire. The interface between the nickel core and the 1.5 µm thick layer of the gold cladding is clearly visible in the focused ion beam (FIB) milled recess on the wire surface.

For the cutting process, the plated wire was mounted on a silicon wafer and embedded in a layer of AZ®4562 photoresist. A DAD 320 (DISCO Cooperation, Japan) wafer dicing tool was used to cut the wire into 350 µm long rods. The photoresist matrix that holds the wire in place and protects them from deformation during the cutting process can subsequently be dissolved with acetone to release and clean the cut via cores.

B. TSV Fabrication

As Fig. 1 shows, the fabrication of the TSVs starts with the formation of the via holes by deep reactive ion etching (DRIE) and thermal oxidation of the via sidewalls to prevent electrical short-cuts between the nickel wire and the substrate. Subsequently, the pre-fabricated gold-coated nickel cores are deployed on the substrate and magnetically assembled into the holes. The magnet on the backside of the substrate ensures that the nickel cores are dragged all the way into the via holes. The assembly is performed on a dry substrate, without the addition of liquid agents. After a complete filling of the vias, most of the excess wires can be magnetically steered away from the via structures and retrieved. The magnetic assembly process has been shown to be capable of filling a large number of via holes with 100% yield [19]. Process step (b) shows the filling and curing of the BCB as insulation layer. To ensure a void-free filling the BCB is cured under vacuum at 0.02 mbar. As a final step, shown in Fig. 1(c), the excess BCB and the protruding ends of the nickel cores are ground off and subsequently gold transmission lines are deposited on both the front and the back side of the substrate.

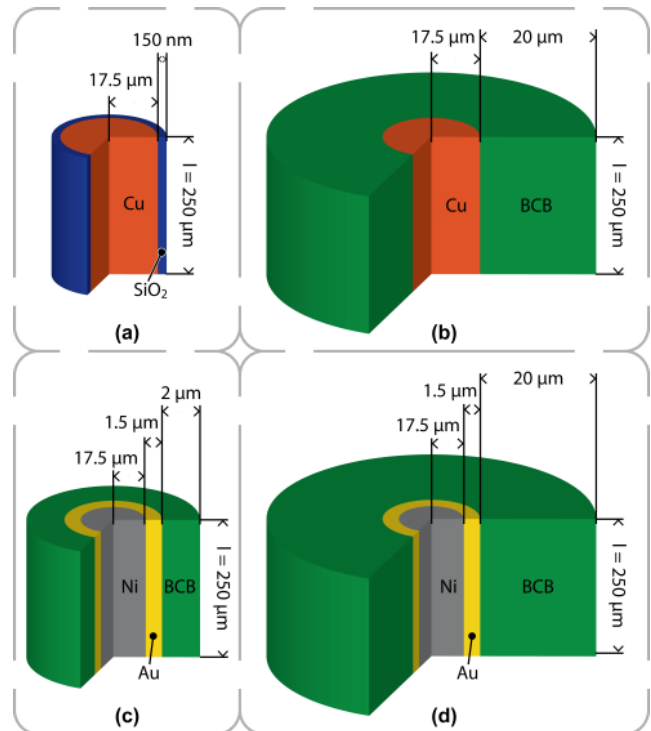

Fig. 5. Different TSV configurations used in the simulation analysis. (a) Conventional copper TSV with thin silicon oxide liner. (b) Copper TSV with thick BCB liner. (c) Nickel TSV with gold cladding and thin BCB liner. (d) Nickel TSV with gold cladding and thick BCB liner.

III. Simulation and Characterization Results

The TSV concepts presented in this paper are evaluated by simulating and measuring a transmission line composed of multiple sections of a standard coplanar waveguide (CPW) and the proposed TSVs as vertical interconnections. All simulations were performed with CST Microwave Studio, taking into account the dielectric losses in silicon and metallic losses

in the metal films. Frequency domain solver was used in the simulations with the calculations based on finite element method. A tetrahedral mesh with a total of 100'081 meshes was applied. The system boundary condition was set to electric ($E_{tan} = 0$). As shown in Fig. 4, the coplanar waveguide (signal line width: 120 µm; gap: 85 µm; and gold thickness: 1.5 µm) is designed with an impedance of 50 Ω at the nominal frequency of 75 GHz. Two 350 µm long CPW sections serving as input and output sections are implemented on top of the substrate. The bottom CPW line length is chosen to be 2450 µm to avoid direct coupling of electromagnetic fields between the input and output sections. The TSVs are used as CPW transitions from the top to the bottom of the substrate.

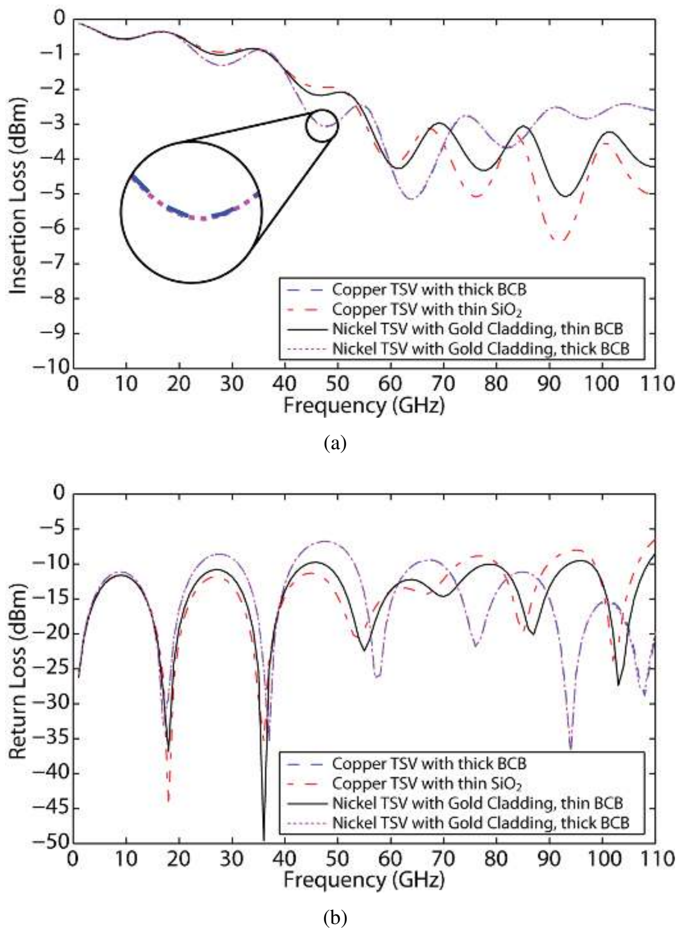

Fig. 6. Comparison of simulated S-parameters for the test transmission line implementing various TSV configurations: (a) insertion loss (S21); and (b) return loss (S11). The insertion loss in (a) reveals very similar performance at low frequencies but superior performance of configurations with a BCB liner above 67 GHz.

Fig. 5 shows the TSV configurations used in the CST Microwave Studio simulations for comparing various available TSV structures. The results are used to emphasize the improvements provided by the proposed novel TSV structure over conventional structures. Fig. 6 shows the simulated insertion and return loss of various TSVs structures. At low frequencies, the insertion loss of the copper TSV closely follows the insertion loss of the TSV proposed in this paper. The copper TSV has a higher insertion loss above 67 GHz. The simulation also reveals that the thicker the BCB is, the better the insertion loss is at millimeter wave frequencies. This can be seen when comparing the insertion loss of the copper TSV with thick and thin insulation layers. The same result can also be deduced by comparing the insertion loss of the gold-coated nickel TSV with thick and thin BCB insulation layers. For thick layers of BCB, the insertion loss is the nearly identical for both copper and gold-coated nickel TSVs.

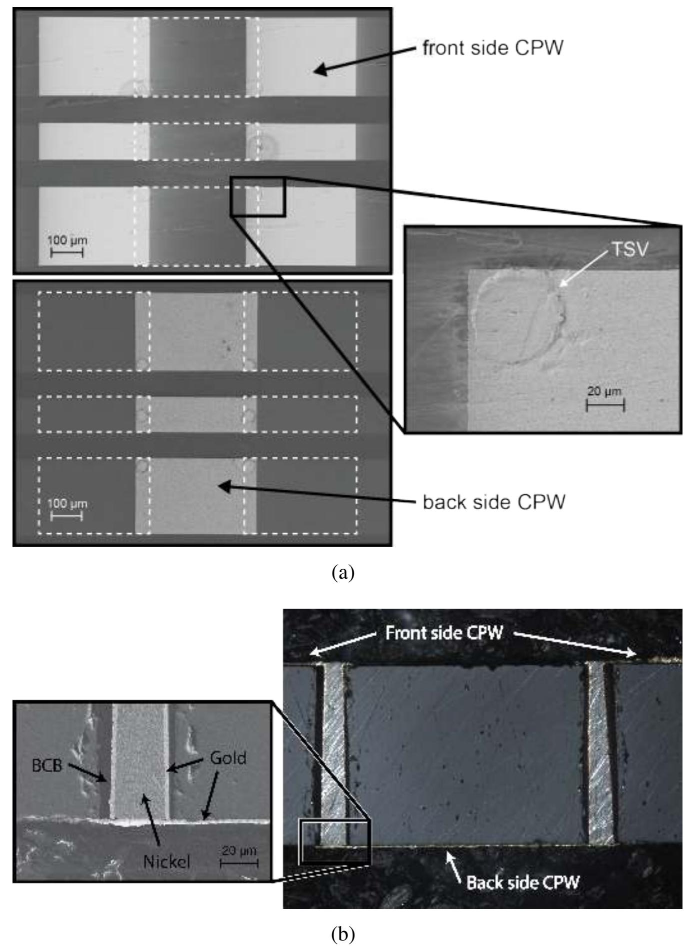

Fig. 7. SEM and microscope pictures of the test structure. (a) coplanar waveguide (CPW) on the front and back side of the substrate. The inset shows a close-up of a TSV transition. (b) cross-section of a TSV transition showing the Ni, Au, and BCB layers, as well as the front and back side CPW. Note that the a slight tilt of the cross-section causes a seemingly smaller TSV diameter towards the front side.

The transmission line used for measurements is fabricated on a high resistivity silicon substrate with a thickness of 250 µm and a resistivity of 5000 - 8500 Ω · cm. Nickel wires with a diameter of 35 µm were used and are compatible with the RF design. With a total via diameter of 42 µm this results in an aspect ratio of 6. The thickness of the gold cladding is chosen to 1.5 µm, which is much thicker than the skin depth of 0.29 µm at 75 GHz. BCB is used to fill the space of 2 µm between the substrate and the via core because it offers a relative permittivity of 2.65, resulting in low parasitic capacitances of the TSVs at millimeter wave frequencies. Fig. 7 shows SEM pictures of the fabricated structures, containing views on both the top and bottom side wave guides as well as a cross-sectional view of a TSV interconnection.

TABLE I
COMPARISON OF EXISTING TSV TECHNOLOGIES FOR HIGH-FREQUENCY APPLICATIONS.

Device	Substrate resistivity [$\Omega \cdot$ cm]	Frequency Band [GHz]	Insertion loss of a single transition [dB]	Insertion loss of the test transmission line [dB]	No. of via transitions	Aspect ratio	Via width	Line Length
[13]	0.15	DC – 10	–	0.08 @ 2 GHz 0.5 @ 6 GHz 1 @ 10 GHz	2	1.3 – 1.47	150 – 170 µm	3 mm
[24]	HRS	78 – 110	0.6 @ 90 GHz	∼ 4 @ 75 GHz ∼ 1.8 @ 86 GHz ∼ 3 @ 110 GHz	2	0.7	150 µm	520 µm
[9]	> 3000	75 – 110	0.07 @ 90 – 98 GHz	∼ 0.25 @ 75 GHz ∼ 0.25 @ 86 GHz ∼ 0.25 @ 110 GHz	2	–	–	∼ 2 mm
[25]	HRS	DC – 40	0.03 dB @ 40 GHz	∼ 0.05 @ 2 GHz ∼ 0.1 @ 6 GHz ∼ 0.125 @ 10 GHz ∼ 0.175 @ 20 GHz ∼ 0.3 @ 40 GHz	2	∼ 0.5	∼ 200 µm	2.7 mm
[8]	HRS	75 – 110	0.25 dB @ 85 – 100 GHz	∼ 1.5 @ 75 GHz ∼ 1 @ 86 GHz ∼ 1.2 @ 110 GHz	2	–	–	∼ 3.6 mm
[17]	> 2000	DC – 30	–	∼ 0.65 @ 2 GHz ∼ 0.75 @ 6 GHz ∼ 0.82 @ 10 GHz ∼ 1 @ 20 GHz ∼ 1.3 @ 30 GHz	2	∼ 5 – 6	∼ 50 – 60	-
[16]	0.01	0.1 – 1.2	–	1 @ 0.6 GHz 1 @ 1.2 GHz	2	12.5	20 µm	40 µm
This work	**> 5000**	**DC – 86**	**0.53 @ 75 GHz**	**0.24 @ 2 GHz** **0.35 @ 6 GHz** **0.5 @ 10 GHz** **0.5 @ 20 GHz** **0.68 @ 30 GHz** **0.93 @ 40 GHz** **2.23 @ 75 GHz** **2.4 @ 86 GHz**	**2**	**6**	**42 µm**	**3.15 mm**

The RF measurements of the fabricated TSVs were performed using an Agilent E8361A PNA vector network analyzer calibrated using a GGB Industries CS-5 calibration standard and 150 µm ground-signal-ground (GSG) coplanar probes and short-open-load-thru (SOLT) calibration. The results suggest a very good electrical yield of the TSV transitions, as all of the roughly ten evaluated devices were functioning correctly. The measurements of the test transmission line, as shown in Fig. 8, agree very well with the simulation results of gold-coated nickel vias with thin BCB liner (see Fig. 5(c)). The measurements reveal that at the nominal frequency of 75 GHz, the return loss is better than 11 dB and the insertion loss is better than 2.23 dB. A single transition of the proposed TSV has an insertion loss of 0.53 dB at 75 GHz when the loss due to the transmission line is de-embedded. Moreover, a return loss of better than 10 dB is achieved up to 86 GHz with the insertion loss being 2.4 dB.

The fabricated TSVs have a very broadband characteristic, as compared to [15]–[17], [25]–[27]. Although the vertical interconnections in [8], [9], [24], [28] achieved slightly larger bandwidths up to 110 GHz, the aspect ratios of these through silicon connections rarely exceed 1, which is much lower than the TSVs proposed in this paper. This is due to the fact that the designs in [9], [24], [28] rely on isotropic etching of the silicon wafer, typically with potassium hydroxide (KOH), while the presented concept utilizes a plasma etching process of the substrate, resulting in a more compact TSV design and a better control of the process parameters. Table I summarizes the performance of the designed TSVs and compares it to a list of various published TSVs. The insertion loss of a single transition, insertion loss of the test transmission line and the frequency band of operation are important parameters used for

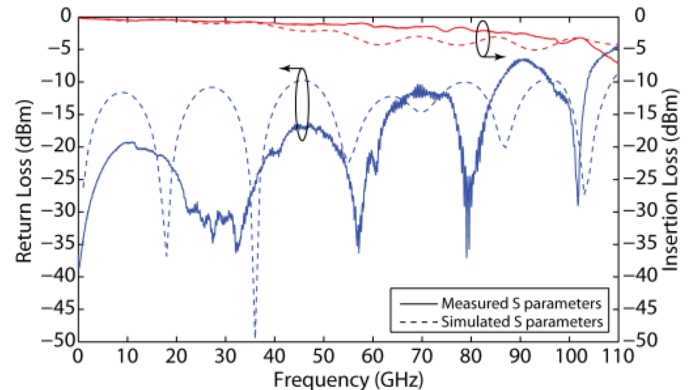

Fig. 8. Measured and simulated S-parameters for the test transmission line implementing the proposed TSV configuration.

comparison.

IV. Conclusions

In this work, high-frequency TSVs that are fabricated by magnetic self-assembly have been developed. By coating 35 µm diameter nickel micro-wires with a 1.5 µm thick gold layer, a new type of magnetically assembled TSVs showing excellent high-frequency performance could successfully be demonstrated. Experimental results reveal a high bandwidth from DC to 86 GHz and low losses showing less than 0.53 dB insertion loss per single TSV transition at 75 GHz. While other concepts achieved slightly larger bandwidths, their aspect ratios rarely exceed 1. The TSVs presented here allow for much higher aspect ratios of more than 6 as well as smaller via diameters, thus facilitating more compact TSV designs and eliminating the necessity of wafer thinning. By using nickel wires with smaller diameters and thicker substrates, aspect ratios of above 20 are feasible as presented in [19]. Furthermore, conventional electro deposition processes typically take half an hour or more, while the proposed magnetic assembly can be performed in a few minutes. As a result, this can potentially reduce the fabrication costs and increase the throughput. In addition, this process allows for a very precise control over via properties such as layer thickness and surface roughness which helps to improve the performance of the TSVs.

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References

[1] M. Motoyoshi, "Through-Silicon Via (TSV)," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 43–48, 2009.

[2] M. Koyanagi, T. Fukushima, and T. Tanaka, "High-Density Through Silicon Vias for 3-D LSIs," *Proceedings of the IEEE*, vol. 97, no. 1, pp. 49–59, 2009.

[3] R. Weerasekera, D. Pamunuwa, L.-R. Zheng, and H. Tenhunen, "Two-Dimensional and Three-Dimensional Integration of Heterogeneous Electronic Systems Under Cost, Performance, and Technological Constraints," *IEEE Trans. Comput.-Aided Des. Integr. Syst.*, vol. 28, no. 8, pp. 1237–1250, 2009.

[4] P. Garrou, C. Bower, and P. Ramm, *Handbook of 3D Integration Technology and Application of 3D Integration Circuits*. Wiley, KGaA, 2008.

[5] J. Lau, R. Lee, M. Yuen, and P. Chan, "3D LED and IC wafer level packaging," *Microelectronics International*, vol. 27, no. 2, pp. 98–105, 2010.

[6] M. Lapisa, G. Stemme, and F. Niklaus, "Wafer-Level Heterogeneous Integration for MOEMS, MEMS, and NEMS," *IEEE J. Sel. Topics. Quantum Electron.*, vol. 17, no. 3, pp. 629–644, 2011.

[7] J. H. Wu and J. A. del Alamo, "Fabrication and Characterization of Through-Substrate Interconnects," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1261–1268, 2010.

[8] J.-P. Raskin, G. Gauthier, L. P. Katehi, and G. M. Rebeiz, "W-band single-layer vertical transitions," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 1, pp. 161–164, Jan. 2000.

[9] K. J. Herrick and L. P. B. Katehi, "RF W-band wafer-to-wafer transition," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 4, pp. 600–608, Apr. 2001.

[10] A. Margomenos, L. Yongshik, and L. P. B. Katehi, "Wideband Si Micromachined Transitions for RF Wafer-Scale Packages," in *2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 183–186.

[11] S. W. Ho, S. W. Yoon, Q. Zhou, K. Pasad, V. Kripesh, and J. H. Lau, "High RF performance TSV silicon carrier for high frequency application," in *Proc. 58th Electronic Components and Technology Conf.*, 2008, pp. 1946–1952.

[12] Q. Chen, T. Bandyopadhyay, Y. Suzuki, F. Liu, V. Sundaram, R. Pucha, M. Swaminathan, and R. Tummala, "Design and demonstration of low cost, panel-based polycrystalline silicon interposer with through-package-vias (TPVs)," in *Proc. 61st Electronic Components and Technology Conf.*, May 2011, pp. 855–860.

[13] V. Sundaram, Q. Chen, Y. Suzuki, G. Kumar, F. Liu, and R. Tummala, "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," in *Proc. 62nd Electronic Components and Technology Conf.*, May 2012, pp. 292–297.

[14] S. A. Khan, N. Kumbhat, A. Goyal, K. Okoshi, P. Raj, and G. Meyer-berg, "High Current-Carrying and Highly-Reliable 30μm Diameter Cu-Cu Area-Array Interconnections without Solder," in *Proc. 62nd Electronic Components and Technology Conf.*, 2012, pp. 577–582.

[15] L. L. W. Leung and K. J. Chen, "Microwave characterization of high aspect ratio through-wafer interconnect vias in silicon substrates," in *2004 IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1197 – 1200.

[16] Y. P. R. Lamy, K. B. Jinesh, F. Roozeboom, D. J. Gravesteijn, and W. F. A. Besling, "RF Characterization and Analytical Modelling of Through Silicon Vias and Coplanar Waveguides for 3D Integration," *IEEE Adv. Packag.*, vol. 33, no. 4, pp. 1072–1079, 2010.

[17] J. Tian, J. Iannacci, S. Sosin, R. Gaddi, and M. Bartek, "RF-MEMS wafer-level packaging using through-wafer via technology," in *Proc. 8th Electronics Packaging Technology Conf.*, 2006, pp. 441–447.

[18] M. J. Wolf, T. Dretschkow, B. Wunderle, N. Jurgensen, G. Engelmann, O. Ehrmann, A. Uhlig, B. Michel, and H. Reichl, "High aspect ratio TSV copper filling with different seed layers," in *Proc. 58th Electronic Components and Technology Conf.*, 2008, pp. 563–570.

[19] A. C. Fischer, S. J. Bleiker, T. Haraldsson, N. Roxhed, G. Stemme, and F. Niklaus, "Very high aspect ratio through-silicon vias (TSVs) fabricated using automated magnetic assembly of nickel wires," *J. Micromech. Microeng.*, vol. 22, no. 10, p. 105001, 2012.

[20] A. C. Fischer, S. J. Bleiker, N. Somjit, N. Roxhed, T. Haraldsson, G. Stemme, and F. Niklaus, "High aspect ratio TSVs fabricated by magnetic self-assembly of gold-coated nickel wires," in *Proc 62nd Electronic Components and Technology Conf.*, 2012, pp. 541–547.

[21] A. C. Fischer, N. Roxhed, T. Haraldsson, N. Heinig, G. Stemme, and F. Niklaus, "Fabrication of high aspect ratio through silicon vias (TSVs) by magnetic assembly of nickel wires," in *24th Conf. Micro Electro Mechanical Systems*, Jan. 2011, pp. 23–27.

[22] L.-T. Hwang, G. A. Rinne, and I. Turlik, "Analysis of a Multilayered-Metal Thin-Film Transmission Line," *IEEE Trans. Adv. Packag.*, vol. 18, no. 2, pp. 381–387, 1995.

[23] The Dow Chemical Company, "Processing Procedures for CYCLOTENE 3000 Series Resins, p 5."

[24] K. J. Herrick, J.-G. Yook, S. V. Robertson, G. M. Rebeiz, and L. P. B. Katehi, "W-Band Micromachined Vertical Interconnection for Three-Dimensional Microwave ICs," in *Proc. 29th European Microwave Conf.*, vol. 3, 1999, pp. 402–406.

[25] A. Margomenos and L. P. B. Katehi, "Fabrication and accelerated hermeticity testing of an on-wafer package for RF MEMS," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 6, pp. 1626–1636, 2004.

[26] H. El Gannudi, V. Cherman, P. Farinelli, N. P. Pham, B. Lieve, H. A. C. Tilmans, and R. Sorrentino, "Design of RF Feedthroughs in Zero-Level Packaging for RF MEMS Implementing TSVs," in *12th International Symposium on RF MEMS and RF Microsystems*, 2011, pp. 0–3.

[27] A. Margomenos and L. P. B. Katehi, "Ultra-wideband three dimensional transitions for on-wafer packages," in *Proc. 34th European Microwave Conf.*, vol. 2, 2004, pp. 645–648.

[28] K. J. Herrick and L. P. B. Katehi, "RF W-band wafer-to-wafer transition," in *2000 IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 73 –76.

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