High Bandwidth Non-Resonant High Voltage Generator for X-Ray Systems

Michael Leibl, Johann W. Kolar, and Josef Deuringer

***Abstract*—High-voltage supplies for medical X-ray systems require up to 150 kV DC at up to 100 kW to supply the tube. The challenge for the power supply however is not only to deal with the high voltage and high power demand, but also to provide short voltage rise- and fall times in the range of 100µs. A coupled interleaved circuit variant of a single active bridge concept, the coupled interleaved single active bridge converter, is demonstrated in this work providing very fast output voltage control due to its non-resonant structure. The conduction modes of the circuit are analysed in detail and compared to the uncoupled interleaved single active bridge approach, demonstrating the advantages of low inverter RMS current, zero voltage switching (or at least zero current switching) over the full operating range with constant switching frequency. Analytic expressions for the output current-duty cycle relationship are provided. Experiments on a 60 kW (low voltage equivalent) prototype show that rise times as low as five switching cycles are possible, allowing to reach the target of 100µs rise time using a switching frequency of only 50 kHz.**

***Index Terms*—DC-DC power conversion, high bandwidth, high voltage generator, X-ray generator.**

I. Introduction

X-RAY tubes used for diagnostic purposes require accelerating voltages of up to 150 kV but are at the same time relatively inefficient. Only ≈1% of the energy used for accelerating the electrons is actually emitted in form of Bremsstrahlung (X-rays) [1]. Therefore, the power demand of medical X-ray tubes ranges from a few kW for dental imaging to more than 100 kW for computed tomography (CT) applications. The major part of the power is dissipated as heat at the anode which is typically a composite of tungsten and copper or molybdenum in order to withstand high temperatures [2]. Due to the surrounding vacuum, cooling capability of the tube is limited and thus also the average power that needs to be provided by the high voltage supply is typically less than 1 kW. Consequently the high voltage transformer is usually not dimensioned for full power continuous operation. Instead high power density transformer designs are common, resulting in a relatively high leakage inductance due to the high number of turns and the required winding isolation distance. Despite the high output voltage, high power transfer and high transformer leakage inductance fast output voltage dynamics are desired. Short output voltage rise- and fall times also allow short pulses to be generated which is beneficial to reduce the patient dose in pulsed fluoroscopy [3]. Another application that benefits from shorter pulses is dual energy CT. Most of nowadays' dual energy systems are equipped with two X-ray tubes emitting radiation at two different energies, typically by applying 80 kV to one and 140 kV to the other tube. A different approach is to use a single tube (single source) which is switched between two voltage levels, requiring rise- and fall times of less than 100 µs [4]. Besides eliminating one tube single source dual energy CT also reduces the patient dose [5]. Although recent achievements in SiC semiconductor technology offer diode break-down voltages up to 35 kV [6], [7], the secondary side of the high-voltage DC-DC converter is typically involving multiple diode rectifier stages connected in series in order to reduce the winding capacitance. Therefore, topologies employing transistors on the secondary side are not feasible due to the excessive gate driver and isolation circuit overhead. The only way to achieve low output voltage fall time is to reduce the output capacitance. For a given voltage ripple specification this can be achieved by increasing the switching frequency or by using interleaving [8]. Therefore, in order to reach a high switching frequency a low switching loss zero voltage switching (ZVS) or zero current switching (ZCS) topology is required for the high-voltage generator. Additionally, the circuit needs to work with high transformer leakage inductance, should provide the possibility of interleaving and should exhibit favorable dynamics for output voltage control.

In this work a coupled interleaved variant of the single active bridge converter (CISABC) is proposed that meets these demands. In Section II the topology is derived first from the uncoupled interleaved single active bridge converter (ISABC) and the steady state operation is analysed in detail. Experimental results obtained on a full-scale hardware prototype are provided in Section III verifying the analysis. Analytic expressions for the duty cycle-output current relationship are provided in the Appendix.

II. Steady-State Analysis

The complete circuit of the high voltage generator proposed in this work is shown in Fig. 1 together with an active three-phase rectifier providing a stabilized DC-link voltage to the inverter and sinusoidal input currents to the mains [9]. At the primary side each of the two inverters, which are operating with 90° phase shift, feeds a series connection of two primary windings, wound on two different transformer cores. Each inverter consists of two series connected half-bridges which, with an additional DC-blocking

Manuscript received October 12, 2017.

M. Leibl and J. W. Kolar are with Power Electronic Systems Laboratory, ETH Zurich, Switzerland (e-mail: michael.leibl@icloud.com).

J. Deuringer is with Siemens Healthcare GmbH, Diagnostic Imaging, 91058 Erlangen, Germany.

Digital Object Identifier 10.24295/CPSSTPEA.2018.00012

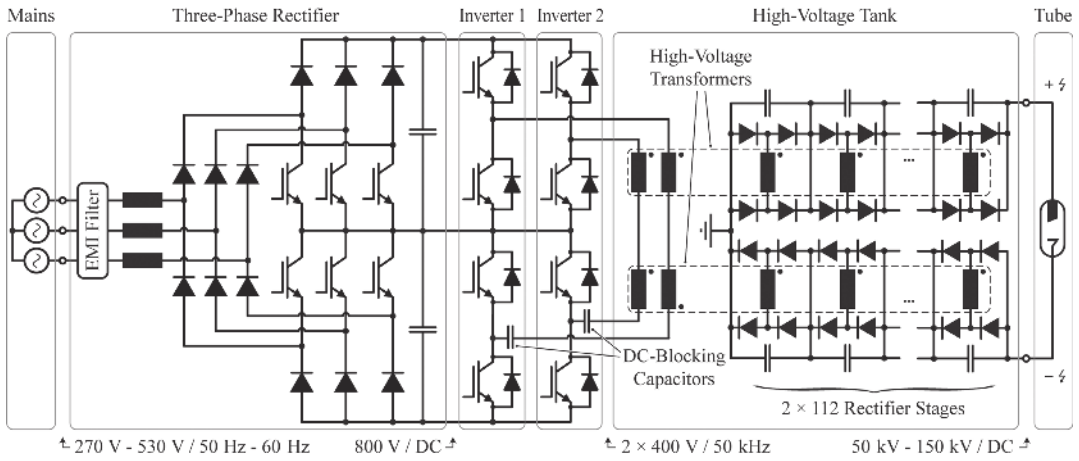


Fig. 1. Circuit of the proposed high voltage generator, consisting of a wide input voltage range active three-phase mains rectifier, providing a stabilized DC voltage for two interleaved inverters, feeding two transformers, each equipped with 112 series connected secondary winding rectifier units, supplying up to 150 kV and up to 60 kW to the X-ray tube.

capacitor, are working as a full-bridge. The separation and series connection of the half-bridges is advantageous for the given application, since it allows the use of low switching loss, low cost 650 V IGBTs for the inverters.

At the secondary side each of the two transformers uses 112 secondary windings, each connected to an individual rectifier stage. Similarly to diode split transformers used in CRT monitors this approach reduces the AC winding capacitance to a negligible value [10]. The winding capacitance is therefore not considered in the analysis and an equivalent secondary winding is used for the following circuit analysis. The proposed high voltage generator uses a coupled interleaved version of the single active bridge converter (SABC). Before analysing the steady-state operation of the CISABC in detail the ISABC, i.e. the converter without the additional coupling of the CISABC is analysed.

A. Interleaved Single Active Bridge Converter (ISABC)

The circuit of the ISABC is shown in Fig. 2, consisting of two full-bridge inverters at the primary and two full-bridge diode rectifiers at the secondary side. The two half-bridges of each inverter are distributed on the two parts of the primary DC-link, using DC-blocking capacitors. Therefore, the two inverters can be considered as parallel connected. The two rectifiers are connected to two series connected DC-links at the secondary side. Therefore, an input parallel output series connection results. Each of two independent transformers links one inverter with one rectifier. The inverters are operated with 90° phase-shift. The first harmonics of the two secondary side DC-link voltage ripples, which occur at twice the switching frequency f_s, are phase shifted by 180° and, therefore, cancel out due to the series connection. Accordingly, the total output voltage U_o only contains ripple components with $4f_s$ and higher. Therefore, a relatively small DC-link capacitance can be used. The steady state behavior of the SABC as described in [11], [12] is briefly reviewed in the following for the case of the ISABC since it serves as reference for the comparison with the CISABC which

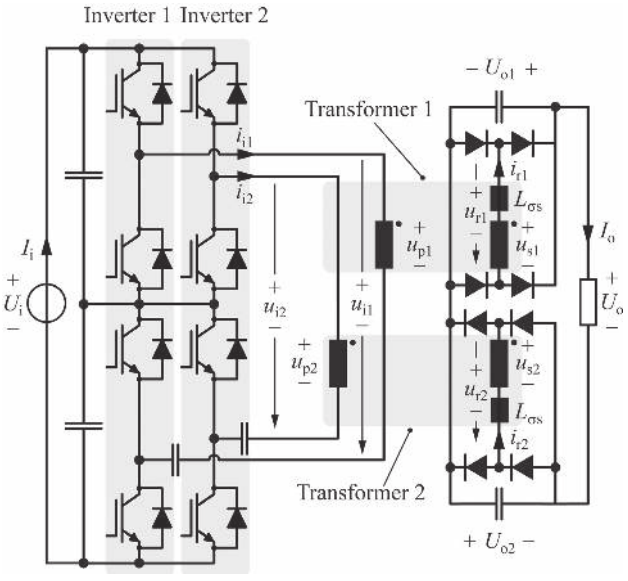


Fig. 2. ISABC circuit in input parallel output series (IPOS) configuration with the two half bridges of each full-bridge inverter distributed on two split DC-links and two full-bridge diode rectifiers connected to two series connected DC-links on the secondary side, linked via two transformers with leakage inductances $L_{\sigma s}$ (reflected to the secondary side).

is introduced in Section II-B.

1) Operating Principle

The only passive elements relevant for the operation of the ISABC are the two leakage inductances of the transformers, represented as lumped elements $L_{\sigma s}$ on the secondary sides. Otherwise the transformers are considered ideal, i.e. the magnetizing inductances are neglected, since they are not essential for the operation. The inverter switching frequency is assumed to be constant, although it could also be employed as control parameter [13]. However, a constant switching frequency is desired since the projected system is operating at a, for IGBTs relatively high, switching frequency of 50 kHz. The output voltage control is therefore solely achieved by varying the inverter duty

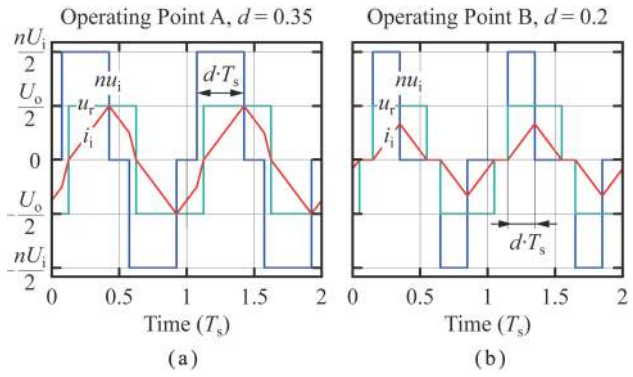


Fig. 3. Steady-state waveforms of one of the two SABCs of the ISABC in CCM (a) and DCM (b) for $\frac{U_o}{nU_i} = 0.5$.

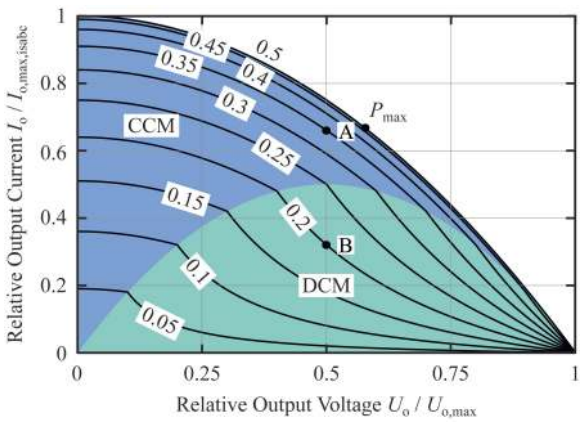


Fig. 4. ISABC output current-output voltage characteristic for different values of duty cycle including the operating points A and B for the waveforms shown in Fig. 3.

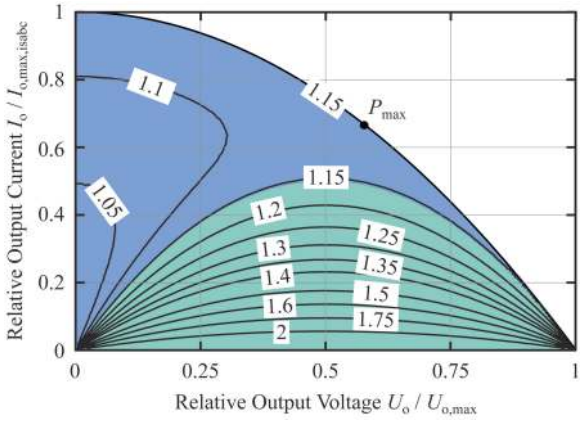


Fig. 5. ISABC RMS inverter current to DC output current ratio.

cycle $d \in [0, 0.5]$.

2) Output Current Characteristic

It is assumed that both SABCs of the ISABC operate with the same duty cycle. At high duty cycle values each of the two SABCs operates in continuous conduction mode (CCM) with typical waveforms as shown in Fig. 3(a). In CCM the steady state output current of the ISABC is derived as

$$I_{\mathrm{o,ccm}} = \frac{nU_\mathrm{i}}{16 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(4d(1-d) - \left(\frac{U_\mathrm{o}}{nU_\mathrm{i}}\right)^2\right) \tag{1}$$

If the duty cycle is less than

$$d = \frac{U_o}{2nU_\mathrm{i}}, \tag{2}$$

discontinuous conduction mode (DCM), as shown in Fig. 3(b), is entered. The steady-state output current in DCM is derived as

$$I_{\mathrm{o,dcm}} = \frac{nU_\mathrm{i}}{2 f_\mathrm{s} L_{\sigma\mathrm{s}}}\left(\frac{nU_\mathrm{i}}{U_\mathrm{o}} - 1\right) d^2. \tag{3}$$

The steady state output current-output voltage characteristic of the ISABC is shown in Fig. 4 for different duty cycles. The regions of CCM and DCM are highlighted showing that a wide operating range is covered by DCM operation. The maximum output current is supplied at the maximum duty cycle $d = 0.5$ and zero output voltage (short circuit), it amounts to

$$I_{\mathrm{o,max,isabc}} = \frac{nU_\mathrm{i}}{16 f_\mathrm{s} L_{\sigma\mathrm{s}}}. \tag{4}$$

The maximum output voltage $U_{\mathrm{o,max}} = nU_\mathrm{i}$ is reached at zero output current (open circuit).

3) Inverter RMS Current

For the calculation of the inverter conduction loss and the transformer winding loss, the inverter root mean square (RMS) current is essential. Fig. 5 shows the RMS inverter current to DC output current ratio of the ISABC. In the CCM region, the ratio is less than $\frac{2}{\sqrt{3}} \approx 1.15$, whereas in DCM the inverter RMS current to DC output current ratio increases dramatically causing high conduction loss. Together with the fact that the maximum output power is reached at relatively low output voltage, therefore at relatively high output-and inverter current, this is the major drawback of the ISABC. This disadvantage can be overcome using a series resonant converter (SRC) [15]. However, the SRC, due to its integrating plant [16], requires more sophisticated control such as cascaded control which is relatively slow, or optimum trajectory control (OTC) which is relatively complex [17]. Compared to that the direct duty cycle-output current relationship (1), (3) of the ISABC allows direct (single control loop) output voltage control. Another solution to reduce the RMS current of the ISABC is to use an inductive output filter [18]. However, due to the high output voltage the filter inductor needs to be split up into one inductor per rectifier stage which is not feasible due to the high number of rectifier stages.

4) Inverter Switched Current

The ISABC offers ZVS on both inverter half-bridges in CCM. In DCM ZVS is only achieved on the leading half-bridge, i.e. the half bridge which is the one causing the first of the two rising and falling edges (Fig. 3(b)). The lagging half-bridge achieves still ZCS in DCM at constant switching

frequency. In comparison the switching frequency of a SRC would need to be varied by a factor of two to obtain ZVS or at least ZCS over the full operating range [19].

B. Coupled Interleaved Single Active Bridge Converter (CISABC)

The CISABC provides a solution to maintain the advantages of the ISABC over the SRC, i.e. ZVS with constant switching frequency and direct output voltage control, while reducing the inverter RMS current. The basic idea is illustrated in Fig. 6. By limiting the inverter duty cycle of a ISABC to 25% the numbers of turns on both sides of the transformers can be cut in half, thus reducing the stray inductances and increasing the output current at 25% duty cycle by a factor of four (Fig. 6(a) - without increasing the peak flux density in the core. Compared to the maximum output current with 50% duty cycle more output current can be transferred if the duty cycle is limited to 25% for all output voltages.

The CISABC achieves these 25% duty cycle voltages at the transformer primary windings using two primary windings on each transformer and connecting them to the inverters as shown in Fig. 7. Because, inverter voltage 1 is the difference and inverter voltage 2 the sum of the two transformer primary voltages, the transformer primary voltages have to exhibit a 25% duty cycle shape as shown in Fig. 6(b) (neglecting the primary leakage inductances for the meantime). The advantage of this circuit is that the secondary side amp-turns are now shared by the two primary windings. Since, the secondary currents, as well as the voltages, are 90° phase shifted this does not cut the inverter currents in half but still reduces them by a factor of $\sqrt{2}$. The following analysis proves this point and considers also the primary leakage inductances which have been neglected up to now.

1) Operating Principle

All three windings of one transformer are wound around the same magnetic path with N_p turns on each primary winding and $N_s = nN_p$ on each secondary winding. The windings of the high voltage transformer are coaxially arranged with one primary winding closest to the core, directly enclosed by the next primary winding and finally with 12.5 mm isolation distance surrounded by the secondary winding. Therefore, the transformer model includes two slightly different primary leakage inductances $L_{\sigma pa}$ and $L_{\sigma pb}$ and the dominating secondary leakage inductance $L_{\sigma s}$.

Due to the symmetry (two inverters, transformers and rectifiers) of the circuit, voltage and current pairs are summarized using vector notation. E.g. the inverter and the rectifier current vectors with the notation of Fig. 7 are expressed as

$$\vec{i}_i = \begin{bmatrix} i_{i1} \\ i_{i2} \end{bmatrix}, \vec{i}_r = \begin{bmatrix} i_{r1} \\ i_{r2} \end{bmatrix}. \tag{5}$$

The secondary current of transformer 1 is the sum of the two primary currents divided by the turns ratio and the secondary current of transformer 2 is the difference of the second primary current and the first primary current divided by the turns ratio. Therefore, the rectifier current vector is expressed as

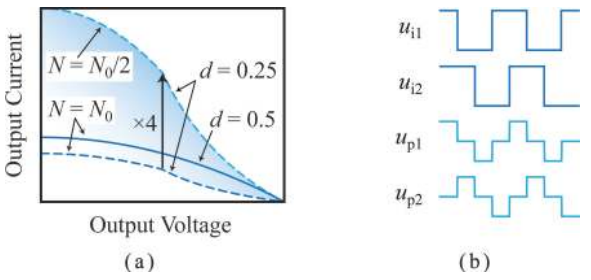


Fig. 6. (a) Reducing the duty cycle of the ISABC from 50% to 25% allows to reduce the number of turns by a factor of two, increasing the maximum output current. (b) Inverter voltages $\boldsymbol{u}_{i1}$, $\boldsymbol{u}_{i2}$ and winding voltages $\boldsymbol{u}_{p1}$, $\boldsymbol{u}_{p2}$ of the CISABC.

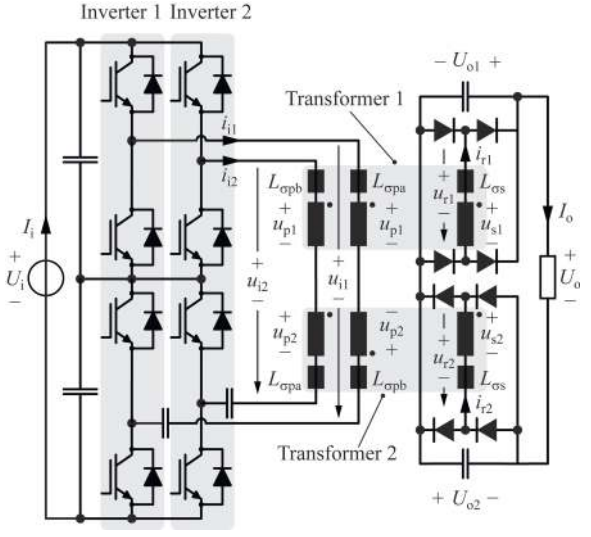


Fig. 7. Basic CISABC circuit in IPOS configuration with the two half bridges of each inverter distributed on two split DC-links.

$$\vec{i}_r = \frac{1}{n}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}\vec{i}_i, \tag{6}$$

and by inverting the matrix the inverter current vector

$$\vec{i}_i = \frac{n}{2}\begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}\vec{i}_r \tag{7}$$

follows. Considering the voltages at the leakage inductance elements, the inverter voltage vector equals

$$\vec{u}_i = \left(L_{\sigma pa} + L_{\sigma pb}\right)\frac{d\vec{i}_i}{dt} + \begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix}\vec{u}_p, \tag{8}$$

and at the secondary side, the rectifier voltage vector is expressed as

$$\vec{u}_r = \vec{u}_s - L_{\sigma s}\frac{d\vec{i}_r}{dt}. \tag{9}$$

With $\vec{u}_s = n\vec{u}_p$, combining (7), (8) and (9) the time derivative of the secondary side currents is obtained as

$$\frac{d\vec{i}_r}{dt} = \frac{1}{L_{\sigma s,tot}}\left(\vec{u}_{r0} - \vec{u}_r\right) \tag{10}$$

with the total leakage inductance referred to the secondary side

$$L_{\sigma s,\mathrm{tot}} = \frac{n^2}{2}\left(L_{\sigma \mathrm{pa}} + L_{\sigma \mathrm{pb}}\right) + L_{\sigma s}, \tag{11}$$

and the no-load rectifier voltage vector

$$\vec{u}_{\mathrm{r0}} = \frac{n}{2}\begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix}\vec{u}_i. \tag{12}$$

In case of no-load ($\frac{\mathrm{d}\vec{i}_{\mathrm{r}}}{\mathrm{dt}} = 0$) the rectifier voltage vector equals the no-load rectifier voltage vector. From (10) it is evident that the rectifier currents result from the difference between the no-load rectifier voltages and the rectifier voltages. Of the three, possibly different leakage inductances $L_{\sigma pa}$, $L_{\sigma pd}$ and $L_{\sigma s}$ only their sum is effectively influencing the current. Therefore, different leakage inductances of the two primary windings because of asymmetric construction due to the coaxial primary winding arrangement still lead to equal current sharing between the inverters. However, the two transformers have to be identical and each inverter needs to connect in series to two different types (a, b) of primary windings, i.e. an outer and an inner one of the coaxial arrangement. The CISABC can, therefore, be modelled by replacing transformers and inverters by two controlled voltage sources with the values of the no-load rectifier voltages (12). Together with the total leakage inductance referred to the secondary side (11) this voltage sources can be imagined to be connected to the output rectifier as shown in Fig. 8. This simplified model allows to study the full steady-state and dynamic behaviour of the CISABC. The no-load rectifier voltage waveforms are shown in Fig. 9 for different values of inverter duty cycle. With maximum duty cycle ($d = 0.5$) the no-load rectifier voltage actually looks like a 25% duty cycle signal. If the inverter duty cycle is reduced to $d = 0.375$ a five-level stepped no-load voltage occurs. The voltage time product of this waveform however is still the same as with maximum inverter duty cycle. In case of $d = 0.25$ the highest level vanishes and a full block rectangular waveform at the half level remains, still having the same voltage time product as with maximum inverter duty cycle. If the duty cycle is further reduced, the zero level is entered four times per switching period, and a gap is inserted in the full block voltage, the voltage time product is now reduced. It is pointed out that the CISABC actually provides five voltage levels to the transformer, potentially allowing a low RMS current in the transformer at low output voltage levels. Simulated waveforms of the CISABC for 50%, i.e. maximum, duty cycle on both inverters with $U_o = 0.75\, nU_i$ are shown in Fig. 10. According to (12), with turns ratio $n = 1$ as in this simulation, the first no-load rectifier voltage u_{r01} equals half of the sum of the two inverter voltages (25% duty cycle no-load rectifier voltage waveform). With $n = 1$, the peak value of this waveform equals the peak value of the inverter voltages, the RMS value, however, is smaller by a factor $\sqrt{2}$. During the time when the no-load rectifier voltage of one transformer equals n times the inverter peak voltage, the rectifier current is building up. As soon as the no-load voltage returns to zero, the rectifier current drops too eventually reaching zero. On the secondary side this particular case is similar to the DCM of the ISABC. On the primary side,

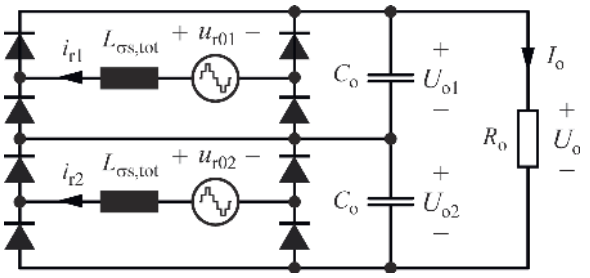


Fig. 8. Equivalent CISABC circuit employing two voltage sources representing the rectifier no-load voltages acting on the total leakage inductances referred to the secondary side.

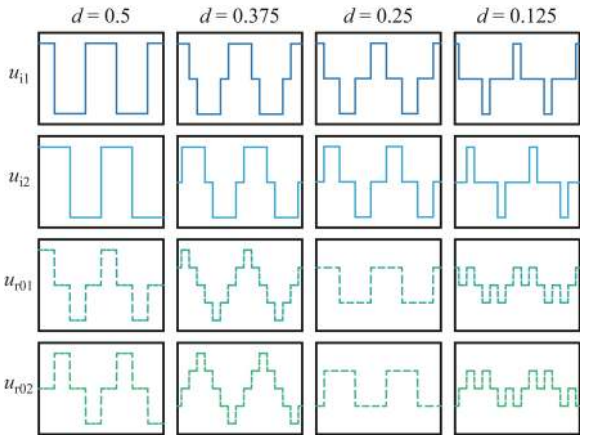


Fig. 9. Inverter voltages $\boldsymbol{u}_{\mathrm{i1}}$ and $\boldsymbol{u}_{\mathrm{i2}}$ and resulting no-load rectifier voltages $\boldsymbol{u}_{\mathrm{r01}}$ and $\boldsymbol{u}_{\mathrm{r02}}$ (dashed) for different values of inverter duty cycle $\boldsymbol{d}$.

according to (7), with $n = 1$ the first inverter current equals half the difference between the first and the second rectifier current and the second inverter current equals half the sum of the two rectifier currents. Since the rectifier currents show half-cycle symmetry all even harmonics are zero. Because the two rectifier currents are also identically shaped but 90° phase shifted all remaining (odd) harmonics are 90° phase shifted as well. Therefore, the rectifier currents are orthogonal which means that each harmonic amplitude of the sum (or difference) of the two rectifier currents equals the square root of the sum of the two corresponding rectifier harmonics squared. The RMS value of the first inverter current is, therefore, calculated as

$$\mathrm{rms}(i_{\mathrm{i}}) = \frac{n}{2}\mathrm{rms}(i_{\mathrm{r1}} - i_{\mathrm{r2}}) = \frac{n}{2}\sqrt{\mathrm{rms}(i_{\mathrm{r1}})^2 + \mathrm{rms}(i_{\mathrm{r2}})^2} \tag{13}$$

and since $rms(i_{r1}) = rms(i_{r2})$, the RMS value of the inverter currents is

$$rms(i_{\mathrm{i}}) = \frac{n}{\sqrt{2}} rms(i_{\mathrm{r}}). \tag{14}$$

Therefore, with the proposed transformer configuration and turns ratio $n = 1$, the RMS value of the inverter currents is by a factor $\sqrt{2}$ lower than the RMS value of the rectifier currents, while the peak value of the rectifier no-load voltage equals the peak value of the inverter voltage. Compared to the ISABC this property allows a significant reduction of the inverter conduc-

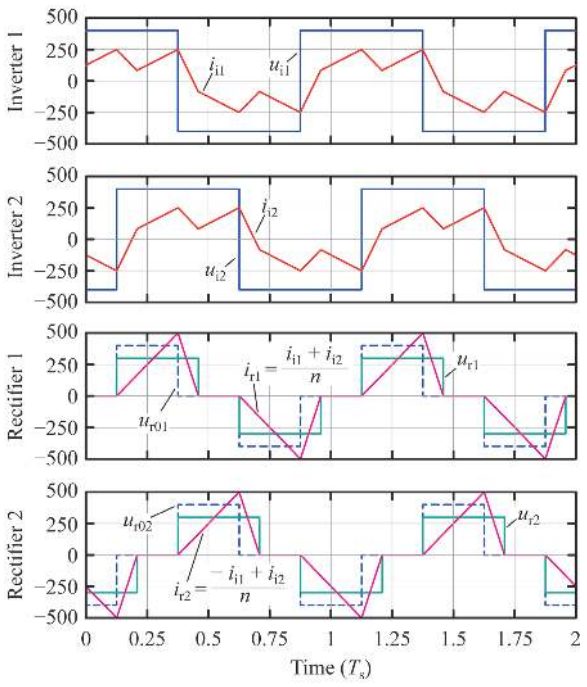


Fig. 10. Simulated primary- and secondary-side voltage and current waveforms of the CISABC according to Fig. 7 with turns ratio $n = 1$ (no-load rectifier voltage shown dashed), total leakage inductance referred to the secondary side $L_{\sigma s,tot} = 1\ \mu H$, switching frequency $f_s = 50\ kHz$, input voltage $U_i = 800\ V$, output voltage $U_o = 600\ V$ and duty cycle $d = 0.5$.

tion loss. Furthermore, for the case shown in Fig. 10, the peak value of one rectifier current occurs when the other is zero, resulting in only half the current peak value being switched by the inverter.

2) Conduction Modes

Due to the five-level characteristic of the rectifier no-load voltage (Fig. 9) three different DCMs and also three CCMs have to be distinguished when aiming to describe the output current-duty cycle relationship. As shown in Fig. 11 it depends on the duty cycle and the relative output voltage which conduction mode occurs. Power transfer for output voltages higher than half the maximum output voltage is only possible in DCM and only if $d > 0.25$. For the working points A, B and C in Fig. 11, representing the three DCMs, the waveforms of no-load voltage, rectifier current and rectifier voltage of one rectifier are shown in Fig. 12. The working points D, E and F in Fig. 11 serve as example for the three CCMs with the according waveforms shown in Fig. 13. The analytic expressions for the output current as function of the duty cycle and the boundaries between the different conduction modes can be derived from Fig. 12 and Fig. 13 as shown in the Appendix.

3) Output Current Characteristic

The output current as function of the output voltage of the CISABC is plotted for different values of duty cycle in Fig. 14 together with the conduction mode boundaries. CCM1 only appears at very high output currents and low output voltages and is therefore not relevant for many applications because of thermal limitations. Therefore, because of the identical relation-

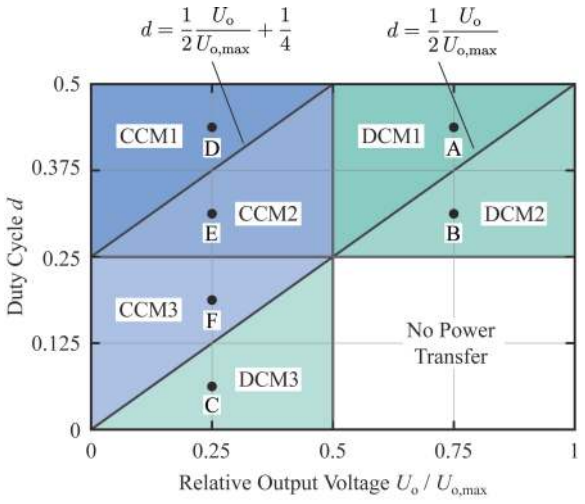


Fig. 11. CISABC conduction modes as function of duty cycle and output voltage relative to maximum output voltage.

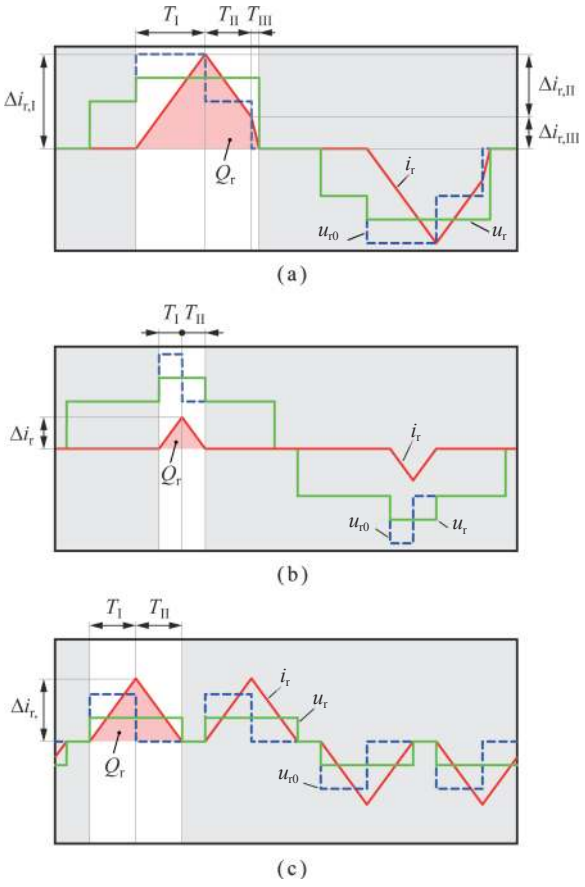


Fig. 12. Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for DCM1 in working point A of Fig. 14(a), for DCM2 in working point B of Fig. 14(b) and for DCM3 in working point C of Fig. 14(c).

ship between duty cycle and output current of CCM2 (46) and CCM3 (54), it is practically sufficient to distinguish between four operating regions for hardware implementation.

The output current characteristic of the CISABC looks similar as the one of the ISABC. The output current decreases

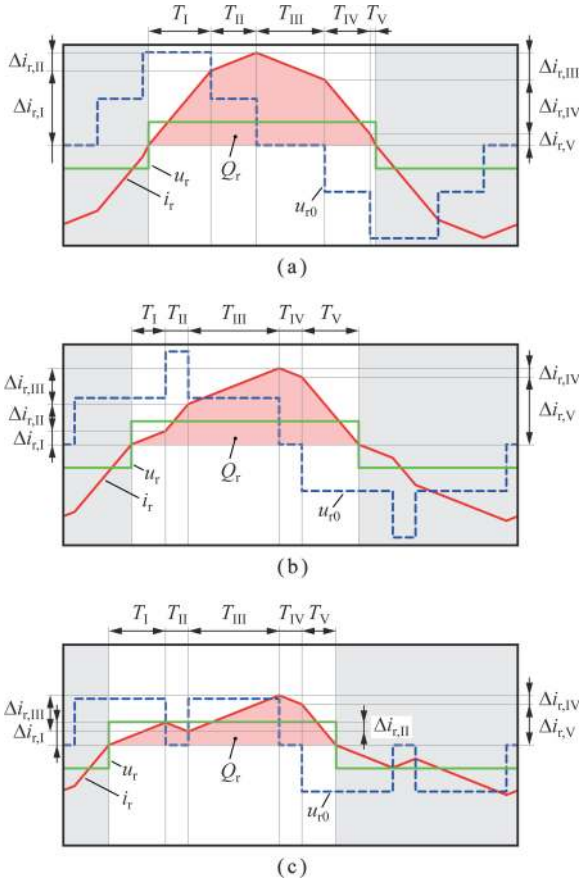


Fig. 13. Rectifier current, rectifier voltage and rectifier no-load voltage waveforms of the CISABC for CCM1 in working point D of Fig. 14(a), CCM2 in working point E of Fig. 14(b), CCM3 in working point F of Fig. 14(c).

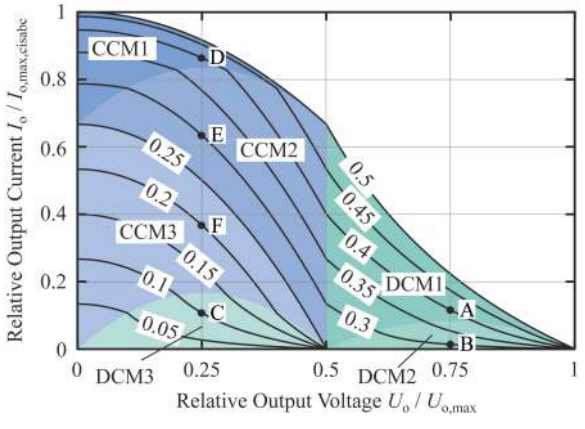


Fig. 14. CISABC output current as function of output voltage for different values of duty cycle with exemplary operating points used for analysing the different conduction modes in Section II-B2.

with increasing output voltage for a given duty cycle and with increasing duty cycle the output current is monotonously increasing. The shape of the characteristic at 50% duty cycle resembles the one of the ISABC at 25% duty cycle (cf. Fig. 4).

From (46) the maximum output current (at $U_o = 0$) of the CISABC can be expressed as

$$I_{o,max,cisabc} = \frac{3nU_i}{64 f_s L_{\sigma s,tot}}. \quad (15)$$

At first sight, this value seems to be smaller than the maximum output current of the ISABC (4). However, for the given application the transformers are designed for maximum power density, and are therefore operating at the maximum flux density allowed by the core material. Because of the 25% duty cycle shape of the rectifier no-load voltage, the maximum voltage time product at the primary winding of the CISABC is only half the one of the ISABC. Therefore, the number of turns necessary to reach the same flux density with the CISABC is only half that of the ISABC, resulting in a four times lower leakage inductance. Therefore, the maximum output current of the CISABC at zero output voltage is three times higher than the one of the ISABC.

4) Inverter RMS- and Peak-Current

Apart from the higher possible power transfer, the fact that the primary side RMS current value is only $\frac{n}{\sqrt{2}}$ times the secondary side RMS value (14) suggests that the primary side RMS currents of the CISABC are lower than the ones of the ISABC. The RMS inverter current to DC output current ratio of the CISABC is shown in Fig. 15. As can be seen the RMS inverter current to DC output current (IC2OC) ratio is less than one on a wide operating range. The plot also shows the output current limit of the CISABC compared to the output current limit of the ISABC, demonstrating that the achievable output current with the CISABC is higher than with the ISABC for all values of output voltage. A direct comparison of the inverter RMS and peak-currents of CISABC and ISABC is provided in Fig. 16. In Fig. 16(a) the inverter current RMS value of the CISABC is related to the one of the ISABC, showing that the inverter RMS current with the CISABC is smaller over the whole operating range covered by the ISABC. At high output voltages the inverter current RMS values are comparable but a significant reduction is achieved in particular at medium output voltage levels. Apart from the higher circuit complexity, the CISABC therefore provides lower RMS current stress on the inverter side. The inverter peak current of the CISABC related to the one of the ISABC is shown in Fig. 16(b). For output voltages less than 30% of the maximum value the inverter peak current is slightly lower with the ISABC, for higher output voltages the inverter peak current is lower with the CISABC. Fig. 16 also shows that the CISABC significantly extends the output current range compared to the ISABC.

5) Inverter Switched Current

Similar to the ISABC the CISABC inherently provides ZVS or at least ZCS in the full operating range. The condition for ZVS is that all rising edges of each inverter voltage u_i occur while the corresponding inverter current i_i is negative and that all falling edges of each inverter voltage u_i occur while the corresponding inverter current i_i is positive (voltage and current directions as in Fig. 2). The switched inverter current related to the DC output current reflected to the primary side is shown in Fig. 17. During the first (leading) falling edge of the inverter voltage (Fig. 17(a)) the switched current is positive in the full

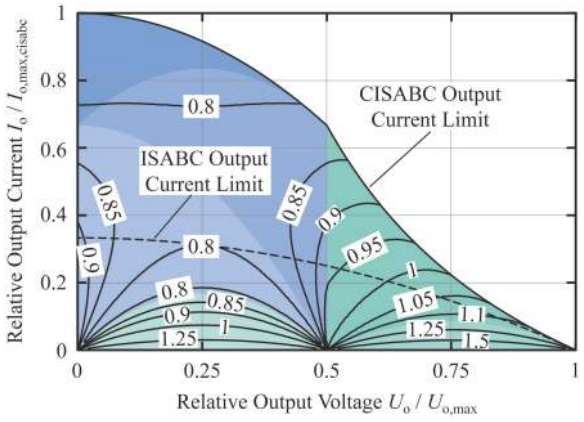
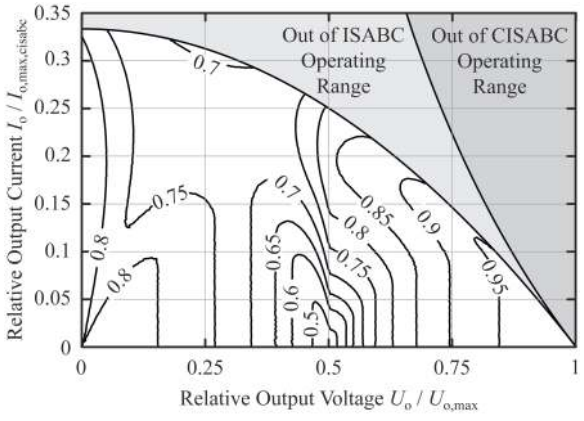
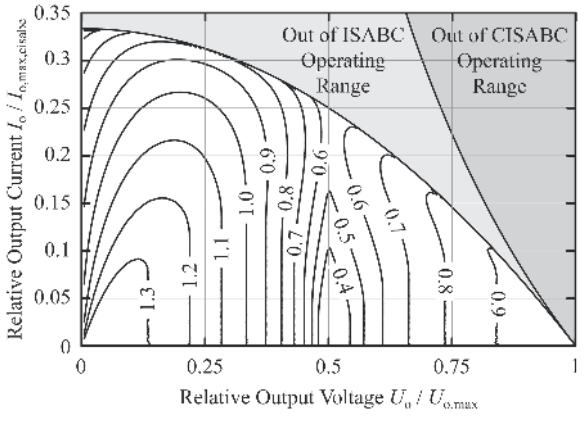


Fig. 15. RMS inverter current to DC output current ratio of the CISABC and output current limit compared to the output current limit of the ISABC.



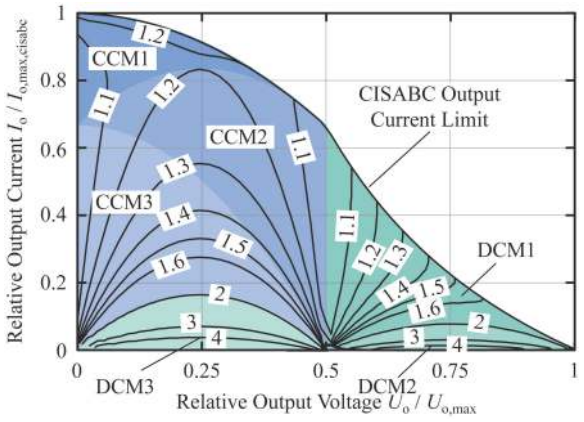
(a)



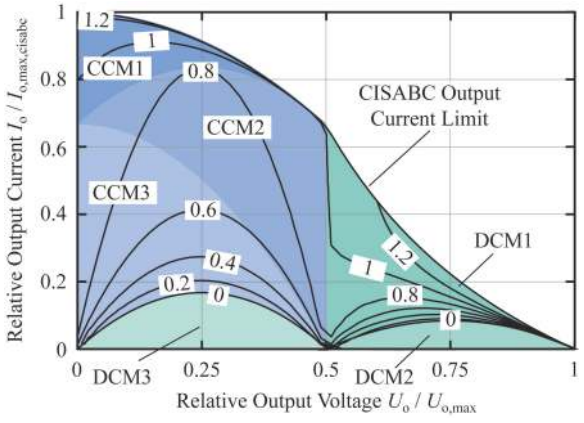
(b)

Fig. 16. Inverter current RMS value (a) and peak value (b) of the CISABC related to the respective values of the ISABC for the part of the operating range covered by both topologies.

operating range. Therefore, the leading half bridge achieves ZVS in the full operating range. During the second (lagging) falling inverter voltage edge (Fig. 17(b)) the switched current is only positive in all continuous conductions modes and in DCM1. In DCM2 and DCM3 the lagging half bridge switches zero current. With nowadays 600 V class insulated gate field



(a)



(b)

Fig. 17. CISABC switched current relative to the output current reflected to the primary side during first falling edge of the inverter voltage (a) and during second falling edge of the inverter voltage (b).

effect transistor (IGBT)s the turn-off losses are actually lower than the turn-on losses, i.e. a soft ZVS commutation is preferred over a hard one. However, the switching loss minimum is still achieved with ZCS which occurs at low output currents at the lagging half bridge.

6) Dimensioning the Leakage Inductance

Based on the maximum required output voltage $U_{o,nom}$ and the inverter input voltage the turns ratio n and the total leakage inductance $L_{\sigma s,tot}$ need to be selected. The choice of the turns ratio leaves some room for optimization, depending on the output voltage / output current requirements of the application. With a low turns ratio (e.g. $n = \frac{U_{o,nom}}{0.9U_i}$) the secondary current is reflected to the primary side with a low gain but at light load the current is discontinuous and thus the RMS current is high. With a high turns ratio (e.g. $n = \frac{U_{o,nom}}{0.6U_i}$) the current shape is continuous even at light load, but the secondary current is reflected with a high gain to the primary side. Usually a good choice is $n = \frac{U_{o,nom}}{0.75U_i}$ which is a compromise between light- and full load efficiency. After the turns ratio is set, the total stray inductance $L_{\sigma s,tot}$ is determined according to (20) with $d = 0.5$ such that the

required output current with some additional margin can be transferred.

III. Experimental Results

In order to demonstrate the functionality of the proposed CISABC circuit and control scheme without requiring high-voltage equipment the prototype uses transformers with a lower ($n = 9 : 6$) turns ratio. The transformer core is the same as will be used for the high voltage version including also the number of turns of the primary windings and the isolation distance between primary and secondary. A picture of the test set-up is shown in Fig. 18. Since only short (< 1 ms) pulses are required to demonstrate the functionality, the two inverters are supplied by a 23.5 mF, 400 V electrolytic capacitor bank. All inverter half-bridges are connected in parallel to this capacitor bank. The inverters are operated with 50 kHz using 650 V IGBTs [20]. The transformers use N87 ferrite cores, two six-turns 0.5 mm foil primary windings and one nine-turn 820 × 200 µm secondary winding that resembles the geometry of the 112 14-turn secondary windings that will be used on the high voltage version. The low winding capacitance of the equivalent transformer is justified, since the total winding capacitance of the high voltage transformer will be comparable, due to the partitioning of the winding into 112 parts each connected to a separate rectifier stage. The AC winding voltage is therefore only 670 V at 150 kV output voltage. The secondary windings of the equivalent transformers used in the low voltage test set-up are connected to two rectifier stages using 650 V Si diodes [21] which connect via two 7.6 µF DC-links to a load resistor, not shown in the picture.

A. Steady-State Operation

Measured waveforms of the inverter and rectifier side voltages and currents representing working point A of the nominal operating range (Fig. 20) are shown in Fig. 19. Note that the rectifier currents are obtained only mathematically using (6) from the measurements taken on the primary side. With the equivalent transformer used, the set voltage for this operating point of 853 V at 71 A represents an output voltage of 150 kV at 400 mA with the real system. This point of maximum voltage and maximum power (60 kW) is located in the region of DCM1, therefore the current on the rectifier side is discontinuous while the current on the inverter side is continuous. The measurement also shows the typical ringing of the rectifier capacitance with the transformer leakage inductance during the current zero state causing small oscillations also in the inverter currents. However, as expected ZVS is obtained at both inverters. The waveforms representing operating point B, i.e. 567 V output voltage and 106 A output current, are provided in Fig. 21. This operating point marks the lowest voltage, equivalent to 100 kV, at which the maximum power of 60 kW has to be transferred. The rectifier current waveform is still continuous and resembles the shape of CCM2. The inverter duty cycle in this measurement is $d = 0.35$ and with $U_{\mathrm{o,max}} = nU_{\mathrm{i}} = 1200\mathrm{V}$ the ratio $\frac{U_{\mathrm{o}}}{U_{\mathrm{o,max}}} = 0.47$, therefore this agrees with the conduction mode

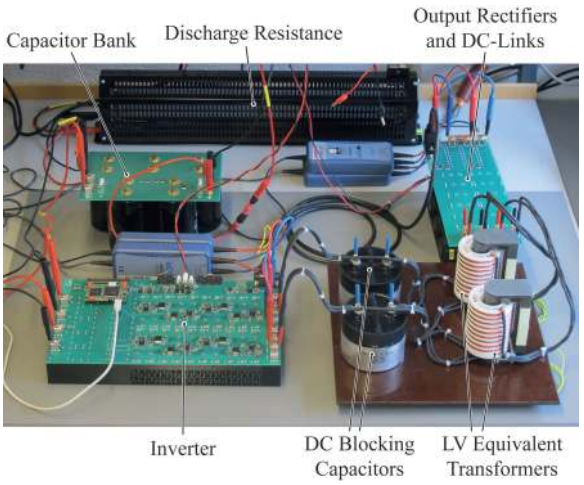


Fig. 18. Experimental set-up of the high voltage generator equipped with **n = 9 : 6** low voltage transformers using same cores and winding geometry as in the projected high voltage transformers.

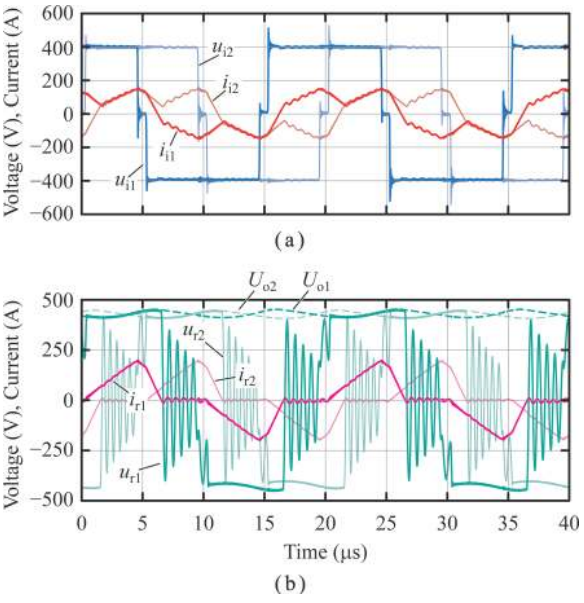


Fig. 19. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point A of Fig. 20 with 853 V output voltage and 60 kW output power.

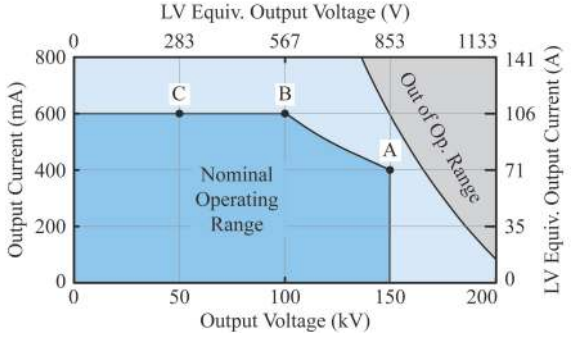


Fig. 20. Nominal operating range and experimentally tested working points shown with separate scales for voltage and current for the high voltage and the low voltage equivalent transformers.

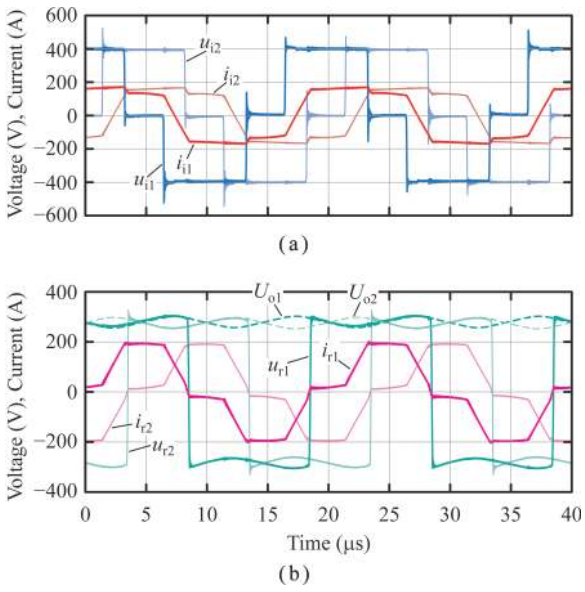


Fig. 21. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point B of Fig. 20 with 567 V output voltage and 60 kW output power.

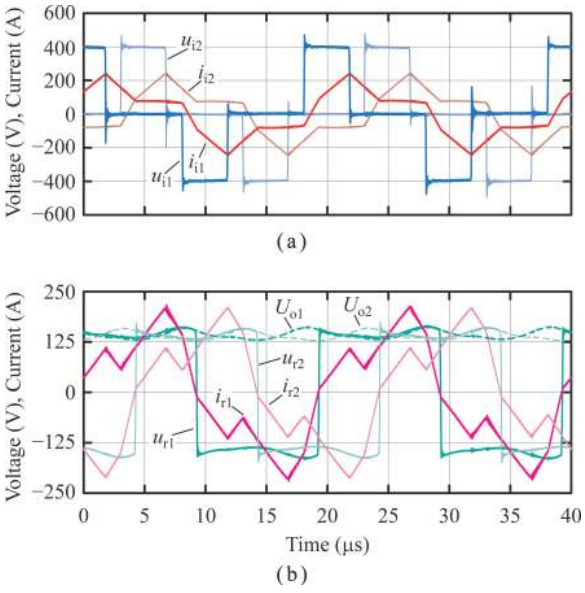


Fig. 22. Measured inverter (a) and rectifier (b) side voltage and current waveforms in operating point C of Fig. 20 with 283 V output voltage and 30 kW output power.

boundaries specified in Fig. 11. Also in this mode both inverters operate with ZVS. The waveforms representing operating point C, i.e. maximum specified output current at $\frac{1}{3}$ of the maximum output voltage are shown in Fig. 22. With the low voltage equivalent transformer the voltage set value is 283 V at 106 A output current, corresponding to 50 kV, 600 mA with the high voltage transformer. With a ratio of $\frac{U_o}{U_{o,max}} = 0.24$ and a duty cycle $d = 0.19$, according to Fig. 11 this operating point is located within the region of CCM3 as the shape of the rectifier current proves. The measurement also confirms ZVS for this operating point.

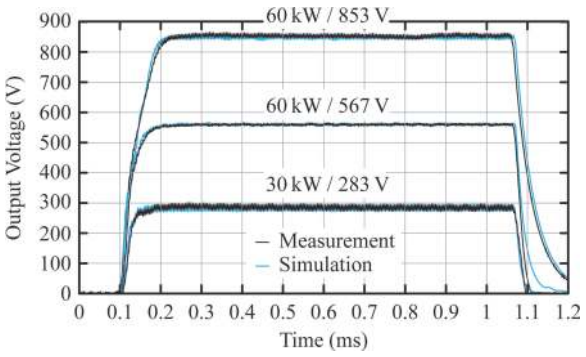


Fig. 23. Measured closed-loop controlled set value pulses for the low voltage equivalent operating points corresponding to Fig. 20 compared to circuit simulations.

B. Output Voltage Control

For the three operating points investigated in the previous section also set value step responses are measured. The results are shown in Fig. 23 and compared to the results obtained from a circuit simulation. As it is shown there is little deviation from the simulation, i.e. it is confirmed that all relevant parasitic elements are modelled. Note that the simulation applies exactly the same control algorithm as it is implemented in the FPGA, including models of the Delta-Sigma ADC (DS-ADC)s used for the output voltage measurements. Of the passive components only the leakage inductance $L_{\sigma s,tot} = 2.8$ μH, the output capacitance $C_o = 7.6$ μF and the load resistance R_o equalling 12 Ω in operating point A, 5.4 Ω in operating point B and 2.7 Ω in operating point C are modelled. Switches and diodes are modelled ideally. As can be seen the output voltage rise time for all operating points is less than 100 μs (5 switching cycles). The achievable rise time is lower for lower values of load resistance.

IV. Conclusion

A novel interleaved circuit variant of the ISABC, the CISABC, is proposed. The circuit connects two transformers, or at least one transformer with two magnetic paths, such that the no-load secondary voltages are obtained proportional to the sum respectively the difference of the two inverter voltages. The circuit exhibits three continuous and three discontinuous conduction modes which are analysed in detail with analytic expressions for the output current - duty cycle relationship and the boundaries between the conduction modes provided. The control strategy is demonstrated on a 60 kW, 50 kHz prototype, achieving 100 μs (five switching cycles) output voltage rise- and fall times.

The CISABC features several advantages over the ISABC and the SRC. Compared to the ISABC, the main advantage is the lower inverter RMS current. Depending on the operating point the inverter current of the CISABC can be as low as half the value obtained with the ISABC. Furthermore, the maximum possible output current which is limited by the leakage inductance is up to three times higher with the CISABC than with the SABC at the same core peak flux density. Compared to the SRC the CISABC mainly provides the advantage of ZVS (or at least ZCS) over the full operating range with constant switch-

ing frequency. Additionally, the non-resonant structure of the CISABC allows fast output voltage control. Finally, compared to non-interleaved circuits the low output voltage ripple of the CISABC allows a small output capacitance which is necessary to achieve short output voltage fall-times with passive rectifiers.

One main disadvantage of the proposed solution is that it requires two transformers, or at least a transformer with two flux paths. For the given application this is acceptable since using two transformers allows to reduce the 150 kV isolation requirement to only 75 kV between winding and core. Further, the CISABC exhibits slightly higher RMS currents on the rectifier side than the ISABC in sections of the operating range. However, since the losses in the rectifier diodes are mainly caused by the average current, which is the same as the one of the SABC, this is only a minor downside.

In summary the low inverter RMS currents and the ZVS or at least ZCS inverter commutation in the full operating range allow to keep the inverter losses low while constant switching frequency guarantees low control complexity. The interleaved operation allows to reduce the output capacitance, and double the duty cycle update rate, such that high output voltage control bandwidth is achieved. The proposed circuit and control structure is, therefore, a good choice for applications that allow only a passive secondary side (diode) rectifier but require fast output voltage rise- and fall times, as demonstrated on a prototype for a high-voltage X-ray supply.

Disclaimer

The concepts and information presented in this paper are based on research and are not commercially available.

Appendix

The derivation of the duty cycle-output current relationship for the different conduction modes and their boundaries are presented in the following.

A. Discontinuous Conduction Modes

1) Discontinuous Conduction Mode 1

For high values of duty cycle and high output voltage, as in working point A indicated in Fig. 14, the CISABC operates in DCM1. The characteristic waveforms of rectifier current, rectifier voltage and rectifier no-load voltage for this case are shown in Fig. 12(a). It is assumed, that the outputs are loaded symmetrically, therefore only the situation of one of the two rectifier sides is considered.

Furthermore, because of the half-cycle symmetry of the signals, only the positive rectifier current half-cycle is regarded. Assuming $0.5 > d > 0.25$ the rectifier no-load voltage varies between all five values. If it is also assumed that $nU_i > U_o > \frac{nU_i}{2}$, the rectifier current is only rising while the rectifier no-load voltage equals nU_i, its full-level. Hence, assuming the rectifier current is actually discontinuous, the rectifier current has to be zero when the rectifier no-load voltage value changes from half-level to full-level and this last rising edge of the rectifier no-load voltage marks the begin of the positive current half-cycle. Each current half-cycle is partitioned into three conduction intervals. During the first interval the rectifier current rises for

$$T_{\mathrm{I}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}} \tag{16}$$

with the switching period $T_s = 1/f_s$. As soon as the rectifier no-load voltage changes to the half its positive maximum level, interval II begins and the rectifier current changes for

$$T_{\mathrm{II}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}} \tag{17}$$

For DCM1 it is assumed, that the current does not reach zero during interval II. Therefore, after T_{II} has passed and the rectifier no-load voltage has changed to zero, the final conduction interval III is maintained until the current reaches zero. The total voltage time product applied to the leakage inductance between two current zero-crossings is zero, i.e. the voltage time product of rectifier voltage and rectifier no-load voltage during the three conduction intervals have to be equal, i.e.

$$nU_{\mathrm{i}} T_{\mathrm{I}} + \frac{nU_{\mathrm{i}}}{2} T_{\mathrm{II}} = U_{\mathrm{o}} (T_{\mathrm{I}} + T_{\mathrm{II}} + T_{\mathrm{III}}) \Rightarrow T_{\mathrm{III}}. \tag{18}$$

This expression yields the duration of the third conduction interval when the current decreases to zero for

$$T_{\mathrm{III}} = \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,III}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{19}$$

Using expressions (16)-(19), the total charge Q_{r} transferred to the output during one half-cycle (Fig. 12(a)) is calculated which, multiplied by twice the switching frequency, finally leads to the average current transferred to the output in DCM1,

$$I_{\mathrm{o,dcm1}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \left(\left(\frac{nU_{\mathrm{i}}}{4U_{\mathrm{o}}} - \frac{1}{2} \right) d^2 + \frac{d}{4} - \frac{1}{16} \right). \tag{20}$$

For the derivation of the output current in DCM1 it is assumed that the rectifier current does not reach zero during interval II. However, reducing the duty cycle in DCM1 also reduces the duration T_{III}, until interval III vanishes. With the assumed output voltage range, requiring that the rectifier current rises only when the full-level rectifier no-load voltage applies, and by requiring $T_{\mathrm{III}} > 0$, the conditions for DCM1,

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} < d < \frac{1}{2} \text{ and } \frac{nU_{\mathrm{i}}}{2} < U_{\mathrm{o}} < nU_{\mathrm{i}}, \tag{21}$$

are obtained.

2) Discontinuous Conduction Mode 2

If the duty cycle at high output voltage ($U_{\mathrm{o}} > \frac{nU_{\mathrm{i}}}{2}$) is reduced below the minimum value for DCM1 the positive rectifier current half-cycle reaches zero already before the second no-load rectifier voltage falling edge. The rectifier side waveforms for this situation, DCM2, are shown in Fig. 12(b) for working point B of Fig. 14. As in DCM1, the positive rectifier current half-cycle begins with the last no-load rectifier voltage rising

edge. During the first conduction interval the rectifier current rises for

$$T_{\mathrm{I}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{22}$$

After the first rectifier no-load voltage falling edge the current decreases until it reaches zero. The duration of this second conduction interval is obtained by setting the voltage time products of rectifier no-load voltage and rectifier voltage during the two conduction intervals equal, i.e.

$$nU_{\mathrm{i}} T_{\mathrm{I}} + \frac{nU_{\mathrm{i}}}{2} T_{\mathrm{II}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}}) \Rightarrow T_{\mathrm{II}}, \tag{23}$$

yielding the duration of conduction interval II,

$$T_{\mathrm{II}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(2d - \frac{1}{2}\right) T_{\mathrm{s}}. \tag{24}$$

With expressions (22) and (24) the average current transferred to the output in DCM2,

$$I_{\mathrm{o,dcm2}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2U_{\mathrm{o}} - nU_{\mathrm{i}}} \left(d - \frac{1}{4}\right)^2, \tag{25}$$

is obtained. Reducing the duty cycle to values less than $\frac{1}{4}$ while $U_{\mathrm{o}} > \frac{n}{2} U_{\mathrm{i}}$ results in a no-load rectifier voltage waveform not reaching the full-level (compare Fig. 9). Therefore, no interval is left with the rectifier current increasing and thus no power is transferred to the output. The conditions for DCM2 are consequently specified as

$$\frac{1}{4} < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} \text{ and } \frac{nU_{\mathrm{i}}}{2} < U_{\mathrm{o}} < nU_{\mathrm{i}} \tag{26}$$

3) Discontinuous Conduction Mode 3

With low values of both output voltage and duty cycle as in operating point C in Fig. 14, DCM3 occurs. The characteristic waveforms for operating point C are shown in Fig. 12(c). The rectifier no-load voltage consists of two pulses with same width and same polarity followed by two of opposite polarity. Since the durations of all pulses are the same and also the durations of all four zero intervals of the rectifier no-load voltage are equal; assuming that the current is discontinuous means that there are four symmetric rectifier current pulses separated by four current zero intervals. One such triangular current pulse is described by

$$T_{\mathrm{I}} = dT_{\mathrm{s}} \text{ and } \Delta i_{\mathrm{r}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{27}$$

Requiring equal voltage-time products of rectifier voltage and rectifier no-load voltage during the current pulse,

$$\frac{nU_{\mathrm{i}}}{2} T_{\mathrm{I}} = U_{\mathrm{o}}(T_{\mathrm{I}} + T_{\mathrm{II}}) \Rightarrow T_{\mathrm{II}}, \tag{28}$$

yields the duration of the current decrease during interval II,

$$T_{\mathrm{II}} = \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} - 1\right) dT_{\mathrm{s}}. \tag{29}$$

Multiplying four times the charge transferred during one such pulse to the output with the switching frequency leads to the average current transferred to the output in DCM3,

$$I_{\mathrm{o,dcm3}} = \frac{nU_{\mathrm{i}}}{2f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \left(\frac{nU_{\mathrm{i}}}{2U_{\mathrm{o}}} - 1\right) d^2. \tag{30}$$

Two conditions have to be fulfilled for DCM3 to occur. First, for the considered shape of the rectifier no-load voltage, the output voltage must be lower than half the input voltage reflected to the secondary side. Second, the duty cycle must be small enough such that the current is actually decreasing to zero during the rectifier no-load voltage zero interval, i.e. $T_{\mathrm{I}} + T_{\mathrm{II}} < \frac{T_{\mathrm{s}}}{4}$. Therefore, the conditions for DCM3 are

$$0 < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{31}$$

B. Continuous Conduction Modes

1) Continuous Conduction Mode 1

A high duty cycle value together with low output voltage as in working point D indicated in Fig. 14 results in continuous current conduction, i.e. CCM. The waveforms of rectifier side voltages and current for this working point are shown in Fig. 13(a). The positive current half-cycle consists of two rising current intervals (T_{I}, T_{II}) followed by three falling current intervals (T_{III}, T_{IV}, T_{V}). While the durations of intervals T_{II}, T_{III}, T_{IV} are defined by the inverter duty cycle, the durations of the first and the last interval are determined by the current zero-crossings. The voltage time products of rectifier no-load voltage and rectifier voltage between two current zero-crossings have to be equal. Assuming that the rising edge current zero crossing is located between the last rectifier no-load voltage rising edge and the first rectifier no-load voltage falling edge this condition can be expressed as

$$nU_{\mathrm{i}} \left(T_{\mathrm{I}} - \left(d - \frac{1}{4}\right) \frac{T_{\mathrm{s}}}{2}\right) = U_{\mathrm{o}} \frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}, \tag{32}$$

yielding T_{I}. During interval I the full rectifier no-load voltage level is applied and the resulting rectifier current increase is described by

$$T_{\mathrm{I}} = \left(\frac{d - \frac{1}{4}}{2} + \frac{U_{\mathrm{o}}}{4nU_{\mathrm{i}}}\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{i,I}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{33}$$

The following interval durations are all directly derived from the inverter duty cycle (compare Fig. 9). For interval II only half of the maximum level of the rectifier no-load voltage applies, thus the rectifier current rises slower described by

$$T_{\mathrm{II}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{34}$$

During the third interval the rectifier no-load voltage is zero

and the rectifier current is thus changing during

$$T_{\mathrm{III}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,III}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \quad (35)$$

During the fourth interval the rectifier current decreases faster with the rectifier no-load voltage now taking its half negative level.

$$T_{\mathrm{IV}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,IV}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{IV}} \quad (36)$$

Finally, during interval V the negative full-level of the rectifier no-load voltage drives the rectifier current back to zero for

$$T_{\mathrm{V}} = \left(\frac{d - \frac{1}{4}}{2} - \frac{U_{\mathrm{o}}}{4nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}}. \quad (37)$$

Using (33)-(37) the charge transferred to the output during one current half-cycle is calculated. Multiplied with twice the switching frequency, the average current transferred to the output in CCM1,

$$I_{\mathrm{o,ccm1}} = \frac{nU_{\mathrm{i}}}{4f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}}\left(d - d^2 - \frac{1}{16} - \left(\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right)^2\right), \quad (38)$$

is obtained. By reducing the duty cycle in CCM1, according to (37), the duration of interval V is also reduced, until the current-zero crossings coincide with the last rising- and falling edges of the rectifier no-load voltage. For lower values of duty cycle, the assumption of the positive slope current zero-crossing being located between the last rising and first falling edge of the rectifier no-load voltage is no longer true. Setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for CCM1, which reaches the maximum possible value of $d = 0.5$ at $U_{\mathrm{o}} = \frac{nU_i}{2}$. Therefore, also the maximum output voltage for CCM1 results from $T_{\mathrm{V}} > 0$ and the conditions for CCM1 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} < d < \frac{1}{2} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \quad (39)$$

2) Continuous Conduction Mode 2

Reducing the duty cycle to values lower than the minimum for CCM1 (39) results in rectifier voltage and current waveforms as shown in Fig. 13(b) simulated for working point E in Fig. 14. In this CCM2 the rectifier no-load voltage, same as in DCM1, utilizes all five levels, i.e. $d > 0.25$, but the positive slope current zero-crossing is located between the third and the fourth (last) rectifier no-load voltage rising edge. Each current half-cycle can be partitioned into five conduction intervals. The begin of the first interval, i.e. the time of the positive slope current zero-crossing, is located such that the voltage time product of the rectifier no-load voltage equals the voltage product of the rectifier voltage during the positive rectifier current half-cycle, i.e.

$$(T_{\mathrm{I}} + T_{\mathrm{II}}) nU_{\mathrm{i}} = U_{\mathrm{o}} \frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}, \quad (40)$$

yields the duration T_{I} of the first interval. During that time the rectifier no-load voltage is at its half-level and the rectifier current is described by

$$T_{\mathrm{I}} = \left(\frac{1}{4} + \frac{U_{\mathrm{o}}}{2U_{\mathrm{i}}} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \quad (41)$$

The duration of the following intervals is determined solely by the edges of the rectifier no-load voltage, i.e. by the inverter duty cycle. During interval II, the rectifier no-load voltage full-level applies and the rectifier current rises during

$$T_{\mathrm{II}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,II}} = \frac{nU_{\mathrm{i}} - U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \quad (42)$$

During interval III, the rectifier current continues to rise but the rectifier no-load voltage is back at its half-level. The interval is thus described by

$$T_{\mathrm{III}} = \left(\frac{1}{2} - d\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,III}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \quad (43)$$

During interval IV the rectifier no-load voltage is zero and the rectifier current decreases for

$$T_{\mathrm{IV}} = \left(d - \frac{1}{4}\right) T_{\mathrm{s}} \text{ by } \Delta i_{\mathrm{r,IV}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{IV}}. \quad (44)$$

Finally, during interval V the negative half-level of the rectifier no-load voltage applies and the current decreases to zero,

$$T_{\mathrm{V}} = \left(\frac{1}{4} - \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right) T_{\mathrm{s}}, \ \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}}. \quad (45)$$

Combining (41)-(45) allows to calculate the charge transferred to the output during one rectifier current half cycle, multiplied with twice the switching frequency yielding the average current transferred to the output in CCM2

$$I_{\mathrm{o,ccm2}} = \frac{nU_{\mathrm{i}}}{8f_{\mathrm{s}}L_{\sigma\mathrm{s,tot}}}\left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \quad (46)$$

The region of CCM2 is limited by three conditions. First, (45) shows that with increasing output voltage the duration of interval V decreases until it reaches zero at $U_{\mathrm{o}} = \frac{n}{2} U_{\mathrm{i}}$. This limit marks the boundary to DCM1. Second, for the rectifier no-load voltage to utilize all five levels it is required (compare Fig. 9) that $d_{\mathrm{ccm2}} > \frac{1}{4}$. Finally, with increasing duty cycle the duration of interval I (41) approaches zero. Requiring $T_{\mathrm{I}} > 0$ places an upper bound on the duty cycle identical with the minimum duty cycle for CCM1 (39). The conditions for CCM2 are summarized as

$$\frac{1}{4} < d < \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} + \frac{1}{4} \text{ and } 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \quad (47)$$

3) Continuous Conduction Mode 3

With duty cycle and output voltage as in working point F in Fig. 14 the CCM3 is entered. The corresponding waveforms of rectifier side current and voltages are shown in Fig. 13(c). The rectifier no-load voltage, as in DCM3, consists of two half-level

voltage pulses with same polarity followed by two pulses of opposite polarity. As in CCM1 and CCM2 five conduction intervals are identified for one rectifier current half-cycle. The first interval starts with the positive slope current zero-crossing, located between rising and falling edge of the first positive rectifier no-load voltage pulse, and ends with the falling edge of the first rectifier no-load voltage pulse. The duration of the first interval is determined by the condition of equal voltage time products of rectifier-no load voltage and rectifier voltage between two rectifier current zero-crossings, i.e.

$$T_{\mathrm{I}} n U_{\mathrm{i}} = U_{\mathrm{o}} \frac{T_{\mathrm{s}}}{2} \Rightarrow T_{\mathrm{I}}. \tag{48}$$

During the first interval the positive half-level of the rectifier no-load voltage applies and the rectifier current changes during

$$T_{\mathrm{I}} = \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,I}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{I}}. \tag{49}$$

During the zero interval between the two positive pulses of the rectifier no-load voltage, interval II, the rectifier current decreases for

$$T_{\mathrm{II}} = \left(\frac{1}{4} - d\right) T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,II}} = -\frac{U_{\mathrm{o}}}{2L_{\sigma\mathrm{s,tot}}} T_{\mathrm{II}}. \tag{50}$$

During the following interval III, the current rises at the same rate as in interval I for

$$T_{\mathrm{III}} = dT_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,III}} = \frac{nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{III}}. \tag{51}$$

The duration and the rectifier current change rate of interval IV are identical as in interval II, i.e.

$$T_{\mathrm{IV}} = T_{\mathrm{II}}, \ \Delta i_{\mathrm{r,IV}} = \Delta i_{\mathrm{r,II}}. \tag{52}$$

During interval V the rectifier current, while the negative half-level of the rectifier no-load voltage applies, decreases for

$$T_{\mathrm{V}} = \left(d - \frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}}\right) T_{\mathrm{s}} \ \text{ by } \ \Delta i_{\mathrm{r,V}} = \frac{-nU_{\mathrm{i}} - 2U_{\mathrm{o}}}{4L_{\sigma\mathrm{s,tot}}} T_{\mathrm{V}} \tag{53}$$

until it reaches zero. Using expressions (49)-(53) the charge transferred to the output during one positive current half-cycle is calculated and multiplied with twice the switching frequency to obtain the average current transferred to the output in CCM3

$$I_{\mathrm{o,ccm3}} = \frac{nU_{\mathrm{i}}}{8 f_{\mathrm{s}} L_{\sigma\mathrm{s,tot}}} \left(d - \left(\frac{U_{\mathrm{o}}}{nU_{\mathrm{i}}}\right)^2\right). \tag{54}$$

Surprisingly, identical expressions for the output current in CCM2 (46) and CCM3 are obtained. Therefore, the boundary $d = 0.25$ between CCM2 and CCM3 could also be discarded. However, additionally a second condition limits the region of CCM3, since reducing the duty cycle also reduces the duration of interval V (53) until it vanishes completely. If the duty cycle is reduced further the current reaches zero before the first negative pulse of the rectifier no-load voltage begins and DCM3 is entered (compare Fig. 12(c)). Therefore setting $T_{\mathrm{V}} > 0$ yields the minimum duty cycle for operation in the region of CCM3, which coincides with the maximum duty cycle for operation in DCM3. Therefore, the conditions for CCM3 can be summarized as

$$\frac{U_{\mathrm{o}}}{2nU_{\mathrm{i}}} < d < \frac{1}{4} \ \text{ and } \ 0 < U_{\mathrm{o}} < \frac{nU_{\mathrm{i}}}{2}. \tag{55}$$

References

[1] F.H. Attix, "X-ray production and quality," in *Introduction to Radiological Physics and Radiation Dosimetry,* Weinheim, Germany: WILEY-VCH, 2004, ch. 9, sec. II-B, pp. 210.

[2] R. Behling, "Diagnostic x-ray sources from the inside," in *Modern Diagnostic X-Ray Sources,* Boca Raton, USA: CRC Press, 2016, ch. 6, sec. 2.2, pp. 233-269.

[3] M. Hernanz-Schulman, M. J. Goske, I. H. Bercha, and K. J. Strauss, "Pause and pulse: Ten steps that help manage radiation dose during pediatric fluoroscopy," *American Journal of Roentgenology*, vol. 197, no. 2, pp. 475-481, 2011.

[4] A. Pokryvailo, C. Carp, and C. Scapellati, "A 100 kW high voltage power supply for dual energy computer tomography applications," in *Proc. of IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, June 2014, pp. 115-118.

[5] B. Li, "Dual-energy CT with fast-kVp switching and its applications in orthopedics," *OMICS Journal of Radiology*, vol. 2, no. 6, pp. 1-8, 2013.

[6] N. Kaji, H. Niwa, J. Suda, and T. Kimoto, "Ultrahigh-voltage sic pin diodes with improved forward characteristics," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 374-381, 2015.

[7] H. Niwa, J. Suda, and T. Kimoto, "Ultrahigh-voltage sic mps diodes with hybrid unipolar/bipolar operation," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 874-881, 2017.

[8] L. Katzir and D. Shmilovitz, "A split-source multisection high-voltage power supply for x-ray," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 373-381, 2016.

[9] M. Leibl, J. W. Kolar, and J. Deuringer, "New current control scheme for the vienna rectifier in discontinuous conduction mode," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE) 2014*, Sep 2014, pp. 1240-1247.

[10] P. Ranstad and H. P. Nee, "On the distribution of ac and dc winding capacitances in high-frequency power transformers with rectifier loads," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 5, pp. 1789-1798, May 2011.

[11] A. Averberg and A. Mertens, "Characteristics of the single active bridge converter with voltage doubler," in *Power Electronics and Motion Control Conference*, *2008. EPE-PEMC 2008. 13th*. IEEE, 2008, pp. 213-220.

[12] R. U. Lenke, J. Hu, and R. W. De Doncker, "Unified steady-state description of phase-shift-controlled zvs-operated series-resonant and non-resonant single-active-bridge converters," in *Proc. of IEEE Energy Conversion Congress and Exposition, (ECCE),* 2009, pp. 796-803.

[13] F. Jauch and J. Biela, "Combined phase-shift and frequency modulation of a dual-active-bridge ac–dc converter with pfc," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8387-8397, 2016.

[14] F. Krismer and J. W. Kolar, "Closed form solution for minimum conduction loss modulation of dab converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 174-188, Jan 2012.

[15] F. da Silveira Cavalcante and J. W. Kolar, "Design of a 5 kw high output voltage series-parallel resonant dc-dc converter," in *Proc. of IEEE 34th Annual Power Electronics Specialist Conference (PESC)*, vol. 4, 2003, pp. 1807-1814.

[16] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE),* Sept 2015, pp. 5021-5029.

[17] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of llc resonant converters for led pwm dimming," *IEEE Transactions on Power Electronics,* vol. 29, no. 2, pp. 979-987, 2014.

[18] H. Wu, K. Sun, L. Zhu, and Y. Xing, "An interleaved half-bridge

three-port converter with enhanced power transfer capability using three-leg rectifier for renewable energy applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 606-616, 2016.

[19] H. Wu, X. Zhan, and Y. Xing, "Interleaved llc (illc) resonant converter with hybrid rectifier and variable-frequency plus phase-shift (vfpps) control for wide output voltage range applications," *IEEE Transactions on Power Electronics,* vol. 32, no. 6, pp. 4246-4257, 2017.

[20] Infineon Technologies AG, "IKZ50N65NH5 - 650V duopack igbt and diode high speed series fifth generation," 10 2014, rev. 2.1.

[21] Infineon Technologies AG, "IDW40E65D2 - Emitter Controlled Diode," 12 2013, rev. 2.1.

Michael Leibl received the B.Sc. from the Vienna University of Technology, Austria, in 2010 and the M.Sc. from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2012 – both in electrical engineering. Until 2017 he was with the Power Electronic Systems Laboratory working on his Ph.D. thesis on three-phase rectifiers and high voltage supplies for X-ray systems, covering his main research interests which include optimized design of inductive components, in particular modelling high frequency winding loss, high power three-phase PFC rectifiers and isolated DC-DC converters. He is currently a Predevelopment Engineer with Brusa Elektronik AG, Switzerland.

Johann W. Kolar received his Ph.D. degree (summa cum laude) from the Vienna University of Technology, Austria. He is currently a Full Professor and the Head of the Power Electronic Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has published over 750 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 140 patents. He has presented over 20 educational seminars at leading international conferences, has served as IEEE PELS Distinguished Lecturer from 2012 through 2016, and has received 25 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Power Electronics Society R. David Middlebrook Achievement Award, the 2014 SEMIKRON Innovation Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award, and the ETH Zurich Golden Owl Award for excellence in teaching. He has initiated and/or is the founder of 4 ETH Spin-off companies. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, Solid-State Transformers, Power Supplies on Chip, as well as ultra-high speed and ultra-light weight drives, bearingless motors, and energy harvesting.

Josef Deuringer received the Dipl.-Ing. (M.Sc.) degree in electrical engineering from the Technical University Munich, Munich, Germany, in 1993 and the Dr.-Ing (Ph.D.) degree in electrical engineering from Friedrich-Alexander University Erlangen-Nürnberg, Erlangen, Germany, in 1998. During his research activities he worked on high power microwave sources for laser applications. After that, he worked for Siemens AG on numerous industrial research and development projects for X-Ray tube beam control electronics and high-voltage generators with high-frequency resonant inverters. He has filed 19 patents in these areas. He is currently the Head of the Department Innovation Electronics and Control, Siemens Healthcare GmbH, business area diagnostic imaging.