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HIGH-DENSITY CAMAC AND FASTBUS CHARGE INTEGRATING ADC FOR USE AT THE LEP OPAL DETECTOR

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A fast, gated charge-integrating front-end has been designed for use in electromagnetic and hadronic calorimetry. Two circuits can be placed on a single socketed minicard thus allowing for the design of 32-channel CAMAC and 96-channel FASTBUS modules. The 15 bit dynamic range and 12 bit resolution, together with the very good linearity and stability of these units make them suitable for extensive use in the LEP OPAL detector.

Introduction

The well-known and expensive Wilkinson, or "run down", charge integrating analog to digital converter (ADC) [1] is no longer used in the design of charge digitizers for large scale High Energy Physics (HEP) experiments. Cheaper multiplexed systems [2-5], where the charge is stored in 32 or more capacitors and sequentially routed to the input of a single successive-approximation ADC, have been successfully built since 1976. Packaging density has steadily increased over the last ten years while the cost of the individual channel has been significantly reduced. The CAMAC and FASTBUS systems described below make use of conventional manufacturing techniques, i.e. discrete components laid on printed circuit boards, without impairing the packaging density and the cost. Two major advantages with respect to an integrated circuit or hybrid technique are that:

(a) the channel to channel dispersion of the digitized charge is well within 1%;

(b) the circuit can be easily manufactured.

The gated charge-integrating front end is presented in the next section; the 32 channel CAMAC and the 96 channel FASTBUS units designed for use in electromagnetic and hadronic calorimetry in the LEP OPAL detector are then described.

The charge integrating front-end

The circuit diagram given in fig. 1 is an improved version of the gated charge integrating front-end described in ref. [6]. In this design, the input offset voltage is reduced from 10 mV to 2 mV and the stability of the input amplifier is no longer critical. The circuit provides a negative current input and a positive voltage reference input. This "quasi-differential" nature of the inputs can be used for common mode rejection of the low frequency hum.

The improved input offset-voltage characteristics are obtained by equalization of the currents in the emitters of the "long-tail pair" at the input of the circuit. The two emitter followers in the feedback loop of the virtual ground input provide for the necessary voltage shift between this input and the collector of the CA3102E. At rest, the GATE is "closed" and the input current is drawn from a dedicated +8 V terminal through an SD215DE MOS-FET switch. Simultaneously, the 620 pF capacitor is bypassed through the CLEAR MOS-FET. This CLEAR level is reset to a "hold" level 20 ns before the GATE opens. The input current is then drawn from the "cold" + 8 V terminal through the integrating capacitor (620 pF, 1%) for the duration of the GATE pulse. The integrated charge is held until the next CLEAR, and a JFET-input buffer (TL 082 ACP) is used to drive the output.

When used as a current integrator, the main characteristics are:

- Sensitivity: 1.6 mV/pC (maximum output : 1.5 V).
- Gate width: 50 ns to 2000 ns.
- Noise (r.m.s.): 25 FC (600 ns gate).
- Maximum input slew rate: 2 mA/ns.
- Fast clear time: 300 ns for less than 300 µV residual at the output.
- Output settling time: 1000 ns.

When used as a voltage processing circuit, all characteristics are preserved except the slew rate which drops to 0.6 mA/ns.

Two channels can be mounted on a 20 mm x 50 mm socketed minicard as shown in fig. 2.

This minicard can be used in a variety of applications ranging from analog trigger circuits to high-performance digitizers. The manufacturing cost of one channel is less than 10 $ and 95% of the circuits have been found to pass a "Go/no-Go" test at the end of the production line.

The integrating capacitor may be selected to be between 100 pF and 620 pF thus allowing for different sensitivities.

The CIADC and CIAFB high-density modules

The outputs of 32 (or 48) front-ends can be multiplexed and simultaneously fed into:

(a) a conventional 12-bit ADC,

and

(b) a x8 amplifier followed by another 12-bit ADC thus allowing for measurements over a 15-bit dynamic range.

Two highly linear digitizers have been designed. The first one is the 32 channel CAMAC unit CIADC shown in fig. 3, the other is the 96 channel FASTBUS CIAFB shown in fig. 4. Both designs are linear within ± 1 count over the whole dynamic range and they have a 1.0 ms conversion time.

The CIADC CAMAC unit

The 32 channel single width module responds to the following CAMAC commands:

NF(2)A(0)	Read nth data word, move to (n + 1)th. Clear LAM at 65th command.
NF(8)A(0)	Test LAM.
C+Z+NF(9)A(0)	Clear module (LAM + charge int. front-ends). Set read to channel 0.
NF(10)A(0)	Test and clear LAM.
LAM	LAM is set when conversion is finished, i.e. ~ 1.0 ms after the GATE. The 65th read command makes LAM = $\overline{\text{LAM}}$.

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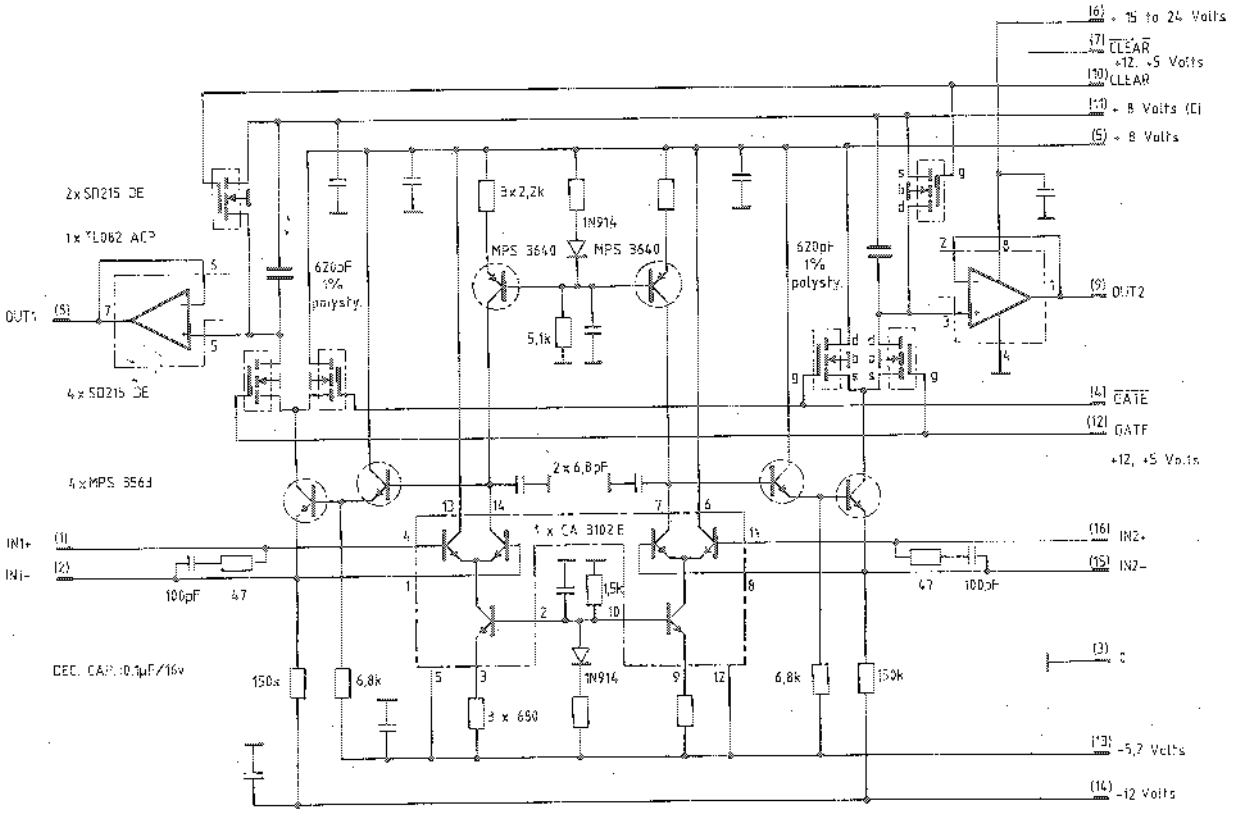

Fig. 1 Schematic of the dual-channel front-end. The input current is integrated by the 620 pF capacitor.

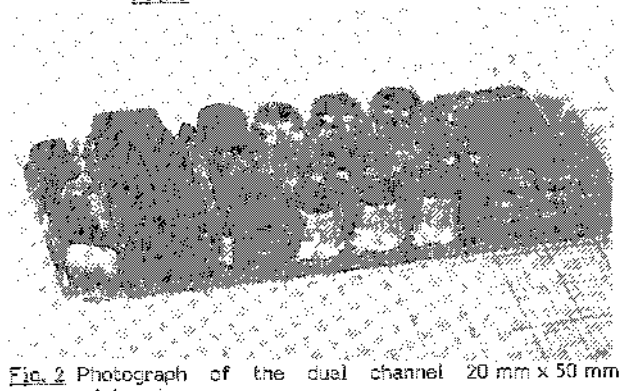

Fig. 2 Photograph of the dual channel 20 mm x 50 mm minicard.

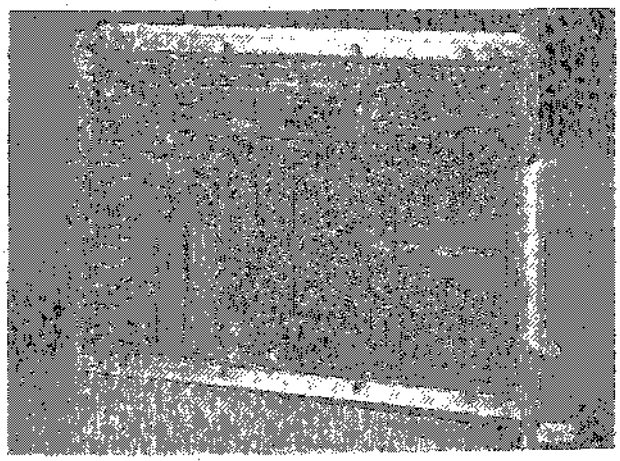

Fig. 3 Side view of the 32-channel CIADC CAMAC module.

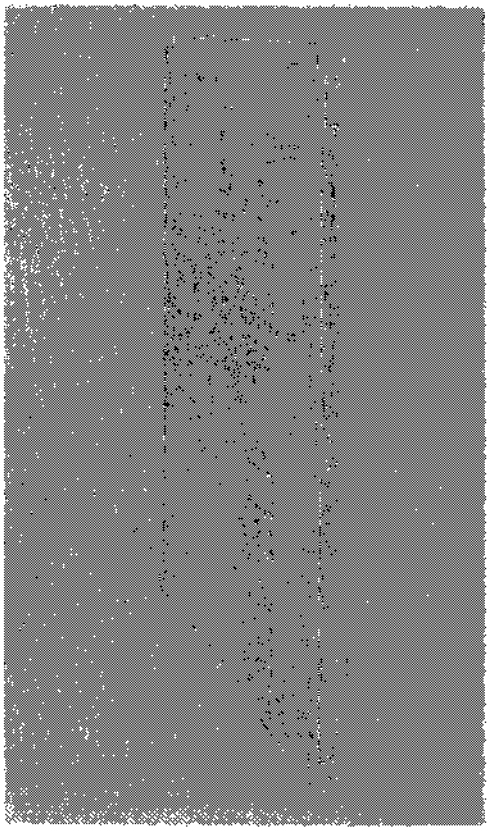

Fig. 4 Photograph of the 96 channel CIAFB FASTBUS module.

The channel-to-data assignments are given below:

- 32 channels numbered 0 to 31 (n), internal address
  data "high" pulse 0 ... 2n ... 62
  data "low" pulse 1 ... 2n + 1 ... 63

- For a FORTRAN ARRAY DATA (64)
  channel n High DATA (2n + 1)
  Low DATA (2n + 2)

Unlike other systems, this CAMAC unit is self contained and can be used in small set-ups without ancillary modules. However, the CAMAC commands have been limited to the mandatory minimum in order to accommodate a maximum number of channels per module. Two analog trigger sums of groups of 16 channels are derived from the outputs of the minicards and fed to two coaxial sockets on the rear panel of the module.

The performance of this unit is identical to that of the FASTBUS module given in the following sections.

The CIAFB 96 channel FASTBUS module

As a result of the very good sample-and-hold characteristics of the front-end, more than 32 channels can be multiplexed and fed to a single digitizer (at the expense of a longer conversion time per module!).

The side view of the FASTBUS unit in fig. 5 shows that the module is divided into two groups of 48 channels. The space used by the successive approximation ADCs is reduced with respect to that in the CAMAC module thus leaving 25% of the mother-board for:

(a) the FASTBUS slave coupler,
(b) the ancillary electronics.

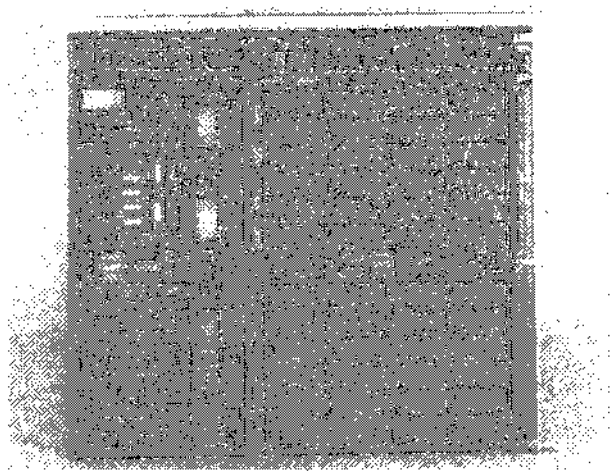

Fig. 5 Side view of the FASTBUS module showing the two groups of 24 minicards. The extra pair of channels in the centre of the mother board is used as a reference to compensate for possible drifts.

The FASTBUS coupler is the Programmable Array Logic (PAL) based circuit described in ref. [7] and successfully used since 1985 in another design [8].

Analog sums of 12 consecutive channels (current sources) are derived from the output of the front-ends. Their channel-to-channel dispersion is less than 1% r.m.s. and the offset is programmable. Therefore, they can readily be used for trigger purposes.

The ancillary electronics includes two test pulsers and conversion can be delayed by means of a programmable timer thus allowing for fast clear of the charge stored in the front ends.

The FASTBUS commands to the CIAFB are given below:

PRIMARY ADDRESSING

The module responds to geographical addressing, and broadcast addressing.

SECONDARY ADDRESSING

CSR SPACE

CSR#0 is the only control register, the bit assignments together with their read R, or write W features are given below.

<31:16>	Module identifier: 683C	R
<31>	Clear the module	W
<30>	Ditto	W
<6>	Enable front panel gate	W
<22>	Disable front panel gate	W
<6>	Gate status	R
<9>	Enable test mode	W
<24>	Disable test mode	W
<8>	Test mode status	R
<7>	Trigger test gate	W

DATA SPACE

Valid secondary addresses are 0:103 and 192:203, the first group is read only whereas the second is read and written.

The 96 channels are at secondary addresses 0:95.

The 8 gated sums of 12 channels are at secondary addresses 96:103.

The 8 offset control registers (8 bit wide) of the gated sums are at secondary addresses 192:199.

The wait-before-conversion time (8 bit wide) is at secondary address 200.

The amplitude of the test pulse (8 bit wide) is at secondary address 201 for channels 0:47 and at secondary address 202 for channels 48:95.

Secondary address 203 exists but it is not used.

The data are right-justified and bits <15:12> and <31:28> are always off; other unused bit positions are left undefined for data with less than 12 bit of information. When the module is wired for 15 bit dynamic range, small charges are digitized in bits <27:16>.

The power dissipation is less than 400 mW per channel and the manufacturing cost does not exceed $ 25 in large quantities (> 1000 ch.).

Performance results

So far, 500 channels of the CAMAC module and 2500 channels of the FASTBUS unit have been successfully built and tested.

Detailed lab tests were cross-checked by various users in different environments. The very good performance of both modules is shown by the results in figs 6 to 10.

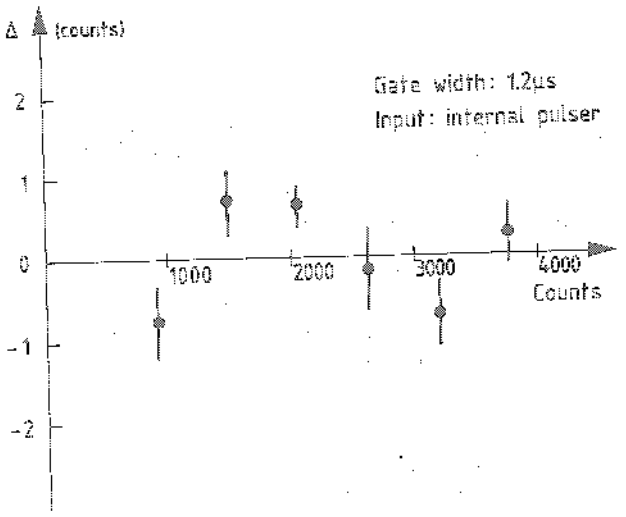

Fig. 6 Deviation from a straight line least square fit showing the ± 1 count integral linearity (15 bit range).

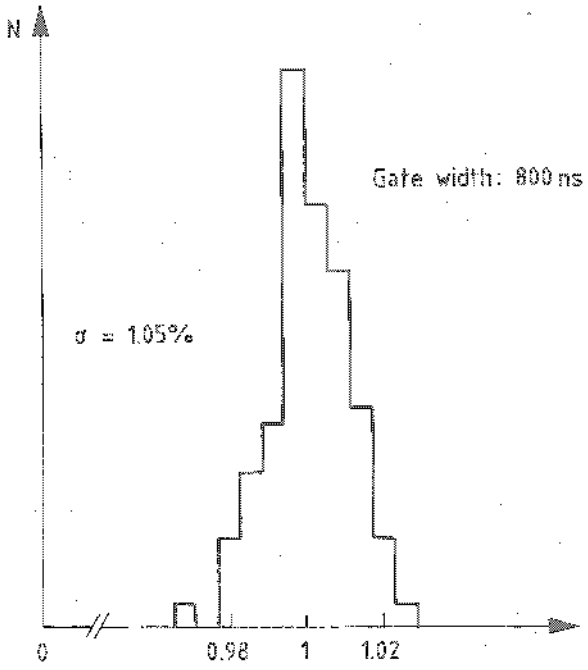

Fig. 8 Normalized channel-to-channel gain spread (15 bit range).

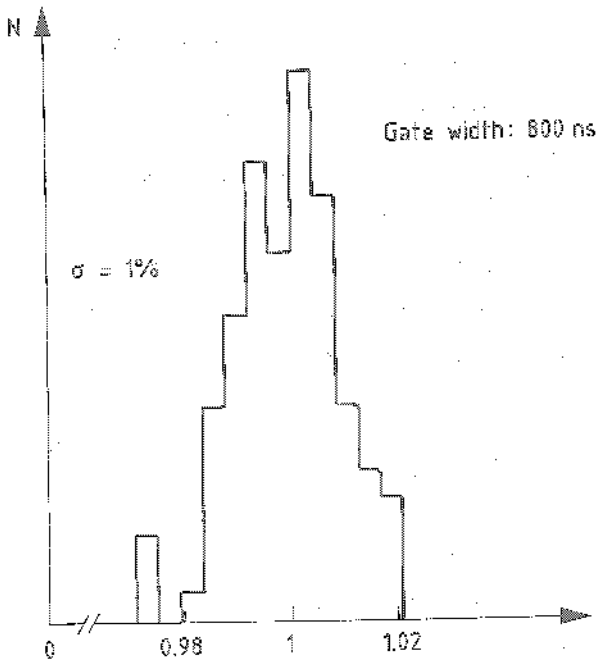

Fig. 7 Normalized channel-to-channel gain spread (12 bit range).

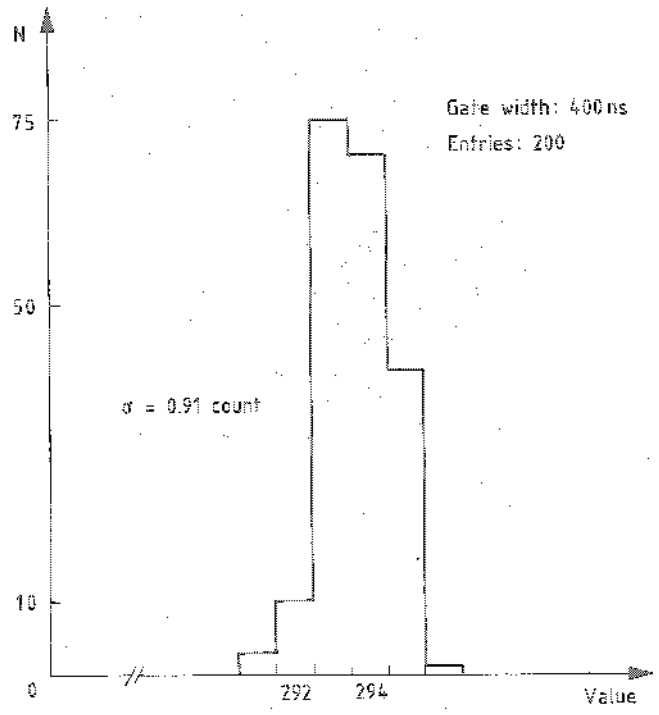

Fig. 9 Typical pedestal distribution for the 15-bit range.

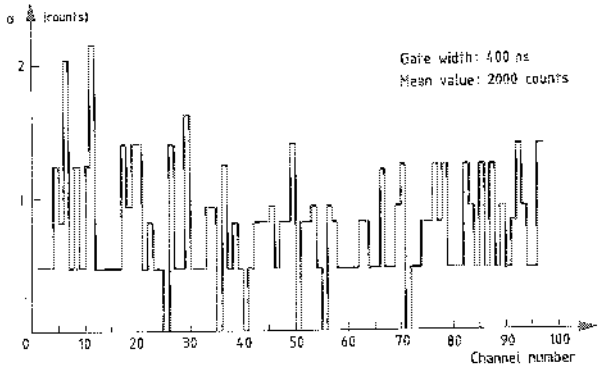

Fig. 10 Measurement spread as a function of the channel number.

The integral linearity is well within ± 1 count over the full dynamic range (fig. 6) and the channel to channel 1% (r.m.s.) gain-spread is confirmed by the two histograms in figs 7 and 8.

A typical pedestal distribution for the 15-bit range is shown in fig. 9 and the spread over the 96 channels of a module in fig. 10.

These results confirm that high sensitivity front-ends can be successfully installed in a FASTBUS environment.

Examples of use at the LEP OPAL detector

The LEP OPAL Collaboration has recently standardized the CIADC and CIAFB units for use in electromagnetic and hadronic calorimetry thus simplifying the operation of this sizeable detector (33 K channels).

An illustration of the detector is shown in fig. 11. It will be installed on the CERN LEP e^+e^- collider in 1988 and should be accumulating physics data in 1989.

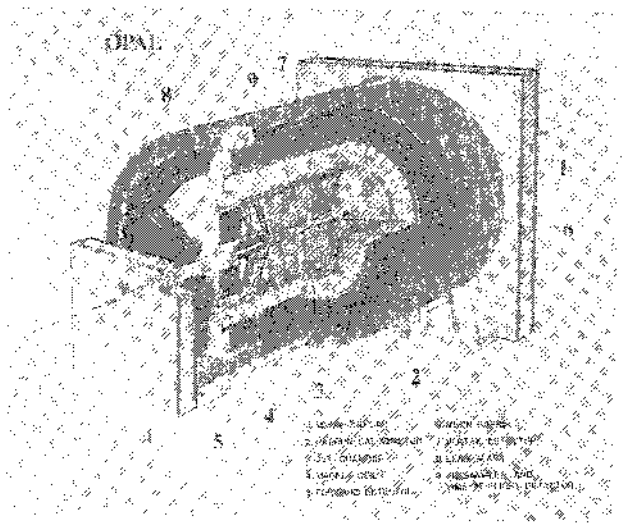

Fig. 11 The CERN LEP OPAL detector.

The CIAFB and CIADC digitizers can easily handle the variety of signals produced by the detector equipment among which one can mention:

- Conventional phototubes (time-of-flight detector).
- Meshed dynode phototubes Hamamatsu R2238 (barrel lead glass calorimeter).
- Vacuum phototriodes together with their associated amplifiers (electromagnetic end-cap calorimeter).
- Strip readout of streamer tubes (presampler and hadron calorimeter).

Signals are of either polarity and they are fed into the converters via coaxial, twisted pair or shielded twisted pair cables.

Thirteen thousand channels will be built by mid-1987 and the detectors should be fully equipped in the course of 1988.

Conclusion

This work shows that conventional techniques can be used for the design and manufacture of high-accuracy, cheap and densely packed charge digitizers. A factor of two more sensitive than other designs, the CIAFB appears to be very reliable and well matched to most HEP detectors.

Acknowledgements

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