High Dynamic Range adaptive ΔΣ-based Focal Plane Array architecture

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***Abstract*—In this paper, an Adaptive Delta-Sigma based architecture for High Dynamic Range (HDR) Focal Plane Arrays is presented. The noise shaping effect of the Delta-Sigma modulation in the low end, and the distortion noise induced in the high end of Photo-diode current were analyzed in detail. The proposed architecture can extend the DR for about $20N\log 2$ dB at the high end of Photo-diode current with an N bit Up-Down counter. At the low end, it can compensate for the larger readout noise by employing Extended Counting. The Adaptive Delta-Sigma architecture employing a 4-bit Up-Down counter achieved about 160dB in the DR, with a Peak SNR (PSNR) of 80dB at the high end. Compared to the other HDR architectures, the Adaptive Delta-Sigma based architecture provides the widest DR with the best SNR performance in the extended range.**

I. INTRODUCTION

Along with the advent of the sub-micron high-speed CMOS image sensors [1] [2] and the promise of 3D integration, the implementation of on-chip image processing algorithms, such as dynamic range extension [3], fixed pattern elimination [4], low light detection [5] and high accuracy optical flow estimation [6] became possible.

High Dynamic Range (HDR) Focal Plane Array architectures have been developed in recent years. In previous research work, several architectures have been analyzed and compared based on their Signal-to-Noise Ratio (SNR) and Dynamic Range (DR) performance [7], namely: (a) Time to Saturate; (b) Multiple Capture; (c) Asynchronous Reset with Residue Readout; (d) Synchronous Reset with Residue Readout; and (e) Delta-Sigma System with and without Extended Counting (EC).

Generally, there are two ways to extend the SNR and DR in the Readout IC (ROIC) system: (a) varying the integration time, and (b) increasing the Well Capacity [7]. In the literature, the architectures of Time to Saturate and Multiple Capture [8] [9] take advantage of the former, while the Asynchronous/Synchronous Reset with Residue Readout and Delta-Sigma System with and without Extended Counting (EC) [10]–[15] architectures employ the idea of recycling the well-capacity. However, because of the continuous shrinking of the feature size in modern process, and the boosting demand for the real time processing, the integration time may not be available to change to compensate the loss in SNR and DR. As a result, recycling the Well-Capacity becomes more desirable in HDR Imager Sensor architectures, although the Well-Capacity still limit the SNR and DR in the high end of Photo-diode current.

In this paper, an Adaptive Delta-Sigma based architecture is presented to further extend the DR with an improved SNR by varying the Well-Capacity in the system. Section II gives a brief Background of the ROIC system, and introduce the Conventional architecture as the Reference for performance comparison. Then, Adaptive Delta-Sigma based architecture is explored in detail in Section III, followed with the analysis of Extended Counting in Section IV. In Section V, the performance of different architectures is compared regarding SNR and DR, and finally a conclusion in Section VI.

II. BACKGROUND

Generally, the performance of an image sensor relies on both the Photo-detector and the Readout circuit (ROIC). The photo-detector converts incident light into Photo-diode current, which discharges the capacitor of the photo-detector linearly. Then, the voltage on the capacitor is digitized and read out by the ROIC. In the short integration time, the Photo-diode current is relatively constant, and the whole process can be viewed as a linear transformation from the incident light into readout voltage. The following discussion will focus on the ROIC aspect to improve the SNR and DR of conventional image sensors.

Besides the Dark Current, which cannot be removed by readout circuits, there are four independent noise sources:

Shot Noise: Coming from the random fluctuations of the Photo-diode current in the integration time;

$$\bar{\sigma^2_{shot}} = i_{ph}t_{int}/q \quad electron; \tag{1}$$

where i_{ph}, t_{int}, and q are the Photo-diode current, integration time, and electron charge respectively.

Reset Noise: Coming from the reset operation of the capacitor in the photo-detector, also known as KTC noise;

$$\bar{\sigma^2_{reset}} = KTC_{int}/q^2 \quad electron; \tag{2}$$

where C_{int}, K, and T are the integrating capacitor, Boltzmann constant, and Kelvin temperature respectively.

Readout Noise: Resulting mainly from the quantization of the analog-to-digital conversion in the ROIC, also known as quantization noise;

$$\bar{\sigma^2_{readout}} = C^2_{int}\Delta^2/12q^2 \quad electron; \tag{3}$$

where Δ is the step size of the quantization.

FPN Noise: Resulting from various nonlinearities in the photo-detector and the readout circuit, which is proportionate to the integration charges, and thus only taking effect in extremely wide dynamic range;

$$\bar{\sigma^2_{fpn}} = pi_{ph}t_{int}/q^2 \quad electron; \tag{4}$$

where p is the percentage estimate of the FPN noise to the integration charges.

Thus, for a conventional architecture, the SNR is given by:

$$SNR = \frac{(i_{ph}t_{int})^2}{qi_{ph}t_{int} + q^2\sigma^2_{reset} + q^2\sigma^2_{readout} + q^2\sigma^2_{fpn}} \quad i_{ph} \leq \frac{qQ_{max}}{t_{int}}; \tag{5}$$

where Q_{max} is the maximum number of electrons on the integrating capacitor, also referred to as *well capacity*.

The Reset noise can be eliminated by Correlated Double Sampling (CDS) technique, and the FPN noise can be neglected due to the relatively small dynamic range of conventional architecture. According to Equation 5, it is always preferable to have the longest integration time available. But the requirement of real time imaging makes it impossible to maintain long integration time.

$$DR = \frac{i_{max}}{i_{min}} = \frac{Q_{max}}{\sigma_{readout}}; \tag{6}$$

Equation 6 gives the DR of the conventional architecture, which is the ratio of the largest unsaturated Photo-diode current to the smallest detectable Photo-diode current.

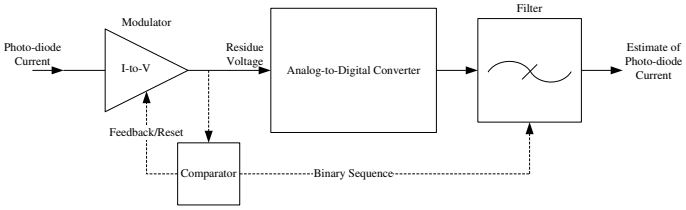

Fig. 1. General Block Scheme of Readout IC Architecture

Figure 1 shows a general block scheme of the readout circuit architecture in image sensors. The Photo-diode current is transformed into voltage through a modulator, which generates a binary sequence depending on the architecture used to evaluate the Well Capacity recycling. Then, the residue voltage on the capacitor is sampled and digitized to form a estimate of Photo-diode current combined with the binary sequence from the modulator. Generally, the modulator is implemented per pixel, while the ADC are shared in group of pixels. CDS technique can be realized by reading the output twice at $t = 0$ and $t = t_{int}$, and the filter can be optimized for different architectures.

In order to evaluate the performance of different architectures, Time-Domain models in MATLAB were built up with various circuit non-idealities taken into account. Simulations were carried out upon the same settings including the noise sources, integration time, well capacity, and etc. The Output from readout circuits was recovered by ideal filters, which means no extra noise was induced during the filtering. Finally, the SNR and DR performance of different architectures was evaluated in frequency domain by FFT with Hanning windows.

III. ADAPTIVE ΔΣ-BASED HDR ARCHITECTURE

Different from the Reset-based architectures, the ΔΣ-based architecture increases the Well Capacity by tracking the Photo-diode current with feedbacks, which makes the current charging/discharging the capacitor much smaller and thus less likely to saturate. In addition, this *Delta* operation makes performance beyond the Well Capacity limitation possible in ΔΣ-based architectures, which leads to the Adaptive ΔΣ-based architecture.

A. First Order Adaptive ΔΣ Modulator

Figure 2 gives the diagram of a first-order single-bit adaptive ΔΣ-based architecture. During each clock cycle, the output voltage of the integrator is compared with the reference voltage V_{ref} to determine the feedback voltage. Instead of fixing the feedback voltage V_{fb} at $V_{max}/2$, where $V_{max} = Q_{max}/C_{int}$, adaptive ΔΣ-based architecture uses $V_{fb} = N \times V_{max}/2$, while N depends on the magnitude of the Photo-diode current. As a result, the difference voltage is decreased correspondingly, which prevents the occurrence of saturation. Typically, this subtract operation is realized by switched capacitor circuits, and extra noise from the switches may be induced into the system. The binary sequence from the comparator is fed into an Up-Down counter, which switches between different feedback voltages. Considering the power and area constraints for per pixel realization, simple counters are employed as decimation filters to recover the estimate of Photo-diode current from binary sequences. In contrary to multi-bit ΔΣ modulators which improve the SNR with smaller quantization step, adaptive ΔΣ-based architecture improves the DR at the cost of larger quantization noise [16] [17]. A global frame reset is desirable such that the initial state of the integrator is determined, which improves SNR [18].

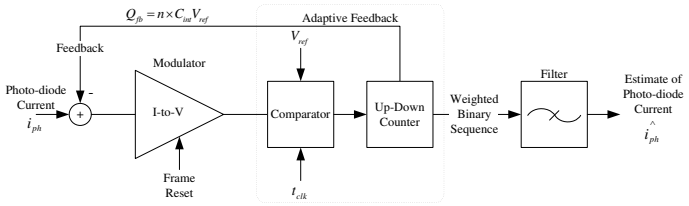

Fig. 2. Block Scheme of Adaptive ΔΣ-based Architecture without Extended Counting

1) Noise Analysis: **Distortion Noise:** For large Photo-diode current, distortion may occur during the adaptive process before the steady state. After the frame reset, the voltage on the capacitor starts to increase. If the Photo-diode current $i_{ph} > Q_{max}/t_{clk}$, where t_{clk} is the clock cycle, the voltage would not stop rising with a feedback voltage of only $V_{fb} = V_{max}/2$. As the Photo-diode current becomes larger and larger, the integrator would saturate before the adaptive process finishes, which results in distortion errors.

$$\bar{\sigma^2_{distortion}} = ((1+\zeta) \times i_{ph} t_{clk} - \zeta(1+\zeta) \times Q_{max}/2 - Q_{max})^2 \quad electron \quad if \quad i_{ph} > 3Q_{max}/2t_{clk} \tag{7}$$

where $\zeta = \lfloor i_{ph} t_{clk}/Q_{max} \rfloor$.

Equation 7 gives the distortion error for specific Photo-diode current, which increases proportionately to i_{ph}. Therefore, the SNR would saturate when the distortion error becomes dominant. As shown in Equation 8, the distortion error is proportionate to the ratio of clock cycle to integration time, leading to a tradeoff between SNR performance and power consumption.

$$\varepsilon = \frac{(1+\zeta)t_{clk}}{t_{int}} - \frac{(\zeta(1+\zeta)+2)Q_{max}}{2i_{ph}t_{int}} \propto \frac{t_{clk}}{t_{int}} \tag{8}$$

where $\zeta = \lfloor i_{ph} t_{clk}/Q_{max} \rfloor$.

Switch Noise: Because of the subtract operation as well as the switching between different feedback voltages, extra switch noise is induced upon the capacitor, which is given by:

$$\bar{\sigma^2_{switch}} \approx \eta \times \lfloor \frac{t_{int}}{t_{clk}} \rfloor \times KTC_{sub}/q^2 \quad electron; \tag{9}$$

where η is an estimate of nonzero feedback cycles in the integration time, and C_{sub} is the capacitor using for feedback subtraction.

FPN Noise: The actual gain of the integrator may drift from the desired value due to the mismatch of capacitance as well as other non-idealities like clock feed-through and charge leakage. And this error would accumulate on the capacitor until next reset.

$$\bar{\sigma^2_{fpn}} = n^2_{sub}(pC_{int}V_{fb})^2/q^2 \quad electron; \tag{10}$$

where p is the percentage estimate of the FPN noise to the feedback charges, and n_{sub} is the number of subtraction in the integration time.

Readout Noise: The quantization noise for this single-bit adaptive ΔΣ-based architecture is shown in Equation 11, assuming $V_{ref} = V_{max}/2$ for the comparator. Although a first order ΔΣ modulation can provide some attenuation, this noise is still too large for low Photo-diode current applications.

$$\bar{\sigma^2_{readout}} = Q^2_{max}/12q^2 \quad electron; \tag{11}$$

Reset Noise: Since there is no extra reset required in the integration period, the reset noise should be the same as conventional architectures.

$$\bar{\sigma^2_{reset}} = KTC_{int}/q^2 \quad electron; \tag{12}$$

Shot Noise: Again, the same as conventional architectures.

$$\bar{\sigma^2_{shot}} = i_{ph}t_{int}/q \quad electron; \tag{13}$$

2) Parameter Setting: **Dynamic Range Improvement:** With an N-bit Up-Down counter, the maximum feedback voltage can be $(2^N - 1)V_{fb}$. Thus, a steady state output of 1's string implies a Photo-diode current of $\hat{i_{ph}} = (2^N - 1)Q_{max}/2t_{int}$. In comparison with ΔΣ-based architectures, adaptive ones achieve a DR improvement given by:

$$\Delta DR(dB) = 20\log(2^N - 1) \approx 20N\log 2 \approx 6.02N; \tag{14}$$

Optimum Reference Voltage: In the high end, it is desirable to set the reference voltage $V_{ref} \leq V(max)/2$, which prevents the integrator from saturating due to full range input current. But still, the reference voltage should be as large as possible to achieve optimum DR performance. As a result, making $V_{ref} = V(max)/2$ is the best choice if the comparator offset does not influence the performance significantly.

Comparator Offset: Given that no distortion is induced, the comparator offset would not affect the performance. Assume the offset is V_{os} and $V_{ref} = V_{max}/2$, then:

$$if \ V_{os} < 0, \quad \lceil \frac{C_{int}(V_{ref} + V_{os})}{i_{ph}t_{clk}} \rceil i_{ph}t_{clk} \geq (C_{int}V_{ref} - i_{ph}t_{clk}) \tag{15}$$

$$if \ V_{os} > 0, \quad 2C_{int}V_{ref} - \lceil \frac{C_{int}(V_{ref} + V_{os})}{i_{ph}t_{clk}} \rceil i_{ph}t_{clk} \geq i_{ph}t_{clk} \tag{16}$$

Conservatively,

$$if \ V_{os} < 0, \quad V_{os} \geq -\frac{i_{ph}t_{clk}}{C_{int}} \tag{17}$$

$$if \ V_{os} > 0, \quad V_{os} \leq V_{ref} - 2\frac{i_{ph}t_{clk}}{C_{int}} \tag{18}$$

According to Equation 17 and 18, the distortion occurs at the low end of Photo-diode current if $V_{os} < 0$, and the high end if $V_{os} > 0$. As a result, the reference voltage V_{ref} should be increased to compensate the offset voltage V_{os}.

Unlike other noise sources, the comparator offset only affects the Photo-diode current within certain range. The distortion tends to repeat when $V_{os} < 0$, which makes the relatively low SNR even worse in the low end of Photo-diode current. Therefore, a positive V_{os} is preferable while compensated by both a larger V_{ref} and recycled well capacity.

3) Simulation Results: In the MATLAB Time-Domain simulation, the Photo-detector was modeled as $Q_{max} = 125000\ electron$ and $C_{int} = 50\ fF$. Thus, the Reset noise $\sigma_{reset} \approx 100\ electron$ with $K = 1.38 \times 10^{-23} J \cdot K^{-1}$ and $T = 300K$. The Switch noise and Gain FPN noise were set as $\sigma_{switch} = 120\ electron$ and $\sigma_{fpn} = 80\ electron$ respectively, while the binary comparator gave a Readout noise of $\sigma_{readout} \approx 18050\ electron$. All noise sources were modeled as white noise, including the Shot noise in the Photo-detector. The integration time is 30 ms. Given a reference voltage of $V_{ref} = Q_{max}/2C_{int}$ and a clock cycle of $t_{clk} = 1\ \mu s$, Figure 3 shows the plot of SNR versus Photo-diode current from $10^{-13}A$ to $10^{-6}A$ for an adaptive ΔΣ-based architecture with 4-bit Up-Down counter.

Due to the extremely large quantization noise in the binary comparator, the SNR is deteriorated in the low end of Photo-diode current. As the current increases, the SNR ramps up at 20dB/dec first, where Reset noise and Readout noise are dominant. Then, the Shot noise takes over, which makes the SNR increase at 10dB/dec until it saturates due to the Gain FPN noise. When the current exceeds the range of conventional ΔΣ architecture, the adaptive process begins. The SNR may drop a little at first due to the distortion error, and rise again as the error compensated by the larger current. However, noise sources other than the Shot and Distortion noise would not change any more in the adaptive process and thus make a higher SNR possible. But still, the adaptive ΔΣ-based architecture cannot provide correct conversion for a Photo-diode current larger than $(2^N - 1)Q_{max}/2C_{int}$, where N is the Up-Down counter bit, which corresponds to the sharp drop in the high end.

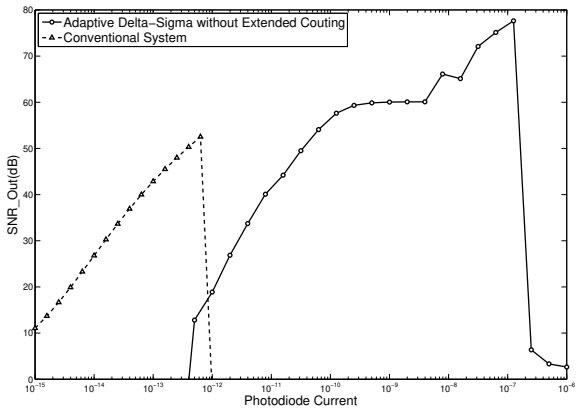

Fig. 3. SNR vs. Photodiode Current for Adaptive ΔΣ-based Architecture without Extended Counting and Conventional Architecture

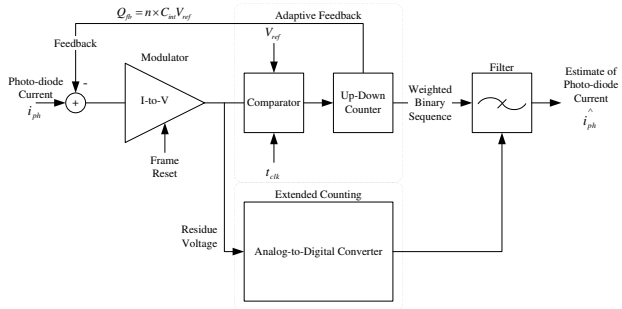

Fig. 4. Block Scheme of Adaptive ΔΣ-based Architecture with Extended Counting

B. Extended Counting

As shown in Figure 3, the adaptive ΔΣ-based architecture cannot provide similar performance in the low end of Photo-diode current as the conventional architecture. Although the quantization error is attenuated by the ΔΣ modulation, it would become too complex to realize high order modulation in order to achieve comparable performance. In addition, extra noise would be induced due to the modulator, which limits the performance in the high end. If the ADC can be shared in groups of pixels or even the whole chip, high order ΔΣ modulation may be feasible as long as the readout speed or multiplexing does not become a bottleneck.

1) Linearized Model: The block diagram of a first-order single-bit adaptive ΔΣ-based architecture with Extended Counting is given in Figure 4. Instead of discarding the residue voltage in the integrator, an extra residue ADC is employed to generate the lower bits, which are attached to the higher bits from the counter to form the final A/D conversion. As a result, the quantization noise is determined by the new residue ADC now, rather than the binary comparator in the modulator. Assuming a M-bit residue ADC is used, the quantization error becomes:

$$\sigma^{2\ \bar{}}_{readout} = Q^2_{max}/12q^2 2^{2(M-1)} \quad electron; \tag{19}$$

Therefore, the final resolution of the readout circuit is N+M-bit, where N is the string length of the counter.

2) Simulation Results: Figure 5 shows the plot of SNR versus Photo-diode current from $10^{-15}A$ to $10^{-6}A$ for both the conventional architecture and the adaptive ΔΣ-based architecture with extended counting. Same parameter settings were used in the adaptive ΔΣ-based architecture except for the Readout noise, $\sigma_{readout} \approx 35\ electron$, corresponding to a 10-bit residue ADC. For the conventional architecture, only Shot noise, Reset noise, and Readout noise were presented, and kept the same as the adaptive one. With extended counting, the DR was improved in the low end of Photo-diode current, and similar performance as the conventional architecture was achieved.

As shown in Figure 6, the adaptive ΔΣ-based architecture extends the DR in the high end of Photodiode current with an improved SNR compared with the conventional one. And the SNR tends to saturate due to the increasing distortion error with longer bits in Up-Down counters. If the Photo-diode current is relatively constant, a common counter can be used instead of an Up-Down one to reduce area and power consumption. And frame reset should be performed as long as the environment changes.

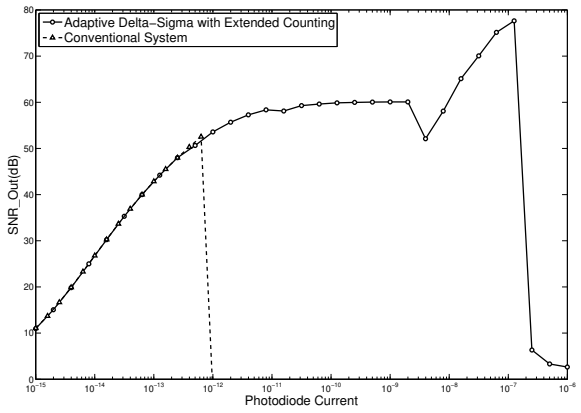

Fig. 5. SNR vs. Photodiode Current for Adaptive ΔΣ-based Architecture with Extended Counting and Conventional Architecture

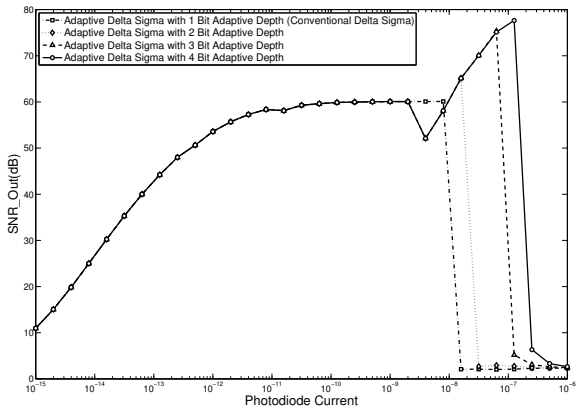

Fig. 6. SNR vs. Photodiode Current for Adaptive ΔΣ-based Architecture with Different Adaptive Depths

C. Design Considerations

SNR/DR Limitation: The SNR at the low end is limited by the Reset and Readout noise, which can be reduced by using a smaller integrating capacitor and a finer residue ADC. However, the parasitic capacitance may deteriorate the performance when it becomes significant compared with the integrating capacitor. In the high end, Switch and Gain FPN noise makes the SNR saturate before the adaptive process begins. Then, the SNR begins to increase again due to the larger equivalent well capacity, and the distortion error is induced while other noise sources are relatively constant. In order to improve the DR, higher clock frequency can be used in the ΔΣ modulator, which prevents the integrator from saturating while putting more stringent requirements on the Op-amp. As a result, the Gain FPN noise may increase due to larger settling errors and slew rate distortion.

Power Consumption: The power consumption is dominated by the integrator, and the residue ADC in use. To ensure tolerable settling error and no slew rate distortion, the gain bandwidth and bias current of the integrator need to be enlarged as the clock frequency increases. The comparator can be realized in discrete version instead of continuous ones to reduce power consumption.

Filter Design: Sophisticated filters such as triangular, zoomer [19], recursive [12], optimal [20], etc. can enhance the SNR performance at the low end of Photo-diode current, at the cost of more circuit complexity and higher power consumption [13].

IV. PERFORMANCE COMPARISON OF HDR ARCHITECTURES

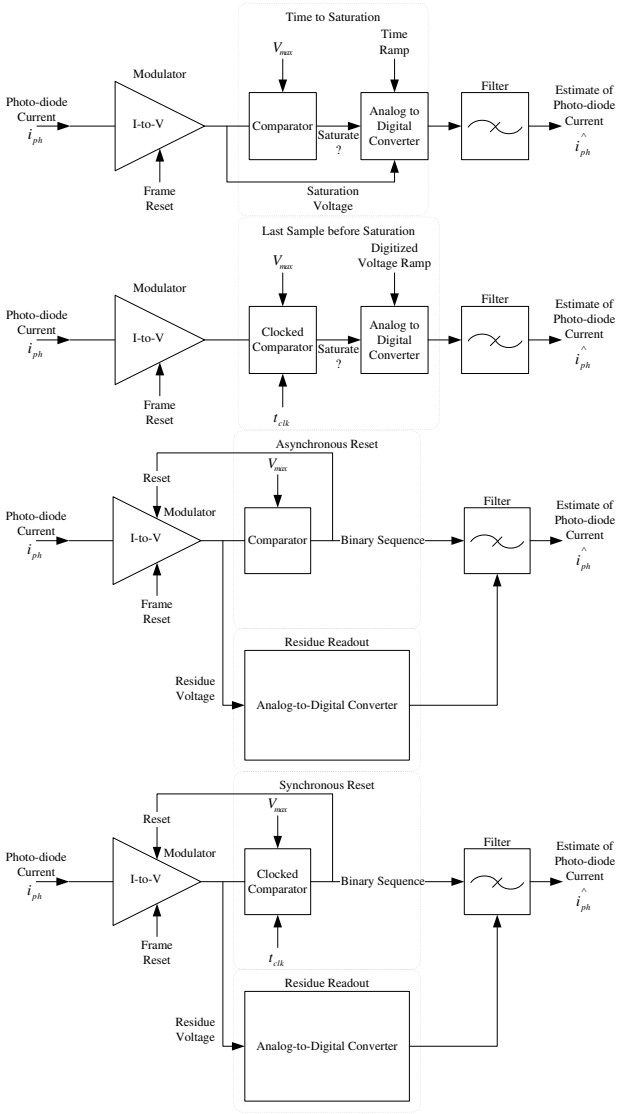

Fig. 7. Block Scheme of Different High Dynamic Range Architectures: (a) Time to Saturation; (b) Multiple Capture; (c) Asynchronous Reset with Residue Readout; (d) Synchronous Reset with Residue Readout

Figure 7 shows four different high dynamic range architectures, namely: (a) Time to Saturation; (b) Multiple Capture; (c) Asynchronous Reset with Residue Readout; and (d)

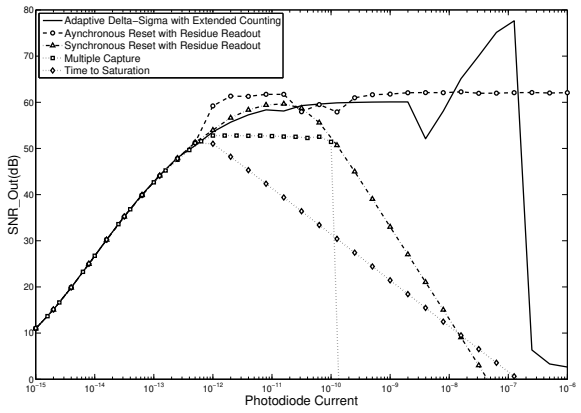

Fig. 8. SNR vs. Photodiode Current for Adaptive ΔΣ-based Architecture with 4-bit Up-Down Counter vs. (a) Time to Saturation; (b) Multiple Capture; (c) Asynchronous Reset with Residue Readout; (d) Synchronous Reset with Residue Readout

Synchronous Reset with Residue Readout. Same or equivalent parameter settings were applied for the noise sources in the simulation, and the performance comparison was illustrated in Figure 8 based on the same photo-detector. According to the figure, all the five architectures give similar performance as they degenerate into the conventional architecture in the low end of Photo-diode current. In the high end, the adaptive ΔΣ-based architecture outperforms the others with extended DR and/or higher SNR. The Asynchronous Reset with Residue Readout architecture needs continuous-time comparators to maintain the DR performance better than the adaptive architecture, which should be fast enough to reset the integrator to avoid possible saturation loss. This may result in huge design challenges for constraints of area and power consumption.

V. CONCLUSION

Adaptive ΔΣ-based architecture is presented in this paper, which extends the DR further with an improved SNR. In order to evaluate the performance of these architectures relative to each other, Time-Domain models were built up in MATLAB with various circuit non-idealities taken into account. According to simulation results, the DR is improved about $N20\log 2$ dB at the high end of Photo-diode current with an N bit Up-Down counter. At the low end, the larger readout noise is compensated by employing Extended Counting. The adaptive ΔΣ-based architecture employing a 4-bit Up-Down counter achieved about 160dB in the DR, with a Peak SNR (PSNR) of 80dB at the high end. Compared to the other architectures, the Adaptive Delta-Sigma based architecture provides the widest DR with the best SNR performance in the extended range.

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