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Review Article

High-Efficiency Crystalline Silicon Solar Cells

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The current cost distribution of a crystalline silicon PV module is clearly dominated by material costs, especially by the costs of the silicon wafer. Therefore cell designs that allow the use of thinner wafers and the increase of energy conversion efficiency are of special interest to the PV industry. This article gives an overview of the most critical issues to achieve this aim and of the recent activities at Fraunhofer ISE and other institutes.

1. INTRODUCTION

The silicon shortage in the past few years might not have been very pleasant economically for the photovoltaic industry, but it might have been beneficial from the technological point of view. If the market and the production continue to grow while the raw material is very limited and also is the highest cost share in the final product, then it is essential to increase the ratio product (i.e., output power of the fabricated cells) to raw material. In the case of silicon solar cells, this means increasing the efficiency and reducing the cell thickness with the later option being already pursued by nearly all solar cell manufacturers. Cell thicknesses in the range of 200 μm or even less are now the industrial standard which is well beyond the old standard of 330 μm. This development has been made possible by tremendous efforts in automation and process technology. In fact, the current photovoltaic industry has its own equipment suppliers who are very specialized while in former times, process equipment used was mostly modified microelectronic equipment, a branch which is specialized for extremely high accuracy and purity but not for 40 000 wafers per day.

The second task, that is, increasing the cell efficiency in the industrial production has also made great progress in the last few years. Cell structures like the A300 of Sunpower or the HIT cell of Sanyo are demonstrating the potential for industrial cells to achieve efficiencies greater than 20%.

This article gives an overview of the recent developments of industrially feasible high-efficiency technologies at Fraunhofer ISE and other institutes. It addresses the most important cell components which need further improvement to reach higher efficiencies.

Justus Liebig, a famous German chemist of the 19th century, has stated the Law of the Minimum: "The yield potential of a crop is like a barrel with staves of unequal length." This was the basis for the development of an efficient fertilizer technology. Similarly, we can use the Law of the Minimum to describe the efficiency potential of a solar cell (see Figure 1).

The capacity of the barrel (i.e., the efficiency potential of the cell) is limited by the length of the shortest stave (in this case, the surface recombination velocity at the rear surface S_{back}). (Of course this is a simplified view of a complex task, since also several loss mechanisms can limit the cell potential at the same time.) Therefore, this article addresses the shortest staves in current industrial cells as surface passivation, contacts, and bulk material. Other aspects such as the front reflectance are already well optimized and need to be tackled only in a second step.

2. SURFACE PASSIVATION

2.1. Dielectric passivation versus back surface field

All cell structures which have shown efficiencies greater than 20% feature an efficient surface passivation with dielectric layers. However, the present state-of-the-art rear surface structure of industrial silicon solar cells is a screen-printed and thermally fired Al back surface field (Al-BSF) which has two major restrictions: (i) the wafer bow due to the firing process and (ii) the lower electrical and optical properties. In particular, S_{back}, the rear surface recombination velocity, is a crucial parameter, but exhibits a great range of values found

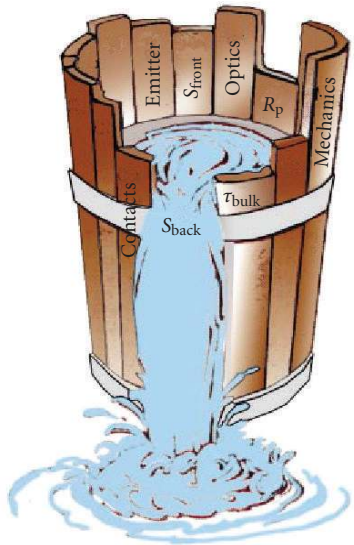


Figure 1: Liebig's law adapted to solar cells.

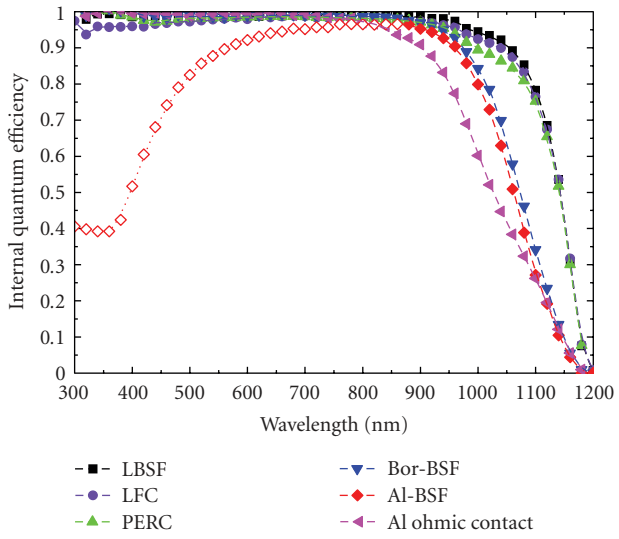


Figure 2: Internal quantum efficiency of different rear surface structures on 1 Ω cm 250 μm thick FZ-Si with a high-efficiency front structure. Note: the low internal quantum efficiency for short wavelengths (open symbols) of the Al-BSF cell is due to a degradation of front surface passivation during firing. Nevertheless, the IQE starting at 900 nm is identical to the performance of industrial cells. (For abbreviations see Table 1.)

in literature. This makes it difficult to evaluate the potential of Al-BSFs versus dielectric passivation.

Thus at Fraunhofer ISE, an experimental study of different rear surface structures combined with a high-efficiency front structure which does not limit the cell performance was performed [1]. This makes it possible to determine the surface recombination velocity S_{back} and the internal reflectivity R_{back} quite accurately [2].

Figure 2 shows the measured internal quantum efficiencies of different rear structures starting from a low-quality

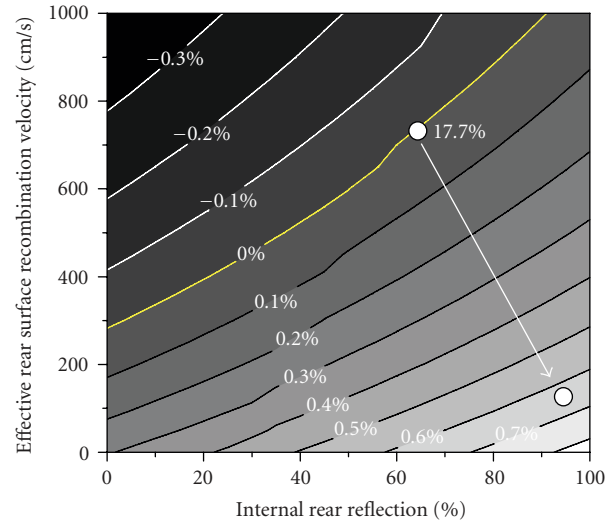


Figure 3: Change in efficiency gain due to variation of S_{back} and R_{back}. The 0% isoline refers to a 220 μm thick industrial solar cell with 60 Ω/sq emitter and Al-BSF on 1 Ω cm monocrystalline silicon with a diffusion length of 400 μm. The second point relates to the LFC parameters.

ohmic Al contact up to a PERL[3]/LBSF[4] rear surface. The effective S_{back} and R_{back} have been extracted from the IQE and reflection measurement.

Using these parameters, it is possible to determine the influence of different rear surface structures on the performance of industrial cells (see Figure 3). The benefit of a dielectric passivation will be even higher with the introduction of a higher-quality emitter and thinner cells.

2.2. Passivation mechanisms of dielectric layers

There are two different mechanisms leading to good surface passivation (for a comprehensive overview about this topic, see [7]): (i) the reduction of interface states D_{it} and (ii) field effect passivation, that is, the strong reduction of one carrier type by incorporation of fixed charges Q_f in the passivation layer. Although these mechanisms or the combination of both lead to low surface recombination velocities, the resulting $S_{eff}(\Delta n)$ curve shows different characteristics (see Figure 4). The reduction of interface states is more effectively reached for thermally grown SiO_2 layers while the field effect passivation together with a moderate reduction of D_{it} is more typical for PECVD deposited layers like SiN_x. Typical values for SiO_2 are $D_{it} = 10^{10}\,cm^{-2}eV^{-1}$ and $Q_f = 10^{10}\,cm^{-2}$ while for SiN_x, values are $D_{it} = 10^{11}\,cm^{-2}eV^{-1}$ and $Q_f = 10^{11}\,cm^{-2}$.

2.3. Deposition temperature

A critical issue for the fabrication of a dielectric passivation layer is the deposition temperature. The best solar cells so far have been passivated by thermally grown oxides [8, 9]. Thermal oxides have been optimized for MOS-technology

Table 1: Internal reflectivities (R_{back}) and rear surface recombination velocities (S_{back}) as extracted from the data in Figure 2. The dielectric passivation layer for the LBSF, LFC, and PERC structure was a thermally grown 105 thick oxide.

Structure	R_{back} [%]	S_{back} [cm/s]
LBSF (local boron back surface field) [4]	94.5	60
LFC (laser-fired contacts) [5]	95.5	110
PERC (Random pyramids, passivated emitter, and rear cell) [6]	95.0	200
Bor-BSF (boron-diffused back surface field)	71	430
Screen-printed Al-BSF (alloyed Al back surface field)	65	750
Evaporated ohmic Al contact	83	10^7

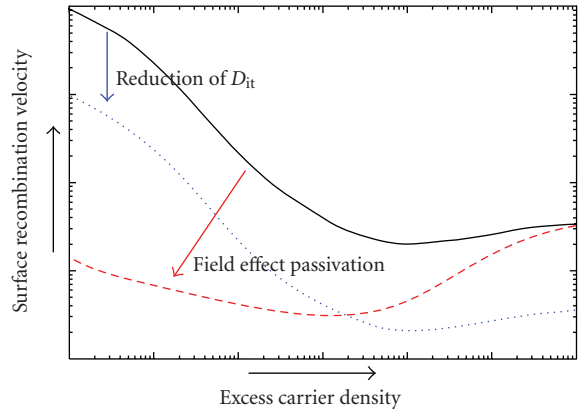


Figure 4: Sketch of the impact of the two passivation schemes, reduction of interface state density, D_{it} (dotted) and field effect passivation (dashed).

for decades. Therefore, extremely low interface state densities and surface recombination velocities have been achieved especially if the well-known "Alneal" treatment [10] is applied. Unfortunately, the typical temperature of thermal oxidation is around 1050°C. This temperature range imposes no problem for high-quality FZ-Si and can even increase the minority carrier lifetime in Czochralski-grown silicon [11] but it is extremely detrimental for block-cast multicrystalline silicon [12, 13]. For such material, the minority carrier lifetime can be reduced by a factor of about 10 [14]. Thus, it is essential to find passivation layers that can be deposited at lower temperatures. It is possible to grow thermal oxides in a wet ambient atmosphere at temperatures of around 850°C [15]. The wet atmosphere increases the oxidation rate drastically, which makes it possible to obtain the typical oxide thickness of 105 nm in a reasonable time. This strategy was applied to multicrystalline silicon and has lead to the actual record for multicrystalline silicon of 20.3% [14]. The average efficiencies of these cells were typically higher than 18%, indicating that low-quality regions have not been degraded by this treatment. Another interesting alternative is the growth of a thin oxide layer at temperatures around 850°C in dry atmosphere. This thin oxide layer has to be combined with a second deposited layer on top and will be discussed later in this paper.

Deposited layers such as PECVD SiN_x are the second best choice. The typical deposition temperatures are in the range of 350° to 400°C. Excellent surface recombination velocities of less than 10 cm/s have been reached [16]. An additional advantage of SiN_x is the incorporation of hydrogen in this layer which could act as a bulk passivation source for multicrystalline silicon. A very fast alternative to PECVD reactors is sputtering by which excellent surface recombination velocities below 30 cm/s have also been achieved [17].

The lowest deposition temperatures between 200°C and 250°C are needed if amorphous silicon is used as the rear passivation layer. This passivation scheme is applied successfully in the HIT structure [18] achieving efficiencies of 21%. Recently, it was shown that amorphous silicon also works well for standard cell structures with diffused emitters [19, 20] and efficiencies above 20% have been reported.

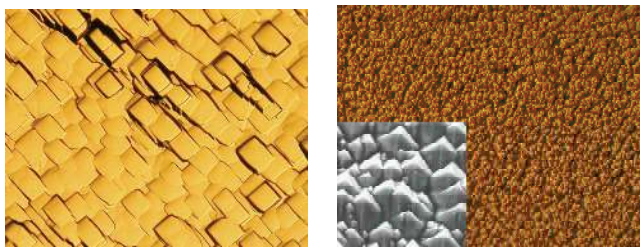
2.4. Preconditioning

Besides the deposition temperature, another technological issue is the preparation of the surface before the fabrication of the dielectric layer. A clean surface is substantial for oxidation processes or else surface contaminants will diffuse into the bulk. This problem is less severe for deposited passivation layers due to the lower process temperatures. However, a very shallow layer of crystal damage which could be left over after a prior etching step will decrease the passivation quality significantly. This problem is less pronounced for oxidized surfaces since a part of the upper silicon layer is taken by the oxidation process (approximately half of the final oxide layer).

Another topic is the surface geometry. In contrast to microelectronics, surfaces of industrial solar cells are generally rough due to the anisotropic damage etch or a wet-chemical texturing process.

It is important to investigate whether a rough surface structure results in lower optical and electrical performance if compared to a smooth shiny etched surface. In order to investigate this issue, we have prepared a set of solar cells with different topographies (see Figure 5) on the same material (FZ-Si) with the following identical cell structure: (front: random pyramids with 105 nm thermal oxide, 120 Ω/sq phosphorus emitter; rear: 105 nm thermal oxide, 2 μm aluminium and LFC contacts).

While the cells with the damage-etched and shiny-etched rear surface nearly show the similar performance (see Table 2), the cells with the textured rear exhibit lower efficiencies mainly due to a loss in current which can be clearly



(a) (b)

Figure 5: (a) Surface topography after alkaline damage etch and (b) random pyramid texturing. Both photos are taken by an optical microscope. The inset in (b) is a scanning microscope picture to show the pyramid geometry more clearly.

Table 2: Results of oxide-passivated cells on 0.5 Ω cm FZ-Si with different rear surface topographies (average of 7 cells).

Rear surface topography	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF	η [%]
Shiny etched	677.1 +/−0.6	38.14 +/−0.15	80.4 +/−0.2	20.8 +/−0.1
Damage etched	678.9 +/−0.3	38.21 +/−0.06	80.9 +/−0.1	21.0 +/−0.04
Random pyramids	673.2 +/−2.2	37.25 0.28	80.1 +/−0.4	20.1 +/−0.2

attributed to the lower performance of the textured rear surface (see the poorer long wavelength response in Figure 6).

De Wolf et al. [21] also demonstrated a similar reduction of passivation quality with increasing surface roughness for PECVD-SiN_x-layers. They also showed that this dependence on surface roughness is much less pronounced after a subsequent firing step.

2.5. Internal reflection

Next to the passivation quality, it is important to analyze the optical properties of a rear surface passivation layer. The "traditional" Si/SiO_2/Al system has very high-internal reflectivity due to the low refractive index of SiO_2 ($n = 1.46$) [22]. A pyramid texture on the front surface results in an oblique light path (angle 41.4° from perpendicular) and total reflection occurs at the rear surface. Thus, for the internal optical reflection at the rear side of the cell, (R_{back}) values of 95% to 89% can be obtained. However, since most of the deposited layers with good passivation quality such as Si-rich SiN_x have a high refractive index, R_{back} is not that high.

Figure 7 shows the reflectivity measurements of solar cells with textured front side and different rear surface passivation layers. If silicon-rich dielectric layers with high-refractive indices ($SiN_x = 2.9$, $SiC_x > 3$) are applied, the R_{back} values are still better than the industrial standard but much lower than the thick thermal SiO_2 layer. Since these layers usually show very low surface recombination velocities, it is favourable to deposit them directly onto the silicon

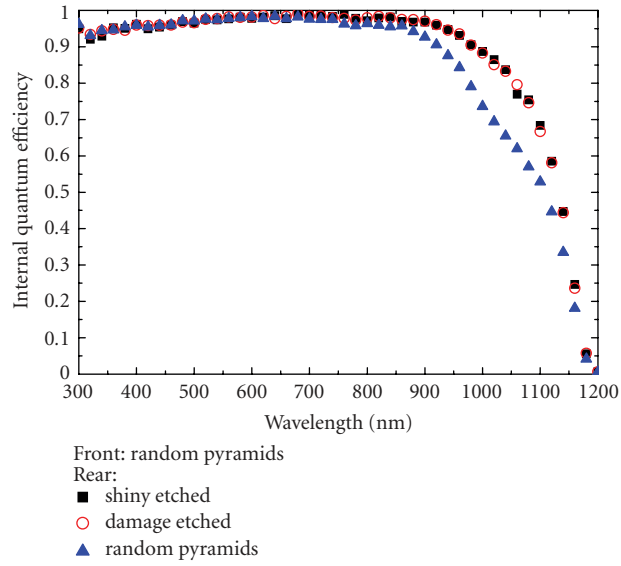


Figure 6: Internal quantum efficiencies of cells with oxide-passivated rear surface on 0.5 Ω cm FZ silicon.

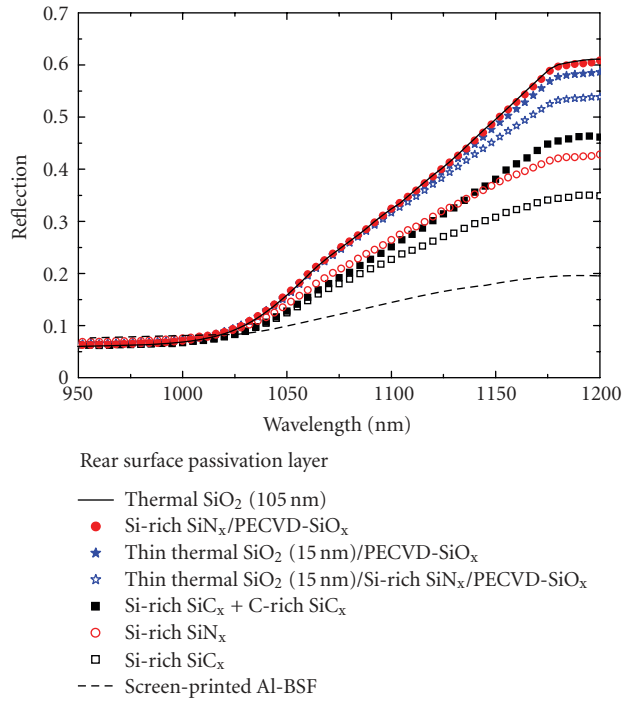


Figure 7: Reflectivity measurements of solar cells with front texture and different rear surface passivation layers. The upper margin is a 105 nm thermal oxide (solid line), the lower margin is screen-printed Al-BSF (dashed line).

surface. In order to improve the optical properties, a second dielectric layer with a lower refractive index [23] should be applied. In fact, a quite strong improvement is observed if a PECVD SiO_2 ($n = 1.46$) is deposited on top of the Si-rich SiN_x layer (red solid circles in Figure 7) and likewise for a C-rich SiC-layer on top of a Si-rich SiC_x layer ($n \approx 2$) (black

solid squares in Figure 7). Also, the optical performance of a thin thermal oxide (15 nm) can be improved by the deposition of a low-temperature PECVD SiO_2 (blue filled stars in Figure 7). Thus, stack systems allow the two important tasks of "passivation" and "reflection" to be achieved by different layers.

2.6. Application to solar cells

Although it seems possible to design a perfect layer or layer system simply by performing lifetime and optical measurements, a final decision has to be made by applying these layers to solar cells. A good example that illustrates that good surface passivation quality is only a necessary but not a sufficient condition is SiN_x passivation. Although SiN_x layers show the very best surface passivation quality on lifetime test wafers, even better than thermal oxidation, none has so far managed to fabricate a cell with efficiencies attainable by the ones featuring the "classical" thermal oxidation. In particular, the short-circuit current is significantly lower. This reduction was explained by Dauwe et al. [24] by the short-circuiting of the inversion layer induced by the fixed charges in the SiN_x layer at the rear contact points. Since the inversion layer is a crucial part of surface passivation mechanism of SiN_x layers, the apparent quality of SiN_x layers on lifetime test wafers "vanishes" when applied to real cells. The best cell efficiencies reported so far using silicon nitride rear surface passivation were 21.5% [25] and 20.6% [26]. In the first case, a very sensitive plasma etch was used to open the contact holes in the SiN_x layer so that the inversion layer was not shunted. In the second case a local boron BSF reduced the shunting of the inversion layer. However, if used with a "rough" process like laser-fired contacts or mechanical sawing, efficiencies higher than 20% would not be reached.

This problem can be solved in two ways: (i) by the development of SiN_x layers whose passivation quality would be more dependent on the reduction of interface states than on the field effect passivation (i.e., reduction of D_{it} and Q_f) [18] or (ii) by the application of thin thermal oxide (10–15 nm) below the SiN_x layer. This oxide layer can be grown rapidly (e.g., RTO) and at relatively low temperatures (850°C). Excellent surface passivation quality has been reported [27, 28]. Additionally, the thin oxide layer will also serve as a front passivation for lighter doped emitters on the front.[1] When such a stack system is applied on the rear, efficiencies of 20.5% have been reported [29].

Another excellent passivation layer is amorphous silicon. For the HIT cell structure [30], it was natural choice to use amorphous silicon as the rear surface passivation since the emitter is also formed by this layer type. This type of passivation is also applied on standard silicon solar cells achieving excellent cell results [26, 31] reaching efficiencies up to 21.7% (V_{oc} = 677 mV) [20].

[1] Since the oxide layer is very thin, it is possible to apply a second front layer with higher refractive index (i.e., SiN_x), resulting in very good optical performance.

Table 3: Solar cell results with SiC_x rear passivation.

Rear surface structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
SiC_x-layer + 2 μm Al + LFC	665	37.5	80.3	20.2

Recently, Martín et al. [32] reported that PECVD-deposited SiC_x-layers also show very good passivation quality ($S < 30$ cm/s). At Fraunhofer ISE, SiC_x layers are used as a diffusion barrier layer for recrystallization of silicon thin-film layers on low-cost substrates [33] due to their excellent thermal stability. The PECVD system used for this process step offers the possibility to perform an in situ plasma cleaning step prior to the deposition itself which would make it possible to optimize the process flow in an industrial line tremendously. In order to optimize the surface passivation quality of these SiC_x layers, 1 Ω cm p-type high-lifetime FZ-Si wafers were used. The wafers were taken out of the box and plasma cleaned. Subsequently, the SiC_x-layer was deposited without any additional wet-chemical process. Excellent surface recombination velocity well below 5 cm/s for Δn between 1×10^{14} cm^{-3} and 1×10^{15} cm^{-3} has been achieved [34]. After the successful development of a highly passivating SiC_x layer, different layer systems based on different compositions were used for the rear passivation of solar cells with a high-efficiency front structure (oxide-passivated 120 Ω/sq emitter and evaporated contacts). Again, not only the deposition but also the surface conditioning was performed in the PECVD reactor. E-gun evaporation was used for the deposition of the 2 μm thick Al layer and the laser-fired contacts process was applied. Although the cells have not been annealed after e-gun evaporation and LFC formation, efficiencies greater than 20% have been achieved (see Table 3).

2.7. Thermal stability

If a dielectric rear surface passivation has to be combined with a standard screen-printed front surface metallization, a critical factor is the stage in the process sequence where the layer will be deposited (see Figure 8). Depositing the dielectric layer on the rear surface after the firing step for the front metallization (option 1 in Figure 8) requires a strong surface conditioning, including etching of the rear emitter layer and severe cleaning since the wafer has already been subject to several "dirty" process steps at that stage. Thus, although the dielectric layer will not see any high-temperature step afterwards, it is a difficult task to obtain good surface passivation.

Alternatively, the rear dielectrical layer could be deposited after the emitter diffusion (option 2 in Figure 8) around the same time as the front surface nitride deposition taking advantage of the clean conditions of the wafer. The rear emitter layer will still need to be etched away prior to rear dielectric deposition, and the deposited layer has to be able to withstand a high-temperature step, that is, the subsequent firing step.

An even more elegant option could be the rear dielectric deposition before the emitter diffusion (option 3). At

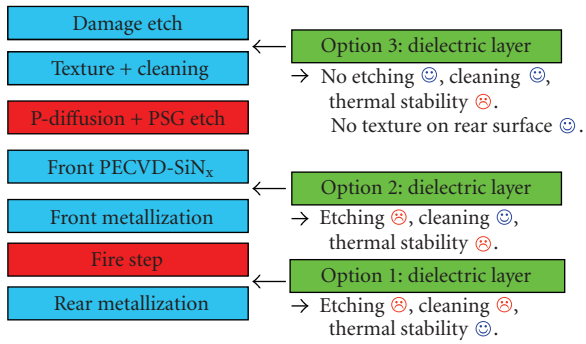


Figure 8: Formation of a dielectric layer within an industrial solar cell process.

that point, the wafer is definitely clean and the rear dielectric will mask the subsequent emitter diffusion from the rear, eliminating the rear etching step. The rear dielectric can also mask the surface texture on the rear side if the texturing processing is well controlled. It was shown that the passivation quality on a nontextured surface is significantly better (see Section 2.4 or [35]). Thus, this process sequence seems to be ideal but of course the passivation layer has to withstand two subsequent high-temperature steps without losing its passivation quality.

Therefore, besides good electrical and optical properties, a high thermal stability is essential for an industrially feasible passivation layer.

The classical choice for a passivation layer with good thermal stability is a silicon dioxide layer thermally grown at temperatures between 800°C and 1050°C. This layer was used for our first test to transfer the LFC technology into an industrial process sequence [36]. However, due to the high process temperature, it could be difficult to use this process in an industrial environment although it was shown that an oxidation at reduced temperatures does not degrade material quality [14] and that in diffusion of surface contaminants during the process is less critical than thought before [37].

A process closer to today's industrial reality is the deposition of silicon nitride using PECVD. However, it was not possible to reach the same passivation quality as of thermal oxides when applied to a solar cell due to detrimental shunting of the inversion layer induced by the SiN_x-layer [24]. Also, thermal stability seems to be an issue although recent works have shown that a medium passivation level can be maintained after a firing step [38].

Recently, Agostinelli et al. have shown that it is possible to reach an efficiency of 17.3% on 105 μm thin Cz-Si with their i-PERC structure which is based on a fire-stable dielectric layer [39]. Reference cells featuring an Al-BSF have shown an efficiency of only 15.1%. This improvement demonstrates impressively the superiority of dielectric rear surface passivation and the feasibility to implement it into an industrial cell process.

As mentioned above, cells passivated with PECVD-deposited amorphous silicon have reached a remarkable efficiency level, but unfortunately this layer type is only temperature stable up to 400°C [20].

Table 4: Carrier lifetime @ $\Delta n = 5 \times 10^{14}$ cm^{-3} of test samples before and after a firing step at 800°C.

Layer system	Lifetime before firing	Lifetime after firing
LS-08	1126	17.8
LS-10	533	0.8
LS-66	341	250

Table 5: Implied open-circuit voltage before and after firing step determined from QSSPC measurement at 1 sun on a solar cell precursor. For layer system, B is the best result and the average of 7 samples after firing is given.

Layer system	max. V_{oc} [mV] before firing step	max. V_{oc} [mV] after firing step
A (best result)	625	639
B (best result)	635	679
B (average)	—	676 +/−2.4

SiC_x is well known to be quite stable with respect to thermal treatments. In fact, Martín et al. [32] reported that the passivation quality does not decrease after a firing step at 730°C. Thus, this material type could be extremely interesting in terms of thermal stability. In order to verify the thermal stability of SiC_x layers developed at Fraunhofer ISE we conducted experiments on lifetime test samples. The lifetime of SiC_x-passivated 1 Ω cm Fz-Si wafers was measured using quasi-steady-state photoconductance measurements (QSSPC) [40] before and after a firing step without any additional anneal step. The firing step was performed at a peak temperature of 800°C in a standard belt furnace. (Note: the chosen temperature of 800°C is lower than that of a standard firing step since it was shown that nonmetallized samples attain temperatures about 50°C to 80°C higher than metallized solar cells.)

The measurement results of a few representative layers in Table 4 show an interesting finding. The lifetime after deposition is not coupled with the fire stability. The layer system LS-66 which has shown good but not the best passivation quality clearly outperforms its "competitors" in terms of "fire stability."

Based on these findings, a second experiment fabricating solar cell precursors on 0.5 Ω cm FZ-Si with an oxide-passivated 120 Ω/sq emitter and different SiC_x rear passivation layers was conducted. In this case, the lifetime measured at one-sun illumination can be translated directly to the implied open-circuit voltage. Again, the structures were measured before and after an 800°C firing step.

Both layer systems shown in Table 5 are well suited for the rear surface passivation even after a firing step. In particular, layer system B is very promising since a very high open-circuit voltage of 679 mV could be obtained.

In the third experiment, solar cells have been fabricated to evaluate the potential of these layers in more detail. Again, high implied voltages of 682 mV after firing have been achieved on untextured solar cell precursors. Metal contacts

Table 6: Results of untextured solar cells with fired SiC_x rear passivation.

Rear surface structure	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
SiC_x-layer + 2 μm Al + LFC	674	33.1	80.6	18.0

have been applied on the front and rear of these samples and the cell performance have been measured (see Table 6)

The obtained open-circuit voltage of 674 mV shows impressively the high potential of SiC_x layers for photovoltaic application.

3. METALLIZATION

Due to its robust process technology and high throughput, screen-printing is the most common technique for the metallization of today's industrial solar cells. However, there are several undesirable features such as poor aspect ratio of the grid lines, high line resistance, and high doping concentration of the underlying emitter required to achieve acceptable values of contact resistance. These aspects motivate the investigation of alternative metallization concepts. This effort is also justified by the tremendous growth of cell area, leading to a strong increase of resistive losses in the front-side grid.

The first industrial cell type which does not use screen-printing for the front-side metallization is the *laser-buried contact cell* [41, 42] produced by BP Solar (see Figure 9).

Here, the contacts are buried into grooves which are machined with a laser and exhibit strong phosphorus diffusion. The contact structure is a multimetal layer with Ni immediately contacting the silicon. The rest of the surface is covered with a lowly doped emitter which is passivated effectively by SiN_x. Due to the low shading losses and the good electrical properties of this emitter, the blue response and the overall performance of this cell structure are very high [41].

It is believed that two-layer metallization processes such as the LGBG process shown above can compete with screen-printing. In the first of the process step a narrow metallization line, the *seed layer*, is created on the silicon surface. This seed layer should have good mechanical and electrical contact to the silicon surface. In the subsequent *growth* step, this line is thickened by a plating process to increase the line conductivity. Using such a two-layer process, it is possible to optimize both steps in terms of metals and process parameters separately and to clearly improve the performance of the front surface metallization. In fact, all high-efficiency cells in our lab are processed using a multilayer process.

3.1. Light-induced plating

For thickening of the seed layers (i.e., the growth step), at Fraunhofer ISE and other institutes [3], the light-induced electroplating process is used, which utilizes the photovoltaic effect of the cell and allows to contact only the fully metallized rear surface during plating (see Figure 10). Thus, the complexity of this selective process is reduced considerably. Furthermore, this process has a much higher deposition rate compared to electroless plating.

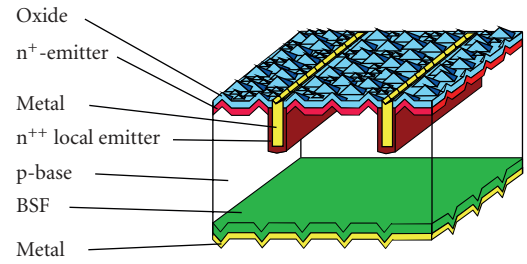


Figure 9: Laser grooved buried grid (LGBG) solar cell (Saturn) of BP Solar.

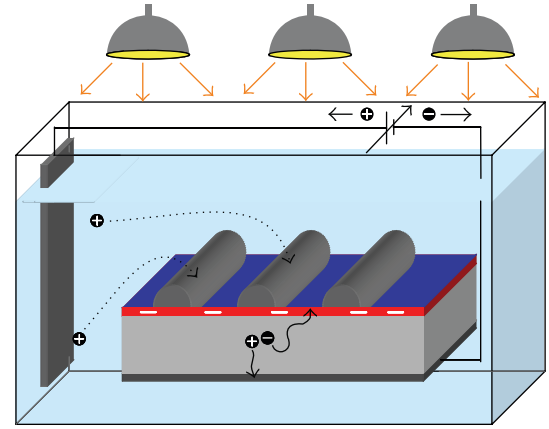


Figure 10: Scheme of the light-induced electroplating process (LIP). The cell is immersed in an electroplating bath with an Ag-electrode (left side) and only contacted at the fully metallized rear side. The applied potential suppresses dissolution on this side. By illuminating the cells, the front electrodes are on a more negative potential, high enough to stimulate deposition of Ag ions. This plating concept simplifies industrial transfer considerably.

The process has been used for our high-efficiency cells for more than a decade and results in highly conducting front contacts with an aspect ratio close to 1 : 2 (height : width). At Fraunhofer ISE, a small batch-type semiautomated electro-plating system was set up several years ago and is working reliably without complex maintenance. Recently, this process was used to increase the conductivity of narrow screen-printed lines. A significant efficiency increase on 15.6 × 15.6 cm^2 industrial multicrystalline cells by 0.3 to 0.5% absolute has been demonstrated [43], while saving silver paste in the screen-printing step. Thus, a short-time-scale transfer of this process into an industrial environment seems to be quite realistic.

Of course, the full potential of the light-induced plating process can only be achieved if the seed layer has better electrical and geometrical properties than screen-printed contacts. In the following sections, four different seed layer technologies, currently under development at Fraunhofer ISE, are discussed.

Table 7: Results of $100 \times 100\,\text{mm}^2$ Cz-Si solar cells. The front grid structure was fabricated using pad printing, firing, and light-induced plating.

Paste	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Hot melt	624	36.1	79.7	17.9
Conventional	627	36.2	76.9	17.4

3.2. Pad printing

Pad printing is a very interesting alternative to screen-printing since smaller structures in the range of less than $50\,\mu$m can be printed. Furthermore, a mature industrial high-volume technology and modified standard screen-printing pastes can be used. Thus, this technology was investigated intensively at Fraunhofer ISE [44]. Although it was possible to print very narrow contact lines, the height of the printed contacts is reduced simultaneously, resulting in decreased line conductivity.

However, in combination with a subsequent light-induced plating process, pad printing would be ideal to form the seed layer. To further increase the printing resolution and the paste transfer from pad to solar cell, we have used hot-melt pastes which have shown very promising results when applied by screen-printing as well [45]. It was necessary to modify the pad printer for the use of hot melt pastes, that is, to heat the printing pattern and the printing table. The process temperatures, printing patterns, and other process parameters have been optimized in order to achieve narrow and continuous lines and a complete transfer of the paste. We processed solar cells on textured $100 \times 100\,\text{mm}^2$ Czochralski silicon with this process using the following principal sequence:

(i) chemical texturing,
(ii) emitter diffusion 60 Ω/sq + PSG etch,
(iii) sputtering of SiN_x:H on the front side,
(iv) screen-printing of Al on the rear,
(v) pad printing of front grid,
(vi) cofiring,
(vii) edge isolation,
(viii) light-induced plating.

The printed lines had a width of $50\,\mu$m. Cell parameters as shown in Table 7 have been achieved. The achieved efficiency of 17.9% shows the high potential of the technology. A similar result was achieved using conventional silver screen-printing paste.

3.3. Laser sintering/melting of metal powder

The second seed layer technology which involves the deposition of a powder of metal particles is deposited on the surface of the cell. The metal powder is sintered or melted locally by a scanning laser to form the contact lines (see Figure 11). The rest of the powder is removed easily from the surface leaving laser-sintered contact lines [46]. Although it is possible to increase the height of the contact lines by repeating the process, we have decided to form only a small seed layer which is thickened subsequently by light-induced silver plating making the approach more economical.

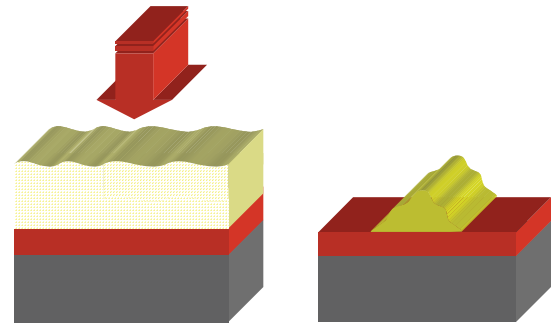


Figure 11: Laser microsintering of metal powder on the front surface of solar cells.

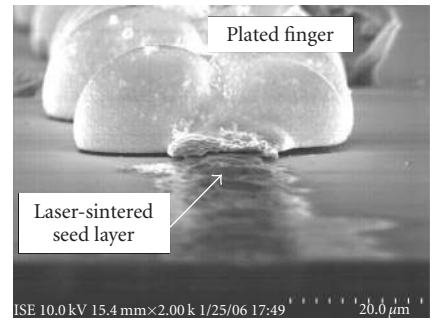


Figure 12: SEM image of a seed layer created by laser microsintering thickened by light-induced electroplating.

Figure 12 shows the structure of a laser-sintered finger after the subsequent light-induced plating step. The contact formed by laser sintering is very fine and thin, while the line conductivity is generated by the plated silver on top of this seed layer.

Initial cell results on small areas ($1 \times 1\,\text{cm}^2$) have shown efficiencies of 14.0%, although a heavily doped emitter (18 Ω/sq) was chosen for these preliminary experiments. We have achieved an open-circuit voltage of 622 mV. The pseudo FF of this cell measured using SunsVoc was determined to be 78%. Although this value is still below the optimum, it shows that it is possible to avoid severe damage in the emitter or space charge region by the laser process. Thus, it should be possible to utilize this technique for solar cell processing.

3.4. Chemical plating of Ni

Nickel plating is well known, used as a part of the laser-buried contact process by BP Solar to fabricate high-efficiency industrial solar cells [41]. However, in this process sequence, it is necessary to form a groove in the silicon surface which then receives a damage etch and a heavily doped phosphorus diffusion. Instead, it would be desirable to use a one-step process to form a front surface structure which initializes the local electroless Ni plating process.

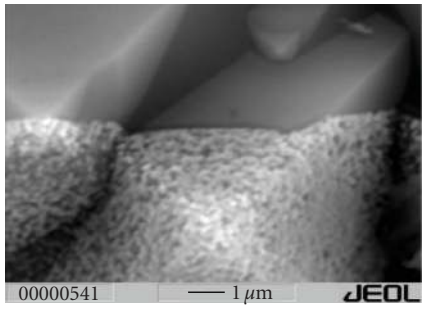


Figure 13: Ni plating on a textured silicon surface.

Table 8: Results of $20 \times 20\,\text{mm}^2$ oxide-passivated FZ-Si solar cells. The front grid structured was fabricated using electroless Ni plating and light-induced plating.

	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Ni plating + LIP	661	38.9	73.4	18.9

This motivates the use of laser ablation process to remove lines of the front surface SiN_x layer of standard cells similar to the approach demonstrated by Dubé and Gonsiorawski [47]. SunsVoc measurements have shown that this process does not damage the underlying silicon, that is, the pn-junction [48].

The Ni plating process was optimized to work on non-grooved surfaces and medium-doped emitter profiles. It is possible to initiate a sufficient Ni plating process (see Figure 13) with the optimized process.

For the initial experiments on cell level, however, we have used cell structures with an oxide-passivated emitter and rear surface. Due to the unfavourable absorption coefficient of silicon oxide, it is not possible to ablate the oxide without damaging the silicon underneath. Thus, a photoresist was used in these experiments to mask a chemical etching step to open the grid structure in the front oxide. The efficiency of 18.9% shows the quality of the developed plating process although there is still room for improvement by reducing the series resistance. Combined with the fact that the grid opening in a SiN_x front surface layer can be achieved by damage-free laser processing [48] or ink-jet masking and subsequent etching, it is believed that Ni plating will be an interesting option for the formation of seed layers even without a heavily diffused groove.

3.5. Metal aerosol jetting

A very elegant way to deposit the seed layer on top of the solar cell would be metal ink jetting. However, standard pastes cannot be used due to the relatively large particle sizes (5–10 μm), resulting in clogging which is a severe problem for jetting. As a rule of thumb, the diameter of the nozzle should be at least six times bigger than the particle size. Thus, the resulting line width would be in the range of screen-printed fingers defeating the purpose of the development.

Therefore, in our setup, the paste is not printed directly. Instead, a metal aerosol is generated and conducted into a specially designed printing head (see Figure 14). In this printing head, the aerosol is wrapped up in a ring-shaped gas flow to avoid the aerosol from being in contact with the tip. The ring-shaped gas flow is also responsible for focusing the aerosol achieving printed line widths to be considerably smaller than the tip diameter. It has been demonstrated, by using a nozzle with an outlet diameter of 200 μm, that printed lines with 50 μm width can be achieved. Additionally, the printing result is independent of the distance between nozzle and substrate which makes the technique suitable for uneven substrates. The metal aerosol jet printer was developed by Optomec Inc., NM, USA. A laboratory version of this printer was installed at Fraunhofer ISE. The set-up was modified and the process parameters for solar cell metallization were optimized [49].

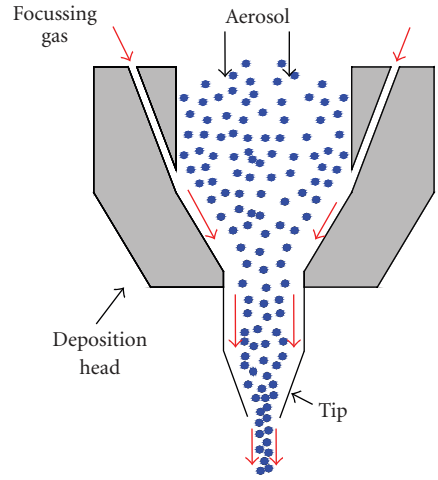


Figure 14: Printing head of the metal aerosol printing technique.

A great variety of modified commercially pastes and nanoparticle inks were tested. Although the printing results (line width, etc.) of the nanoparticle inks were excellent, the electrical (contact resistance and conductivity) and mechanical (adhesion) properties were not satisfying. Thus, we have used modified standard Ag pastes and despite their relatively large particle size, we managed to get small line widths of around 50–60 μm. This process was used to fabricate the front grid of industrial multicrystalline solar cells with the following processing sequence:

(i) textured multicrystalline silicon,
(ii) emitter diffusion (55 Ω/sq) + PSG etch,
(iii) deposition of PECVD SiN_x,
(iv) screen-printing of Al-BSF,
(v) aerosol printing (modified commercial Ag Paste),
(vi) cofiring,
(vii) edge isolation,
(viii) light-induced plating.

Two different finger widths were printed resulting in 160 μm and 70 μm wide lines after plating, respectively. Table 9 shows the results of the finished solar cells as measured at Fraunhofer ISE CalLab. The cells with a finger width of 160 μm exhibit a high fill factor demonstrating that

Table 9: Results of $50 \times 50\,mm^2$ multicrystalline solar cells with Al-BSF and SiN_x front passivation. The front grid structure was fabricated using metal aerosol jet printing, firing and light-induced plating.

Finger width	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
160 μm	617	32.7	79.4	16.0
70 μm	618	34.2	77.4	16.4

Table 10: Results of $125 \times 125\,mm^2$ monocrystalline solar cells with Al-BSF and SiN_x front passivation. The front grid structure was fabricated using metal aerosol jet printing, firing, and light-induced plating.

Finger width	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
90 μm	620	35.8	80.2	17.8

the contact formation works excellently. However, since the shading loss is not reduced, the efficiency is similar to the screen-printing references. The cells with 70 μm fingers show a much smaller shading loss than standard cells resulting in increased current and a significantly higher efficiency of 16.4%. The fill factor is satisfying. The overall benefit for this new and promising technique will be even higher if especially optimized pastes are used for future devices.

In a further batch, solar cells were processed on 12.5 cm $\times$ 12.5 cm, 3 to 6 Ω cm, boron-doped Cz-Si wafers. These cells exhibit a textured surface with a 45 Ω/sq emitter covered by a sputtered SiN_X antireflection coating. After conventional screen-printing and drying of the back side, the front side was printed using the metal aerosol jet printer. After firing in a fast firing single wafer furnace, the front contacts were thickened by light-induced plating and edge isolated by laser scribing and breaking. The same paste as for the multicrystalline cells was used with the addition of phosphorus. The idea is to form a higher emitter doping level directly under the contacts, in order to achieve good adhesion and low contact resistivity to the emitter surface.

Remarkable efficiencies up to 17.8% have been achieved (see Table 10) compared to the best efficiency of 17.2% achieved by screen-printed reference cells, again demonstrating a significant efficiency increase for the metal aerosol jet-printed cells compared to conventional screen-printed ones.

4. BULK PROPERTIES

Certainly, even the best cell structure will not result in high efficiencies if the material quality is too low. Therefore, the investigation of electrically active defects is of great importance for photovoltaic material. Especially for multicrystalline silicon, it is very important to understand thermal treatments, gettering [12, 50], and hydrogen passivation in order to increase the carrier diffusion length. These measures were extremely important to obtain the record efficiencies on small (20.3% on 1 cm^2) [14] and large area (18.1% on 137.7 cm^2) [51] multicrystalline substrates.

However, the material issue will become less critical as the wafers used for PV production are getting thinner. Thus, the decisive ratio diffusion length to thickness increases by decreasing the denominator. This is especially interesting for high-efficiency cell structures since the high-quality surface structures are capable of retaining cell performance as the cell thickness decreases. For example, the world record efficiency of 20.3% on multicrystalline silicon using a fully surface passivated cell structure was achieved on 99 μm thick material while an efficiency of "only" 19.9% was achieved for a 218 μm thick wafer of the same material type [14]. Using high-efficiency cell structures, efficiencies greater than 20% have been achieved on extremely thin monocrystalline wafers of less than 50 μm [52, 53].

Most of the monocrystalline silicon solar cell manufacturers use boron-doped Czochralski silicon as starting material. This material type shows a severe *degradation* of minority carrier lifetime induced by illumination or carrier injection [54, 55]. The responsible metastable defect is related clearly to the existence of boron and oxygen [11, 56]. Three options are promising for a reduction of this degradation: (i) the use of *thinner wafers* to improve the ratio diffusion length/cell thickness [57], (ii) *decreasing the boron concentration* to reduce the light-induced degradation [58, 59], or (iii) the application of the *regeneration process* as recently demonstrated by Herguth et al. [60].

But also alternative material types are of interest. In fact, cells from *gallium-doped Cz-silicon* show no degradation [61]. The only issue occurring with this material might be the large variation of doping concentration over the ingot due to the low segregation coefficient of gallium. Nevertheless, adapted cell structures show excellent results over a wide doping range [62].

A strong reduction of the oxygen concentration to values below 1 ppma results also in a perfect suppression of light-induced degradation. *Magnetic Czochralski* (MCz) *silicon* has shown a very high-efficiency potential [61, 63]. Another material, PV-FZ [64], with a negligible oxygen concentration was discussed to be introduced into the large-scale PV production a few years ago. This material type has shown very high and stable carrier lifetimes for p- and n-doping, but unfortunately the availability of this material type is still not clear at the moment.

Another material type of interest is certainly *n-type* silicon. *n-type* Czochralski-grown material shows no carrier-induced degradation even in the presence of a significant oxygen concentration [56, 65]. Also for multicrystalline silicon, excellent minority carrier lifetimes have been measured [66, 67] This superior material quality is mainly due to the fact that for most relevant defects, the ratio of electron to hole capture cross sections is much greater than unity. Therefore, compared to p-type silicon, the minority carrier lifetime for the same defect concentration is much greater in the case of n-type silicon since this parameter is mainly influenced by the whole capture cross section.

The only disadvantage of *n-type* silicon is the fact that it is not compatible with conventional industrial cell structures. Therefore, it is mainly used in advanced cell types. Prominent high-efficiency cell structures in industrial production which make use of this material are the amorphous silicon (a-Si)/monocrystalline silicon (c-Si) heterojunction

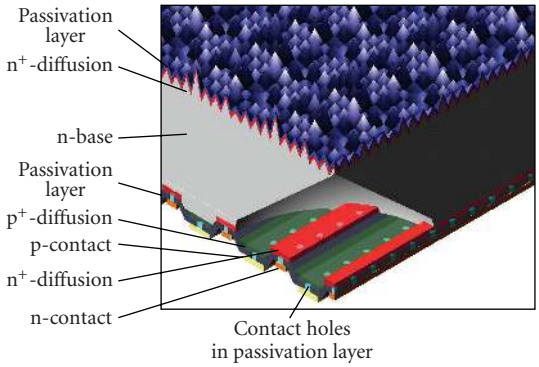


Figure 15: Point-contact cell of SunPower (redrawn after [68]).

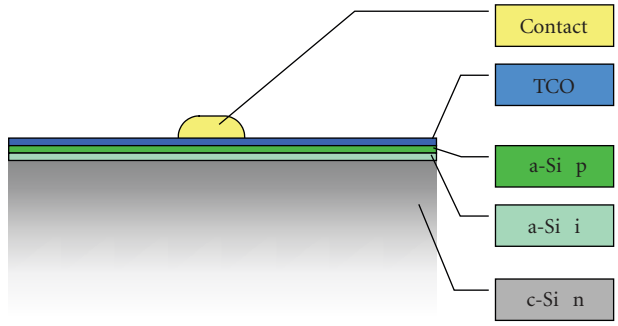


Figure 16: Front structure of the HIT cell.

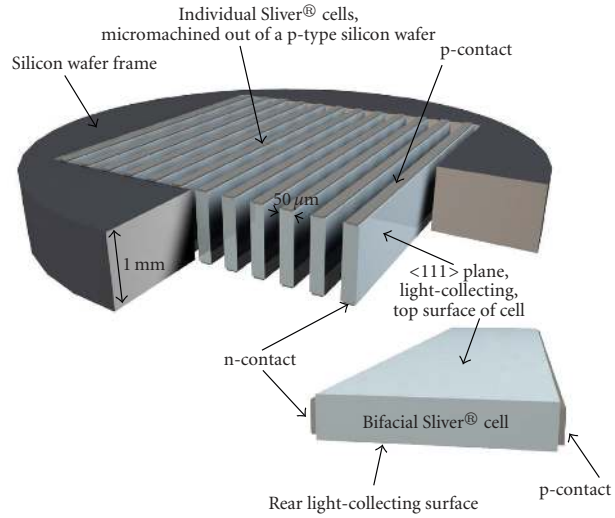


Figure 17: Sliver cells (taken from [73]).

with intrinsic thin layer (HIT) cell [30] and the back-contact cell A300 of SunPower [68] featuring a boron rear emitter (see next section). But also simpler cell structures using Al-diffused rear emitters have shown excellent performance [69, 70].

5. CELL STRUCTURES

To achieve the highest efficiencies, it is of course not enough to optimize a single aspect of a cell but different measures have to be combined in designing a cell structure to achieve high efficiencies. In what follows, a few examples of high-efficiency cell structures are described briefly.

The A-300 of SunPower [68] (see Figure 15) is a strongly simplified version of the point-contact cell originally developed for concentrator applications at Stanford University [8].

The main feature of this 20% cell in mass production is the absence of any metal contacts on the front side since both electrodes are placed on the rear surface as an interdigitated grid. Thus, nearly all carriers have to diffuse from the front surface where they are photo generated to the collecting *pn*-junction at the rear surface. Therefore, the bulk diffusion length has to be high (see previous section) and especially the surface recombination velocity at the front has to be very low. The task is managed by an excellently passivating SiO_2 layer on a lowly doped n^+-front surface field. Although, back-contact cells are obviously extremely attractive in terms of efficiency and aesthetics, they also pose very high demands on material quality and process technology. Especially the fabrication of the rear surface structure, that is, the separation of p- and n-diffused regions or p- and n-electrodes is an issue. One interesting opportunity for this task is the use of laser technologies [71].

In contrast to the A300, the p^+-emitter on the n-substrate for the HIT cell of Sanyo [30] is not based on boron diffusion but is formed by the deposition of p-doped a-Si layer (see Figure 16). Also, the rear surface is passivated by an a-Si layer in order to obtain the full potential of the monocrystalline n-type silicon. Efficiencies above 20% can be well achieved using this cell structure.

Another cell structure utilizing excellent surface passivation is the Sliver cell (see Figure 17). Very thin (50–60 μm) strips of silicon are micro machined from a 1-2 mm thick monocrystalline wafer [72, 73]. The strips are processed including many high-efficiency features while still supported by the wafer at their edges. After processing, they are separated and mounted into a module. Due to the excellent surface passivation on these cells, it is possible to reach efficiencies above 19%.

Rear contact cells on low-quality material cannot use a back junction cell structure as in the A300. It is necessary to implement a collecting emitter on the front side of the cell to make the cell structure less sensitive to low-diffusion lengths [74]. This emitter has to be connected to the rear electrode of the cell. This can be either obtained by metallized vias connecting the front fingers with the rear bus bar in the metal-wrap-through (MWT) structure [75] (see Figure 18) or by emitter-diffused holes in the emitter-wrap-through (EWT) structure [76] (see Figure 19). For a very comprehensive review of these cell types see [77].

The big advantage of the MWT structure is that it is relatively easy to be adapted to existing industrial cell production lines. The only difference in cell design compared to the standard is the bus bar being transferred to the rear side, with the fingers remaining on the front side. Due to the high lateral conductivity of the metal grid, a relatively low number of

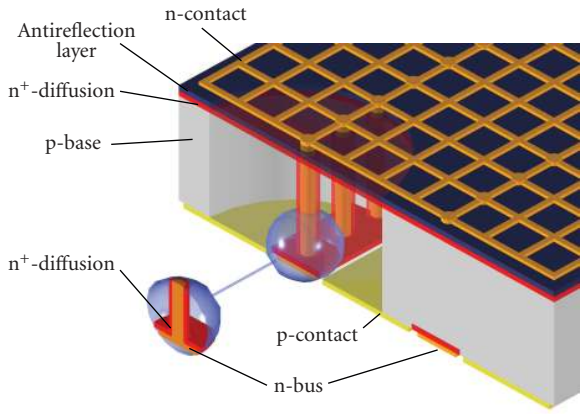


Figure 18: Structure of a metal-wrap-through (MWT) cell.

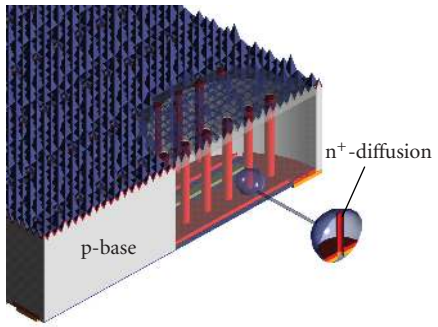


Figure 19: Structure of an emitter-wrap-through (EWT) cell.

vias is needed. The MWT is commercialized by Photovoltech. A similar cell structure called the PUM cell is developed by ECN [78].

In EWT cells [76, 79], the complete metal structure is located on the rear side. Due to the limited lateral conductivity of the front emitter, more vias are needed compared to the MWT structure. However, this should not be a limitation in production due to the capability of state-of-the-art laser equipment responsible for the formation of vias. The EWT cell design has been demonstrated to be capable of achieving high efficiencies of 21.4% [80], and suitable for industrial production as demonstrated by Advent Solar, Inc. Nm, USA, [81] resulting in cell efficiencies above 15%.

6. CONCLUSION

High-efficiency cell structures help to reduce the costs of photovoltaic energy generation in two ways: (i) by increasing the efficiency and hence the power output *per area* of used silicon or (ii) by allowing the use of thinner wafers achieving same level or even improved efficiency and hence the power output *per volume* or per weight. However, in order to allow for an industrial production of high-efficiency silicon solar cells, several design or technology limitations have to be addressed. This paper has discussed four important aspects associated with high-efficiency cells, that is, (i) the surface passivation, (ii) metal contacts, (iii) material quality, and (iv) cell structure.

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REFERENCES

[1] M. Hermle, E. Schneiderlöchner, G. Grupp, and S. W. Glunz, "Comprehensive comparison of different rear side contacting methods for high-efficiency solar cells," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, pp. 810–813, Barcelona, Spain, June 2005.

[2] D. Kray, M. Hermle, and S. W. Glunz, "Theory and experiments on the back side reflectance of silicon wafer solar cells," to appear in *Progress in Photovoltaics: Research and Applications*.

[3] J. Zhao, A. Wang, P. P. Altermatt, S. R. Wenham, and M. A. Green, "24% efficient PERL silicon solar cell: recent improvements in high efficiency silicon cell research," in *Proceedings of the 1st World Conference on Photovoltaic Energy Conversion (WCPEC '94)*, pp. 87–99, Waikoloa, Hawaii, USA, December 1994.

[4] J. Knobloch, A. Aberle, W. Warta, and B. Voss, "Starting points for raising the efficiency of practical silicon solar cells," in *Proceedings of the 5th International Photovoltaic Science and Engineering Conference*, Kyoto, Japan, November 1990.

[5] E. Schneiderlöchner, R. Preu, R. Lüdemann, and S. W. Glunz, "Laser-fired rear contacts for crystalline silicon solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 10, no. 1, pp. 29–34, 2002.

[6] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Applied Physics Letters*, vol. 55, no. 13, pp. 1363–1365, 1989.

[7] A. G. Aberle, *Crystalline Silicon Solar Cells: Advanced Surface Passivation and Analysis*, The University of New South Wales, Sydney, Australia, 1999.

[8] R. A. Sinton, Y. Kwark, J. Y. Gan, and R. M. Swanson, "27. 5-percent silicon concentrator solar cells," *Electron Device Letters*, vol. 7, no. 10, pp. 567–569, 1986.

[9] J. Zhao, A. Wang, and M. A. Green, "24% efficient PERL structure silicon solar cells," in *Proceedings of the 21st IEEE Photovoltaic Specialists Conference*, vol. 1, pp. 333–335, Kissimimee, Fla, USA, May 1990.

[10] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley, New York, NY, USA, 1982.

[11] S. W. Glunz, S. Rein, W. Warta, J. Knobloch, and W. Wettling, "On the degradation of Cz-silicon solar cells," in *Proceedings of the 2nd World Conference on Photovoltaic Energy Conversion*, pp. 1343–1346, Vienna, Austria, July 1998.

[12] D. Macdonald and A. Cuevas, "The trade-off between phosphorus gettering and thermal degradation in multicrystalline silicon," in *Proceedings of the 16th European Photovoltaic Solar Energy Conference*, pp. 1707–1710, Glasgow, UK, May 2000.

[13] O. Schultz, S. Riepe, and S. W. Glunz, "Influence of high-temperature processes on multicrystalline silicon," *Solid State Phenomena*, vol. 95-96, pp. 235–240, 2004.

[14] O. Schultz, S. W. Glunz, and G. P. Willeke, "Multicrystalline silicon solar cells exceeding 20% efficiency," *Progress in Photovoltaics: Research and Applications*, vol. 12, no. 7, pp. 553–558, 2004.

[15] M. Stocks and A. Cuevas, "Surface recombination velocity of thermally oxidised multicrystalline silicon," in *Proceedings of the 2nd World Conference on Photovoltaic Energy Conversion*, pp. 1623–1626, Vienna, Austria, July 1998.

[16] J. Schmidt, T. Lauinger, A. G. Aberle, and R. Hezel, "Record low surface recombination velocities on low-resistivity silicon solar cell substrates," in *Proceedings of the 25th IEEE Photovoltaic Specialists Conference*, pp. 413–416, Washington, DC, USA, May 1996.

[17] W. Wolke, J. Catoir, G. Emanuel, J. Liu, M. Ruske, and R. Preu, "Surface passivation for solar cells by large scale inline sputtering of silicon nitride," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, pp. 733–736, Barcelona, Spain, June 2005.

[18] M. Tanaka, S. Okamoto, S. Tsuge, and S. Kiyama, "Development of HIT solar cells with more than 21% conversion efficiency and commercialization of highest performance hit modules," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion (WCPEC '03)*, vol. 1, pp. 955–958, Osaka, Japan, May 2003.

[19] M. Schaper, J. Schmidt, H. Plagwitz, and R. Brendel, "20.1%-efficient crystalline silicon solar cell with amorphous silicon rear-surface passivation," *Progress in Photovoltaics: Research and Applications*, vol. 13, no. 5, pp. 381–386, 2005.

[20] M. Hofmann, S. W. Glunz, R. Preu, and G. Willeke, "21%-efficient silicon solar cells using amorphous silicon rear side passivation," in *Proceedings of the 21st European Photovoltaic Solar Energy Conference*, pp. 609–613, Dresden, Germany, September 2006.

[21] S. de Wolf, G. Agostinelli, G. Beaucarne, and P. Vitanov, "Influence of stoichiometry of direct plasma-enhanced chemical vapor deposited SiNx films and silicon substrate surface roughness on surface passivation," *Journal of Applied Physics*, vol. 97, no. 6, Article ID 063303, 8 pages, 2005.

[22] M. A. Green, *Solar Cells: Operating Principles, Technology and System Applications*, The University of New South Wales, Sydney, Australia, 1998.

[23] M. Hofmann, E. Schneiderlöchner, W. Wolke, and R. Preu, "Silicon nitride-silicon oxide stacks for solar cell rear side passivation," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, pp. 1037–1040, Paris, France, June 2004.

[24] S. Dauwe, L. Mittelstädt, A. Metz, and R. Hezel, "Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells," *Progress in Photovoltaics: Research and Applications*, vol. 10, no. 4, pp. 271–278, 2002.

[25] S. W. Glunz, R. Preu, S. Schaefer, et al., "New simplified methods for patterning the rear contact of RP-PERC high-efficiency solar cells," in *Proceedings of the 28th IEEE Photovoltaic Specialists Conference*, pp. 168–171, Anchorage, Alaska, USA, September 2000.

[26] S. Dauwe, L. Mittelstädt, A. Metz, J. Schmidt, and R. Hezel, "Low-temperature rear surface passivation schemes for >20% efficient silicon solar cells," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion*, vol. 2, pp. 1395–1398, Osaka, Japan, May 2003.

[27] J. Schmidt, M. Kerr, and A. Cuevas, "Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO_2/plasma SiN stacks," *Semiconductor Science and Technology*, vol. 16, no. 3, pp. 164–170, 2001.

[28] J. Y. Lee, J. Dicker, S. Rein, and S. W. Glunz, "Investigation of various surface passivation layers using oxide/nitride stacks of silicon solar cells," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion (WCPEC '03)*, vol. 2, pp. 1069–1072, Osaka, Japan, May 2003.

[29] O. Schultz, M. Hofmann, S. W. Glunz, and G. P. Willeke, "Silicon oxide/silicon nitride stack system for 20% efficient silicon solar cells," in *Proceedings of the 31st IEEE Photovoltaic Specialists Conference*, pp. 872–876, Orlando, Fla, USA, January 2005.

[30] K. Kawamoto, T. Nakai, T. Baba, et al., "A high-efficiency HIT^{TM} solar cell (21.0% 100 cm^2) with excellent interface properties," in *Proceedings of the 12th International Photovoltaic Science and Engineering Conference (PVSEC '01)*, pp. 289–290, Jeju, Korea, June 2001.

[31] P. J. Rostan, U. Rau, V. X. Nguyen, T. Kirchartz, M. B. Schubert, and J. H. Werner, "Low-temperature a-Si:H/ZnO/Al back contacts for high-efficiency silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 90, no. 9, pp. 1345–1352, 2006.

[32] I. Martín, M. Vetter, A. Orpella, J. Puigdollers, A. Cuevas, and R. Alcubilla, "Surface passivation of p-type crystalline Si by plasma enhanced chemical vapor deposited amorphous SiC_x:H films," *Applied Physics Letters*, vol. 79, no. 14, pp. 2199–2201, 2001.

[33] S. Janz, S. Reber, F. Lutz, and C. Schetter, "SiC as an intermediate layer for CsiTF solar cells on various substrates," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, pp. 1016–1019, Barcelona, Spain, June 2005.

[34] S. Janz, S. Riepe, M. Hofmann, S. Reber, and S. W. Glunz, "Phosphorus-doped SiC as an excellent p-type Si surface passivation layer," *Applied Physics Letters*, vol. 88, no. 13, Article ID 133516, 2 pages, 2006.

[35] W. Warta, S. W. Glunz, J. Dicker, and J. Knobloch, "Highly efficient 115-μm-thick solar cells on industrial Czochralski silicon," *Progress in Photovoltaics: Research and Applications*, vol. 8, no. 5, pp. 465–471, 2000.

[36] E. Schneiderlöchner, G. Grupp, G. Emanuel, et al., "Silicon solar cells with screen printed front contact and dielectrically passivated laser-fired rear electrode," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, pp. 447–450, Paris, France, June 2004.

[37] D. Macdonald, A. Cuevas, K. McIntosh, L. Barbosa, and D. de Ceuster, "Impact of Cr, Fe, Ni, Ti and W surface contamination on diffused and oxidised n-type crystalline silicon wafers," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, pp. 627–630, Barcelona, Spain, June 2005.

[38] G. Agostinelli, P. Choulat, H. F. W. Dekkers, S. de Wolf, and G. Beaucarne, "Advanced dry processes for crystalline silicon solar cells," in *Proceedings of the 31st IEEE Photovoltaic Specialists Conference*, pp. 1149–1152, Orlando, Fla, USA, January 2005.

[39] G. Agostinelli, P. Choulat, H. F. W. Dekkers, Y. Ma, and G. Beaucarne, "Silicon solar cells on ultra-thin substrates for large scale production," in *Proceedings of the 21st European Photovoltaic Solar Energy Conference*, Dresden, Germany, September 2006.

[40] R. A. Sinton, A. Cuevas, and M. Stuckings, "Quasi-steady-state photoconductance, a new method for solar cell material and device characterization," in *Proceedings of the 25th IEEE Photovoltaic Specialists Conference*, pp. 457–460, Washington, DC, USA, May 1996.

[41] T. M. Bruton, N. B. Mason, S. Roberts, et al., "Towards 20% efficient silicon solar cells manufactured at 60 MWp per annum," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion (WCPEC '03)*, vol. 1, pp. 899–902, Osaka, Japan, May 2003.

[42] M. A. Green and S. R. Wenham, Australian Patent No. 5703309, 1984.

[43] A. Mette, C. Schetter, D. Wissen, S. Lust, S. W. Glunz, and G. Willeke, "Increasing the efficiency of screen-printed silicon solar cells by light-induced silver plating," in *Proceedings of the 4th World Conference on Photovoltaic Energy Conversion*, vol. 1, pp. 1056–1059, Waikoloa, Hawaii, USA, May 2006.

[44] D. M. Huljić, S. Thormann, R. Preu, R. Lüdemann, and G. Willeke, "Pad printed front contacts for c-Si solar cells—a technological and economical evaluation," in *Proceedings of the 29th IEEE Photovoltaic Specialists Conference (PVSC '02)*, pp. 126–129, New Orleans, La, USA, May 2002.

[45] A. Mette, D. Erath, R. Ruiz, G. Emanuel, E. Kasper, and R. Preu, "Hot melk ink for the front side metallisation of silicon solar cells," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, Barcelona, Spain, June 2005.

[46] M. Alemán, A. Streek, P. Regenfuß, et al., "Laser microsintering as a new metallization technique for silicon solar cells," in *Proceedings of the 21st European Photovoltaic Solar Energy Conference and Exhibition*, Dresden, Germany, September 2006.

[47] C. E. Dubé and R. C. Gonsiorawski, "Improved contact metallization for high efficiency EFG polycrystalline silicon solar cells," in *Proceedings of 21st IEEE Photovoltaic Specialists Conference*, vol. 1, pp. 624–628, Kissimimee, Fla, USA, May 1990.

[48] A. Grohe, C. Harmel, A. Knorz, S. W. Glunz, R. Preu, and G. P. Willeke, "Selective laser ablation of anti-reflection coatings for novel metallization techniques," in *Proceedings of the IEEE 4th World Conference on Photovoltaic Energy Conversion*, vol. 2, pp. 1399–1402, Waikoloa, Hawaii, USA, May 2006.

[49] A. Mette, P. L. Richter, M. Hörteis, and S. W. Glunz, "Metal aerosol jet printing for solar cell metallization," to appear in *Progress in Photovoltaics: Research and Applications*.

[50] O. Schultz, S. W. Glunz, S. Riepe, and G. P. Willeke, "High-efficiency solar cells on phosphorus gettered multicrystalline silicon substrates," *Progress in Photovoltaics: Research and Applications*, vol. 14, no. 8, pp. 711–719, 2006.

[51] M. McCann, B. Raabe, W. Jooss, R. Kopecek, and P. Fath, "18.1% efficiency for a large area, multi-crystalline silicon solar cell," in *Proceedings of the 4th World Conference on Photovoltaic Energy Conversion (WCPEC '06)*, vol. 1, pp. 894–899, Waikoloa, Hawaii, USA, May 2006.

[52] D. Kray, H. Kampwerth, E. Schneiderlöchner, et al., "Comprehensive experimental study on the performance of very thin laser-fired high-efficiency solar cells," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, pp. 608–611, Paris, France, June 2004.

[53] A. Wang, J. Zhao, S. R. Wenham, and M. A. Green, "21.5% efficient thin silicon solar cell," *Progress in Photovoltaics: Research and Applications*, vol. 4, no. 1, pp. 55–58, 1996.

[54] H. Fischer and W. Pschunder, "Investigation of photon and thermal induced changes in silicon solar cells," in *Proceedings of the 10th IEEE Photovoltaic Specialists Conference*, pp. 404–411, Palo Alto, Calif, USA, November 1973.

[55] J. Knobloch, S. W. Glunz, V. Henninger, et al., "21% efficient solar cells processed from Czochralski grown silicon," in *Proceedings of the 13th European Photovoltaic Solar Energy Conference*, pp. 9–12, Nice, France, October 1995.

[56] J. Schmidt, A. G. Aberle, and R. Hezel, "Investigation of carrier lifetime instabilities in Cz-grown silicon," in *Proceedings of the IEEE 26th Photovoltaic Specialists Conference (PVSC '97)*, pp. 13–18, Anaheim, Calif, USA, September-October 1997.

[57] K. A. Münzer, K. T. Holdermann, R. E. Schlosser, and S. Sterk, "Improvements and benefits of thin crystalline silicon solar cells," in *Proceedings of the 2nd World Conference on Photovoltaic Energy Conversion*, pp. 1214–1219, Vienna, Austria, July 1998.

[58] S. Rein, W. Warta, and S. W. Glunz, "Investigation of carrier lifetime in p-type Cz-silicon: specificlimitations and realistic prediction of cell performance," in *Proceedings of the 28th IEEE Photovoltaics Specialists Conference*, pp. 57–60, Anchorage, Alaska, USA, September 2000.

[59] S. W. Glunz, S. Rein, J. Y. Lee, and W. Warta, "Minority carrier lifetime degradation in boron-doped Czochralski silicon," *Journal of Applied Physics*, vol. 90, no. 5, pp. 2397–2404, 2001.

[60] A. Herguth, G. Schubert, M. Kaes, and G. Hahn, "Avoiding boron-oxgen related degradation in highly boron-doped Cz silicon," in *Proceedings of the 21st European Photovoltaic Solar Energy Conference*, pp. 530–537, Dresden, Germany, September 2006.

[61] S. W. Glunz, S. Rein, J. Knobloch, W. Wettling, and T. Abe, "Comparison of boron- and gallium-doped p-type Czochralski silicon for photovoltaic application," *Progress in Photovoltaics: Research and Applications*, vol. 7, no. 6, pp. 463–469, 1999.

[62] S. W. Glunz, S. Rein, and J. Knobloch, "Stable Czochralski silicon solar cells using gallium-doped base material," in *Proceedings of the 16th European Photovoltaic Solar Energy Conference*, pp. 1070–1075, Glasgow, UK, May 2000.

[63] J. Zhao, A. Wang, and M. A. Green, "24.5% efficiency PERT silicon solar cells on SEH MCZ substrates and cell performance on other SEH CZ and FZ substrates," *Solar Energy Materials and Solar Cells*, vol. 66, no. 1–4, pp. 27–36, 2001.

[64] J. Vedde, T. Clausen, and L. Jensen, "Float-zone silicon for high volume production of solar cells," in *Proceedings of the 3rd World Conference on Photovoltaic Energy Conversion*, vol. 1, pp. 943—946, Osaka, Japan, May 2003.

[65] T. Yoshida and Y. Kitagawara, "Bulk lifetime decreasing phenomena induced by light-illumination in high-purity p-type CZ-Si crystals," in *Proceedings of the 4th International Symposium on High Purity Silicon IV*, pp. 450–454, San Antonio, Tex, USA, October 1996.

[66] A. Cuevas, M. J. Kerr, C. Samundsett, F. Ferrazza, and G. Coletti, "Millisecond minority carrier lifetimes in *n*-type multicrystalline silicon," *Applied Physics Letters*, vol. 81, no. 26, pp. 4952–4954, 2002.

[67] S. Riepe, H. Lautenschlager, J. Isenberg, et al., "Increased wafer yield for solar cells in top and bottom regions of cast multicrystalline silicon," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, pp. 986–989, Paris, France, June 2004.

[68] K. R. McIntosh, M. J. Cudzinovic, D. D. Smith, W. P. Mulligan, and R. M. Swanson, "The choice of silicon wafer for the production of low-cost rear-contact solar cells," in *Proceddings of the 3rd World Conference on Photovoltaic Energy Conversion (WCPEC '03)*, vol. 1, pp. 971–974, Osaka, Japan, May 2003.

[69] S. W. Glunz, E. Schneiderlöchner, D. Kray, et al., "Laser-fired contact solar cells on p- and n-type substrates," in *Proceedings of the 19th European Photovoltaic Solar Energy Conference*, pp. 408–411, Paris, France, June 2004.

[70] C. Schmiga, A. Froitzheim, M. Ghosh, A. Metz, J. Schmidt, and R. Brendel, "Solar cells on n-type silicon materials with screen-printed rear aluminium-P^+ emitter," in *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, Barcelona, Spain, June 2005.

[71] D. M. Huljic, T. Zerres, A. Mohr, et al., "Development of a 21% back-contact monocrystalline silicon solar cell for large-scale production," in *Proceedings of the 21th European Photovoltaic Solar Energy Conference*, Dresden, Germany, September 2006.

[72] M. J. Stocks, K. J. Weber, A. W. Blakers, et al., "65-micron thin monocrystalline silicon solar cell technology allowing 12-fold reduction in silicon usage," in *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion*, vol. 1, pp. 184–187, Osaka, Japan, May 2003.

[73] A. W. Blakers, K. J. Weber, E. Everett, E. Franklin, and P. Deenapanray, "Sliver cells—a complete photovoltaic solution," in *Proceedings of the 4th World Conference on Photovoltaic Energy Conversion (WCPEC '06)*, vol. 2, pp. 2181–2184, Waikoloa, Hawaii, USA, May 2006.

[74] D. Kray, S. Rein, D. Oßwald, et al., "High-efficiency emitter-wrap-through cells," in *Proceedings of the 17th European Photovoltaic Solar Energy Conference*, pp. 1299–1302, Munich, Germany, October 2001.

[75] E. van Kerschavers, S. de Wolf, and J. Szlufcik, "Screen printed metallisation wrap through solar cells," in *Proceedings of the 16th European Photovoltaic Solar Energy Conference*, pp. 1517–1520, Glasgow, UK, May 2000.

[76] J. M. Gee, K. W. Schubert, and P. A. Basore, "Emitter wrap-through solar cell," in *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference*, pp. 265–270, Louisville, Ky, USA, May 1993.

[77] E. van Kerschaver and G. Beaucarne, "Back-contact solar cells: a review," *Progress in Photovoltaics: Research and Applications*, vol. 14, no. 2, pp. 107–123, 2005.

[78] J. H. Bultman, M. W. Brieko, A. R. Burgers, J. Hoornstra, A. C. Tip, and A. W. Weeber, "Interconnection through vias for improved efficiency and easy module manufacturing of crystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 65, no. 1–4, pp. 339–345, 2001.

[79] A. Schönecker, D. Eikelboom, P. Manshanden, et al., "ACE designs: the beauty of rear contact solar cells," in *Proceedings of the 29th IEEE Photovoltaic Specialists Conference*, pp. 106–109, New Orleans, La, USA, May 2002.

[80] S. W. Glunz, J. Dicker, D. Kray, et al., "High-efficiency cell structures for medium-quality silicon," in *Proceedings of the 17th European Photovoltaic Solar Energy Conference*, pp. 1287–1292, Munich, Germany, October 2001.

[81] P. Hacke, J. M. Gee, M. Hilali, et al., "Current status of technologies for industrial emitter-wrap-through solar cells," in *Proceedings of the 21st European Photovoltaic Solar Energy Conference*, pp. 761–764, Dresden, Germany, September 2006.