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High Efficiency Non-isolated Three Port DC-DC Converter for PV-Battery Systems

Kevin Tomas-Manez, Alexander Anthon, Zhe Zhang, Ziwei Ouyang Department of Electrical Engineering Technical University of Denmark (DTU) Kongens Lyngby, Denmark Toke Franke
Silicon Power GmbH
Danfoss
Flensburg, Germany

Abstract—This paper presents a nonisolated Three Port Converter (TPC) with a unidirectional port for photovoltaic (PV) panels and a bidirectional port for energy storage. With the proposed topology single power conversion is performed between each port, so high efficiencies are obtained. A theoretical analysis is carried out to analyze all operating modes and design considerations with the main equations are given. A 4kW laboratory prototype is developed and tested under all operating conditions. Results obtained feature on efficiencies higher than 97% for all operating modes and all power levels from light load to full load.

Keywords—Energy storage, multiport converter, boost, buck, interleaved converter.

I. INTRODUCTION

Renewable energy generation has been gaining increasing interest in the last two decades of which photovoltaic (PV) generation is one of the most significant with a total global capacity of 177GW in 2014 [1]. However, the continuously growing number of decentralized energy sources negatively affects the quality of the grid voltage [2, 3]. In particular, the influence of distributed energy production has caused the power quality to deteriorate. In some areas the quality impaired so much such that the PV-inverter disconnects from the grid, due to the power quality being outside the range of the inverter setting resulting in disability to feed power to the grid [2, 3]. However, the deterioration in grid quality is not the only reason that the PV-plant work less reliable. Typically the electricity customers can experience a very high grid voltage in their electrical installations due to high injection of power from PV-plants to the grid [2, 3].

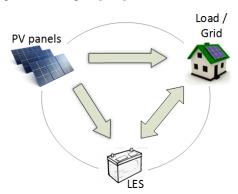


Fig 1. Power flow for a PV system with LES and grid support.

A local energy storage (LES) system can supply and buffer energy and thereby support the power quality of the electricity grid [3, 4, 5]. If the energy that severely deteriorates the power quality, instead of being feed directly to the electricity grid with full power is send in a smaller degree to the grid and in larger degree to the local energy storage system this resolves the problems with high power over a low timeframe. Later in the day when the production from the PV-plant is lower, power from the LES can be fed to the consumer, thereby equalizing the power to the grid over the day, and hence reducing the impact on the power quality. On the other hand, when distributed energy sources produce such amount of energy that the grid cannot support, local energy storage can support the grid by storing the surplus energy from other resources [3, 4, 5]. According to this description, power systems for grid-connected PV systems with LES need to operate with multiple power flows as shown in Fig 1.

Therefore, during the last decade an interest on research about three port dc-dc converters (TPC) capable of interfacing PVs to DC bus with energy storage systems has arisen. Previous work has demonstrated the advantages of TPC over single-input-single-output (SISO) topologies such as high efficiency, high power density, reduction of conversion stages and centralized control system and energy management system [6, 7, 8]. TPC topologies can be classified into three main categories: non-isolated, partially isolated, where two ports have a common ground, and isolated topologies.

Isolated and partially isolated TPC are generally derived from three basic cells [9]: half bridge, boost-half bridge and full bridge. Isolated topologies do not require a dc common bus, but rather use a magnetic coupling through a high-frequency transformer [9]. On the other hand, partially isolated topologies might require a common dc bus as well as magnetic coupling [9]. Besides providing isolation, these topologies have the advantages of wide voltage ranges [10, 11], zero-current and zero-voltage switching [12, 13] and simplicity to increment the number of ports [14, 15].

Non-isolated topologies are mostly derived from common step-down and step-up converters such as buck and boost dcdc converters. The main advantages of non-isolated TPC compared to isolated and partially isolated topologies are their

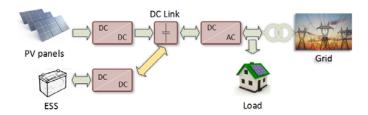


Fig 2. Block diagram of the traditional grid-connected PV plant with energy storage system (ESS) or LES.

high efficiency and high power density. Generally, these topologies are most commonly found to be two independent converters with a common DC bus as shown in Fig. 2 [16, 17]. This results in a lower efficiency when transferring energy from PV panels to the LES due to energy has to be converted at least two times.

Where previous work generally reports efficiency improvements in power conversion units by utilizing new kind of switching devices made of Silicon Carbide [18, 19, 20] or proposing optimized design procedures for the given topology [21, 22], this work follows a more direct approach by reducing the number of conversion stages while keeping its simplicity. This is done by adapting well-known buck and boost topologies capable of operating with all the power flows within one power conversion stage as shown in Fig.3. The objectives of this paper are to explain the different operation modes and design of the converter together with experimental results of the converter focusing on steady-state analysis and efficiency analysis under all operation modes.

II. PROPOSED TOPOLOGY

The proposed converter topology is illustrated in Fig 4. This converter can interface three different ports, i.e. battery, PV panels and the load. It allows operation as a single-input-single-output (SISO), dual-input-single-output (DISO) and single-input-dual-output (SIDO) converter, fulfilling in that way all the required power flows sketched in Fig 1.

A. Circuit description

The converter is directly derived from common and well-known buck and boost topologies. In applications where high voltage gain is not required, buck and boost topologies typically imply improved performance and efficiency [23, 24] due to the low number of passive components and power devices. Furthermore, simplicity of the topology and its well reported modelling equations, eases the design of the power stage as well as the control system.

An important drawback of conventional buck and boost converters are their poor performance for high-power highcurrent applications since the power is processed by two

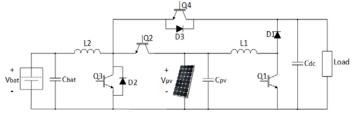


Fig 4. Proposed TPC topology.

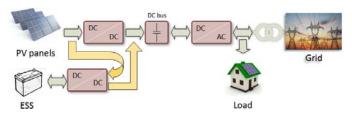


Fig 3. Block diagram of the proposed grid-connected PV plant with energy storage system (ESS) or LES.

power devices and required passive devices increase in size. Interleaving of converters is a common practice in buck and boost converters to increase the power rating and obtain a better performance and reduce passive components [25]. However, it comes with the challenges of unequal current sharing and increased complexity of the power stage. Besides reaching higher power levels, other benefits can be obtained by means of interleaving as have been addressed in other references:

- Input current and output voltage ripple reduction [26].
- Reduced EMI filter [27].
- Phase-shedding to improve efficiency at light load [28]
- Utilization of coupled magnetics to increase power density [29].

The proposed converter is composed by four power devices Q1, Q2, Q3 and Q4 which are the controllable switches to regulate the power flow and the voltages at the different ports. For D2 and D3 integrated freewheeling diodes can be used if IGBTs are utilized. On the other hand, for optimal efficiency operation external fast recovery or SiC diodes can be used. Two inductors are necessary, where L1 belongs to the boost stage for energy transfer from PV to Load and L2 is used for energy storage during the battery charge and discharge operation. Cpv and Cbat refer to the input capacitors of PV panels and battery respectively and Cdc refers to the capacitors of the DC bus. The load emulates the power demand from the household or the grid.

B. Operational principle

In Fig the equivalent circuits for each operating mode are highlighted. Maximum two controllable switches are used for the same operating mode, while the other two are inactive. The different case scenarios are subsequently described:

- 1. PV panels to Load/Grid (Fig 5a): When power is generated from the PV panels and the battery is fully charged, energy is transferred from the PV side to the loads through the boost stage L1-Q1-D1. Only one control signal (d1) for Q1 is required.
- 2. PV panels to Battery (Fig 5b): When there is no load, power generated from PV panels is used to charge the batteries through the buck stage L2-Q2-D2. In this case scenario the direct energy storage PV-Battery sketched in Fig is performed. One control signal (d2) for Q2 is required.
- 3. PV panels to Battery and Load (Fig 5c): When load power is low, power from PV panels is partially used to charge the battery and sent to the load through both the buck and boost stage.

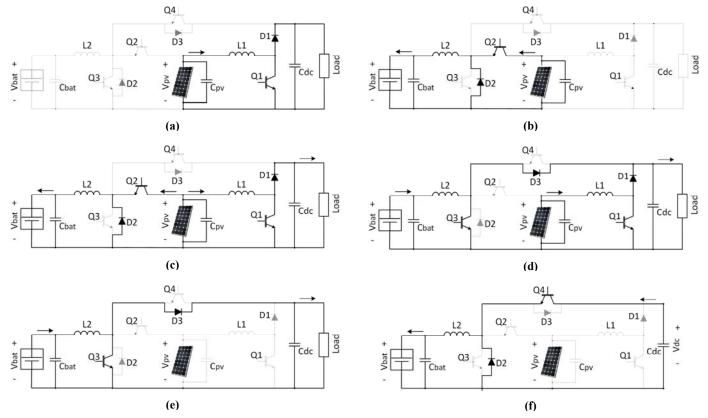


Fig 5. Operational circuitry for all operating modes, (a) PV to Load, (b) Direct storage PV to Battery, (c) PV to Battery and Load, (d) PV and Battery to Load, (e) Battery to Load, (f) Battery charge from Grid.

- 4. PV panels and Battery to Load/Grid (Fig 5d): When the load demand is high or the grid needs to be supported, power can be supplied from both, PV panels and battery. Power from PV panels is again supplied to the load from the boost stage L1-Q1-D1. Power from the battery to the Load is transferred through the boost stage L2-Q3-D3. Two control signals are required, d1 for Q1 and d3 for Q3.
- 5. Battery to Load (Fig 5e): When no power is generated from the PV panels, the load can be supplied with the battery through the boost stage L2-Q3-D3 using one control signal d3.
- Grid to Battery (Fig 5f): For a grid-connected application, the battery can be charged from the grid through the buck converter composed by L2-Q4-D2. Only one control signal (d4) for Q4 is required.

III. DESIGN PROCEDURE

The proposed topology allows an easy modular design to achieve higher power levels by means of interleaving as previously explained. Therefore, for the following design equations, interleaving of stages will also be considered.

A. DC Voltage Gain

Assuming an ideal converter operating in steady-state and CCM, by using the volt-second balance law on inductors L1 and L2 DC voltage gain for each operating mode can be calculated according to Eqs. 1-4.

$$\frac{V_{DC}}{V_{PV}} = \frac{1}{1 - d1} \quad PV \text{ to Load}$$
 (1)

$$\frac{V_{Bat}}{V_{PV}} = d2 \qquad PV \text{ to Battery} \tag{2}$$

$$\frac{V_{DC}}{V_{Bat}} = \frac{1}{1 - d3} \quad Battery \ to \ Load \tag{3}$$

$$\frac{V_{Bat}}{V_{DC}} = d4$$
 DC bus to Battery (4)

B. DC and AC Current and Voltage of Passive Components

DC current through the inductors and voltage across the capacitors are given in Eqs. (5)-(9). Note that the current sign in the following equations is defined according to the current flow for each case scenario in Fig for a better understanding. With Eqs. (5)-(6) the inductors can be designed accordingly and current ratings of semiconductors can be defined. With Eqs. from (7)-(9), capacitors can be chosen in terms of maximum voltage rating.

$$I_{L1,i} = \frac{I_{PV}}{n} \tag{5}$$

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{PV}}{n \cdot d2}$$
 PV to Battery

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{DC}}{n \cdot (1 - d3)} \quad Battery \ to \ Load \qquad (6)$$

$$I_{L2,i} = \frac{I_{Bat}}{n} = \frac{I_{DC}}{n \cdot d4}$$
 DC bus to Battery

$$V_{Cpv} = V_{PV} = V_{DC}(1 - d1) \tag{7}$$

$$V_{Chat} = V_{Bat} \tag{8}$$

$$V_{Cdc} = V_{Load} = V_{DCbus} \tag{9}$$

Where *n* refers to the number of stages and i=1..n.

The AC current through inductors should also be analyzed for each operation mode in order to find the worst case scenario.

$$\Delta i_{L1,i} = \frac{V_{PV}}{L1 \cdot f_s} d1$$

$$\Delta i_{L2,i} = \frac{V_{PV} - V_{Bat}}{L2 \cdot f_s} d2 \quad PV \text{ to Battery}$$
(10)

$$\Delta i_{L2,i} = \frac{V_{PV}}{L2 \cdot f_s} d3$$
 Battery to Load (11)

$$\Delta i_{L2,i} = \frac{V_{PV}}{L2 \cdot f_s} d3$$
 DC bus to Battery

Where f_s refers to the switching frequency.

Battery and DC bus capacitors, C_{Bat} and C_{DC} , should be chosen in the case scenarios when Battery port and DC bus port are operating in output mode to assure a stable output voltage. Therefore AC voltage across these capacitors can be defined as follows:

$$\begin{cases}
\Delta V_{Cdc} = \frac{V_{DC}}{Load \cdot C_{DC} \cdot n \cdot f_s} d1 & PV \text{ to Load} \\
\Delta V_{Cdc} = \frac{V_{DC}}{Load \cdot C_{DC} \cdot n \cdot f_s} d3 & Battery \text{ to Load}
\end{cases} (12)$$

$$\Delta V_{Cbat} = \frac{\Delta i_{Bat}}{8 \cdot C_{Bat} \cdot n \cdot f_s} \tag{13}$$

Where Load is the lead resistance in Ohms, $\varDelta i_{L1}$ refers to the AC current through L1, $\varDelta i_{L2}$ refers to the AC current through L2 in the cases "PV to Battery" and "DC bus to Battery", $\varDelta i_{Bat}$ refers to the AC current contained in I_{Bat} .

The AC current of I_{Bat} can be calculated with equations from (14)-(16) [26].

$$\Delta i_{Bat} = \frac{v_{Bat}}{L^2} \left(\frac{1 - 3 \cdot d}{d'} \right) \frac{d'}{n \cdot f_s} (0 < d < 0.33)$$
 (14)

$$\Delta i_{Bat} = \frac{V_{Bat}}{L2} \left(\frac{2 - 3 \cdot d}{d'} \right) \frac{d'}{n \cdot f_{S}}$$
 (0.34 < d < 0.66) (15)

$$\Delta i_{Bat} = \frac{V_{Bat}}{L2} \left(\frac{3 - 3 \cdot d}{d'} \right) \frac{d'}{n \cdot f_{S}}$$
 (0.67 < d < 1) (16)

IV. EXPERIMENTAL VERIFICATIONS

A two stages interleaved prototype as shown in Fig. 6 was built and steady-state and efficiency experiments are carried out, which are presented in this section. A photograph of the converter implemented is shown in Fig. 7. The main specifications and parameters of the prototype are shown in Tables I and II. Specification of the converter has been determined according to PV systems for household installations.

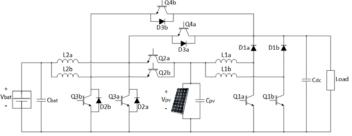


Fig 6. Proposed TPC topology with interleaved stages.

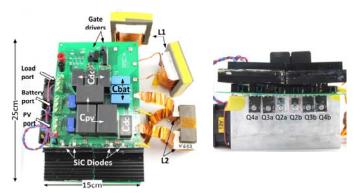


Fig 7. Prototype implemented

Table I. System Specifications.

Parameter	Value
Max. output Power (DC bus)	4000W
Max PV port Power	4000W
Max. Battery Charge/ Discharge Power	2400W
DC Bus Voltage	600V
PV Voltage range	200 - 500V
Battery Nominal Voltage	150V

A. Seady-State Response of Prototype

The steady-state waveforms of the prototype developed operating in the different operation modes are shown in Figs. 8-12. Fig. 8 shows the PV and DC bus port current and voltage waveforms when operating under PV to DC Bus operation at 2kW. The voltage ripple at the DC bus port is 1.4V (below than 0.5% ripple) and PV current ripple is reduced to 350mA due to interleaving the power stages. Fig. 9 shows PV port and battery port voltage and current waveforms under PV to Battery operation at 1kW, where the AC current at the Battery port is 100mA and the voltage ripple below 2V (below than 1.5% ripple). Fig. 10 shows battery port and DC bus port current and voltage waveforms in Battery to DC Bus operation at 1.6kW. In that case DC bus ripple is also kept below 0.5% ripple with 2.5VAC voltage. Fig. 11 shows DC bus port and battery port waveforms under DC Bus to Battery operation at 1kW. Fig. 11 shows the waveforms under PV port to Battery and DC Bus ports (SIDO) operation at 2kW delivering approximately 33% of the power to the battery port and 67% to the DC bus port. With the waveforms presented it can verified that the converter is able to operate in steady-state under all operation modes required.

Table II. Converter parameters and components.

Parameter	Value
IGBTs: Q1a, Q1b	IGW25N120H3
IGBTs: Q2a, Q2b, Q4a, Q4b	IGW30N100T
IGBTs: Q3a, Q3b	IGP40N65F5
SiC Diodes: D1a, D1b, D3a, D3b	IDH05S120
SiC Diodes: D2a, D2b	IDH15S120
Inductors: L1a, L1b	1mH
Inductors: L2a, L2b	0.8mH
Magnetic core L1	K8044E026
Magnetic core L2	K6527E060
PV Input Capacitor: Cpv	Film Cap. 15uF*2
Battery Port Capacitor: Cbat	Film Cap. 15uF*3
Load Port Capacitor: Cdc	Film Cap. 5μF*4, 15uF*1
Switching Frequency	20kHz

B. Efficeicny measurements

Conversion efficiency for the converter is determined measuring input and output voltage and current using an Agilent 34401A Precision DMM, with input voltage provided by a programmable power supply (Regatron) and output power dissipated in resistive loads. Power loss due to the fan operation and gate drivers is not considered, this was measured to be 6W in total.

Efficiencies have been measured under all operation modes for different power levels and PV voltage levels. Results are presented in Figs. 13-17. In particular, highest efficiencies are measured in the PV to Battery operation with a maximum efficiency of 98.7% with V_{pv} =500V at 1.2kW and lowest efficiency of 98.1% with V_{pv} =200V at 2.4kW. Lowest efficiencies are measured in Battery to DC bus and DC bus to Battery operation mode, shown in Figs. 15 and 16. Overall, worst case operation in terms of efficiency, is encountered when the converter is operating at high duty cycles, such that the IGBTs experience a high current stress.

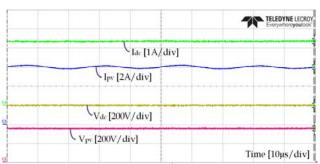


Fig 8. Steady-state waveforms in PV to DC bus operating mode.

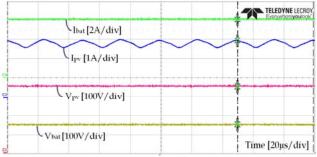
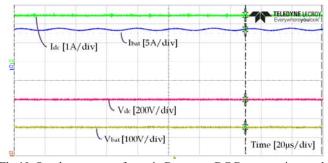


Fig 9. Steady-state waveforms in PV to Battery operating mode.



 $\textbf{Fig 10.} \ \textbf{Steady-state} \ waveforms \ in \ \textbf{Battery to DC Bus operating mode}.$

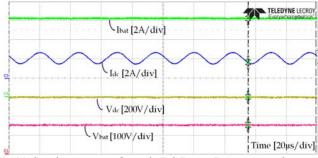
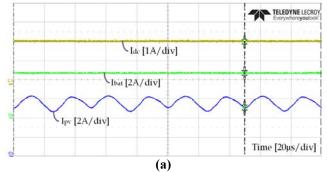


Fig 11. Steady-state waveforms in DC Bus to Battery operating mode.



Vdc [200V/div]

Vbat [100V/div]

Time [20µs/div]

(b)

Fig 12. Steady-state waveforms under PV to Battery and DC Bus operating mode; voltage (a) and current (b).

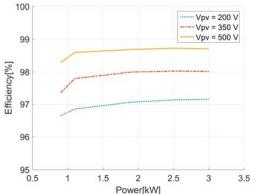


Fig 13. Efficiency results in PV to DC Bus operation.

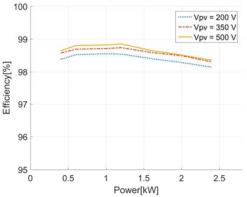


Fig 14. Efficiency results in PV to Battery operation.

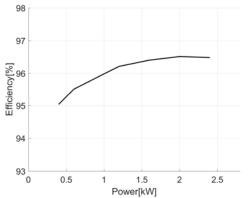


Fig 15. Efficiency results in Battery to DC Bus operation.

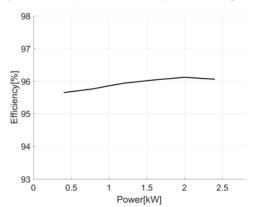


Fig 16. Efficiency results in DC Bus to Battery operation.

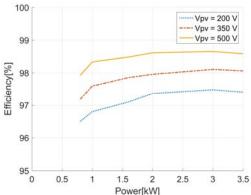


Fig 17. Efficiency results in PV to DC Bus and Battery operation.

V. CONCLUSION

In this paper, a three port dc-dc converter for PV systems with battery storage was presented. The converter was designed for household applications suitable for grid-tied systems, with a maximum power capability of 4kW and a maximum battery charge/discharge power of 2.4kW. This paper presented the topology operation modes and the design procedure. Experimental results show that this topology can operate under high efficiencies under a wide operating range and operation modes. The TPC converter presented is based on the well-known conventional buck and boost converter topologies, thereby easing the design and modelling. Furthermore, converter modularity to increase power rating is achieved by means of interleaving without adding high complexity to the design, as shown with the experimental prototype. Therefore, the proposed converter is suitable for high efficiency PV systems with battery storage where no galvanic isolation is required.

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