

Review

High-efficiency Silicon Heterojunction Solar Cells: A Review

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Abstract. Silicon heterojunction solar cells consist of thin amorphous silicon layers deposited on crystalline silicon wafers. This design enables energy conversion efficiencies above 20% at the industrial production level. The key feature of this technology is that the metal contacts, which are highly recombination active in traditional, diffused-junction cells, are electronically separated from the absorber by insertion of a wider bandgap layer. This enables the record open-circuit voltages typically associated with heterojunction devices without the need for expensive patterning techniques. This article reviews the salient points of this technology. First, we briefly elucidate device characteristics. This is followed by a discussion of each processing step, device operation, and device stability and industrial upscaling, including the fabrication of solar cells with energy-conversion efficiencies over 21%. Finally, future trends are pointed out.

Keywords. Photovoltaics, solar cells, silicon, heterojunctions, high efficiency.

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1 Introduction

Photovoltaic (PV) devices convert sunlight directly into electricity. With the sun providing the Earth with more than 10,000 times the energy humans currently consume, PV has the potential to be a large and environmentally benign energy source [1]. For a long time it remained expensive compared to traditional grid electricity. However, solar electricity can now compete with grid electricity at a price of 0.10–0.20 €/kWh. This is explained by the steady cost reduction of PV technology, mainly driven by increases in

manufacturing scale but also by important advances in technology [2, 3].

The PV properties of crystalline silicon (*c*-Si) were discovered at Bell Laboratories in New Jersey in 1941, and first concepts for silicon-based PV devices were described [4]. By 1954, a *c*-Si solar cell with an energy-conversion efficiency η of 6% was developed at the same facilities using diffused *p*-*n* junctions [5]. This device can be regarded as the first modern solar cell and its intended use was for the energy supply of telephone repeater stations. Cost considerations decided differently, however, and the first applications were found in satellites.

Large-scale terrestrial PV deployment was triggered in the early 1970s due to the rapidly rising cost of fossil fuels at the time and increasing environmental concerns about their use. Ever since then *c*-Si has dominated the PV market, with a current share close to 90%. Two factors explain this: *c*-Si is a stable, non-toxic, and abundant semiconductor with well-known physical properties. Next, the same material has had extraordinary success in the microelectronics industry, and the PV community profited significantly from the former's accumulated expertise. With *c*-Si wafers making up 40–50% of the cost of a finished PV module, increasing efficiency is a key route to cost reduction, enabling lower silicon usage per Watt of PV power. This, together with a reduced balance-of-system cost for high-efficiency PV modules, explains the interest in high-efficiency *c*-Si solar cell technology.

The ever-increasing electronic quality of silicon ingots has been an important lever for improving efficiencies of *c*-Si solar cells. Device processing has also become increasingly more sophisticated [2]. Generally, solar cells must generate charge carriers by optimal absorption of the spectrum of the sun, but also assure that these excess charge carriers are efficiently collected with minimal recombination on their way to the terminals of the device. This is the main driver to avoid recombination of generated charge carriers at the surfaces of solar cells, which becomes increasingly important when using thinner wafers. Over the years, a variety of surface-passivation layers were introduced for this purpose. Historically, most of the presently used passivating films were initially developed for gate dielectrics in microelectronics. Among these, arguably the best known is thermally grown silicon dioxide (SiO₂). The *c*-Si based solar cell with the highest energy conversion efficiency reported to date (25% under a standard air mass 1.5 global (AM 1.5 G) 1-sun spectrum) featured SiO₂ films as well [6, 7]. In microelectronics, device scaling-down dictates the search for alternative dielectrics to SiO₂ [8].

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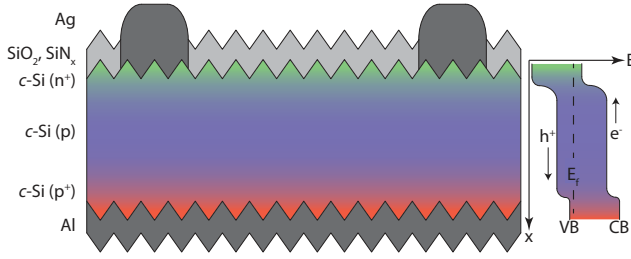


Figure 1. Sketch of diffused-junction solar cell, including its band diagram. The wafer is *p*-type. Structure is not drawn to scale.

In PV, a similar quest exists. Here, it is motivated rather by the (too) high processing temperatures such oxides require [9]. Wet-thermal oxides are grown at lower temperatures [10], and have proven their use in solar cells [11, 12]. Other PV-suitable dielectrics include amorphous silicon-nitride (*a*-SiN_x:H) [13, 14], SiO₂/*a*-SiN_x:H stacks [9, 15], or aluminum-oxide (Al₂O₃) films [16–18]. As the front-side passivation layer is insulating, contacts to the emitter are made by “spiking” the metal (usually silver) to the emitter, making direct contact with the electronically active absorber [19–21]. The sketch given in Figure 1 shows a device with a passivated front surface, but a fully metallized rear. High-efficiency diffused-junction solar cells for mass production increasingly feature a dielectric passivation layer at the rear as well, through which the base contact is “spiked” as well [22, 23].

Despite nearly recombination-free surfaces, enabled by the described dielectric passivation layers, the presence of highly recombination-active metal contacts remains an important efficiency limitation for *c*-Si solar cells. At best, ignoring cost issues, a trade-off between total contact area and surface passivation is made by locally opening the dielectric films. Recombination can then further be reduced by defining a locally diffused region of higher doping underneath the metal contacts [6]. However, this translates into an increase of the number of processing steps, which makes manufacturing less attractive.

A more elegant solution consists of the use of passivating (heterostructure) contacts, which simultaneously fulfill the passivation and contacting roles. In this article, we review the salient points of this technology and discuss its current status and future trends. This article is organized by following the fabrication processing sequence of silicon heterojunction (SHJ) solar cells.

2 The Heterojunction Concept

Key to the success of SHJ devices is the separation of highly recombination-active (ohmic) contacts from the crystalline surface by insertion of a passivating, semiconducting film with a wider bandgap [24]. For SHJ devices, ideally,

charge trickles through this buffer layer sufficiently slowly to build up a high voltage, but fast enough to avoid carriers recombining before being collected. The buffer layer may thus be considered as a semi-permeable membrane for carrier extraction [25]. The interface state density at the wafer surfaces should be minimal, else the buffer layers will enhance rather than inhibit recombination. The SHJ concept shows a great affinity in principle with metal-insulator-semiconductor (MIS) solar cells, which rely on quantum-mechanical tunneling of carriers through an insulating buffer layer [26]. However, such tunneling does not necessarily occur in SHJ devices, and diffusive transport of carriers may be at least as important [27]. For SHJ devices, hydrogenated amorphous silicon (*a*-Si:H) films a few nanometers thick are appealing candidates for buffer layers: their bandgap is slightly wider than that of *c*-Si and they can be doped relatively easily [28], either *n*- or *p*-type, enabling the fabrication of electronic heterojunctions.

The first *a*-Si:H/*c*-Si heterostructures were studied in 1974 by Fuhs and coworkers [29]. A few years later, intrinsic *a*-Si:H films were found to passivate *c*-Si surfaces remarkably well [30]. The first solar cell using a silicon heterojunction was reported in 1983 by Hamakawa and coworkers in the form of an *a*-Si:H/poly-Si heterojunction bottom cell in a tandem junction solar cell, the so-called Honeymoon cell [31, 32]. At about the same time, the electronic junction between doped *a*-Si:H and *c*-Si was increasingly investigated [33, 34]. In the late 1980s Sanyo, Japan started to incorporate heterojunctions into *c*-Si wafer-based solar cells. This was motivated by the study of the detailed properties of low-temperature emitters applicable to thin-film poly-Si solar cells [35]. The first devices used an *n*-type *c*-Si wafer and a thin boron-doped *a*-Si:H(*p*) emitter, and yielded efficiencies close to 12%. These solar cells featured somewhat modest fill factors (*FF*), which triggered further device characterization. This revealed a large (dark) reverse current density, pointing to a large interface state density [35]. A major breakthrough came with the introduction of a thin buffer layer of undoped *a*-Si:H between doped emitter and wafer, the so-called Heterojunction with Intrinsic Thin-layer (HIT) structure, to reduce the interface state density. This brought the efficiency up to 14.5% [35]. Notably, whereas the introduction of a buffer layer may have been motivated by the occurrence of modest *FF* values, with an increase of about 30 mV, it was the open-circuit voltage (*V*_{oc}) that especially benefitted from the use of such a buffer layer. Quite generally, it is the intrinsic buffer layer more than any other feature that enables the record-high values for *V*_{oc} and high efficiencies characteristic of SHJ solar cells. Using a similar heterostructure as a passivating back contact boosted cell efficiency to over 18% [36]. This result underlines the importance of having a heterostructure contact also at the rear side of the solar cell. A sketch of an *a*-Si:H/*c*-Si heterojunction solar cell with front and rear buffer layers, as developed by Sanyo,

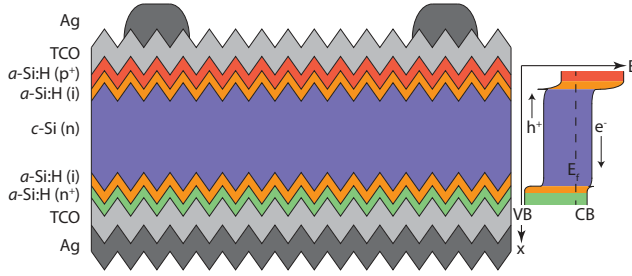


Figure 2. Sketch of a SHJ solar cell as first developed by Sanyo, Japan, including its band diagram. The wafer is *n*-type. Structure is not drawn to scale.

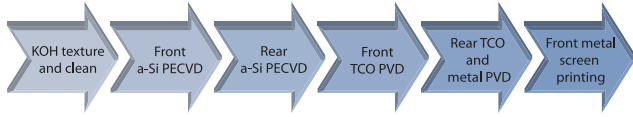


Figure 3. Basic process steps for SHJ devices.

and its band diagram, are given in Figure 2. Not coincidentally, the structure of the heterojunction solar cell shown in Figure 2 is remarkably similar to that of heterojunction injection lasers [37]. Both devices confine charge carriers to a semiconductor active layer by sandwiching it between wider bandgap films. By the turn of the millennium, an efficiency in excess of 20% was reported by Sanyo for large-area ($>100 \text{ cm}^2$) devices [38], which was further improved to an impressive value of 23.7% over the last few years [39]. Notably, this most recent result was obtained on a wafer only $98 \text{ }\mu\text{m}$ thick, about half of the current industrial standard for diffused-junction solar cells.

From a processing perspective, major advantages of the SHJ technology are the full exploitation of the excellent passivation properties of *a*-Si:H films, low-temperature ($<200^\circ\text{C}$) processing that enables the use of very thin wafers without causing substrate warping, and the small number of process steps to fabricate the device. The full device processing sequence is given in Figure 3.

Starting from an *n*-type *c*-Si wafer, an intrinsic *a*-Si:H passivation layer and a *p*-doped *a*-Si:H emitter are deposited on the front (illumination) side successively using plasma-enhanced chemical vapor deposition (PECVD). On top of the silicon layers, an anti-reflective transparent conductive oxide (TCO) film with a low sheet resistance ($3\text{--}100 \text{ }\Omega/\text{sq}$) is deposited by physical vapor deposition (PVD). Current collection at the front is made possible by a screen-printed metallic grid. On the back side, an intrinsic *a*-Si:H passivation layer is followed by a back-surface field (BSF) made from an *n*-type *a*-Si:H film. On this doped film, a stack of a TCO layer and a metallic contacting layer is deposited. Alternatively, a TCO layer combined with a metallization grid can be used, and the device can be finished with either a white back sheet for standard modules or a transparent back sheet for bifacial module configura-

tions. For the *a*-Si:H deposition sequence, one can also decide to deposit first the *i/n* stacks, followed by their *i/p* counterparts, to remedy possible defect creation, discussed in a following paragraph.

3 Substrates and Surface Preparation

Although the first diffused-junction *c*-Si solar cells were made on *n*-type *c*-Si, the space community quickly adopted *p*-type substrates for their improved space radiation hardness [40]. This is not a significant concern for terrestrial PV. However, *p*-type *c*-Si became the standard material for this market as well. Despite this, most contemporary high-efficiency *c*-Si based solar cells are based on *n*-type Czochralski (Cz) wafers. This is explained by several factors.

First, the cost of wafers is strongly influenced by their purity. Most transition metal point defects have larger electron- than hole-capture cross-sections. Consequently, for the same impurity concentration, the minority-carrier lifetime in the bulk, τ_{bulk} , of *n*-type material is usually higher than in its *p*-type counterpart [41]. Second, whereas light-soaking may detrimentally affect τ_{bulk} of *p*-type *c*-Si Cz material, e.g., when either boron and oxygen [42] or boron and iron [43] are simultaneously present, no such effects are known to exist for (uncompensated) *n*-type wafers. By choosing *n*-type wafers, Cz material can be used instead of the much more expensive, but oxygen leaner, float-zone (FZ) variant, without much loss in electronic quality. Third, surface states, mainly present in the form of silicon dangling bonds, feature a large electron-to-hole capture cross-section ratio (>100). Consequently, passivation of *p*-type *c*-Si wafers is usually more difficult to achieve than that of *n*-type wafers [44].

The preferred material for SHJ devices is mono- rather than block-cast multi-crystalline silicon. One reason is that, due to the inherent low-temperature processing of SHJ cells, no processing-induced improvement in the bulk of the wafer can be expected from impurity gettering [45] or defect hydrogenation [46]. Good-quality material with millisecond lifetimes throughout the wafers should be used from the start. Additionally, mono-crystalline wafers feature much better defined surfaces, which may be critical for conformal film deposition.

Usually, Si(100) substrates are taken for solar cell fabrication. Due to bond-density dependent crystal dissolution, Si(111) faceted pyramids are then revealed during anisotropic etching in alkaline solutions [47, 48]. This both lowers external optical reflection and improves internal reflection [49, 50]. The bases of the pyramids are typically $5\text{--}10 \text{ }\mu\text{m}$ on a side. Texturing is often combined in a single step with the removal of wire-saw damage, which can penetrate $5\text{--}10 \text{ }\mu\text{m}$ deep from each surface. To circumvent potential alkaline contamination of surfaces, al-

ternative random pyramid texturing solutions have been explored, including the use of tetramethyl ammonium hydroxide (TMAH) [51].

Importantly, the flat facets of pyramids allow for uniform deposition of the nanometer-thin a -Si:H films by PECVD, and the slightly thicker TCO layers by PVD, as both deposition techniques are fairly directional. As an example, a -Si:H layers deposited on pyramidally textured monocrystalline silicon are approximately 1.7 times thinner than films deposited for the same duration on flat surfaces [52]. Achieving uniform layer thickness is likely impossible on isotropically etched multi-crystalline surfaces, which have U-shaped valleys [53].

Prior to film deposition, well-controlled surfaces are required to obtain high-quality passivation [54–56]. Hydrofluoric acid (HF) etching is known from the semiconductor industry to produce c -Si surfaces which are contamination-free and chemically stable for subsequent processing [57]. Usually, such etching is part of a more elaborate cleaning scheme consisting of sequential oxidation (e.g., by peroxide solutions) followed by oxide removal in HF solutions (RCA cleaning) [58]. The oxidation step grows a layer on the wafer surface which encapsulates contaminants. The reduction step etches the oxide from the surfaces, removing these impurities. Surface states are hydrogenated simultaneously [59]. Promising results were recently reported using ozone-based treatments to replace the more costly and elaborate RCA clean [60]. In any case, of significant importance is the fast subsequent transfer of cleaned surfaces to the film deposition systems.

4 a -Si:H Film Deposition

4.1 Intrinsic a -Si:H Films

As argued earlier, for any high-efficiency c -Si solar cell, high-quality surface passivation is of extreme importance. Intrinsic a -Si:H films have been known for a few decades to yield good c -Si surface passivation [30, 61, 62], and have proved to be on par with the best dielectric films. Most a -Si:H(i) films are deposited by PECVD with silane (SiH_4), possibly diluted in H_2 , as a precursor. A plasma excitation frequency of 13.56 MHz is often used [63–66, 92], though the successful use of very high frequencies (VHF, e.g., 40 MHz [67, 92], or 70 MHz) [52, 68] was reported too. For device-grade films, typical deposition temperatures and pressures are 200 °C and 0.1–1 Torr. Other techniques reported to give good results are direct-current PECVD [69], hot-wire (also known as catalytic) CVD [70–72], electron cyclotron resonance CVD [73], and expanding thermal plasmas [74].

Hydrogenated amorphous silicon layers passivate c -Si surfaces mainly by hydrogenation of silicon dangling bonds, leading to a reduction of the interface defect density [30]. Classically, carrier recombination via defects is

assumed to happen via a Shockley–Read–Hall two-charge-state level. However, the defect responsible for interface recombination is more likely to be the silicon dangling bond. At equilibrium, according to the position of the Fermi level, this defect is either in a neutral, positively charged, or negatively charged state, accommodating respectively 1, 0, and 2 electrons. Based on this amphoteric behavior, new interface recombination models have been introduced and experimentally verified for a -Si:H/ c -Si structures [75–77]. We remark that chemical passivation removes such recombination-active defects, whereas field-effect passivation electrically shields defects from charge carriers in the wafer.

A necessary condition for good passivation is that the interface between wafer and a -Si:H film be atomically sharp [63, 78–80], meaning that silicon epitaxial growth is avoided, i.e., that no crystalline material is deposited. Once the films are deposited, post-deposition annealing varies both the electronic and material properties of the samples under study, and may be exploited to gain further physical insight. At low temperatures, annealing has proved to be quite beneficial for the electronic passivation of such interfaces [68, 72, 74, 81, 82]. As an example, Figure 4 shows how the effective carrier lifetime, τ_{eff} , changes over time when a c -Si wafer passivated on both surfaces with a -Si:H(i) is subjected to isothermal annealing. We note that for sufficiently well-passivated wafers, $1/\tau_{\text{eff}} \cong 1/\tau_{\text{bulk}} + 2 * S/W$, with S the surface recombination velocity and W the wafer thickness. Irrespective of the film deposition conditions, lifetime data can be fitted with satisfying accuracy to stretched exponentials of the form [68]

$$\tau_{\text{eff}}(t_{\text{ann}}) = \tau_{\text{eff}}^{\text{SS}} \left[1 - \exp \left[- \left(\frac{t_{\text{ann}}}{\tau} \right)^{\beta} \right] \right], \quad (1)$$

where β is the dispersion parameter ($0 < \beta < 1$), τ is the effective time constant, $\tau_{\text{eff}}^{\text{SS}}$ the steady-state value of τ_{eff} , and t_{ann} is the annealing time. From such a trend, it can be argued that annealing-induced passivation originates from a transfer of hydrogen from a higher silicon-hydride state in the a -Si:H film (close to the interface) to a monohydride c -Si surface state [68]. Infrared absorption measurements of the interface may point to a similar conclusion [81, 83]. Alternatively, low-temperature annealing-induced lifetime improvement can also be interpreted as due to equilibration of the interface with the network disorder present in the passivating film [65]. Regardless of the microscopic interpretation, the a -Si:H(i)/ c -Si interface passivation is attributed to chemical surface state passivation, rather than a field effect [68, 77].

Despite millisecond lifetimes, good passivation after annealing is not a sufficient criterion for a device-grade layer. Of much greater importance for high-efficiency devices is the passivation quality provided by as-deposited films. Con-

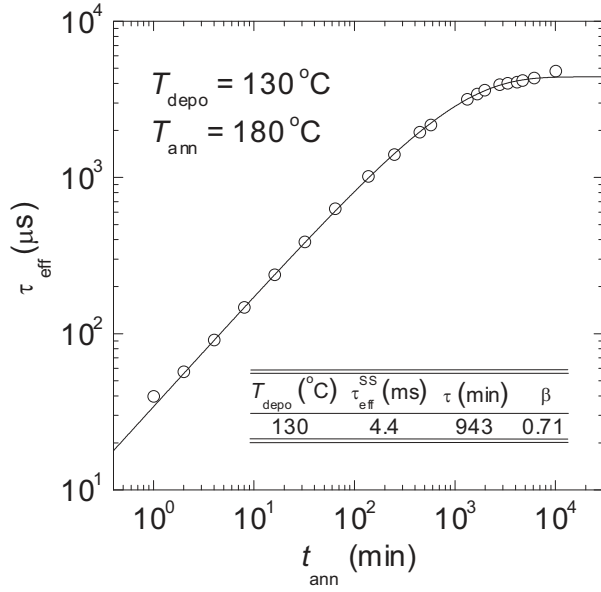


Figure 4. Measured values for τ_{eff} as function of t_{ann} for a $\sim 3.0 \Omega \cdot \text{cm}$ FZ wafer passivated on both sides by ~ 50 nm $a\text{-SiH}(i)$ films. τ_{eff} was calculated at $\Delta n = \Delta p = 1.0 \times 10^{15} \text{ cm}^{-3}$. The annealing temperature was fixed at 180°C . Symbols represent measured data. The solid line represents a stretched-exponential fit to the data. Values for the fitting parameters are given in the inset table. Data taken from [68].

sequently, it is crucial to control the properties of the $a\text{-Si:H}$ layers during deposition as accurately as possible [84]. Hydrogenated amorphous silicon layers have been studied in situ with various optical methods such as spectroscopic ellipsometry [64, 85, 86], Fourier-transform infrared (IR) spectroscopy [64], second-harmonic generation spectroscopy [70], and even carrier-lifetime measurements [87]. Since the properties of materials deposited by PEVCD are directly linked to the plasma properties, plasma diagnostics are very useful too, giving fundamental insight into deposition mechanisms. Optical emission spectroscopy of the plasma is an established technique for this purpose [88]. Recently, IR absorption spectroscopy using a quantum cascade laser was shown to probe in situ the SiH_4 depletion fraction during deposition with unprecedented resolution [89].

On glass, (as-deposited) device-grade intrinsic $a\text{-Si:H}$ is usually obtained close to the amorphous-to- (micro-) crystalline transition [90]. For plasma-deposited films, the transition is determined by the actual SiH_4 concentration in the plasma, $c_p = c(1-D)$, where c is the input SiH_4 concentration and D the SiH_4 depletion fraction in the plasma [91]. The transition occurs at relatively low c_p values, and is therefore obtained either by using plasmas where SiH_4 is highly diluted in hydrogen or by pure SiH_4 plasmas that are highly depleted. Recent work focused on the role of

the actual SiH_4 concentration during deposition of passivation layers [67]. These experiments confirmed that highly-depleted pure SiH_4 plasmas yield the best surface passivation. To come closer to the transition without risking detrimental epitaxial growth, hydrogen (H_2) plasma treatments during $a\text{-Si:H}$ growth via brief interruptions of the deposition have proven to be very effective as well [92].

4.2 Doped $a\text{-Si:H}$ Films

To fabricate heterojunction devices, doped films are required to form the emitter and BSF. Doped $a\text{-Si:H}$ layers are usually deposited in similar plasma systems as the intrinsic buffer layers, where for p -type layers either trimethylboron (TMB) or diborane (B_2H_6) is mixed in the SiH_4 gas flow, and for n -type films phosphine (PH_3) is used. These dopant gasses are generally strongly diluted in H_2 . As the introduction of dopant gasses in process chambers may result in persistent memory effects during subsequent depositions, either multi-chamber deposition systems or adequate chamber cleaning procedures need to be used when fabricating high-efficiency devices.

Although doped films principally produce a field effect at the interface with the wafer, their electronic passivation properties are often found to be inferior to those of intrinsic films [93, 94]. An example of the difference in passivation quality between intrinsic and doped $a\text{-Si:H}$ films can be seen in Figure 5. In this graph, τ_{eff} of samples with layers of device-relevant thicknesses deposited in EPFL's state-of-the-art processing sequence are shown. All results represent films in their as-deposited state (without any post-deposition annealing), deposited on random-pyramid textured wafers of $200 \mu\text{m}$ thickness. Despite higher defect densities in progressively thinner films [95], minority carrier lifetimes as high as 7 ms (at an excess carrier density of 10^{15} cm^{-3}) were obtained with intrinsic films as thin as 15 nm. The excess carrier density of the sample under 1-sun illumination at V_{oc} conditions is marked by an open circle in the figure. Defining the implied- V_{oc} as the energetic distance between the electron and hole quasi-Fermi levels,

$$\text{implied-}V_{\text{oc}} = \frac{kT}{q} \ln \left(\frac{(n_0 + \Delta n)(p_0 + \Delta p)}{n_0 p_0} \right), \quad (2)$$

one obtains a value of 738 mV at 1 sun for the intrinsic layers shown. In expression (2), k is Boltzmann's constant, T the temperature, q the elementary charge, n_0 and p_0 the electron and hole densities in the dark given by the doping of the wafer, and Δn and Δp the excess carrier densities during excitation (usually, $\Delta n = \Delta p$). Doped films deposited directly on wafer surfaces provide much poorer passivation. Figure 5 shows a lifetime curve for a sample with 15 nm thin p - and n -type layers deposited on the wafer surfaces. At an excess carrier density of 10^{15} cm^{-3} , a carrier lifetime of less than 0.1 ms is obtained. Under 1-sun illumination, this corresponds to an implied- V_{oc} value of only

613 mV. Similarly, SHJ devices with doped films deposited directly either on n - or p -type c -Si surfaces were limited by their low V_{oc} values [73]. Such drastic passivation loss is almost certainly related to doping-related defect generation in the amorphous host matrix. This effect is most severe for p -type films [96], but can also play a role in n -type films [94]. Note that this effect is not so much caused by the presence of dopant atoms in the a -Si:H material, but rather due to the shift of the Fermi level away from midgap [93, 97]. Such a shift can significantly lower the formation energy of native defects that counteract intentional doping. Increased doping may thus lead to higher defect densities, which ultimately pin the Fermi level. A marked increase in Urbach energy with doping is likely related to similar phenomena [95]. We note that the link between doping and defect formation is also well known for thick a -Si:H films [98].

Due to such defect formation, it is challenging to simultaneously fulfill both the surface passivation and doping requirements. For this reason, a few-nanometer-thick intrinsic buffer layer is typically inserted between the c -Si surface and the doped a -Si:H films for device fabrication, as was first demonstrated by Sanyo [35]. The benefit of inserting an intrinsic buffer layer underneath the doped layers is clearly demonstrated by the data in Figure 5 for a -Si:H stacks with total thicknesses of 25 nm. Again, on one wafer side a p -type a -Si:H layer was deposited, while the other side received an n -type film, making this asymmetric structure a SHJ solar cell precursor. At an excess carrier density of 10^{15} cm^{-3} , a carrier lifetime higher than 3 ms is now obtained. Under 1-sun illumination, this yields an implied- V_{oc} value of 729 mV. The slightly lower passivation quality compared to the case of intrinsic a -Si:H films without doped overlayers may be explained either by defect formation in the intrinsic layer induced by the p -type overlayer [96, 97], or by probing of the electron wavefunction through the ultra-thin i -layers into the defective doped overlayers [99].

4.3 Absorption in a -Si:H Films

The passivation provided by the intrinsic a -Si:H buffer layers produces the long effective carrier lifetimes shown in Figure 5. The fact that charge carriers can trickle through such layers eliminates the need to make contacts directly to the wafer with recombination-active metallization. These two considerations enable the high V_{oc} 's for which SHJ cells are known. However, the lifetime of minority carriers generated in the a -Si:H layers—particularly in the doped layers—is very short so that absorption in these layers is mostly parasitic. This is not a problem at the rear of the cell since the wafer absorbs all visible light, but light absorbed in the a -Si:H stack at the front of the cell leads to short-circuit current density (J_{sc}) losses [100]. Taguchi et al. first showed that the defect-rich p -layer in n -type SHJ devices reduces short-wavelength external quantum efficiency

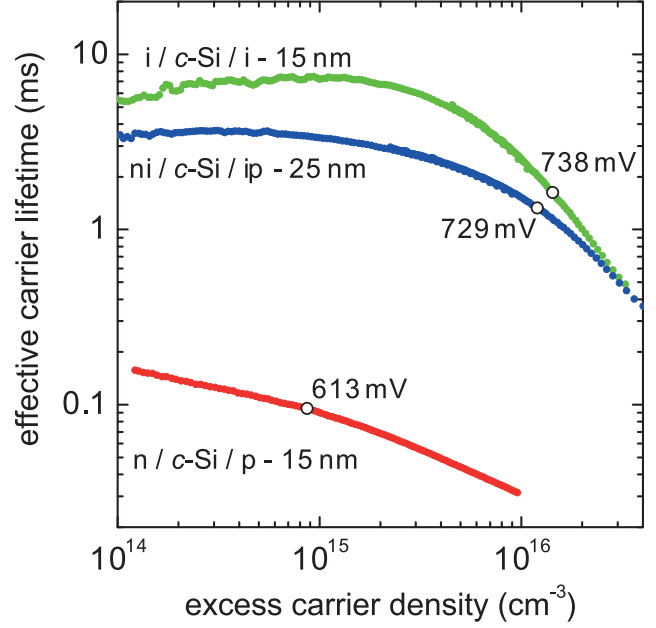


Figure 5. Passivated wafers, including solar cell precursor, consisting of device-relevant a -Si:H stacks. The wafers are random-pyramid textured n -type FZ-Si, with a resistivity of about 3 Ohm.cm. The indicated voltages correspond to the implied- V_{oc} under 1 sun illumination.

(EQE) and thus J_{sc} [35]. Thinning the p -layer leads to a near-linear increase in J_{sc} . However, V_{oc} and FF were reported to decrease rapidly for p -layers as thin as 3 nm, setting a minimum tolerable layer thickness [101].

Similarly, short-wavelength parasitic absorption in the front i -layer also causes a steady decrease in J_{sc} in finished devices, although a careful analysis of the variation in J_{sc} for various i -layer thicknesses indicates that around 30% of the carriers created in the i -layer are collected [100]. Again, a minimum tolerable thickness is set by the V_{oc} . This parameter drops rapidly for i -layers thinner than 5 nm, triggering a small drop in FF as well [100]. This trend originates from poor wafer surface passivation caused by the increasing proximity of the (defective) doped layers to the c -Si surface. An estimate of the J_{sc} losses at wavelengths below 600 nm for different intrinsic and p -type layer thicknesses is given in Figure 6. The data point with no buffer layer and p -type emitter represents the J_{sc} loss associated solely with parasitic absorption in the TCO film (compared to a SiN_x film). Overall cell efficiency is maximized for layers that are thick enough to passivate and collect carriers, but no thicker [36, 101, 102].

5 Transparent Conductive Oxide Deposition

As the lateral conductivity of doped a -Si:H layers is poor, the front of SHJ devices must be coated with a TCO layer

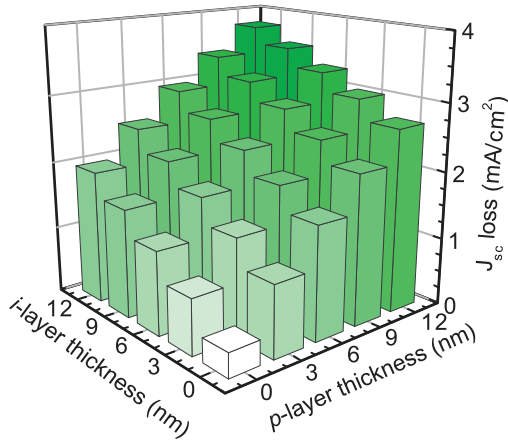


Figure 6. Estimate of the losses in J_{sc} associated with increasing intrinsic and p -type layer thicknesses. Data taken from [100].

to transport charge to the device terminals. This is similar to thin-film a -Si:H devices [103], however, SHJ solar cells usually also feature a metallic grid electrode as the front terminal. The sheet resistance $R_{sh} = 1/(qN\mu t)$ of the TCO must be sufficiently low (typically $<100 \Omega/\text{sq}$) to avoid deteriorating FF . The front TCO also serves as an antireflection coating in SHJ devices and, with a refractive index of about 2 at 600 nm, its thickness t is fixed at approximately 75 nm to minimize reflection losses. With t predetermined and mobility μ limited by material choice, low R_{sh} can only be achieved by increasing the free carrier concentration N . Free carriers, however, absorb parasitically in the IR, so that gains in FF are often offset by losses in J_{sc} [100]. Moreover and unfortunately, further increasing N usually leads to a decrease in μ [104]. Optimizing front TCO layers, as well as searching for high-mobility TCO materials, thus represents an important driving factor to further improve device performance.

For bifacial SHJ cells, a TCO layer with similar properties is required at the rear. A TCO layer is also common in cells with full rear metallization, but layer design in this case is not dictated by lateral transport constraints. Rather, the rear TCO layer in cells with full metallization serves primarily as a contacting and optical layer, and should be as transparent as is possible without incurring contact resistance losses.

Sputtered indium tin oxide (ITO) is often the TCO material of choice in SHJ devices [105, 106], in large part due to its great success in flat panel displays. Carrier mobilities of $\mu_{ITO} = 20\text{--}40 \text{ cm}^2/\text{Vs}$ are typical in ITO, and N_{ITO} may be tuned from $10^{19}\text{--}10^{21} \text{ cm}^{-3}$ by adjusting the flow of oxygen during sputtering, giving front ITO layers with sheet resistances as low as $20 \Omega/\text{sq}$ for films $\sim 80 \text{ nm}$ thin [107]. Several groups have recently been investigating alternative materials with higher carrier mobilities and therefore lower absorption for the same sheet resistance. These include

sputtered aluminum-doped zinc oxide (ZnO:Al) [108], low-pressure CVD boron-doped zinc oxide (ZnO:B) [109, 110], hydrogen-doped indium oxide (IO:H) [111], and other indium-oxide based materials [112].

An open question, and a potential challenge in implementing new TCOs in SHJ cells, is how the alignment of the TCO band structure with that of the doped a -Si:H layers underneath affects carrier transport [113]. As practically all available TCOs are n -type, an Ohmic contact with n -type a -Si:H can be assured. This is different for p -type a -Si:H, where the a -Si:H/TCO interface must rather allow for efficient band-to-band tunneling, where holes collected from the c -Si base into the p -type a -Si:H layer recombine with electrons from the TCO [114]. Thus, it is, as practice has shown, possible to make contact to both the emitter and base with the same TCO material. Finally, we remark that precise control of the TCO/metal contact may be equally crucial to obtain high FF values. Taking all of these considerations into account motivates the development of stacked TCO layers, where the different requirements can be decoupled.

6 Metallization

Fabricating narrow and tall metal lines helps reduce resistive and shadow losses at the front of SHJ devices. Screen printing is the most popular method of metallization in c -Si PV, with typical conductor lines $75\text{--}100 \mu\text{m}$ wide. The printed contacts of SHJ solar cells are usually cured at temperatures around 200°C . This is mainly to prevent damage to the films underneath, especially doped a -Si:H films that may be sensitive to excessively high annealing temperatures [93]. Low-temperature pastes for SHJ cells have a completely different composition, and hence rheological and printing performance, than metallization pastes used for standard diffused junction solar cells, which are usually fired at temperatures over 800°C . The challenge with low-temperature pastes is to achieve high conductivity while maintaining low contact resistance to the underlying TCO.

There are two types of low-temperature pastes which can be used for SHJ solar cells. Thermoplastic pastes have higher amounts of solvent, and controlling the curing temperature prevents solvent entrapment in the bonding area. For these pastes, heating initializes polymerization (curing) and helps long polymer chains to move freely, while cooling reduces their motion. Thermoset pastes behave differently. During polymerization, thermoset polymers form chemical bonds between adjacent chains. The result is a three-dimensional network that is much more rigid than the two-dimensional (linear) thermoplastic structure. An alternative, but closely related, metallization method is stencil printing. Stencils are thin foils of stainless steel in which patterns are cut with a laser or chemically etched. Electroformed stencil technology is able to provide openings down

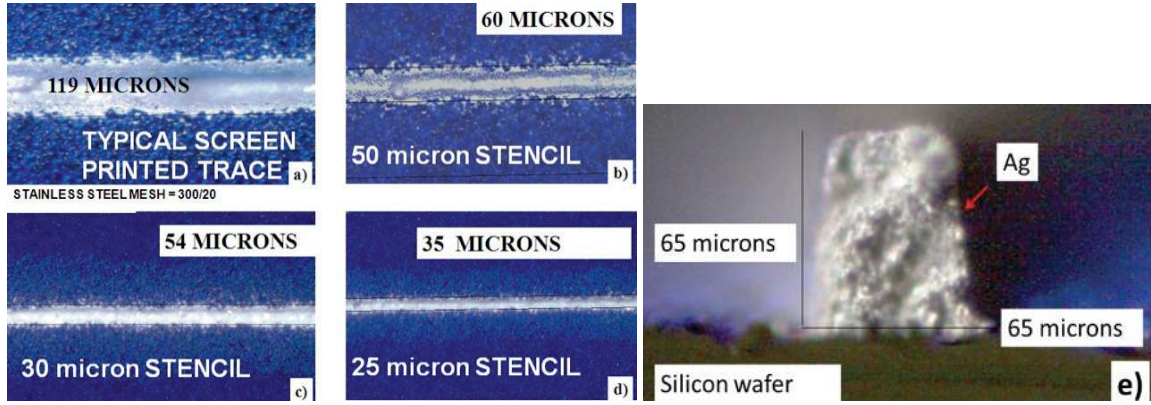


Figure 7. Examples of fine-line printing with low-temperature pastes, combined with stencil printing technology. Narrow lines down to 30–35 μm are obtained under laboratory conditions. Double print technology allows the achievement of narrow lines with high aspect ratio. Data taken from [115].

to 15 μm wide. Figure 7 shows examples of stencil printing a)–d) and double stencil printing (e) [115]. These pictures show that stencil printing produces lines down to 35 μm in width for a 25 μm stencil opening. Double printing allows one to achieve lines with aspect ratios of 1:1, as illustrated in Figure 7 e). This result was obtained through careful control of the snap-off distance in order to form a gasket on top of the first printed layer and not on the wafer [115].

The best low-temperature silver pastes reach resistivities down to 10–15 $\mu\Omega \cdot \text{cm}$, which is still a factor of 4 to 6 higher than that of standard high-temperature pastes. Consequently there is a strong drive for SHJ devices to move to alternative metallization schemes. Recently, good results were achieved using either additional busbars (total of 5) on $6 \times 6 \text{ inch}^2$ pseudo square wafers [116], or densely spaced metallic wires, replacing the busbars using technology developed by Day4 Energy in Canada [117]. An encapsulated SHJ cell with a certified efficiency of 19.3% was achieved using the latter scheme [117].

Increasing concerns [118] about the market price of silver motivate the search for alternative conductive pastes, including low-temperature copper pastes [119]. As ITO is a good barrier to metals [120], including copper, such pastes are attractive candidates for conventional metallization of SHJ cells. Perhaps even more attractive is copper plating for metallization. Its potential for the front grid metallization of SHJ devices was recently demonstrated by Kaneka, Japan, with large-area devices featuring efficiencies as high as 22.1% [121].

7 Device Results

Tables 1 and 2 show the best published SHJ devices fabricated on n - and p -type substrates by various groups working on this topic, to date. These tables clearly underline how SHJ technology recently emerged on a global

scale, with several groups now readily achieving efficiencies well above 20% and V_{oc} 's above 700 mV. Remarkably, while most other labs still achieve their best results on wafers thicker than 200 μm , Sanyo's record device is fabricated from a wafer only 98 μm thick. It is thanks to excellent passivation by the a -Si:H layers, but also to the use of such thin wafers that the value of the V_{oc} for this device is pushed as high as 745 mV, the highest V_{oc} for any (single junction) c -Si solar cell. When comparing this result to theoretical calculations of the maximum efficiency of silicon solar cells, one realizes that this is a very remarkable result. Such calculations yield a maximum V_{oc} (under 1-sun illumination) of 769 mV for a 100 μm wafer [122]. In these calculations, only the intrinsic radiative and Auger recombination processes were considered. To approach such maximum V_{oc} values in practice, the development of conductive passivating contacts was pointed out as a key requirement [122]. Sanyo's results clearly demonstrate that the SHJ concept is highly suitable for such a purpose. We remark here that the V_{oc} of the cell fabricated by our group is very close to the implied- V_{oc} shown for the solar cell precursor in Figure 5, demonstrating the usefulness of carrier lifetime measurements as a diagnostic tool throughout the full SHJ solar cell process.

Comparing results on p - and n -type substrates, a discrepancy can be seen, even though we showed that it is possible to break the 700 mV V_{oc} barrier for p -type substrates [123]. Further work is needed to find out whether there are fundamental reasons, apart from those mentioned in section 3, for the observed deviation in results on p - and n -type wafers [124, 125]. We note here that by using an epitaxially grown n -type emitter passivated with a -Si:H, IBM, USA demonstrated solar cells on p -type FZ wafers with efficiencies in excess of 20% [126]. At the rear, a regular heterostructure BSF is present, making this cell a hybrid SHJ solar cell.

Affiliation	η (%)	V_{oc} (mV)	J_{sc} (mA \cdot cm $^{-2}$)	FF (%)	A (cm 2)	Status	Year
Sanyo [39], Japan	23.7	745	39.4	80.9	100, Cz	IC	2011
Kaneka [121], Japan	22.1	729	38.5	79.1	\sim 220, Cz	–	2011
RRS [116], Switzerland	21.9	735	38.5	77.5	4, Cz	–	2011
EPFL [127], Switzerland	21.8	726	37.8	79.7	4, FZ	–	2011
HHI [128], Korea	21.1	721	36.6	79.9	\sim 220	–	2011
CEA-INES [129], France	21	732	36.9	78.3	105, FZ	–	2011
CIC [112], Japan	20	685	36.9	79.2	243, Cz	–	2011
HZB [130], Germany	19.8	639	39.3	78.9	1, FZ	IC	2006
NTUST [131], Taiwan	19.6	690	39.1	72.7	1, FZ	PR	2011
Univ. Hagen [132], Germany	19.3	675	37	77.3	FZ	IC	2009
FhG-ISE [133], Germany	18.7	\sim 705	\sim 35.0	\sim 75	4, FZ	–	2010
IEC [69], USA	18.3	694	35.7	74.2	0.55, Cz	IC	2008
LG [134], Korea	18.2	687	33.3	78.9	1, FZ	–	2010
NREL [135], USA	18.2	694			0.9	–	2009
Titech [136], Japan	17.9	671	35.2	76	<1 , Cz	PR	2008
AIST [137] [#] , Japan	17.5	656	35.6	75	0.2	PR	2009
Sungkyunkwan Univ. [138], Korea	17.4	631	36.3	76.1	Cz	PR	2011
LPICM [139], France	17.2	701	30.8	79.6	4	–	2011
Utrecht Univ. [140], the Netherlands	16.7	681	33.5	73.1	1 FZ	–	2011
CNR-IMM [141], Italy	16.2	573	36.6	77	1, Cz	–	2005
Delft Univ. [142], the Netherlands	15.8	646	32.9	74.3	FZ	PR	2011
Univ. Toronto [143], Canada	15.5	679	31.7	72.4	4.2, FZ	–	2011
Kyung Hee Univ. [144], Korea	14	575	34.4	71	Cz	PR	2011
ECN [145], the Netherlands	13.2	635	29.1	72	21, FZ	–	2010
KIER [146], Korea	12.8	<600			Cz	–	2009
ENEA [147], Italy	12.4	526	31.9	74	mc	–	2010
UPC [189], Spain	10.9	525	28.6	72.8	FZ	PR	2006

[#] active area efficiency. The status column indicates whether the result was independently confirmed (IC), or appeared in a peer-reviewed publication (PR).

Table 1. Device results on n -type c -Si wafers.

For reference, Table 3 gives the most remarkable homo-junction silicon solar cell efficiencies. At 25%, the passivated emitter, rear locally diffused (PERL) solar cell developed at the University of New South Wales (UNSW), Australia shows the highest efficiency reached for a c -Si wafer-based device [6]. This cell was fabricated from a p -type FZ wafer. While the result is by all means impressive, it cannot be repeated in mass manufacturing due to the many processing steps involved, including extensive lithographical patterning needed for contact opening definition. The V_{oc} values of the best SHJ cells sig-

nificantly exceed those of the UNSW device, underlining the beneficial effect of using buffer layers as semi-permeable (carrier) membranes. The interdigitated back-contact (IBC) solar cell, developed by SunPower, USA, shown in the same table, is made with actual production technology. This cell was fabricated from a n -type Cz wafer. Of note, the most recent results for such interdigitated back-contacted solar cells were obtained using “passivating contacts”, likely explaining the impressive V_{oc} values, but of which further details are undisclosed [157].

Affiliation	η (%)	V_{oc} (mV)	J_{sc} (mA · cm ⁻²)	FF (%)	A (cm ²)	Status	Year
EPFL [123], Switzerland	19.7	717	37.9	72.7	4, FZ	–	2011
NREL [71], USA	19.3	678	36.2	78.6	0.9, FZ	IC	2010
Titech [148] [#] , Japan	19.1	680	36.6	76.9	0.8, FZ	PR	2011
HZB [149], Germany	18.5	633	36.8	79.1	1	PR	2009
Univ. Stuttgart [150], Germany	18.1	670	35.7	75.6	2	–	2010
LPICM [151], France	17	662	33.0	77.6	25, Cz	PR	2009
ENEA [152], Italy	17	601	37.1	76.3	2.25	PR	2004
Univ. Hagen [132], Germany	16.6	655	31.0	81.6	FZ	–	2009
NCHU [190], Taiwan	16.4	645	34.8	73.0	1	PR	2008
IMEC [153], Belgium	16.4	644			1, FZ	–	2005
Univ. of Valencia [154], Spain	15.2	591	33.8	77.6	1, Cz	–	2010
CAS [155], China	15.1	585	34.6	74.7	<1, Cz	PR	2009
Utrecht Univ. [156], the Netherlands	14.9	571	33.3	78	1, FZ	–	2005
UPC [193], Spain	14.5	613	30.3	77.9	FZ	PR	2008
SUNY [54], USA	10.6	550	30	64	0.03	PR	1997

[#] active area efficiency. The status column indicates whether the result was independently confirmed (IC), or appeared in a peer-reviewed publication (PR).

Table 2. Device results on *p*-type *c*-Si wafers.

Affiliation	η (%)	V_{oc} (mV)	J_{sc} (mA · cm ⁻²)	FF (%)	A (cm ²)	Year
UNSW [6], Australia	25	706	42.7	82.8	4 FZ, <i>p</i>	1998
SunPower [157], USA	24.2	721	40.5	82.9	155 Cz, <i>n</i>	2010

Table 3. Best *c*-Si homojunction solar cells for *p*- and *n*-type *c*-Si wafers.

8 Device Operation

8.1 Basic Considerations

The TCO/doped *a*-Si:H interface was already briefly discussed. Due to the *n*-type nature of most TCOs, the *n*-type and *p*-type contacts must act as Ohmic and band-to-band tunneling junctions, respectively [114]. The detailed properties of the interfaces, including the band offsets between the *a*-Si:H layers and the *c*-Si wafer, are crucial in carrier transport, as they influence band bending in the structure and carrier transport across the junction. For relatively dense *a*-Si:H films, the *a*-Si:H/*c*-Si conduction and valence band offsets are approximately 0.25 and 0.45 eV, respectively [158]. These values depend on the deposition conditions: the valence band offset increases linearly with the hydrogen content of the films, though the conduction band offset remains essentially fixed [158]. This may explain why not all films that passivate well are necessarily suitable for high-efficiency SHJ devices. Doping of the films or substrate does not alter the band offsets [159]. We remark that band offsets are usually determined by photoelectron spectroscopy [158–160], although a simpler coplanar conductance technique was recently proposed as well [161].

To better understand the precise transport mechanism in SHJ devices, (temperature-dependent) dark *I*-*V* measurements have been proven to be simple and useful, as was pointed out early on by Sanyo [35]. Such characterization was pursued by several other groups too [27, 54, 162–165]. Typically, dark *I*-*V* measurements reveal two distinct operation regimes for SHJ devices [165, 166]. At low bias (0.1 V < *V* < 0.4 V) multistep tunneling [33, 167] is the dominant mechanism, and is influenced by the detailed band structure of the heterojunction (including band offsets and the density of states in the *a*-Si:H gap) [27]. Here, the insertion of a high-quality intrinsic *a*-Si:H buffer layer may be crucial for suppressing the probability of tunneling through localized states in *a*-Si:H [27]. However, the current density in this regime is much smaller than J_{sc} , making this mechanism not so relevant for the performance of high-quality devices [27, 165]. At high forward bias (0.4 V < *V* < 0.8 V) the diffusion model that is valid for conventional homojunction solar cells determines carrier transport for SHJ devices as well. In this regime, the most relevant microscopic parameter is the interface passivation quality, which directly dictates V_{oc} [27].

As argued earlier, to assure high V_{oc} values, excited carriers should only be collected just before they would recombine. To accomplish this, an essential condition is the absence of defects leading to interface recombination [24]. Next, to act as a semi-permeable carrier membrane, the band offsets and the (low) carrier mobility of the buffer layers are of fundamental importance [168]. The beneficial effect on the V_{oc} of a low carrier mobility in the emitter of a solar cell can actually be understood from basic (homojunction) device physics. Consider the saturation current density J_0 , which is the sum of an emitter and base contribution:

$$J_0 = qn_0p_0\sqrt{\frac{kT}{q}}\left[\frac{1}{N_M^E}\sqrt{\frac{\mu_m^E}{\tau_m^E}} + \frac{1}{N_M^B}\sqrt{\frac{\mu_m^B}{\tau_m^B}}\right]. \quad (3)$$

In this expression, $N_M^{i=E,B}$ are the majority-carrier concentrations, while $\mu_m^{i=E,B}$ and $\tau_m^{i=E,B}$ are the minority-carrier mobilities and lifetimes in, respectively, the emitter (E) and base (B). As a high V_{oc} demands a low J_0 value, it is advantageous to use emitters with a low minority-carrier mobility-to-lifetime ratio. We remark that the experimental values obtained for the carrier mobility of a -Si:H are slightly too high to yield the V_{oc} 's typically obtained for SHJ devices, however. This points to the fact that band offsets may play a role too in operation of a -Si:H films as semi-permeable carrier membranes, and thus the operation of SHJ devices. More quantitatively, simulation programs such as AFORS-HET developed by HZB in Germany [169], or others [170], or device-circuit modeling [171] may further aid in understanding SHJ device operation.

8.2 Operation in the Field

In practical applications, solar cells are exposed to sunlight for many hours a day for many years. The operating temperature of PV modules can be quite high, and the temperature coefficient, i.e., the efficiency loss per unit change in temperature, is an important parameter. With values of about $-0.45\%/K$ for diffused-junction solar cells, high-quality SHJ devices outperform their conventional counterparts in the field with values $<-0.25\%/K$ [116, 172]. The smaller temperature sensitivity is mainly due to the high V_{oc} of SHJ devices [27].

Next, Si dangling bond generation by light soaking is an important phenomenon affecting the performance of thin-film silicon solar cells. Annealing at low temperatures can restore intrinsic a -Si:H films to their original state, yielding a fully reversible phenomenon, the so-called Staebler–Wronski effect (SWE) [173]. For thin-film silicon devices, the SWE can result in a relative efficiency drop of close to 20% [174]. The passivation of c -Si by a -Si:H films was observed to suffer from similar degradation [175–177]. As an example, we observed a minority carrier lifetime drop from 8 ms to 5 ms on a c -Si(111) wafer passivated with a -Si:H(i)

after more than 500 hrs of light soaking, and the long-term degradation was found to follow a power law [176]. Extrapolation leads to a carrier lifetime still in excess of 2 ms after 40 years of light exposure. Actual carrier lifetimes will probably be higher, as the data already appear to saturate after about 500 hrs, likely due to the self-limiting nature of the SWE. As the V_{oc} depends logarithmically on the carrier lifetime, such a drop in passivation should only result in at most a few mV loss over several decades of exposure. Medium-term degradation experiments point to the same conclusion for SHJ devices [36] as well as SHJ modules [178].

9 Industrialisation

So far the only company to have implemented a large volume production capacity (>600 MW) for SHJ devices and PV modules is Sanyo, Japan. With its key patents expiring [179], and with the recent results obtained by several groups worldwide, there is now a large interest in commercialization of this technology. This arises from several factors:

- The SHJ fabrication process is similarly simple in number of processing steps as standard c -Si solar cell processes (without local back contacts and a selective emitter, as sketched in Figure 1), but allows for efficiencies above 20% on n -type Cz wafers.
- There is a lot of experience in the flat-panel display and thin-film PV industries in the development of tools for providing the key high-quality layers (a -Si:H and TCO layers). Hence, upscaling and very low coating costs should not be an issue.
- The high temperature coefficient of SHJ modules leads to a better energy yield.
- SHJ cells benefit more from thinner wafers than any other c -Si cell type because of their near-perfect interface passivation.

Several companies are working on SHJ cells (e.g., Sanyo [27, 35, 36, 38, 39, 84, 172, 180, 197], Kaneka [121], and CIC [112] in Japan, and Hyundai Heavy Industries [128], and LG Electronics [134] in Korea) and some equipment providers offer production solutions as well, including Roth and Rau, Switzerland/Germany [66, 92, 116, 117]. Challenges for production include sourcing high-quality n -type Cz material, carefully controlling all process steps from cleaning to TCO deposition, and developing a module design that is compatible with TCOs and low-temperature contacting schemes.

10 Future Directions

Figure 8 compares the internal quantum efficiency of the best UNSW cell, introduced in Table 3, with a recent HIT

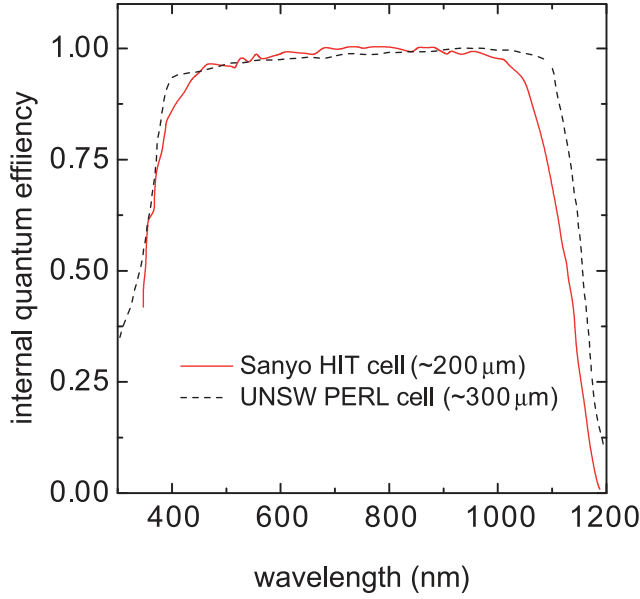


Figure 8. Comparison of the internal quantum efficiency of a UNSW PERL cell with a recent heterojunction device from Sanyo. Data taken from [172] and [196].

cell developed by Sanyo [172, 180]. Clearly, important further gains in efficiency are possible by reducing parasitic absorption at both the front and rear of SHJ devices and by increasing the optical confinement of the devices [100]. Parasitic absorption can be lowered by improving the transparency of the TCO films and by using silicon-based alloys for window layers, similar to high-efficiency thin-film silicon solar cells [181]. For SHJ devices, such films should not jeopardize surface passivation and emitter formation. Tested alternatives to replace the *a*-Si:H stacks are (microcrystalline) silicon oxides [136, 137, 182, 183] and carbides [148, 184–186]. Microcrystalline silicon has a lower but indirect bandgap and features a higher doping efficiency, making it an attractive material for emitter [52, 187–190] and BSF formation [189, 191–193] as well. Of note is that such films may also resolve possible contact problems between TCO-layers and doped films [192, 194].

To increase J_{sc} even further, other device designs that reduce front metal contact shading are needed. A natural choice here is to combine the IBC solar cell design from SunPower with SHJ contacts. Such a device eliminates all metal at the front of the cell, and places both emitter and BSF at the rear. Not only is this design aesthetically pleasing, but with the emitter placed at the rear, the antireflection coating and front passivation layer can be made much more transparent too, as they do not have to fulfill transport roles anymore. IBC-SHJ cells have been pursued by several groups (see Table 4). Impressively, LG, Korea, reported recently efficiencies as high as 23.4% without any

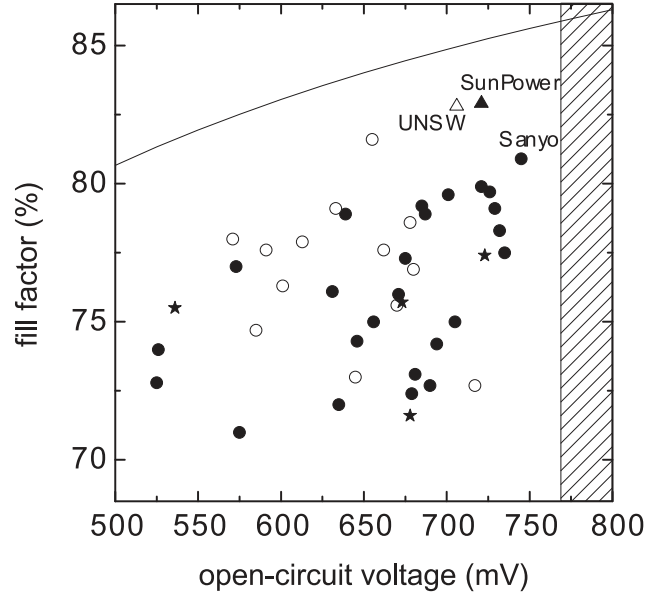


Figure 9. V_{oc} vs. FF relation for published devices. Discs: SHJ solar cells, stars: IBC-SHJ devices, triangles: homo-junction devices. Open symbols: *p*-type wafers, closed symbols: *n*-type wafers.

high-temperature processing step [195] underlining the potential of this combination.

Next, for all *c*-Si PV technologies, a general trend is the use of ever thinner wafers, mainly explained by the high cost of *c*-Si in a finished PV module. Obviously, thinner wafers allow one to cut more wafers from the same ingot, lowering the per-wafer cost. From a processing point of view, thinner wafers need increasingly good passivation of their surfaces, and process-induced warping becomes a concern. As SHJ fabrication occurs at low temperatures, warping is absent for wafers down to at least 70 μm thick [197]. Next, thanks to almost perfect passivation, V_{oc} actually increases in SHJ cells when using thinner wafers. Innovative light management schemes are required for thin wafers, however, to ensure that high values for J_{sc} are maintained.

It may be useful at this point to consider semi-empirically how high the efficiency of a SHJ device ultimately may be. For this, we plotted in Figure 9 the FF vs. V_{oc} relation for all devices given in Tables 1–4, including the results of UNSW and SunPower. The crosshatched area represents the highest theoretical achievable V_{oc} for any single-junction *c*-Si device of 100 μm , under 1-sun illumination, which is 769 mV [122]. Next, we plotted the ideal FF as a function of the V_{oc} , valid for homo-junction devices, which is given by the empirical relation [203],

$$FF = \frac{\frac{qV_{oc}}{kT} - \ln\left(\frac{qV_{oc}}{kT} + 0.72\right)}{\frac{qV_{oc}}{kT} + 1}. \quad (4)$$

Affiliation	η (%)	V_{oc} (mV)	J_{sc} (mA · cm ⁻²)	FF (%)	A (cm ²)	Year
LG [195], Korea	23.4	723	41.8	77.4	4, n	2011
HZB [198], Germany	20.2	673	39.7	75.7	1, FZ, n	2011
CEA-INES [199], France	15.7	678	32.4	71.6	25, FZ, n	2010
IEC [200], USA	15	670	34.2	65.2	FZ, n	2010
ENEA [201], Italy	11	687	32	50	FZ, p	2007
Univ. Toronto [202], Canada	8.1	536	20	75.5	1, FZ, n	2009

Table 4. Device results of IBC-SHJ devices.

In this expression, the diode ideality factor is assumed to be 1, and the series (shunt) resistance of the device are assumed to be infinitely small (large). The figure shows that, considering the V_{oc} limit, ideally $FF = \sim 86\%$ may be obtained. Assuming that for a SHJ device a value for J_{sc} equal to that experimentally realized in the PERL cell can be achieved one obtains an efficiency value of 28%. From Figure 9, it is clear that major improvements may be required to bring the FF closer to its ideal value, including an increased understanding to what extent these values may be possible for SHJ devices.

Finally, we point out that SHJ contacts are also finding increasing use in non-wafer-based PV technologies. A first example is the use of a SHJ emitter in fine-grained polycrystalline thin-film silicon solar cells, where a classical diffused junction would destroy the absorber material due to too high processing temperatures [54, 204, 205]. As a matter of fact (and as pointed out already), it was precisely this application that started all SHJ activities for Sanyo [35]. SHJ emitters have also been used in hot-wire/PECVD grown core-shell microwire structures [206]. The efficiency of these devices was extremely low ($\sim 0.1\%$), however. Nonetheless, this may be a viable approach for certain niche PV applications when high-quality microwire arrays are used [207] and film conformality is mastered. Third, SHJ contacts have recently been applied to both germanium [208] and gallium arsenide [209] substrates, which are materials with much higher absorption coefficients compared to c -Si, enabling much lower material consumption.

11 Conclusions

In this article, the technology of silicon heterojunction solar cells was discussed and reviewed. We explained how the record-high values for the V_{oc} are linked to the surface passivation properties of extremely thin amorphous silicon layers, but also to the ability of such thin layers to act as a semi-permeable carrier membrane. Control of the different interfaces present in the heterojunction structure is of high importance to enable very high efficiency values. On a global scale a rapidly increasing number of groups mas-

ter these techniques, and show that with industrially viable processes devices with energy conversion efficiencies well above 20% are now a reality for n -type c -Si Cz wafers. These results show that silicon heterojunction technology indeed holds great promise to produce high-efficiency solar cells on an industrial scale.

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