

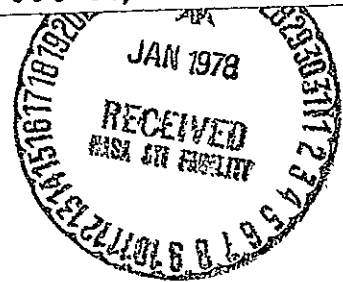
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HIGH FREQUENCY CAPACITOR-DIODE VOLTAGE MULTIPLIER  
DC-DC CONVERTER DEVELOPMENT

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16. Abstract A power conditioner was developed which used a capacitor-diode voltage multiplier to provide a high voltage without the use of a step-up transformer. The power conditioner delivered 1200 Vdc at 100 watts and was operated from a 120 Vdc line. The efficiency was in excess of 90 percent. The component weight was 197 grams. A modified boost-add circuit was used for the regulation. A short-circuit protection circuit was used which turns off the drive circuit upon a fault condition, and recovers within 5 ms after removal of the short. High energy density polysulfone capacitors and high-speed diodes were used in the multiplier circuit.					
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## FOREWORD

This report documents work performed by the Hughes Aircraft Company during the period of 14 June 1976 to 14 July 1977 for the NASA Lewis Research Center under Contract NAS 3-20111. The NASA Project Manager was William T. Harrigill. The Program Manager at Hughes Aircraft Company was Jack J. Kisch. Mr. Robert M. Martinelli was responsible for the circuit design.

## ABSTRACT.

A power conditioner was developed which used a capacitor-diode voltage multiplier to provide a high voltage without the use of a step-up transformer. The power conditioner delivered 1200 Vdc at 100 watts and was operated from a 120 Vdc line. The efficiency was in excess of 90 percent. The component weight was 197 grams. A modified boost-add circuit was used for the regulation. A short-circuit protection circuit was used which turns off the drive circuit upon a fault condition, and recovers within 5 ms after removal of the short. High energy density polysulfone capacitors and high-speed diodes were used in the multiplier circuit.

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## 1.0 INTRODUCTION

Voltage multiplier power supplies have been used for many years. Cockroft and Walton built an 800 kV supply for an ion accelerator in 1932.<sup>1</sup> Since that time the capacitor-diode voltage multiplier (CDVM) has been used primarily when high voltages and low currents were required. The use of CDVM circuits reduces the size of the high voltage transformer and, in some cases, makes it possible to eliminate the transformer entirely.

Until recent years the CDVM circuit was not seriously considered for high efficiency, low weight power supplies delivering a considerable amount of power. However, recent technological developments have made it possible to design CDVM converters with an efficiency comparable to that of the more conventional transformer-rectifier-filter circuit, but at a considerably lower weight. Several developments in the component field have contributed to this possibility. The availability of fast switching diodes and transistors has made it possible to operate the converter at higher frequencies, resulting in a reduced value of the capacitance required in the CDVM. Also, the development of high power density capacitors using polyvinylidene fluoride (PVF2) or polysulfone films has resulted in a significant reduction in the size and weight of the CDVM capacitors.

During the years 1974 through 1976, W. T. Harrigill and I. T. Meyers of the NASA Lewis Research Center developed a 100 W, 1000 Vdc converter operating at frequencies of 50 to 200 kHz. This work also provided the initial analyses for this type of circuit<sup>2,3,4</sup> thereby demonstrating the feasibility of designing a highly efficient, low weight CDVM power supply.

The objective of this program was to extend the available technology for CDVM power conditioners to include control and regulation circuitry.



The circuits to be developed were for a 1200 Vdc, 100W converter operating from a 120 Vdc line and having an internal operating frequency of 50 to 150 kHz.

As a result of this study a CDVM converter was developed which had an efficiency of more than 90 percent at 100W with a component weight of approximately 200 grams. It was demonstrated that the calculated MTBF of over 500,000 hours was comparable to that of a transformer/rectifier power supply.

The ability of the circuit to meet the specification requirements, shown in Appendix D, was demonstrated by building two breadboard power supplies. Extensive tests were performed to verify the operation of these power supplies.

## 2.0 CIRCUIT CONSIDERATIONS

During the first phase of the program, studies were conducted to determine the optimum configuration of the voltage multiplier, drive circuits, and regulation techniques. The results of these tradeoff studies are presented here. A complete discussion of the final circuit design is given in Section 3.0.

### VOLTAGE MULTIPLIER

To compare four different configurations of the capacitor-diode voltage multiplier circuit, designs were generated for each circuit assuming 100W load, 2 percent output voltage ripple and times nine voltage multiplication. Figure 1 shows the four circuits which were considered. Two single-phase circuits were evaluated; one (Type A) resulted in a voltage equal to the input voltage  $V_{in}$  on each capacitor, the other (Type B) resulted in two times  $V_{in}$  on each capacitor. Type A and Type B two-phase circuits were also compared. Assuming equal capacitor values throughout the multiplier, the capacitance value for each configuration was derived in terms of load current, number of stages, output peak-to-peak ripple voltage, and switching frequency. The equations are summarized below. See Appendix A for derivations.

Single-phase, Type A	$C_{1A} = 40.5 \frac{I_L}{\Delta V f}$	$C_{TOT} = 17 C_{1A}$
Single-phase, Type B	$C_{1B} = 12.5 \frac{I_L}{\Delta V f}$	$C_{TOT} = 17 C_{1B}$
Two-phase, Type A	$C_{2A} = 18 \frac{I_L}{\Delta V f}$	$C_{TOT} = 16 C_{2A}$

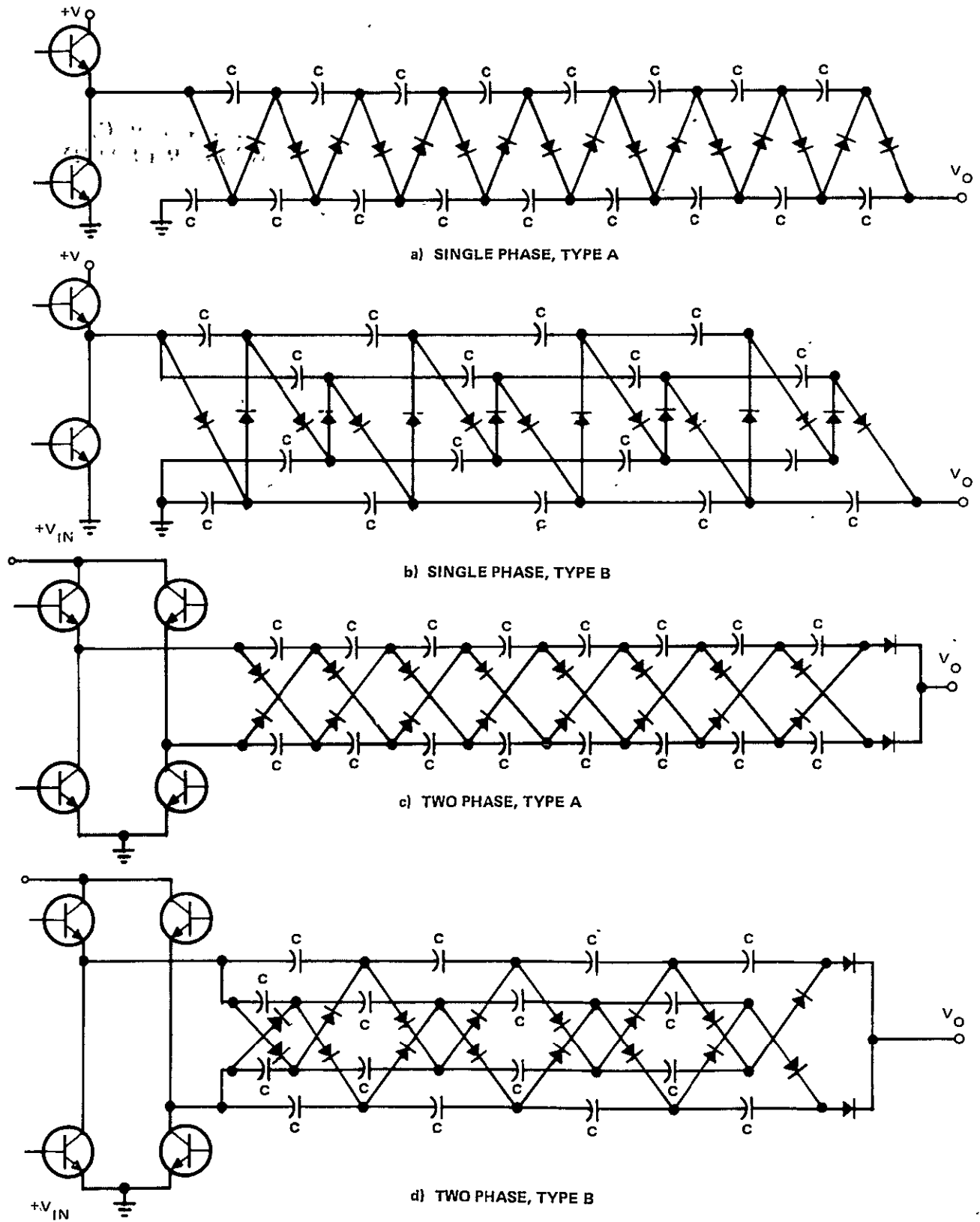


Figure 1. Capacitor-diode voltage multiplier circuit designs.

$$\text{Two-phase, Type B} \quad C_{2B} = 5 \frac{I_L}{\Delta V f} \quad C_{TOT} = 16 C_{2B}$$

where:

$I_L$  = average load current

$\Delta V$  = peak-to-peak output ripple voltage

$f$  = switching frequency of the chopper

Table 1 summarizes the results of the comparison of the four configurations. The table shows that the Type B circuits require a lower total capacitance, but the Type A circuits require a lower total energy storage. As the weight of the capacitors is approximately proportional to the energy ( $1/2 CV^2$ ), it appears that the Type A circuit would result in the lower capacitor weight. This presumes, however, that full use is made of the voltage rating of the capacitor. This is not the case when PVF2 film capacitors are used. The thinnest PVF2 film presently available has a thickness of 6  $\mu\text{m}$  and this thickness has a rating of approximately 500 Vdc. Hence, for PVF2 film the Type B circuit makes more efficient use of the voltage rating of the capacitor and will result in the smaller overall capacitor weight. For other film materials, such as polysulfone and polycarbonate, which are available in thinner gauges, the Type A circuit will offer a slight weight advantage.

The two-phase circuit requires four power transistors as compared to two for the single-phase circuit. The two-phase circuit, however, offers some significant advantages. First, the total capacitance and energy storage required are reduced to approximately 40 percent of the capacitance and energy storage required for the single-phase circuit, assuming equal output ripple voltage for each type. Also, as derived in Appendix B, the rectifier forward losses in the two-phase system are one-half of those in the single-phase system. Other advantages of the two-phase system are lower peak currents in the transistors and lower rms currents in the capacitors. As the two-phase system results in less capacitance and improved efficiency, it was decided to build the converter using the two-phase circuit. Furthermore, the initial decision was made to build the Type B circuit as the lowest voltage PVF2 capacitor film was rated at 500 volts and the higher voltage Type B circuit makes more efficient use of this rating.

TABLE 1. COMPARISON OF CDVM CIRCUITS

Parameter	Single-Phase Type A	Single-Phase Type B	Two-Phase Type A	Two-Phase Type B
<u>COMPONENT COUNT</u>				
Number of Transistors	2	2	4	4
Number of Diodes	17	17	18	18
Number of Capacitors	17	17	16	16
<u>COMPONENT REQUIREMENTS</u>				
Transistor Peak Current*	2	2	1	1
Diode Peak Current*	2	2	1	1
Transistor Voltage	$V_{in}$	$V_{in}$	$V_{in}$	$V_{in}$
Diode Reverse Voltage	$V_{in}$	$2V_{in}$	$V_{in}$	$2V_{in}$
Capacitor Voltage	$V_{in}$	$2V_{in}$	$V_{in}$	$2V_{in}$
Transistor "On" Losses*	1.00	1.00	1.00	1.00
Rectifier Forward Losses*	1.89	1.89	1.00	1.00
Total Capacitance (for 2 percent ripple)	23.9 $\mu$ F	7.38 $\mu$ F	10.0 $\mu$ F	2.78 $\mu$ F
Total energy (Joules)	0.218	0.269	0.0911	0.101
*Relative values only.				

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## DRIVE CIRCUIT

Power transistors may be driven in two basic modes — saturated or unsaturated. Saturated drive results in low "on" losses at the maximum load current. However, as shown in Table 2, devices presently available typically have storage times ranging from  $1 \mu\text{s}$  to  $5 \mu\text{s}$ . As the transistor chopper is driven at 100 kHz, where the total "on" time is only  $5 \mu\text{s}$ , it was deemed necessary to operate in the unsaturated mode to prevent "shoot-through" currents which occur when the two chopper transistors in one phase are "on" simultaneously. The unsaturated drive causes the storage time to be reduced by an order of magnitude, while the voltage across the resistor during the "on" period is increased only approximately 0.5 Vdc.

Two unsaturated drive schemes were attempted: a single transformer current drive circuit, and a two transformer voltage drive circuit. Problems with magnetic coupling in the drive transformer and unwanted interaction between the two phases during the switching interval eliminated the single transformer current drive scheme. The drive method utilized in the final design is the two transformer circuit shown in Figure 2. The drive transformer,

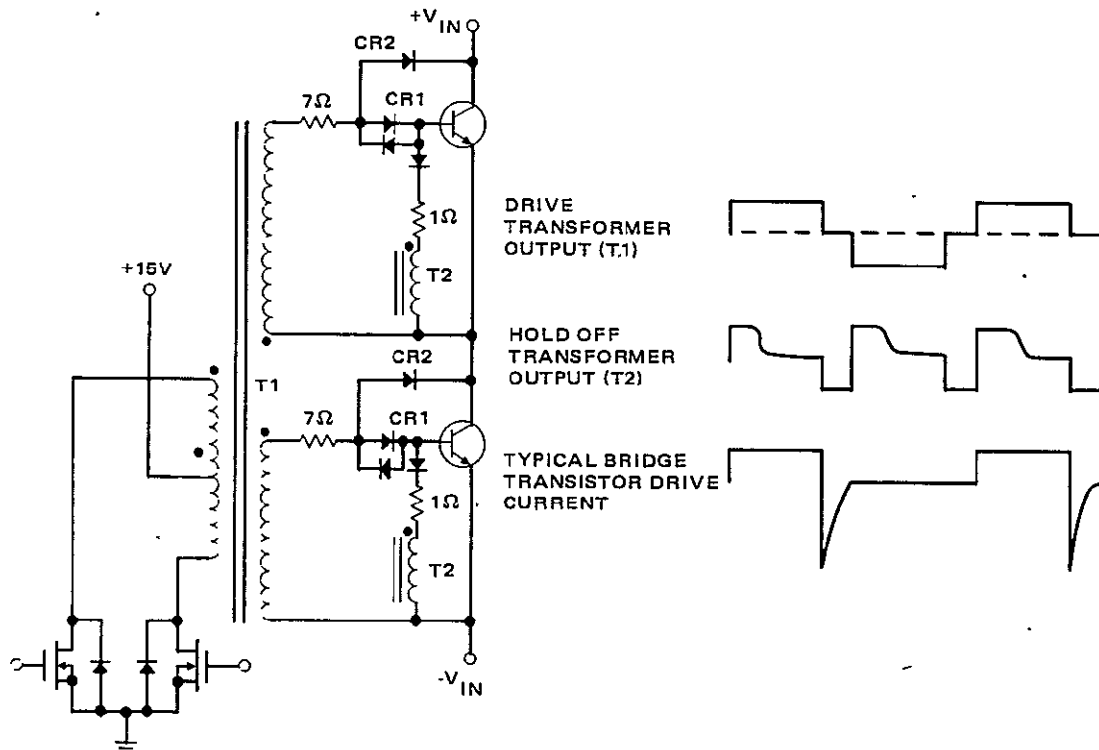


Figure 2. Voltage drive - unsaturated transistor operation.

TABLE 2. EVALUATION OF POWER TRANSISTORS

Part No.	Manufacturer	Comments
XGSQ5030	General Semiconductor Industries, Inc.	Excellent rise and fall times (150 ns), low storage time (1.2 $\mu$ s in the circuit). Does not fully saturate for approximately 3 to 5 $\mu$ s.
2N6579	TRW Semiconductors	Excellent rise and fall times (200 ns), fair storage time (2.2 $\mu$ s in the circuit). Does not fully saturate for approximately 2 to 4 $\mu$ s.
SDT 12303	Solitron	Similar to TRW 2N6579.
2N6542	Motorola	Results in somewhat lower efficiency than XGSQ5030 transistors. Spec ratings approximately the same as XGSQ5030.
2N6547	Motorola	Specifications are similar to 2N6542, except higher current rating. Have to be operated in the unsaturated mode as storage time results in excessive overlap in transistors.
MJ7160	Motorola	Similar to TRW 2N6579.

$T_1$ , provides drive current during the "on" time. Transformer  $T_2$  removes stored charge from the base of the transistors during the transition interval to guarantee that there will be no overlap in the "on" times of the upper and lower transistors.

The rectifiers,  $CR_1$  and  $CR_2$ , clamp the base drive so that if the transistor tries to saturate, the base drive is shunted through  $CR_2$ . This guarantees that the stored charge in the base junction will be minimized at the end of the half cycle when collector currents normally approach zero.

#### REGULATION TECHNIQUES

Three regulation techniques were compared as shown in Figure 3: a Buck Regulator, a Boost Add Regulator and a Modified Boost Add Regulator.

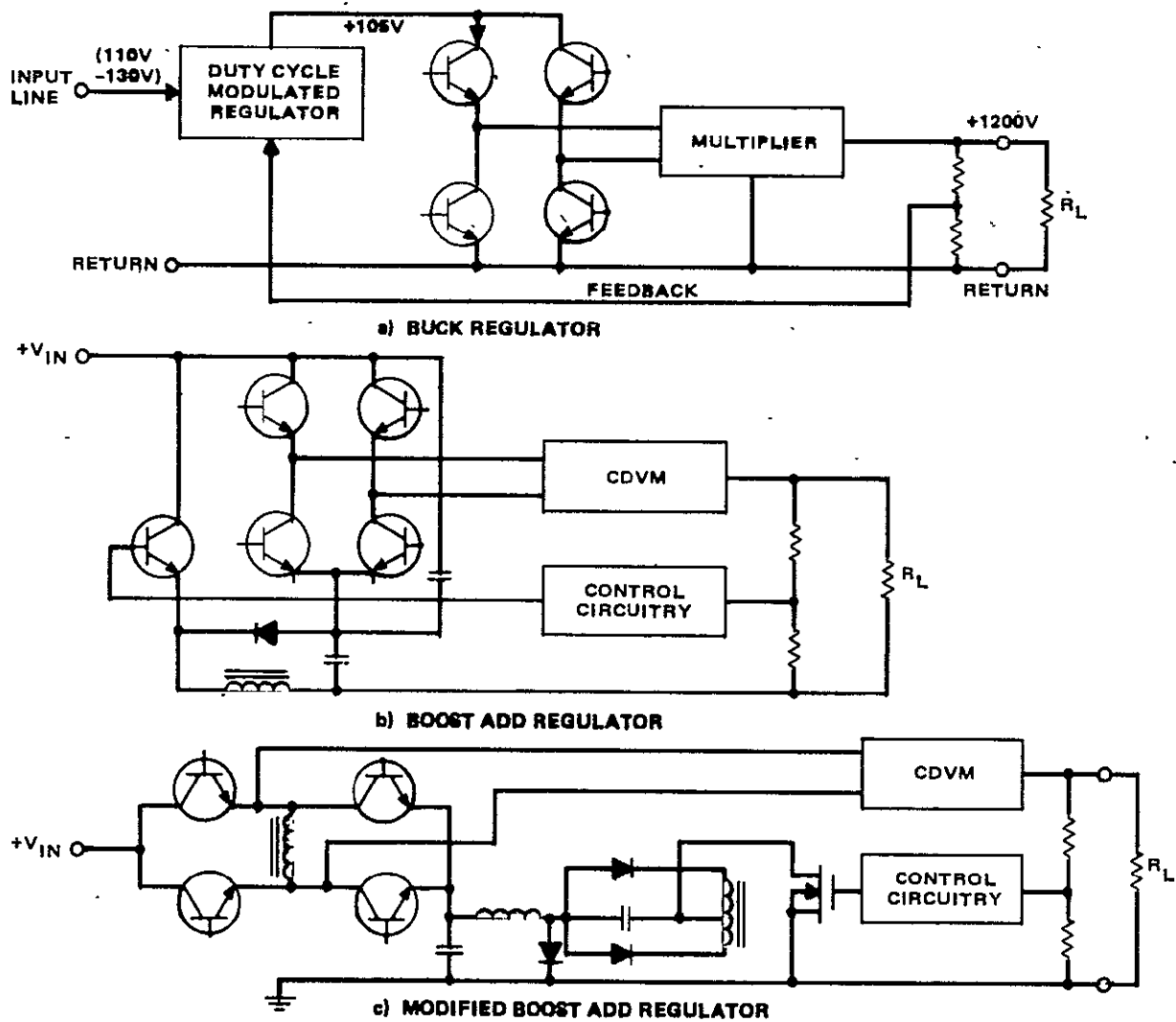


Figure 3. Regulation techniques.

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Table 3 presents the regulator tradeoff summary. The Buck Regulator was the least desirable choice as it reduced the input voltage to the CDVM which would lower the overall efficiency of CDVM converter. The Modified Boost Add Regulator is the lightest system because of its high operating frequency. Efficiency of both Boost Add circuits were equivalent. Although the transformer-rectifier in the Modified Boost Add Circuit tends to decrease efficiency, the switching losses are higher in the Boost Add converter because of the slower high voltage switch and higher voltage across the switch. The Modified Boost Add circuit was chosen because it is the lightest and can provide a moderately regulated AC voltage which can be rectified and used to efficiently generate the 15 Vdc bias supply by adding a small secondary winding to the transformer.

TABLE 3. REGULATOR TRADEOFF SUMMARY

Technique	Advantage	Disadvantage
Buck Regulator	<ol style="list-style-type: none"> <li>1. Efficient due to high duty ratio (0.8 to 0.9).</li> </ol>	<ol style="list-style-type: none"> <li>1. Increases number of CDVM stages, therefore efficiency is reduced.</li> <li>2. Generates noise on bus which must be filtered.</li> <li>3. Switching losses tend to be high due to high bus voltage.</li> </ol>
Boost Add Regulator	<ol style="list-style-type: none"> <li>1. Low transistor "on" time results in good efficiency.</li> <li>2. Operates CDVM at higher voltage which results in higher CDVM efficiency.</li> </ol>	<ol style="list-style-type: none"> <li>1. Switching losses tend to be high due to operation from bus voltage.</li> </ol>
Modified Boost Add Regulator	<ol style="list-style-type: none"> <li>1. Runs at high frequency (400 kHz) which results in small inductor and capacitor.</li> <li>2. Provides regulated secondary voltage which can be used to efficiently generate 15 Vdc bias supply.</li> <li>3. Requires a low voltage switch which can switch faster than high voltage transistors.</li> </ol>	<ol style="list-style-type: none"> <li>1. Efficiency of transformers and extra diode drop on secondary tend to reduce regulator efficiency.</li> </ol>

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### 3.0 FINAL CIRCUIT DESIGN

The major components of the 100W regulated power supply are shown in Figure 4. The two-phase transistor chopper is driven at 100 kHz by a two transformer voltage drive system. Diode clamps prevent the transistors from saturating. The capacitor-diode circuit is driven by the chopper through a small inductor which limits the peak currents in the transistors during the interval in which the capacitors are being charged. The output inductor, L2, limits the currents in the CDVM transistors, capacitors and diodes when a short occurs in the load. The 400 kHz control signal is pulse-width modulated by the control amplifier U1 and the comparator U2 and supplied to the regulator circuit. The 100 kHz output voltage from transformer T3 is rectified into a negative voltage which is switched in series with inductor L1 by the power FET Q1. Inductor L1 and capacitor C1 filter the pulsewidth modulated signal to a controlled negative d. c. voltage which increases the voltage on the CDVM capacitors.

#### CAPACITOR-DIODE CIRCUIT

The capacitor-diode circuit is a two-phase Type B circuit. Each capacitor is a 0.2  $\mu\text{F}$ , 500 Vdc unit, operating with approximately 270 Vdc across the capacitor. The capacitor charging paths for each half cycle are shown in Figure 5. When the A input is high, C1 must supply the load current ( $\hat{I}$ ). In a half cycle C2 must supply twice the load current because it must supply the current which flows through C1 plus the current flowing through CR3. The average current in C3 is three times the load current and the average current in C4 is four times the load current. Similarly, the currents in C5, C6, C7 and C8 are  $\hat{I}$ ,  $2\hat{I}$ ,  $3\hat{I}$  and  $4\hat{I}$  respectively. In a steady state

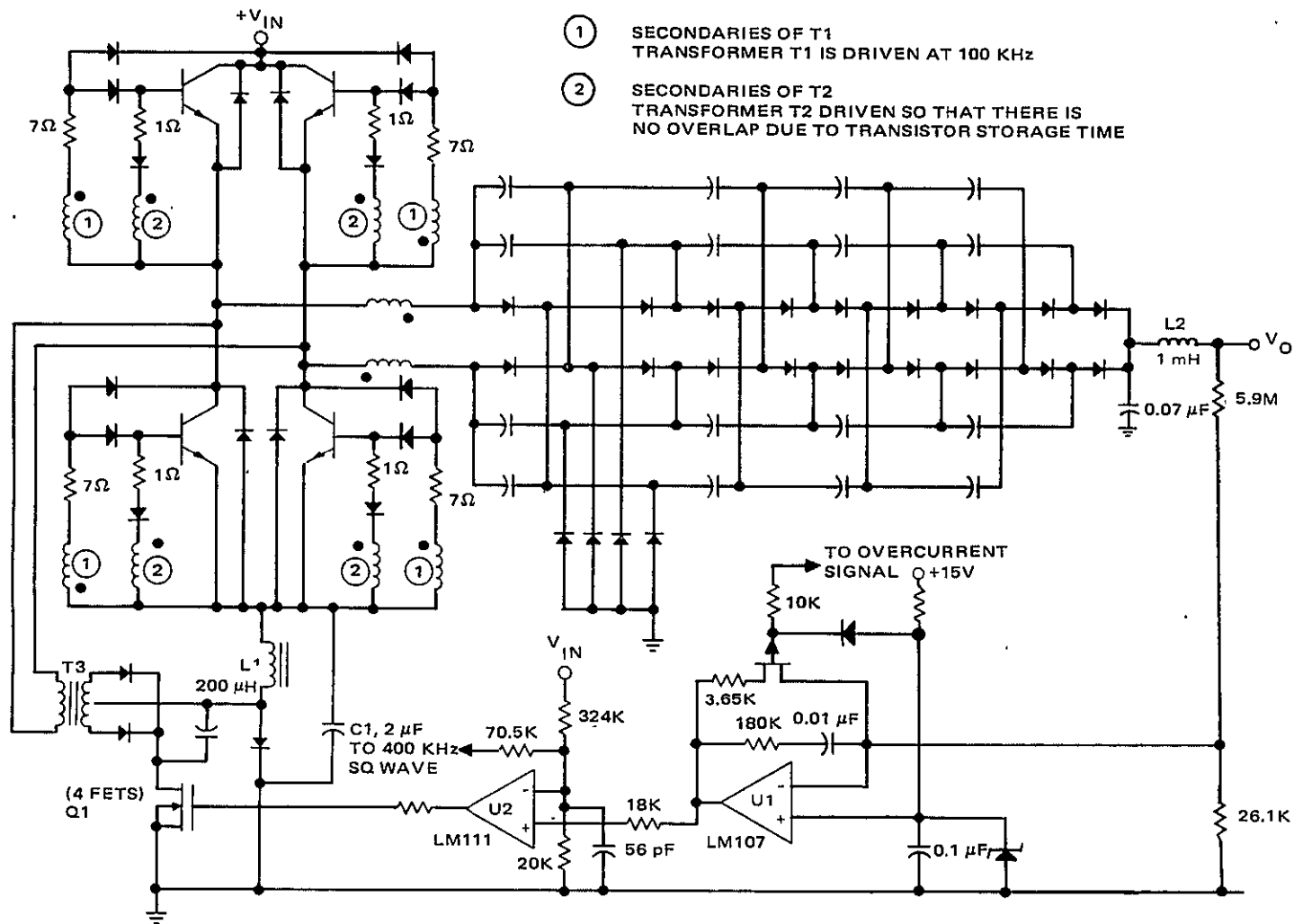


Figure 4. Driver and regulator circuit.

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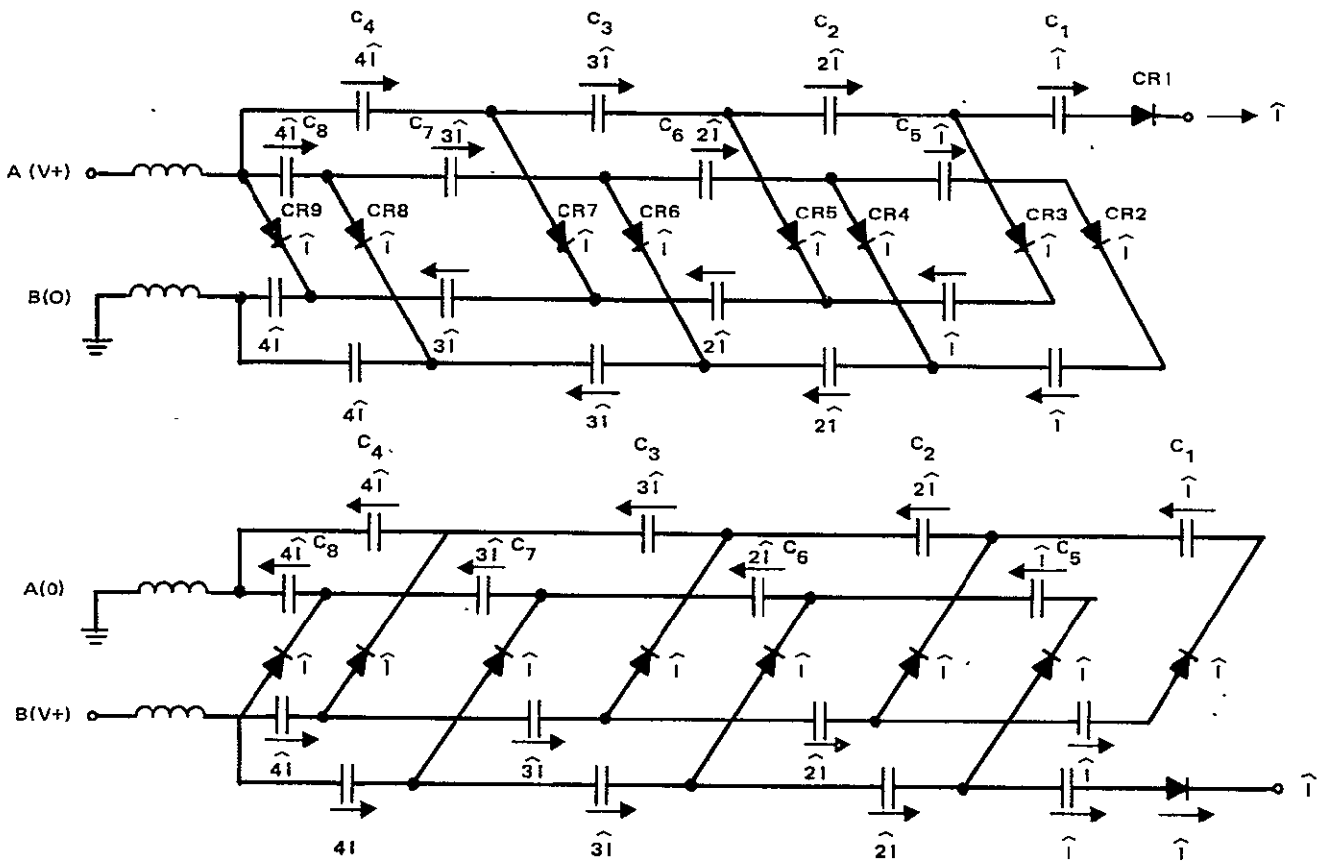


Figure 5. Current paths for the two-phase CDVM.

condition, when A goes to zero and B goes high, the average current in each capacitor must be of the same magnitude but in the opposite direction from the previous half cycle. Due to the voltages on the capacitors at the beginning of each half cycle and the effect of the inductors at the input of the CDVM, the rectifiers will conduct sequentially, starting with CR1 and ending with CR9. If these rectifiers had no forward voltage drop there would be no overlap in the rectifier currents. However, as the rectifiers have a finite forward impedance, some overlap will occur. The rectifier currents are summed in the capacitors; hence, one would suspect to see a series of current pulses in each capacitor, equal to the number of diode commutation paths in series with that particular capacitor. This characteristic is reflected in Figure 6 which shows the currents in the CDVM capacitors.

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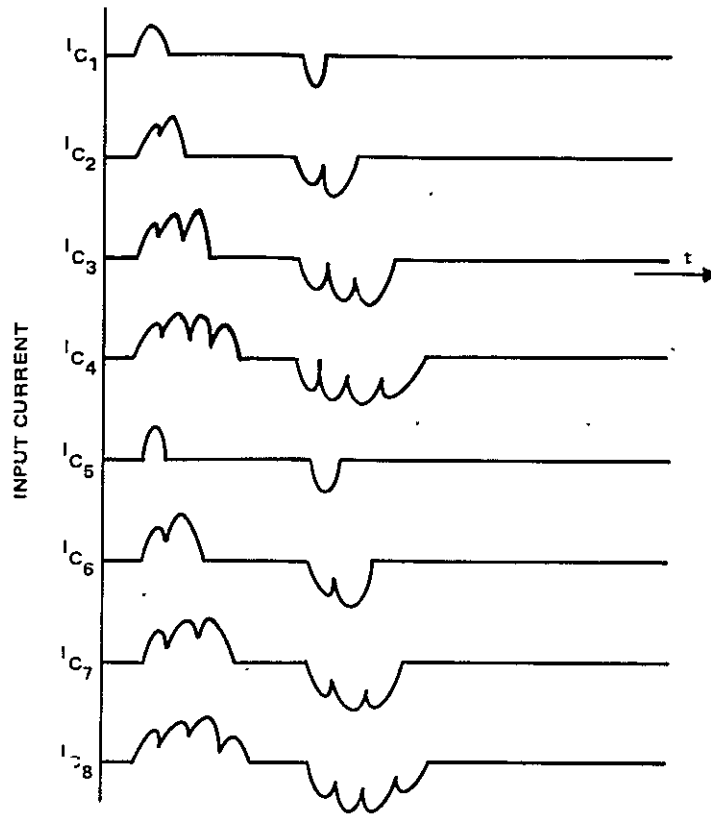


Figure 6. Currents in the multiplier capacitors.

#### INPUT INDUCTORS

The efficiency of the CDVM circuit is improved when an input inductor is connected in series with each phase. This can be explained by comparing the losses in a capacitor charged through a series resistor and a diode with those in a capacitor charged through a diode, resistor and inductor.

In Figure 7a, a capacitor is charged through a resistor. The total energy dissipated in the resistor is found by integrating the current squared times the resistance with respect to time. An ideal diode is assumed (i. e.,  $V_f = 0$ ,  $R_{\text{reverse}} = \text{infinite}$ ). Then:

$$i(t) = \frac{V_o}{R} e^{-t/\tau} \quad \text{where } \tau = R \left( \frac{C_1 C_2}{C_1 + C_2} \right)$$

$$W_{R,C} = \int_0^{\infty} R \left( \frac{V_o}{R} e^{-t/\tau} \right)^2 dt$$

$$= \frac{V_o^2}{R} \int_0^{\infty} e^{-2t/\tau} dt = \frac{V_o^2}{R} \left[ -\frac{\tau}{2} e^{-2t/\tau} \right]_0^{\infty} = \frac{V_o^2}{R} \frac{\tau}{2}$$

Hence,

$$W_{R,C} = \frac{1}{2} \left( \frac{C_1 C_2}{C_1 + C_2} \right) V_o^2$$

When an inductor is added in series with the capacitor and the resistor, as in Figure 7b, the situation is radically changed. If the system is highly underdamped, as is normally the case in a CDVM, the current with respect to time is

$$i(t) = \frac{V_o}{L} e^{-at} \sin(\omega t) \quad 0 \leq t \leq \pi/\omega$$

$$i(t) = 0 \quad \pi/\omega \leq t \leq \infty$$

where

$$\omega = \sqrt{\frac{1}{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)} - \frac{R^2}{4L^2}}$$

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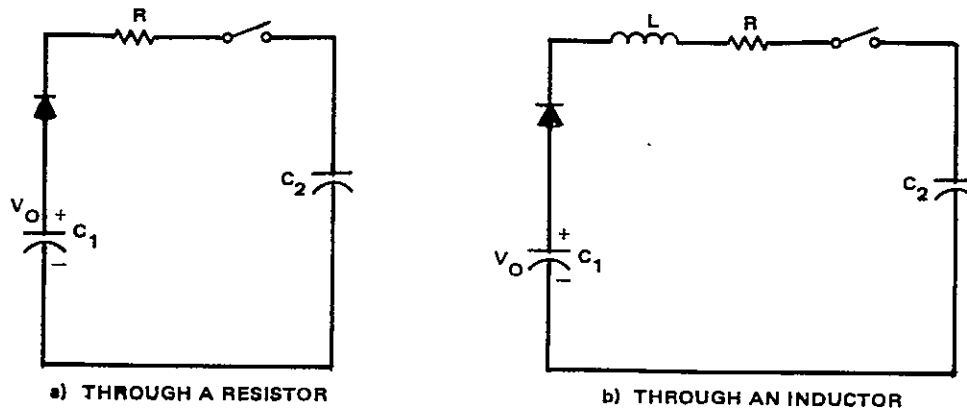


Figure 7. Capacitor charging circuit.

As the system is underdamped, that is

$$\frac{1}{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)} \gg \frac{R^2}{4L^2},$$

$$\omega \approx \sqrt{\frac{1}{L \left( \frac{C_1 C_2}{C_1 + C_2} \right)}} \text{ and}$$

$$i(t) \approx \frac{V_0}{\omega L} \sin(\omega t) \text{ for } 0 \leq t \leq \pi/\omega$$

Integrating  $i(t)^2 R$  results in:

$$\begin{aligned} W_{R, L, C} &= \int_0^{\pi/\omega} \left[ \frac{V_0}{\omega L} \sin(\omega t) \right]^2 R dt \\ &= \frac{V_0^2 R}{\omega^2 L^2} \int_0^{\pi/\omega} \sin^2(\omega t) dt \\ &= \frac{V_0^2 R}{\omega^2 L^2} \left[ \frac{1}{\omega} \frac{\pi}{2} \right] \end{aligned}$$



Hence,

$$W_{R,L,C} \approx \frac{1}{2} \left( \frac{C_1 C_2}{C_1 + C_2} \right) V_o^2, \left[ \pi R \sqrt{\frac{C_1 C_2}{C_1 + C_2} \frac{1}{L}} \right]$$

In the first case the losses were independent of the value of the resistance, but when an inductor is added, the losses become a function of the inductance, capacitance, and resistance. Comparing the two cases we find that

$$W_{R,L,C} \approx W_{R,C} \left( \pi R \sqrt{\frac{C_1 C_2}{C_1 + C_2} \frac{1}{L}} \right)$$

For a typical multiplier where

$$R = 0.03 \Omega$$

$$L = 10 \times 10^{-6} \text{ Henries}$$

$$C_1 = C_2 = 2 \times 10^{-6} \text{ Farads}$$

the losses are

$$W_{R,L,C} = W_{R,C} (0.0298)$$

Thus, adding the inductance to the circuit caused the losses to be reduced by a factor of approximately 34, which is a dramatic reduction of the capacitor charging losses.

The value of the inductor is chosen so that the equivalent input capacitance of the CDVM, and the inductance will resonate at the switching frequency. This will result in quasi-sinewave currents where the current is approximately zero during the switching interval. Therefore, the switching losses in the transistors are nearly eliminated, except those due to the currents required to charge the transistor junction capacitances, the rectifier reverse capacitances and any stray capacitance in the circuit.

## SWITCHING TRANSISTORS

The currents in the switching transistors are equal to the sum of the currents in capacitors C4 and C8 and diode CR9. Due to the inductor, which is in series with the transistor, the current is a fairly smooth waveform. As C4 carries  $4I_L$ , C8 carries  $4I_L$  and CR9 carries  $I_L$ , the average current in the upper transistor during a given half cycle will be nine times the load current. If the current is assumed to be sinusoidal over the full half cycle, the peak current in this transistor is  $\pi/2$  times the average current. However, in the actual circuit the current flows for less than a half cycle and thus the peak current will be

$$I_{c \text{ peak}} = 9 I_L \frac{\pi}{2} \frac{T}{t}$$

where  $T/t$  is the ratio of the period of a half cycle to the conduction period of the transistor.

The conduction period may be adjusted by varying the value of inductance in series with the multiplier. In this particular design the current was restricted to approximately 3/4 of the period. As a result the peak current in the transistor was  $9 \times 0.083 \times \pi/2 \times 4/3 = 1.56A$ .

## DRIVE CIRCUIT

Once the peak collector currents for the switching transistors are known, the drive circuit can be designed. To guarantee that the transistor will have adequate base drive it was decided to provide 160 mA of drive current. This would require the switching transistors to have a minimum current gain ( $h_{FE}$ ) of 10.

The drive circuit is shown in Figure 8. The logic is synchronously clocked to preclude false turn-on of the VMP22 drive transistors which would result from a race condition in the CMOS circuitry. The drive circuit is clocked by an astable multivibrator running at 800 kHz. The 800 kHz signal is fed through a series of flip-flops that provide the required sequence of drive pulses. The outputs of the various flip-flops is shown in Figure 9.

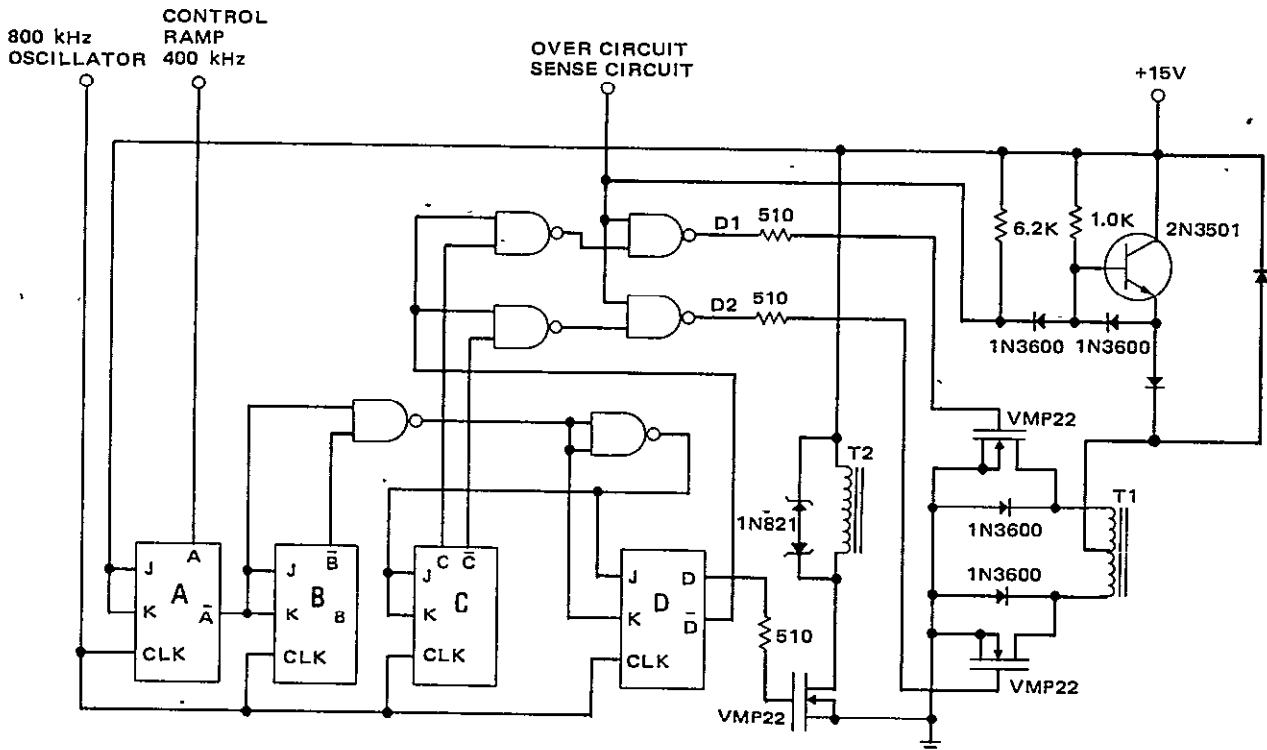


Figure 8. Drive circuit.

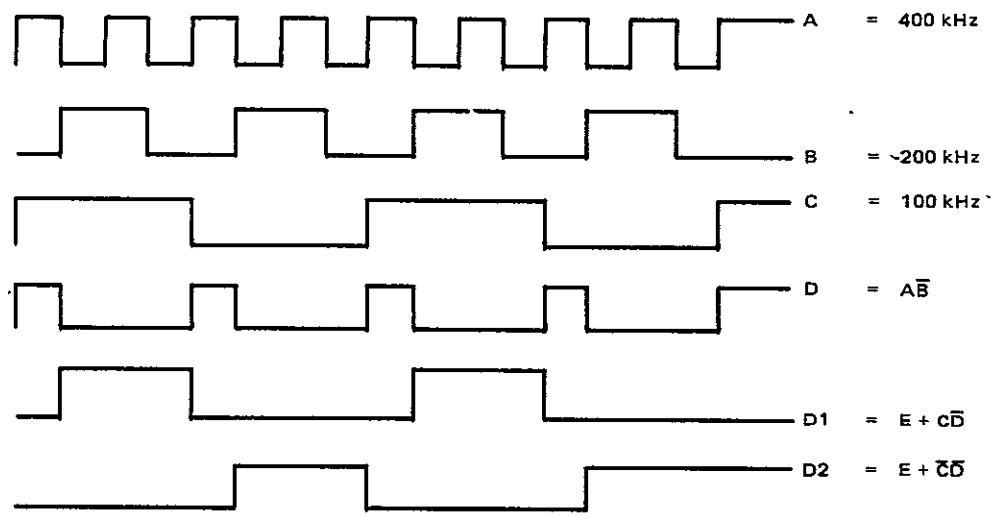


Figure 9. Drive circuit logic waveforms.

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The first JK flip-flop (A) divides the frequency to 400 kHz. This 400 kHz signal is used to generate a ramp in the control circuit. The next JK flip-flop (B) divides the signal to a 200 kHz square wave. The third flip-flop (C) provides the basic drive signal of 100 kHz. The last flip-flop (D) is used to drive transformer T2 which is used to remove the stored charge from the "on" transistors in the chopper. An overcurrent signal (E) from the short-circuit sense circuit immediately disables the drive circuit when an over-current condition is present at the output of the CDVM.

### SHORT-CIRCUIT PROTECTION

The overcurrent sensing circuit is shown in Figure 10. The load current is returned to ground through a  $2\ \Omega$  sense resistor. When a load fault occurs, transistor Q1 turns on and discharges the voltage on capacitor C2. When the voltage on C2 falls below the reference voltage (VR1), the output of the control amplifier U1 goes low and this disables the drive circuit. When the load current decays below the trip point, Q1 turns off and C2 begins to recharge. When the voltage on C2 becomes greater than the reference voltage, the drive circuit is allowed to function until the output current again exceeds the trip point. If the circuit is operating into a continuously shorted load, the short-circuit protection will recycle the unit once every millisecond until the short is removed.

The output inductor, L2 (Figure 4), protects the rectifiers, capacitors and transistors from damage due to large peak currents during the fault and the subsequent recycling. With each capacitor (C) in the CDVM fully charged the total energy stored in the multiplier is

$$\begin{aligned}
 W &= 1/2 C_{TOT} V^2 = 1/2 \times 16 \times C V_{in}^2 \\
 &= 1/2 \times 16 \times 0.2\ \mu\text{F} \times 270^2 \\
 &= 0.117\ \text{J}
 \end{aligned}$$

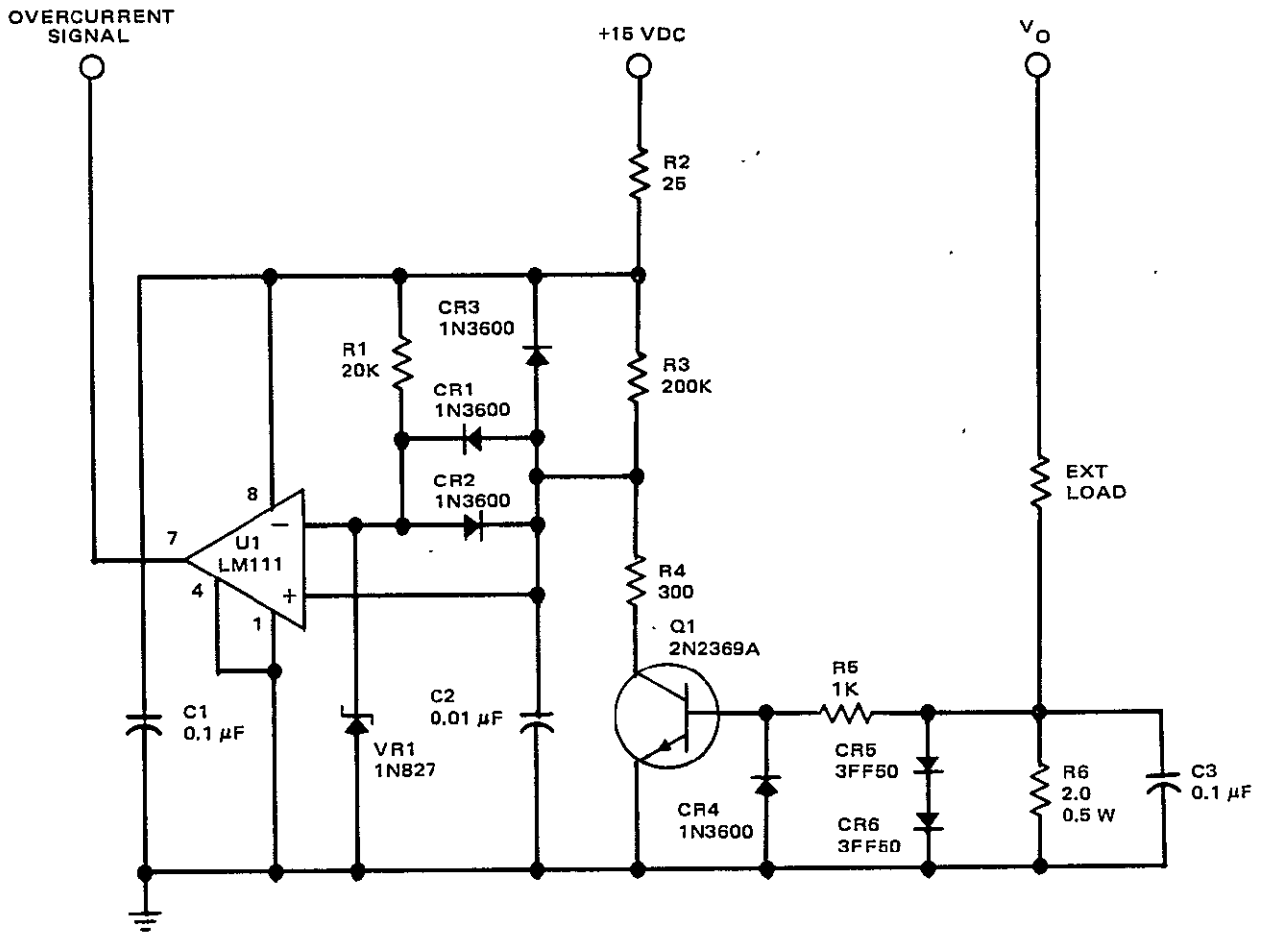


Figure 10. Short-circuit sense circuit.

If that total energy must be stored in the inductor during the fault, the peak current may be found from the energy equation,

$$W = 1/2 LI^2$$

$$I_p = \sqrt{\frac{2W}{L}}$$

$$= \sqrt{\frac{2 \times 0.117}{L}}$$

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During a fault condition the 1 mH output inductor tends to partially saturate causing its inductance to drop to approximately 300  $\mu$ H. Then

$$I_p = \sqrt{\frac{2 \times 0.117}{300 \times 10^{-6}}} = 27.9 \text{ Apk}$$

This current is shared by two rectifiers, so that each one carries a maximum of 14 Apk. As the rectifiers are capable of handling current impulses of 25 Apk at low duty cycles, the rectifiers will be operating in a safe area during a load fault.

During a fault or recycle condition, the transistors are stressed highest during the restart period. During the first "on" cycle, the transistor will see a peak current determined primarily by the current gain ( $h_{FE}$ ) of the transistor and the base drive current. With 160 mA of base drive, the maximum current which the transistors are able to supply is  $h_{FE(\max)} i_b$ . Assuming an  $h_{FE}$  of 35, the maximum collector current would be approximately 5.6A. The worst case condition (in terms of safe area operating conditions) would occur when one of the two conducting transistors has a very high  $h_{FE}$  ( $\approx 100$ ) and the other has a low  $h_{FE}$  ( $\approx 30$ ). The low  $h_{FE}$  device would have to support the line voltage and carry the full current. Using the 200  $\mu$ s active-region safe operating area curve for a MJ7160 power transistor, the transistor would be able to support 8A and 150 Vdc. As the transistor actually operates in a region where the peak current is less than 6A and the voltage across the transistor is less than 130 Vdc during the first pulse, less than 6A and 90 Vdc during the second pulse and less than 6A and 43 vdc during the third pulse, the transistor will not be overstressed during a restart.

#### BIAS SUPPLY

To complete the converter, a 15 Vdc bias supply is required to provide power to the CMOS logic, drive circuitry, and control circuitry. Figure 11 shows the bias supply designed for the 100W CDVM converter. During startup, all power is supplied directly from the line through the Darlington transistor

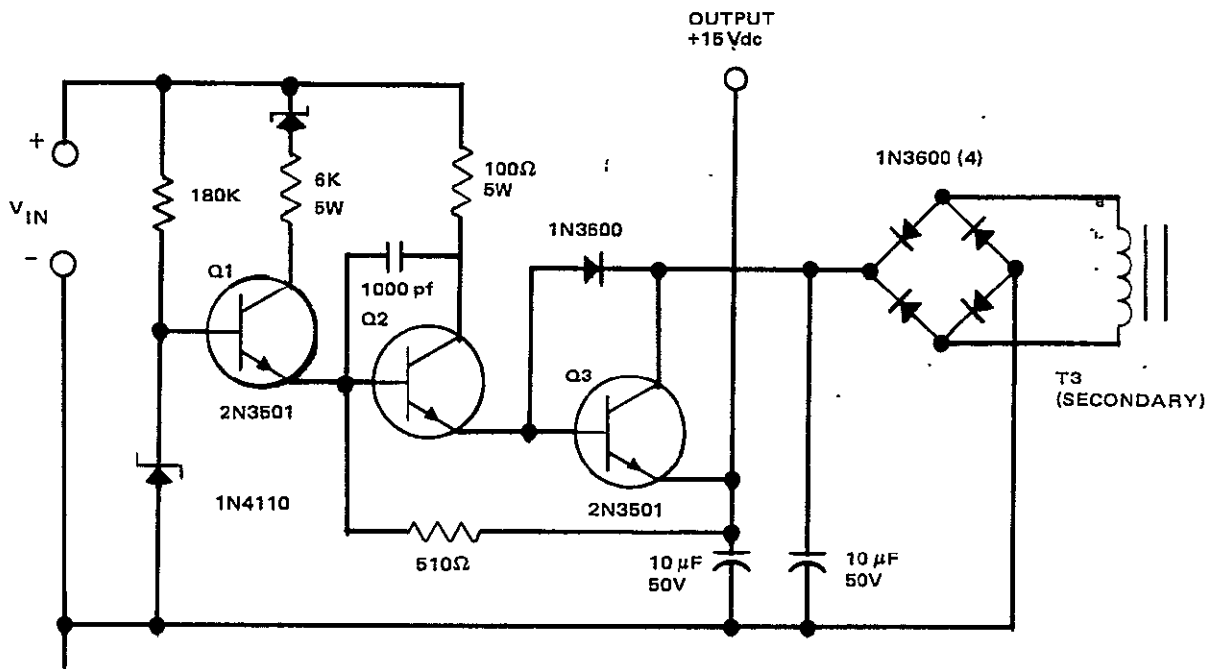


Figure 11. 15 vdc bias voltage supply.

pair Q1 and Q2. Once the converter is operating, the 15 Vdc bias voltage is supplied primarily from the rectified a. c. voltage from the secondary of T3. Only the drive current for Q3 is supplied directly from the 130 vdc bus.

The efficiency of the 15 Vdc supply is approximately 64 to 69 percent. As the supply delivers approximately 1.6W to the drive and logic circuits, the total input power varies between approximately 2.4 and 2.6W.

#### CONTROL LOOP

The control loop was designed using the model shown in Figure 12. Before the control amplifier circuit could be designed, it was first necessary to characterize the frequency response of the CDVM circuit. Measurements were taken which resulted in the frequency response plot shown in Figure 13. It is interesting to note that the multiplier behaved as a single pole followed by a high frequency zero. The single pole is the result of the energy transfer characteristic of the CDVM, while the high frequency zero is the result of

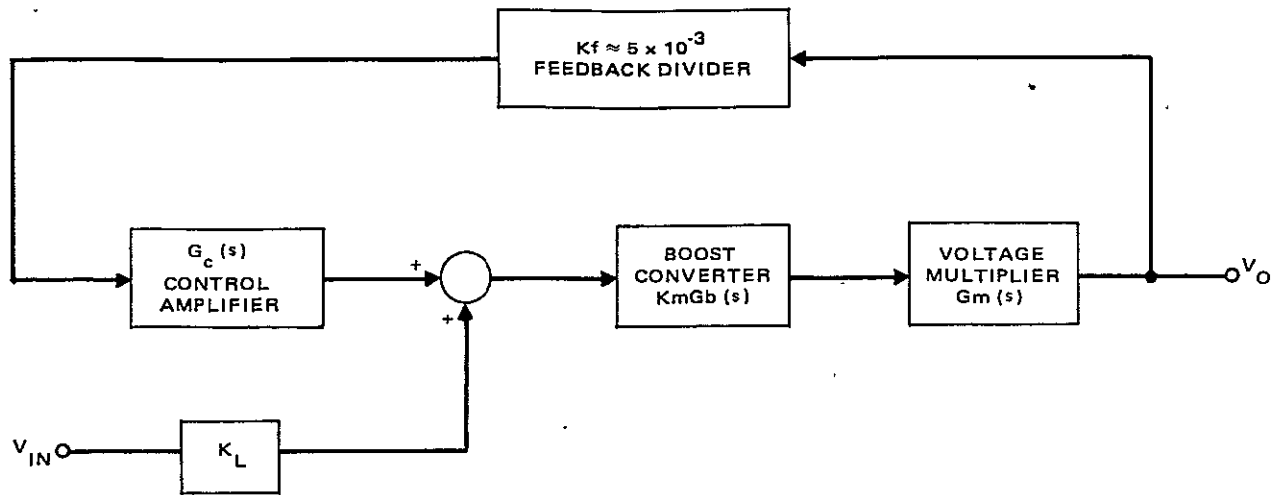


Figure 12. Control loop model.

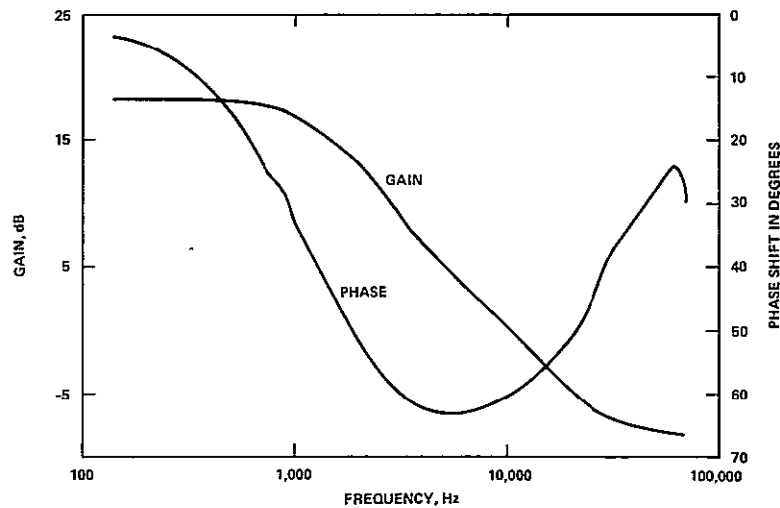
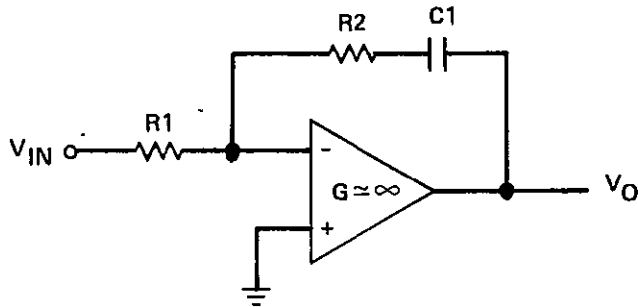


Figure 13. Capacitor multiplier transfer function.

direct a. c. coupling to the load through the CDVM capacitors. The control amplifier (Figure 14) was designed to be an integrator at low frequency and have a fixed gain at high frequency.

The straight line Bode approximation of the loop gain is shown in Figure 15. The gain crosses the zero dB line at approximately 7 kHz with a





$$G_c(s) = -\frac{R_2 + \frac{1}{sC}}{R_1} = -\frac{R_2 sC + 1}{R_1 sC}$$

Figure 14. Equivalent circuit of the control amplifier.

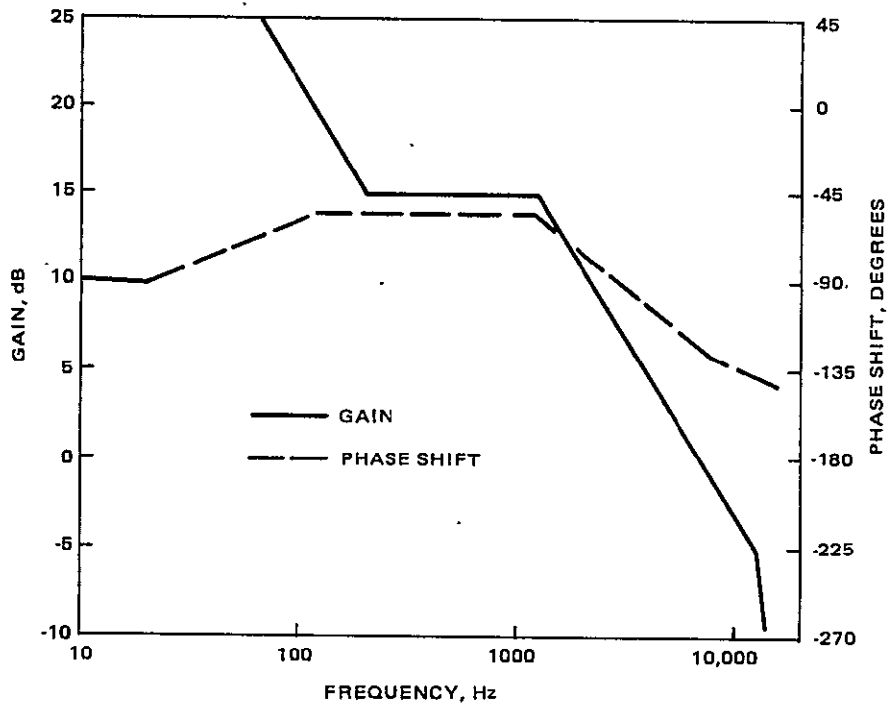


Figure 15. Open loop frequency response (Bode straight line approximation).

phase margin of approximately 45 degrees. This large phase margin is reflected in the final transient response data which shows no appreciable overshoot in the response to step changes in the load.

Line compensation is used in the design to improve the response time to transients on the input bus. Figure 16 shows the line compensation technique. A change in the input bus voltage causes the d. c. level of the ramp to shift rapidly to correct the line transient.

#### LOSS SUMMARY

The various losses in the CDVM converter are identified in Table 4. The calculations for these losses are shown in Appendix C. In general, the losses are evenly distributed throughout the converter. The most significant losses are in the boost circuit and in the switching transistors.

The predicted efficiency for the 100 W CDVM converter is 91.9 per cent with an input voltage of 120 Vdc.

The actual efficiency, as measured on the engineering breadboard with 2N6579 transistors in the chopper circuit, is shown in Figure 17.

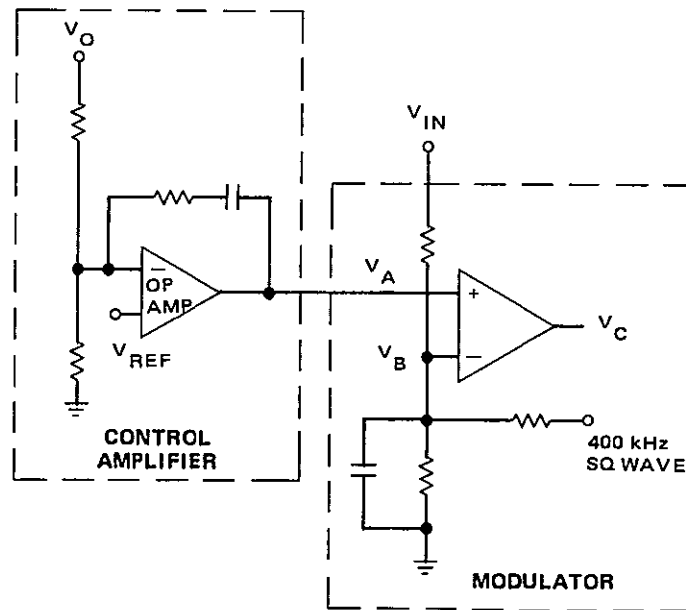


Figure 16. Line compensation technique.

TABLE 4. PREDICTED CDVM CONVERTER LOSSES

$P_O = 100\text{W}$   
 $V_{IN} = 120\text{ Vdc}$   
 TRANSISTORS - MJ7160

	Watts
1. Transistor "On" Losses	1.83
2. Transistor Switching Losses	1.03
3. Drive and Control Power	1.60
4. Diode Forward Losses	0.83
5. Capacitor ESR Losses	0.09
6. Boost Circuit Losses	2.53
7. 15 vdc Bias Supply Losses	0.94
<b>TOTAL</b>	<b>8.85</b>

$$\text{Efficiency} = \frac{100}{100 + 8.85} = 91.9\%$$

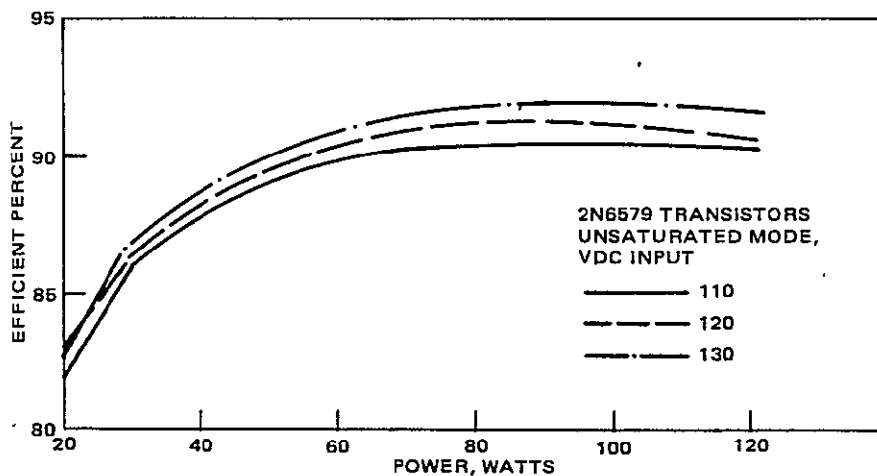


Figure 17. Efficiency of CDVM power supply.

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## COMPONENT WEIGHT

A summary of the weights of the electronic components of the power supply is shown in Table 5. The table shows the weight of the major components as well as the distribution of the weights between the various parts of the circuit.

The weight for the multiplier as shown in Table 5 represents the weight of the uncased capacitors, diodes and a 0.07  $\mu\text{F}$  output capacitor which consists of three of the 0.22  $\mu\text{F}$  capacitors connected in series. These components were assembled together in a single case as shown in Figure 18. The packaged weight of this assembly was 109.9 grams. The weight breakdown for this module is shown in Table 6.

TABLE 5. WEIGHT SUMMARY

A. Power Circuitry		
Bridge Transistors	25.60	
Multiplier (Capacitors and Diodes)	37.30	
Drive Circuit	18.55	
Inductors	20.30	
Drive Transformers	11.80	
		TOTAL 113.55 grams
B. Regulation Circuitry		
Control Amplifier	11.37	
Boost Circuitry	27.16	
		TOTAL 38.53 grams
C. Short Circuit Protection		
Inductor	25.50	
Comparator	4.66	
		TOTAL 30.16 grams
D. Bias Supply		TOTAL 14.38 grams
Power Supply Total		196.62 grams

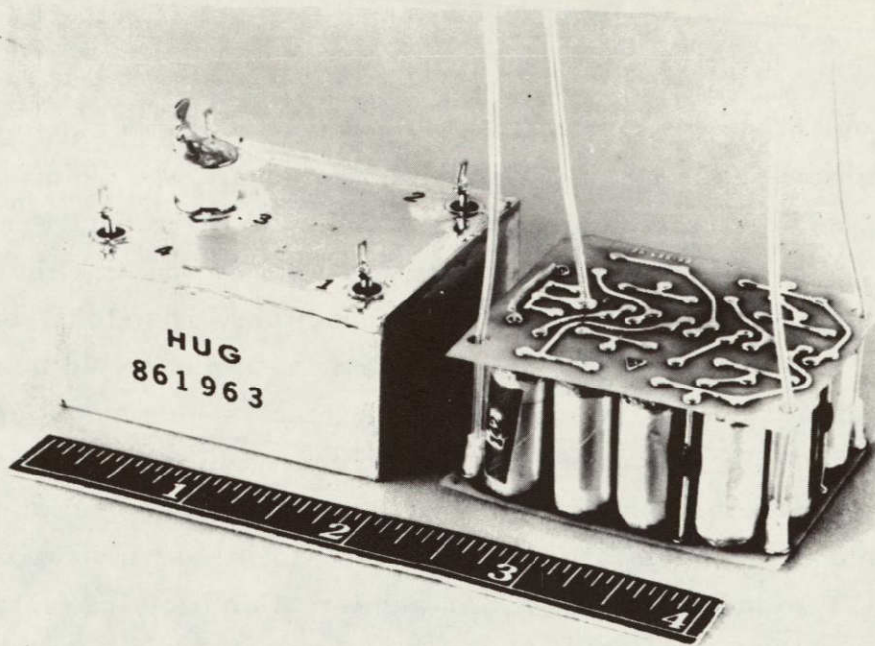


Figure 18. Capacitor-diode module.

TABLE 6. WEIGHT OF CASED MULTIPLIER

Capacitors (19 ea.)	28.5 grams
Diodes (22 ea.)	8.8
Circuit Boards (2 ea.)	5.0
Case	25.2
Terminals (5 ea.)	3.4
Solder	15.0
Impregnant	25.0
Total	110.9 grams

#### RELIABILITY

The objective of this part of the study was to provide a comparison of the predicted reliabilities of the CDVM converter designed under this program and a conventional transformer/rectifier power supply of equivalent characteristics. The transformer/rectifier circuit used for the comparison was that of an 8 cm ion engine power supply, designed by Hughes Aircraft Company for the NASA Lewis Research Center, modified to delete those portions of the circuit not present in the CDVM supply.

As the objective was to compare the two circuits rather than to compute an absolute number for the MTBF, a consistent analysis was used for both power supplies. The analysis consisted of a Generic Part Count Prediction Method. This method of reliability prediction starts by counting the number of parts in each generic type class (such as capacitors, resistors, etc.) for the system under consideration. Each number is then multiplied by a failure rate typical of the class and environment. The rates are based on operating conditions assumed to be a stress ratio not exceeding 40 percent of the maximum part rating and a temperature typical of a system designed for the particular environment. The failure rates used were those indicated in the Hughes Reliability Handbook R-67-4. An additional multiplying factor was incorporated into the calculations to compensate for the various quality assurance levels to which part types would be procured.

The general model used in obtaining the system failure rate was:

$$\lambda_S = \sum (\lambda_{GP} N_G \pi_Q)$$

where

$\lambda_S$  = System failure rate

$\lambda_{GP}$  = Generic part type failure rate (space environment)

$N_G$  = Number of parts of the generic type

$\pi_Q$  = Quality level of parts used (high reliability)

The final results, indicated in Table 7, show that there is a 25 percent difference in the failure rate of the two systems. However, the overall difference in the failure rate is extremely small (0.47 failures per million hours).

The increase in the failure rate is due to the large number of capacitors and diodes used in the multiplier circuit, and the use of four parallel connected transistors in the regulator circuit. Since failure rates were based on generic parts counts, and not on the actual failure rates for the particular

TABLE 7. RELIABILITY PREDICTION

Capacitor-Diode Voltage Multiplier Circuit				
	Qty	Failure Rate (F/10 <sup>6</sup> hrs each)	$\pi Q$	Failures/10 <sup>6</sup> hours
Resistors	41	0.008	0.35	0.115
Diodes	70	0.015	0.40	0.420
Capacitor	34	0.020	0.35	0.240
IC	6	0.260	0.30	0.470
Transistor	20	0.060	0.40	0.480
Transformer	3	0.080	0.50	0.120
Choke	3	0.080	0.50	0.120
Total	177			1.97 MTBF = 507614 hours
Transformer-Rectifier Circuit				
Resistors	40	0.008	0.35	0.112
Diodes	51	0.015	0.40	0.306
Capacitor	20	0.020	0.35	0.140
IC	5	0.260	0.30	0.390
Transistor	13	0.060	0.40	0.312
Transformers	4	0.080	0.50	0.160
Choke	2	0.080	0.50	0.080
Total	135			1.5 MTBF = 666666 hours

capacitors and transistors used, the difference in predicted failure rates may deviate considerably from that of Table 7. However, the actual failure rates of these devices are unknown at the present time.

BREADBOARD CONSTRUCTION

Two identical breadboards were constructed. The layout of the breadboard assemblies is shown in the photograph of Figure 19. The short-circuit

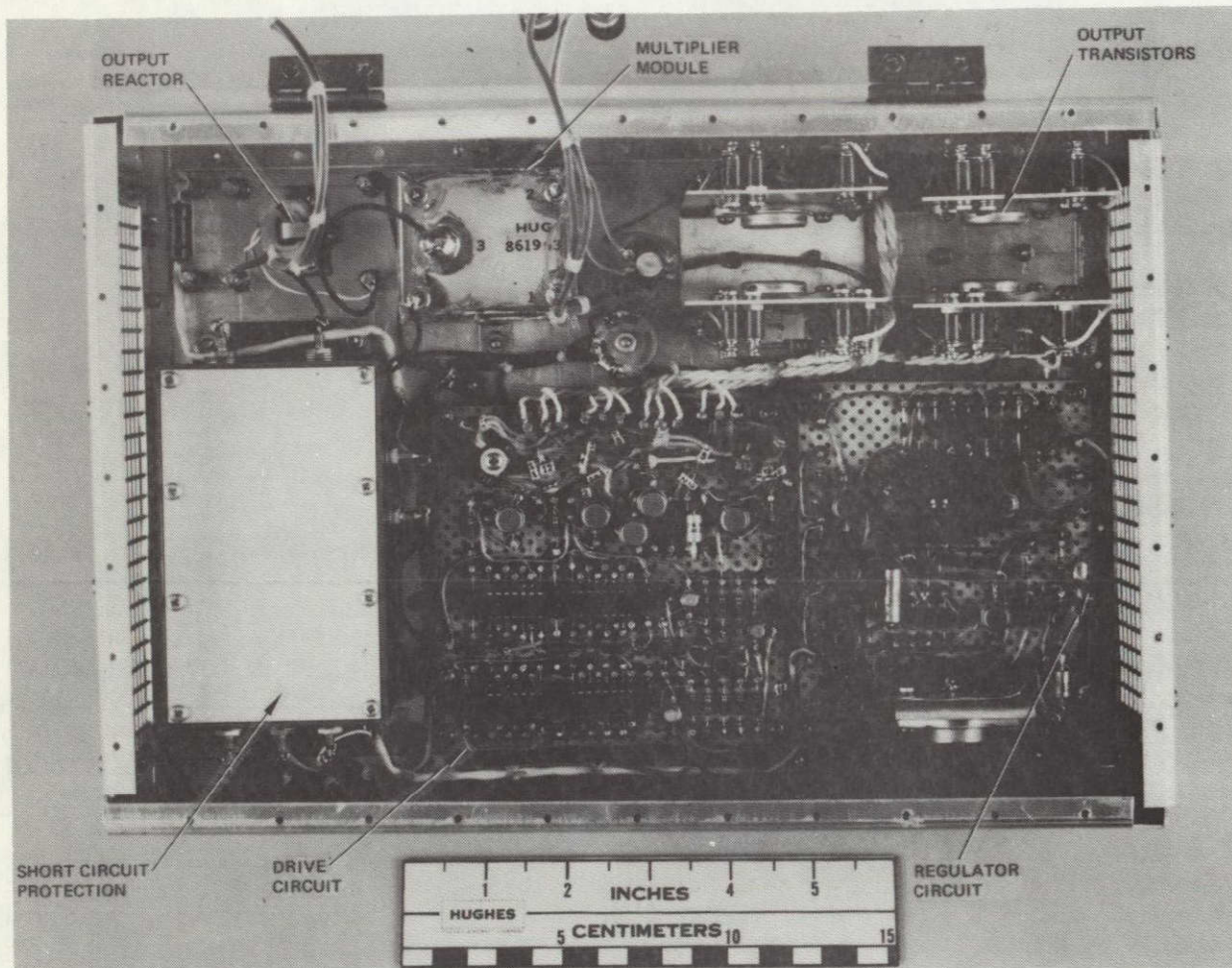


Figure 19. CDVM breadboard assembly.

protection circuitry is encased in a metal container to provide the required shielding. The CDVM module contains the multiplier capacitors, diodes and output filter capacitors.



#### 4. CAPACITOR SELECTION

As shown in the previous section the overall reliability of the CDVM converter is greatly dependent on the reliability of the capacitors. Also, the weight of the capacitor-diode module represents a considerable portion of the total component weight. As part of the capacitor selection four types of capacitors were considered: tantalum, ceramic, foil wound and metallized film.

Tantalum capacitors were considered to be unsuitable for this circuit because of the high AC currents present. Ceramic capacitors, although having a small physical size, operate at energy densities of 0.005 to 0.01 Joules/gram which is approximately one tenth the energy density reported for metallized film capacitors<sup>5</sup>. For the same insulation stresses, foil wound capacitors will have a lower energy density than metallized film capacitors because of the additional weight of the aluminum foil.

#### FILM SELECTION

For the metallized film capacitors two insulation systems were considered — polyvinylidene fluoride (PVF2) and polysulfone. Reference 5 gives the maximum energy density for uncased capacitors as 0.188 Joules/gram for PVF2 and 0.2 Joules/gram for polysulfone capacitors rated 2  $\mu$ F at 500 Vdc.

The thinnest film available in PVF2 is 6  $\mu$ m thick. Capacitors wound from this film would be rated at 600 Vdc; with 270 Vdc applied to the capacitor, this would represent a derating to 33 percent of rated value. The same thickness of film (6  $\mu$ m) should be used to fabricate the polysulfone capacitors to

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provide adequate derating. However, because the dielectric constant of the polysulfone film is lower than that of the PVF2 film, the resulting polysulfone capacitor is larger than the PVF2 capacitor.

The voltage multiplier capacitors see considerable a. c. currents at the operating frequency of 100 kHz, particularly in the first stages of the multiplier. To assure reliable operation of the capacitors and maintain high efficiency of the CDVM, the losses in the capacitors must be held to a minimum, which means that a low dissipation factor at 100 kHz is required. Figure 20 shows the dissipation factors of the two films considered. The dissipation factor of the polysulfone film is 0.3 percent at 100 kHz while that of the PVF2 film is 10 percent.

Although the use of PVF2 capacitors would result in a lower weight (0.7 grams per capacitor versus 1.5 grams per capacitor for polysulfone), it was felt that the requirements for low loss at 100 kHz dictated the use of polysulfone capacitors for this application.

#### FINAL DESIGN

For the final design capacitors made of 6  $\mu\text{m}$  metallized polysulfone were used. The capacitors were wound using controlled-winding tension. For the terminations used a special flame-spray process was used to obtain a low termination resistance. The capacitors were assembled into a common case

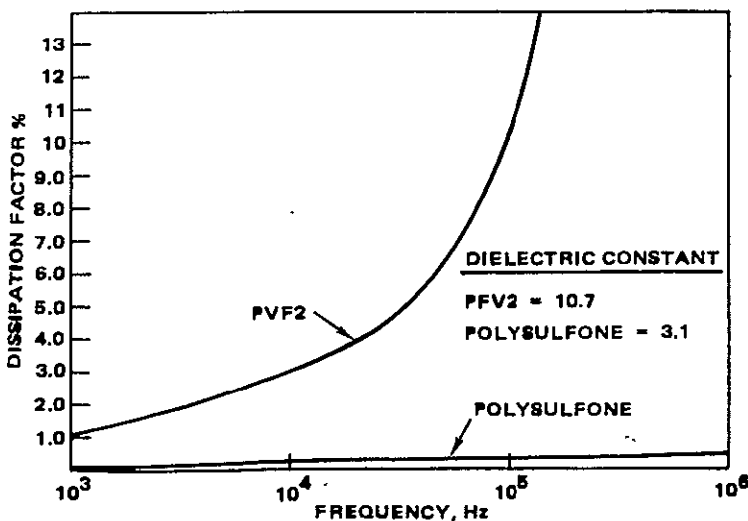


Figure 20. Dissipation factors of PVF2 and polysulfone films.

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with the diodes and output filter capacitor. The assembly is shown in Figure 18. The cased assembly was impregnated with a silicone fluid, which provides insulation as well as conductive cooling.

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## 5. TEST RESULTS

Extensive testing was performed on the engineering breadboard as well as on the two deliverable breadboards to characterize the CDVM converter operation. Test data was taken in five principle areas to demonstrate conformance with the design requirements:

1. Efficiency
2. Output Regulation
3. Output Ripple Voltage
4. Transient Response
5. Short-Circuit Recovery

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The efficiency goals for the CDVM supply were 90 percent at full load and 80 percent for one fifth of full load. Table 8 summarizes efficiency test data for the engineering breadboard and the two deliverable breadboards.

At full load, the efficiency varied between 90.3 and 92.0 percent for the three units tested. The highest efficiency was recorded on the original engineering breadboard. A design change in the 15 Vdc supply explains the difference (0.2W) between the engineering breadboard and SN 2. A 510 $\Omega$  resistor was added (see Figure 11) which keeps at least 2.3 mA flowing in Q1 at all times. This results in an additional 0.3W loss in the 15 Vdc bias supply. However, it was necessary to add the resistor to handle collector to base leakage current in Q2. The lower efficiency in SN 3 is most likely due to higher switching losses since there was an additional 1W loss for all load conditions. Most other losses such as transistor "on" losses or rectifier forward losses are a function of the load current. The efficiency varied between 76.3 and 81.6 percent at the 20W level. The fixed losses such as drive power and switching losses dominated the losses for the 20W

TABLE 8. CDVM CONVERTER EFFICIENCY (PERCENT)

	P <sub>OUT</sub> = 100W			P <sub>OUT</sub> = 50W			P <sub>OUT</sub> = 20W		
	V <sub>IN</sub> = 110 vdc	V <sub>IN</sub> = 120 vdc	V <sub>IN</sub> = 130 vdc	V <sub>IN</sub> = 110 vdc	V <sub>IN</sub> = 120 vdc	V <sub>IN</sub> = 130 vdc	V <sub>IN</sub> = 110 vdc	V <sub>IN</sub> = 120 vdc	V <sub>IN</sub> = 130 vdc
Engineering Breadboard	91.0	91.5	92.0	89.1	89.6	90.1	82.0	83.0	81.6
SN 2	90.8	91.3	91.5	88.7	88.6	88.4	79.2	78.8	78.4
SN 3	90.3	90.9	91.0	87.4	87.7	87.8	77.1	76.7	76.3

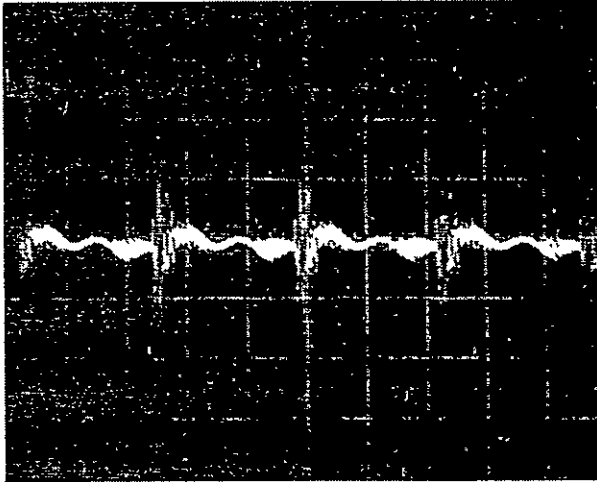
load condition. This 15 Vdc bias supply power represented by far the most significant loss ( $\approx 12.2$  percent). Another significant loss was the switching loss which accounts for approximately 5 percent at the 20W load condition.

The output voltage was required to be regulated to within 1 percent of 1200 Vdc for all line and load conditions. Since the control circuit used an integrator type design at low frequencies, the 1 percent regulation was easy to meet. Table 9 summarizes the worst case output voltage change over all load and line conditions. The 0.126 percent regulation meets the requirement.

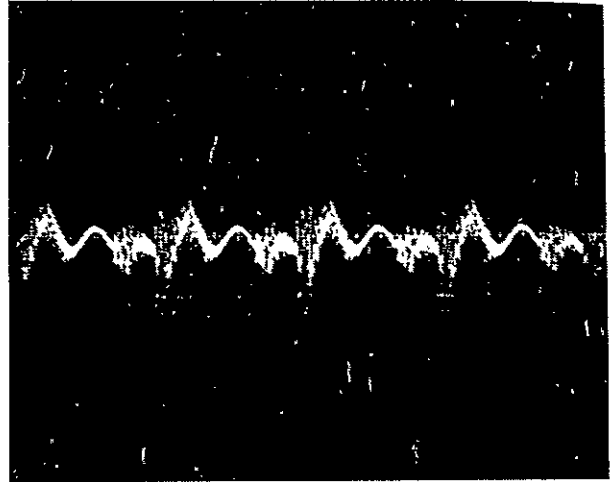
The output ripple voltage is shown in Figure 21 for a 20W load and a 100W load. The output ripple voltage is less than 10 Vpp including switching noise from the 100 kHz chopper. In the engineering breadboard the output filter was a pi filter where both capacitors were 0.02  $\mu$ F ceramic capacitors. In the final module, it was desired to put the filter capacitor inside of capacitor-diode module and to use three of the 0.2  $\mu$ F capacitors in series to get a 0.067  $\mu$ F capacitor. This capacitor is connected across the output of the capacitor diode module and provides adequate filtering without using the filtering characteristics of the short circuit inductor.

TABLE 9. OUTPUT VOLTAGE REGULATION

	V <sub>max</sub>	V <sub>min</sub>	$\Delta V$	Percent Regulation
SN 2	1192.4 Vdc	1190.9 Vdc	1.5	0.126
SN 3	1199.3 Vdc	1198.6 Vdc	0.7	0.053



a) 5V/DIV  
2 SEC/DIV  
 $P_o = 20W$



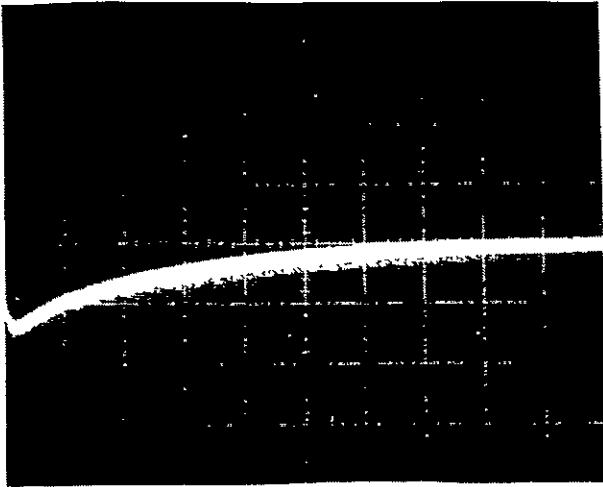
b) 5V/DIV  
2 SEC/DIV  
 $P_o = 100W$

Figure 21. Output ripple voltage.

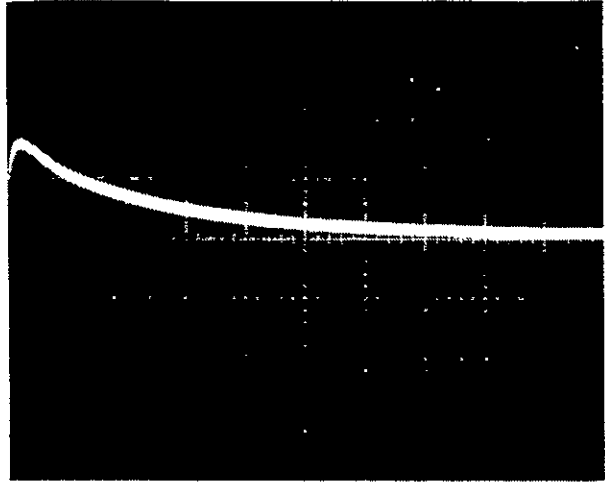
After testing the unit with the final capacitor diode module, it was found that the response time to return to within 1 percent of the normal output voltage was slightly longer than 1 ms. It was observed that the  $0.067 \mu F$  capacitance at the CDVM output was the cause. As a result, the gain of the control amplifier was readjusted. The results of the new transient load and line test are summarized in Figure 22. With the new compensation, the circuit recovers to within 1 percent of its steady state value within 0.5 ms for all conditions.

The larger capacitor on the capacitor-diode module output also affected the short-circuit recovery time. With the pi filter (two  $0.02 \mu F$  capacitors), the output voltage ramped up from 10 to 90 percent of 1200 Vdc in approximately 0.9 ms. With the new capacitor in the circuit, it required 1.6 ms, which is still well within the 5 ms requirement. The short-circuit recovery response is shown in Figure 23.

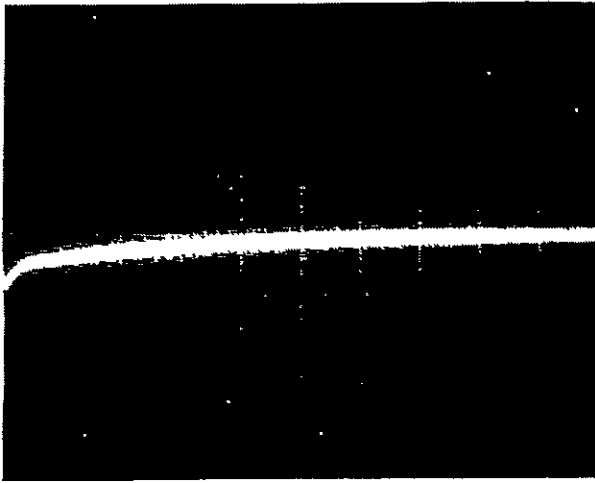
To verify the operation of the CDVM converter at the temperature extremes, the output voltage and efficiency were measured at  $0^\circ C$ ,  $22^\circ C$  and  $50^\circ C$ . The results of these tests are shown in Table 10. The short-circuit protection also operated satisfactorily at the temperature extremes.



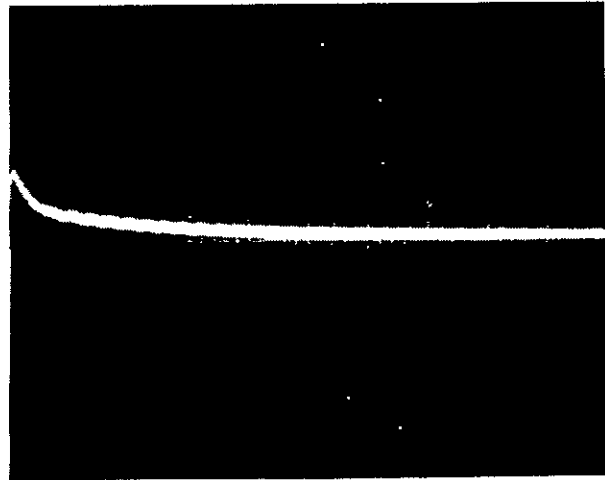
a) LOAD - 10V/DIV, 0.5 ms/DIV,  
Po = 20W → 100W, Vin = 110Vdc



b) LOAD - 10V/DIV, 0.5 ms/DIV  
Po - 100W → 20W, Vin = 110Vdc

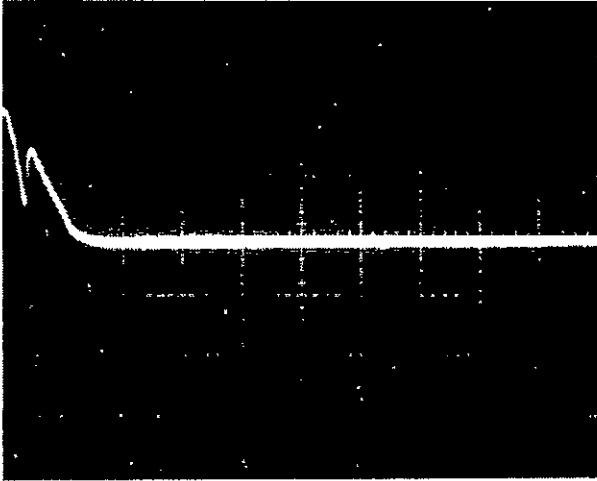


c) LOAD - 10V/DIV, 0.5 ms/DIV,  
Po = 20W → 100W, Vin = 130Vdc

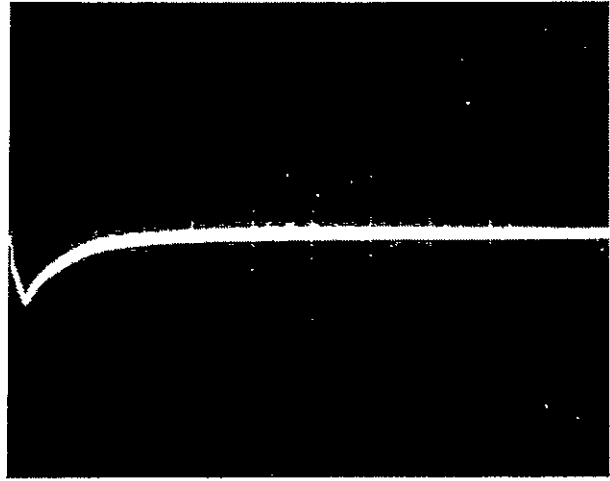


d) LOAD - 10V/DIV, 0.5 ms/DIV,  
Po = 100W → 20W, Vin = 130Vdc

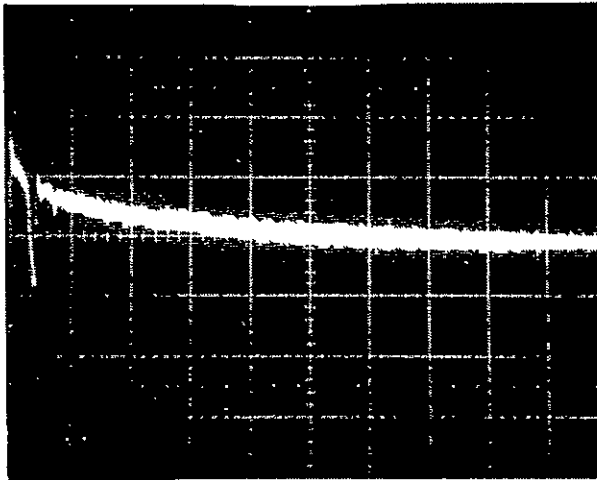
Figure 22. Transient load and line tests. (sheet 1 of 2)



e) LINE — 10V/DIV, 0.5 ms/DIV,  
Po = 20W, Vin = 110Vdc→130Vdc



f) LINE — 10V/DIV, 0.5 ms/DIV,  
Po = 20W, Vin = 130Vdc→110Vdc



g) LINE — 10V/DIV, 0.5 ms/DIV,  
Po = 100W, Vin = 110Vdc→130Vdc

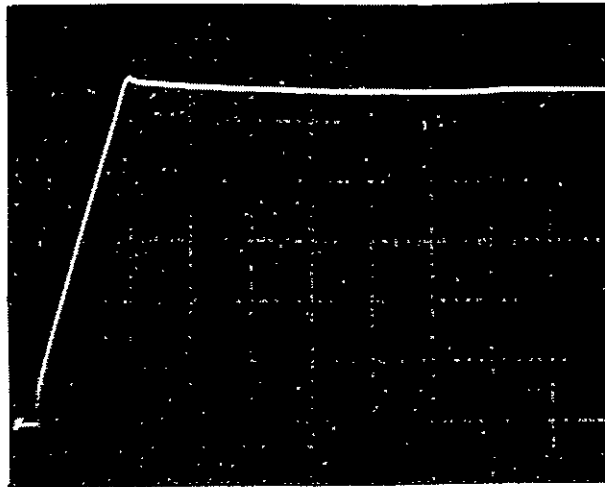


h) LINE — 10V/DIV, 0.5 ms/DIV,  
Po = 100W, Vin = 130Vdc→110Vdc

Figure 22. Transient load and line tests. (sheet 2 of 2)

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OUTPUT VOLTAGE - 200V/DIV, 1 ms/DIV,  
 $P_o = 100W$ ,  $V_{in} = 110 V_{dc}$

Figure 23. Short circuit recovery response.

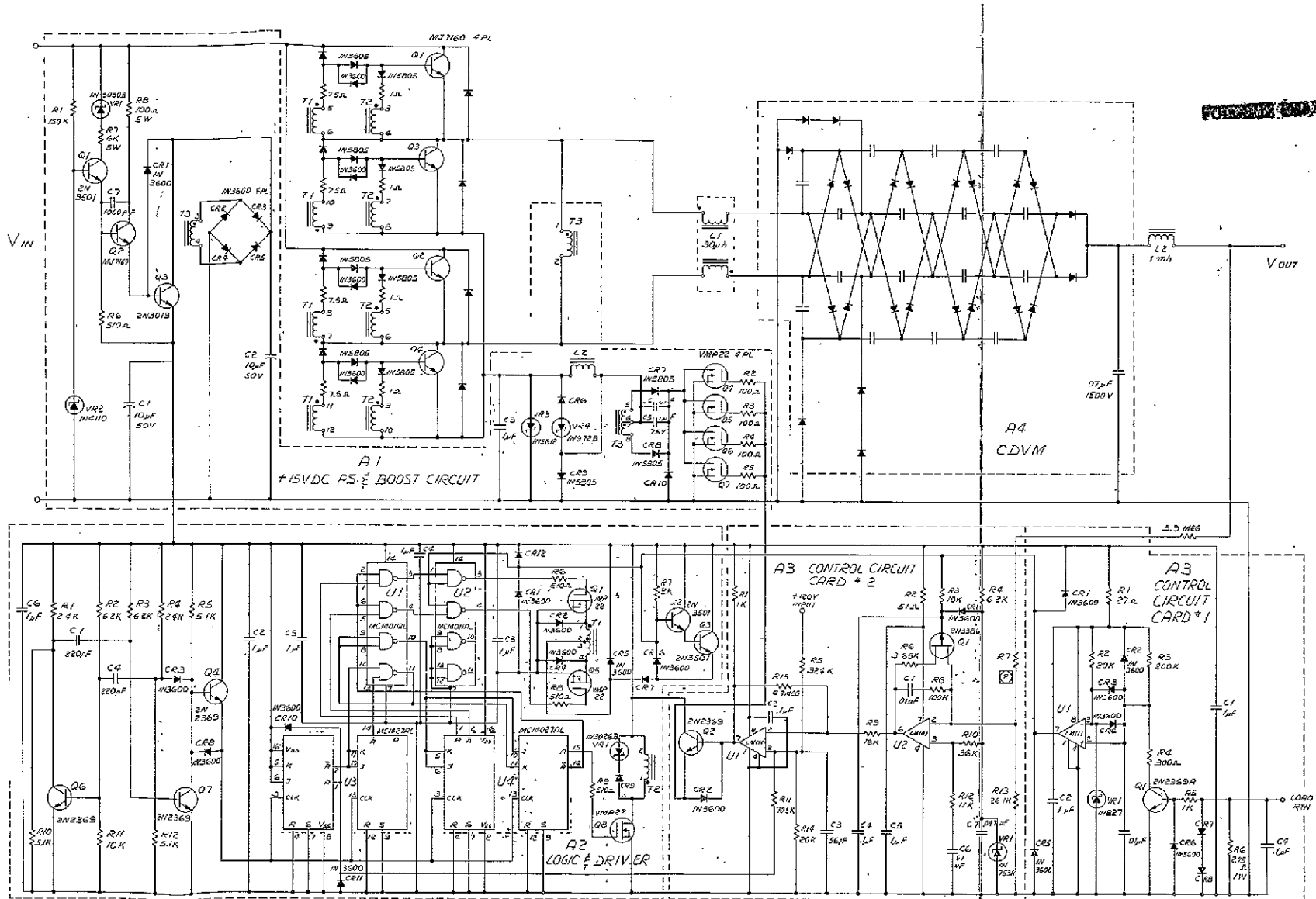
TABLE 10. CDVM CONVERTER PERFORMANCE AT TEMPERATURE EXTREMES

(S/N 2)

Ambient Temperature (°C)	$P_{OUT} = 100$ Watts			$P_{OUT} = 20$ Watts		
	Input Voltage (Vdc)	Output Voltage (Vdc)	Efficiency, Percent	Input Voltage (Vdc)	Output Voltage (Vdc)	Efficiency, Percent
22	110	1207.9	90.3	110	1193.0	78.3
22	130	1200.3	92.1	130	1193.2	77.2
0	110	1192.5	89.1	110	1183.1	79.5
0	130	1209.7	89.6	130	1183.5	78.7
50	110	1214.3	90.2	110	1202.7	76.5
50	130	1218.9	90.8	130	1203.2	75.8

A life test was performed to demonstrate the long term stability and reliability of the circuit. At the time of issuance of this report, the power supply had accumulated 3000 hours of operation with no noticeable change in operating characteristics.

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NOTES - UNLESS OTHERWISE SPECIFIED  
 1. ALL DIODES ARE 3FF50  
 2. VALUE TO BE DETERMINED AT ASSEMBLY

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Figure 24. Capacitor-diode voltage multiplier regulator.

## 6. CONCLUSIONS AND RECOMMENDATIONS

This work has demonstrated that it is feasible to construct a highly efficient, low weight CDVM power supply. It was shown that it is possible to build a fully regulated and short-circuit protected 1200V, 100W supply with a component weight of less than 200 grams. Although this weight is only approximately 60 percent of that of a conventional transformer-rectifier supply, it was shown that the calculated MTBFs for the two supplies are approximately equal.

The weight advantages were derived from unique circuit design, as well as the use of new, high energy density capacitors. Major advantages of the power supply techniques developed under this program are low weight, high efficiency at high operating frequency and the elimination of the usually bulky and expensive power-transformer. The major disadvantage is the lack of isolation that the power-transformer provides.

The program has also provided a clearer insight into the application of components to high frequency CDVM circuits, particularly with respect to the CDVM capacitors and switching transistors. It was found that the selection of the proper components for this application is critical, if a reliable system is to be achieved.

Finally, it should be noted that the weight analyses in this report are based exclusively on the weight of the components. The weight of the mechanical structures, such as the case, circuit boards, heatsinks, and wire, often represent a major portion of the total package weight. Therefore, lightweight packaging techniques must be used, if the advantage of the CDVM circuit is to be maintained.

## 7. ACKNOWLEDGEMENTS

Mr. Robert M. Martinelli of the Space and Communications Group performed most of the work on circuit design, assisted in the Laboratory by Larry J. Murdy. The CDVM module was designed by Watson H. Kilbourne. Mr. Robert S. Buritz was responsible for the fabrication of the capacitors, assisted by Mr. Edward G. Wong. Mr. Wong also fabricated the CDVM modules. Mr. William E. Michel and Mr. G.I. Cardwell provided valuable consultation on circuit design. Dr. Robert D. Parker consulted in the design of the capacitors.

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## 8. REFERENCES

1. J. D. Cockroft and E. T. S. Walton, "Experiments with High Velocity Positive Ions - Further Developments in the Method of Obtaining High Velocity Positive Ions", Proceedings of the Royal Society, Volume 136A, pp. 619-630, 1932.
2. W. T. Harrigill, Jr., and I. T. Meyers, "High Performance DC-DC Conversion with Voltage Multipliers", Power Electronics Specialists Conference '74 Record, pp. 91-96, 1974.
3. W. T. Harrigill, Jr., and I. T. Meyers, "Efficiency and Weight of Voltage Multiplier Type Ultra Lightweight DC to DC Converters", Power Electronics Specialists Conference '75 Record, pp. 31-37, 1975.
4. W. T. Harrigill, Jr. and I. T. Meyers, "Regulation of a Lightweight, High Efficiency Capacitor Diode Voltage Multiplier DC-DC Converter", Power Electronics Specialists Conference '76 Record, pp. 186-189, 1976.
5. R. D. Parker, Technological Development of High Energy Density Capacitors, Report No. NASA CR124926, 1976.

## APPENDIX A. OUTPUT RIPPLE VOLTAGE DERIVATION

Assumptions:

- (1) All capacitors are the same value, C
- (2)  $I_L$  (Load Current) = 0.0833A
- (3) f (Chopper frequency) = 100 kHz
- (4)  $\Delta V$  (output peak-peak ripple voltage) = 24V
- (5) V = total voltage on each capacitor

### 1. SINGLE PHASE, TYPE A

Over a given half cycle,

$$\Delta V = \left[ \frac{I_L}{C} + \frac{3I_L}{C} + \frac{5I_L}{C} + \dots + \frac{17I_L}{C} \right] \Delta t$$

but  $\Delta t = \frac{1}{2f}$ , so

$$\Delta V = \left[ \frac{I_L}{C} + \frac{3I_L}{C} + \frac{5I_L}{C} + \dots + \frac{17I_L}{C} \right] \frac{1}{2f}$$

$$\Delta V = 40.5 \frac{I_L}{C f}$$

Solving for C,

$$C = 40.5 \frac{I_L}{\Delta V f}$$

but  $C_{TOT} = 17C$ , so

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$$C_{TOT} = 688.5 \frac{I_L}{\Delta V f} = \frac{688.5 \times 0.0833}{24 \times 100 \times 10^3} \approx 23.9 \mu\text{F}$$

The total energy storage is

$$W = 1/2 C_{TOT} V^2 = 1/2 (23.9 \mu\text{F}) (135)^2 = 0.218 \text{ Joule}$$

## 2. SINGLE PHASE, TYPE B

Over a given half cycle,

$$\Delta V = \left[ \frac{I_L}{C} + \frac{3I_L}{C} + \frac{5I_L}{C} + \frac{7I_L}{C} + \frac{9I_L}{C} \right] \Delta t$$

but  $\Delta t = \frac{1}{2f}$ , so

$$\Delta V = \left[ \frac{I_L}{C} + \frac{3I_L}{C} + \frac{5I_L}{C} + \frac{7I_L}{C} + \frac{9I_L}{C} \right] \frac{1}{2f}$$

$$\Delta V = 12.5 \frac{I_L}{C f}$$

Solving for C,

$$C = 12.5 \frac{I_L}{\Delta V f}$$

but  $C_{TOT} = 17C$ , so

$$C_{TOT} = 212.5 \frac{I_L}{\Delta V f} = \frac{212.5 \times 0.0833}{24 \times 100 \times 10^3} = 7.38 \mu\text{F}$$

The total energy storage is

$$W = 1/2 C_{TOT} (2V)^2 = 1/2 (7.38 \times 10^{-6}) (270)^2 = 0.269 \text{ Joule}$$

### 3. TWO PHASE, TYPE A

Over a given half cycle,

$$\Delta V = \left[ \frac{I_L}{C} + \frac{2I_L}{C} + \frac{3I_L}{C} + \dots + \frac{8I_L}{C} \right] \Delta t$$

but  $\Delta t = \frac{1}{2f}$ , so

$$\Delta V = \left[ \frac{I_L}{C} + \frac{2I_L}{C} + \frac{3I_L}{C} + \dots + \frac{8I_L}{C} \right] \frac{1}{2f}$$

$$\Delta V = 18 \frac{I_L}{C f}$$

Solving for C,

$$C = 18 \frac{I_L}{\Delta V f}$$

but  $C_{TOT} = 16C$ , so

$$C_{TOT} = 288 \frac{I_L}{\Delta V f} = \frac{288 \times 0.0833}{24 \times 100 \times 10^3} = 10.0 \mu F$$

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The total energy storage is

$$W = 1/2 C_{TOT} V^2 = 1/2 (10 \times 10^{-6}) (135)^2 = 0.0911 \text{ Joule}$$

### 4. TWO PHASE, TYPE B

Over any given half cycle

$$\Delta V = \left[ \frac{I_L}{C} + \frac{2I_L}{C} + \frac{3I_L}{C} + \frac{4I_L}{C} \right] \Delta t$$



but  $\Delta t = \frac{1}{2f}$  so

$$\Delta V = \left[ \frac{I_L}{C} + \frac{2I_L}{C} + \frac{3I_L}{C} + \frac{4I_L}{C} \right] \frac{1}{2f}$$

$$\Delta V = \frac{5I_L}{C f}$$

Solving for C,

$$C = \frac{5I_L}{\Delta V f}$$

but  $C_{TOT} = 16 C$  so

$$C_{TOT} = \frac{80I_L}{\Delta V f} = \frac{80 \times 0.0833}{24 \times 100 \times 10^3} = 2.78 \mu F$$

The total energy storage is

$$W = \frac{1}{2} C_{TOT} (2V)^2 = \frac{1}{2} (2.78 \mu F) (270)^2 = 0.101 \text{ Joule}$$

## APPENDIX B. RECTIFIER FORWARD LOSSES CALCULATION

### 1. SINGLE-PHASE CDVM

There is only one path to the output. Therefore, over a full cycle, the average rectifier current must be equal to the load current. If there are  $n$  rectifiers between the input and output of a CDVM, the total loss in the rectifiers is

$$P_{1\Phi} = n I_L V_{fwd}.$$

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### 2. TWO-PHASE CDVM

Since there are two independent paths to the output, the average current in each rectifier over a full cycle will be  $I_L/2$ . In this comparison, there will be  $n'$  rectifiers carrying  $1/2 I_L$ . The total rectifier loss will be

$$P_{2\Phi} = n' (1/2 I_L) V_{fwd}.$$

The ratio of rectifier losses in the  $1\Phi$  CDVM to the losses in the  $2\Phi$  CDVM is

$$\frac{P_{1\Phi}}{P_{2\Phi}} = \frac{n I_L V_{fwd}}{n' \frac{I_L}{2} V_{fwd}}.$$

But  $n' = n + 1$  for both CDVMs to have the same output voltage. Therefore

$$\frac{P_{1\Phi}}{P_{2\Phi}} = \frac{2n}{n + 1}$$

for  $n = 17$  ( $V_o = 9 \times V_{in}$ )

$$\frac{P_{1\Phi}}{P_{2\Phi}} = \frac{2 \times 17}{17 + 1} = 1.89$$

## APPENDIX C. POWER DISSIPATION EQUATIONS

### 1. TRANSISTOR "ON" LOSSES

The average current in the transistors is

$$I_{ave} = \frac{P_{in}}{V_{in}} = \frac{P_o}{\eta V_{in}}$$

The average power in the transistors is then  $P_{ave} \approx I_{ave} V_{ce (on)}$  but 2 transistors always carry current.

$$P_{fwd} = \frac{2P_o V_{ce (on)}}{\eta V_{in}}$$

with  $P_o = 100W$ ,  $\eta = 0.91$ ,  $V_{ce (on)} = 1V$ ,  $V_{in} = 120 vdc$

$P_{fw} = 1.83W$
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### 2. TRANSISTOR SWITCHING LOSSES

During the switching interval, capacitance must be charged by the device which is being turned "on". Four basic terms have been included

$C_{junction}$  = Transistor junction capacitance  $\approx 100 pF$

$C_{chassis}$  = Capacitance between transistor collector and chassis ( $\approx 100 pF$ )

$C_{rect}$  = Reverse junction capacitance of a single CDVM rectifier ( $\approx 14 pF$ )

$C_{stray}$  = Stray capacitance to ground ( $\approx 30 pF$ )

The total losses due to these terms are

$$P_s = 1/2 C_{\text{chassis}} V_{\text{in}}^2 f \times 4 + 1/2 C_{\text{junction}} V_{\text{in}}^2 f \times 4$$

$$+ 1/2 \times 9 C_{\text{rect}} V_{\text{in}}^2 f + 1/2 C_{\text{stray}} V_{\text{in}}^2 f \times 4$$

$$P_{\text{sw}} = 1/2 V_{\text{in}}^2 f (4 C_{\text{chassis}} + 4 C_{\text{junction}} + 9 C_{\text{rect}} + 4 C_{\text{stray}})$$

with  $V_{\text{in}} = 140 \text{ vdc}$ ,  $f = 100 \text{ kHz}$

$$P_{\text{sw}} = 1/2 (140)^2 (100 \times 10^3) [400 \text{ pF} + 400 \text{ pF} + 126 \text{ pF} + 120 \text{ pF}]$$

$P_{\text{sw}} = 1.03 \text{ W}$
----------------------------------

### 3. DRIVE AND CONTROL POWER

15 Vdc power into the logic and drive circuit was measured at 1.6W.

### 4. DIODE FORWARD LOSSES

The equation for the diode forward losses were derived for a two-phase CDVM in Appendix B.

APPENDIX B  
 EQUATION 10

$$P_{\text{rect}} = n' \frac{I_L}{2} V_{\text{fwd}}$$

for  $n' = 18$ ,  $I_L = 0.0833$  and  $V_{\text{fwd}} = 1.1 \text{ V}$

$P_{\text{rect}} = 0.825 \text{ W}$
-------------------------------------

## 5. CAPACITOR ESR LOSSES

The RMS current for each capacitor has been calculated assuming each rectifier conducts for 1/5 of the half cycle. There are four distinct groups of capacitors. The  $C_1$  group carry  $I_L$  average while  $C_2$ ,  $C_3$  and  $C_4$  carry  $2I_L$ ,  $3I_L$  and  $4I_L$  respectively. The RMS current in each capacitor is calculated below.

The peak current is determined by the average current ( $I_{ave}$ ) required to flow and the duty cycle (D). Assuming sinusoidal waveforms,

$$I_{pk} = \frac{1}{D} \times \frac{\pi}{2} I_{ave}$$

to convert to RMS,

$$\begin{aligned} I_{RMS} &\approx \sqrt{D} \frac{\sqrt{2}}{2} \times I_{pk} \\ &\approx \sqrt{D} \times \frac{\sqrt{2}}{2} \frac{1}{D} \frac{\pi}{2} I_{ave} \end{aligned}$$

$$I_{RMS} \approx \frac{\pi\sqrt{2}}{4\sqrt{D}} I_{ave}$$

The duty cycle for  $C_1$  through  $C_4$  are 1/5, 2/5, 3/5 and 4/5 respectively. Then, the RMS currents are:

$$I_{RMS} (C_1) = 0.207$$

$$I_{RMS} (C_2) = 0.292$$

$$I_{RMS} (C_3) = 0.358$$

$$I_{RMS} (C_4) = 0.414$$

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The total capacitance ESR losses are then

$$P_{\text{ESR}} = \left( \left[ I_{\text{RMS}}(C_1) \right]^2 R + \left[ I_{\text{RMS}}(C_2) \right]^2 R + \left[ I_{\text{RMS}}(C_3) \right]^2 R + \left[ I_{\text{RMS}}(C_4) \right]^2 R \right)$$

With  $R = 0.05\Omega$  and  $I_{\text{RMS}}(C_x)$  as defined above, the total capacitance ESR loss is:

$P_{\text{ESR}} \approx 0.085 \text{ W}$
--

## 6. BOOST CIRCUIT LOSSES

The boost circuit has four main losses.

1. Transformer losses
2. Bridge rectifier losses
3. Switch losses
4. Commutating rectifier losses

The transformer is assumed to be 99 percent efficient. Assuming the input voltage 120 Vdc, the voltage across the chopper must be approximately 138 Vdc. Therefore, the boost circuit must process 18 vdc and 0.92 adc, i.e., 16.5W. The loss in the transformers is therefore approximately 0.166W. The secondary of the transformer is rectified to about 40 Vdc. Therefore, the average current in the bridge rectifier is  $16.5/40 = 0.413\text{A}$ . The loss in the rectifiers is

$$2 I_{\text{rect}} V_{\text{fwd}} = 2 \times 0.413 \times 1.0\text{V} = 0.826\text{W}$$

The FET switch will carry the full bus current while it is "on". The average power in the switch is

$$I_{in}^2 R_{sw} \frac{t_{on}}{T} = I_{in}^2 R_{sw} \frac{V_o}{V_{C1}} = (0.92)^2 (0.8\Omega) \frac{18}{40} = 0.305 W$$

Switching losses (assuming  $t_r = t_f = 50$  ns) are

$$P_{sw} = 1/2 V_{C1} I_{in} \times f [t_r + t_f]$$

$$V_{C1} = 40V, I_{in} = \frac{109W}{120V} = 0.91A, \text{ and } f = 400 \text{ kHz}$$

$$P_{sw} = 0.728 W$$

The commutating rectifier dissipation is

$$I_{in} \times V_{fwd} \times \left(1 - \frac{t_{on}}{T}\right) = 1.92 \times 1.0 \left(1 - \frac{18}{40}\right) = 0.506 W$$

The total power dissipation in the boost converter is then

$$P_{Boost} = 0.166 + 0.826 + 0.305 + 0.728 + 0.506$$

$P_{Boost} = 2.53 W$
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## 7. BIAS SUPPLY LOSSES

There are two power sources of losses for the 15 Vdc bias supply; directly from the line through a dissipative regulator or from the rectified secondary of  $T_3$ . The a. c. voltage from the  $T_3$  secondary is a 19.4V square wave. The current in the bridge rectifier and in the pass transistor is

$$(19.4 - 15) I_{bias}$$

where  $I_{bias} = 0.107A$



The loss in the transistor and bridge rectifier is then 0.47W. The driver for the pass transistors pulls between 3.5 and 5.5 mA from the 120 Vdc bus depending on the  $h_{FE}$  of the pass transistor. Taking the average of the two, the power loss in the driver stage is

$$(V_{bus} - 15 \text{ Vdc}) (0.0045) = (120 - 15) (0.0045) = 0.473 \text{ W}$$

The total loss in the bias supply is

$$P_{BS} = 0.470 + 0.473$$

$P_{BS} = 0.943 \text{ W}$
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APPENDIX D  
STATEMENT OF WORK

## APPENDIX D. STATEMENT OF WORK

### EXHIBIT "A"

The Contractor shall perform the work described below:

#### SPECIFIC TASKS

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#### I. TASK 1 - Converter Design

- A. The Contractor shall conduct a study and a detailed electrical design of a regulated DC-DC converter using a high frequency capacitor diode voltage multiplier that will meet the characteristics outlined in Section VI entitled "Specifications for DC-DC Converters Using High Frequency Capacitor Diode Voltage Multiplication", hereafter referred to as "Specifications". The study and design shall be based on those approaches described in NASA TMX-71566, "High Performance DC-DC Conversion With Voltage Multipliers", and NASA TMX-71735, "Efficiency and Weight of Voltage Multiplier Type Ultra Lightweight DC-DC Converters". The study and the detailed design shall include:
1. An investigation of various methods for the regulation of the output voltage to compensate for changes in output power and input voltage.
  2. An assessment of critical component requirements and availability (transistors, inductors, capacitors, diodes and other components) applicable to this converter technology.
  3. An investigation of low loss, lightweight signal generators and switch driving circuits.
  4. An investigation of the use of an output filter, together with the use of small CDVM unit capacitors, to reduce total weight.
  5. An investigation of output short circuit self-protection methods.
  6. An engineering evaluation of the inherent potential reliability (complete with an identification of potential failure modes) of the proposed CDVM electrical design versus a conventional chopper transformer rectifier design.
- B. The Contractor shall use ultra lightweight capacitors, such as those made with thin films of polysulfone or polyvinylidene

fluoride, or with ceramic dielectrics. This consideration shall include the polyvinylidene and polysulfone dielectric film capacitors described in NASA report number CR-124926. The Contractor shall prepare drawings described in the Schedule and present details of the converter electrical design, the assessment of critical component availability, the inherent reliability, and breadboard physical layout at a design review at Lewis Research Center. The design and layout shall be subject to approval by the NASA Project Manager before the Contractor proceeds with fabrication as required in Task 2.

## II. TASK 2 - Breadboard Fabrication

Based on the results of Task 1 and the approved design, the contractor shall procure parts and fabricate two identical breadboard models of the CDVM dc-dc converter. Accurate documentation of the CDVM converter electrical component weight shall be made.

## III. TASK 3 - Testing and Evaluation of Breadboards

The Contractor shall prepare a test plan for detailed electrical performance tests to be conducted on one of the two breadboards and, limited acceptance tests of the other units. The detailed performance tests shall be formulated to demonstrate conformance with the "Specifications" and to substantiate the inherent CDVM characteristics which affect the potential reliability as evaluated in subparagraph 6 of Task 1. The plan shall be submitted to the NASA Project Manager for approval. The Contractor shall conduct performance tests in accordance with the approved plan.

## IV. TASK 4 - Delivery

At the conclusion of the technical effort the contractor shall ship all breadboards to NASA Project Manager, and shall provide complete updated design evaluation drawings, parts lists, component weight documentation and instructions for operation, along with any special cables and connectors required for typical laboratory operation.

## V. TASK 5 - Reporting Requirements

- A. Technical, financial, and scheduler reporting shall be in accordance with the attached Reports of Work clause, which is hereby made a part of this contract.
- B. The Contractor shall not report data in columns 7b, 9a, and 9b of NASA Form 533P.

- C. The Monthly Contractor Financial Management Performance Analysis Report (NASA Form 533P) and the Monthly Technical Progress Narrative Reports shall be due in the offices of the addressees on or before the fifteenth calendar day of the month following the month being reported.
- D. The number of copies to be submitted for each monthly report is as follows:
1. Fifteen copies of the Monthly Technical Progress Narrative.
  2. Eight copies of the Contractor Financial Management Performance Analysis Report (NASA Form 533P).
- E. The reporting categories to be reported in the Contractor's monthly reports are as follows:
- NASA Form 533P, Monthly Contractor Financial Management Report:
- |                 |                   |                                      |
|-----------------|-------------------|--------------------------------------|
| Task 1          | Hours and Dollars | Converter Design                     |
| Task 2          | Hours and Dollars | Breadboard Fabrication               |
| Task 3          | Hours and Dollars | Testing and Evaluation of Breadboard |
| Task 4          | Hours and Dollars | Delivery                             |
| Task 5          | Hours and Dollars | Reporting Requirements               |
| Subtotal        | Hours and Dollars |                                      |
| Fixed Fee       | Dollars           |                                      |
| Total Resources | Dollars and Hours |                                      |
- F. Within twenty working days after completion of the technical effort, the Contractor shall orally present a summary of the effort and the results of Tasks 1 through 3 at the NASA Lewis Research Center.

VI. SPECIFICATIONS FOR DC-DC CONVERTER USING HIGH FREQUENCY CAPACITOR DIODE VOLTAGE MULTIPLICATION

Rated output voltage:	1200 vdc
Rated output power range:	20 to 100W
Output voltage ripple (peak-to-peak):	1.0 percent or less
Input voltage range:	110 to 130 vdc
Output voltage regulation:	1.0 percent or less
Short circuit protection:	Shall survive a continuous short at the converter output terminals and return to the regulated output voltage within 5 ms after removal of the short.

Total component weight:	150 grams
Internal operating frequency:	Between 50 and 150 kHz
Efficiency:	Greater than 90 percent at 100W and not less than 80 percent within the output power range.
Operating ambient temperature range:	0° to 50°C Circuit design and breadboard layout shall recognize the thermal constraints associated with potential use of this converter concept in a vacuum environment. However, the breadboards need be designed only for operation in air.
Response time of regulating control system:	For a step change of 20V or less within the input voltage range, the output voltage shall recover to within 1.0 percent of 1200V for all loads between 20 and 100W in one (1) ms or less. For a step change of 80W or less within the output power range, the output voltage shall recover to within 1.0 percent of 1200V in one (1) ms or less.

## VII. CONTROL OF EQUIPMENT AND RECORDS

Equipment used in the acquisition of data shall be calibrated, evaluated, maintained, and controlled to ensure its accuracy and reliability.

### A. Calibration

Data acquisition equipment shall be calibrated at scheduled intervals or prior to and after use. The equipment shall be calibrated against certified standards which are readily traceable to National Bureau of Standards.

### B. Evaluation

Data acquisition equipment shall be evaluated prior to use to determine its accuracy, stability, and repeatability. The evaluation results shall be documented. The evaluation required is dependent on the type of equipment and its intended use.

1. Commercial equipment for which sufficient information is available relative to its accuracy, stability, and repeatability need not be evaluated if used according to established practices. However, the equipment shall be calibrated and the results documented.

2. Specially designed equipment shall be evaluated. The equipment shall be checked out prior to actual use by using actual test procedures and conditions to verify the suitability of the equipment for use, adequacy of procedures, ease of operation, accuracy, stability, and repeatability. The results shall be documented.
- C. An equipment log shall be maintained for each apparatus and instrument. Dated entries shall be made for all calibration results, all uses of equipment, all inspection data, and all maintenance operations on the equipment.
- D. Technical record logs shall be established by the Contractor and dated entries shall be made to document the performance of the testing required under this statement of work.
- E. The above equipment and technical record logs shall be fully maintained and be available for review by the NASA Project Manager. The data in these logs shall not be construed as being within the definition of proprietary data. These logs shall be construed as subject data and shall be delivered to the NASA Project Manager upon written request of the Contracting Officer.

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