High Frequency Electrical Model of Through Wafer Via for 3-D Stacked Chip Packaging

Chunghyun Ryu, Jiwang Lee, Hyein Lee, *Kwangyong Lee, *Taesung Oh, and Joungho Kim

Terahertz Interconnection and Package Laboratory, Department of Electrical Engineering,
Korea Advanced Institute of Science and Technology, 373-1 Kusong, Yusong, Daejeon 305-701, Korea.
Lab. homepage) tera.kaist.ac.kr, Tel) +82-42-879-9873, Fax) +82-42-869-8058,
E-mail) sdomain@eeinfo.kaist.ac.kr, teralab@ee.kaist.ac.kr
*Dept. of Material Science & Engineering, Hongik Univ. 72-1 Sangsudong, Seoul 133-706, Korea

Abstracts

In this paper, we propose an equivalent circuit model of through wafer via which has height of 90µm and diameter of 75µm. The equivalent circuit model composed of RLCG components is developed based on the physical configuration of through wafer via. Then, the parameter values of the equivalent circuit model are fitted to the measured s-parameters up to 20GHz by parameter optimization method. The proposed model shows through wafer via is dominantly characterized by the capacitance of thin oxide around the via and resistive characteristic of lossy silicon substrate. From simulated TDR/TDT and eye-diagram waveforms of the proposed equivalent circuit model, it is found that parasitic effects of the via cause slow rising time of a signal during transmission of the signal to the through wafer via. However, unlike to the most cases, the slow rising time of through wafer via will not degrade signal integrity severely. At last, we show the effect of dimension of through wafer via on performance of signal transmission using 3-D full wave simulation.

Introduction

As demands for consumer products, such as mobile phone, PDA, digital camera, and other mobile devices increase, there have been strong needs for high-density package which include multiple chips within the package. 3-D chip stacking package has been proposed as a way to overcome the density and size limitation of conventional single-chip package. Through wafer via, which is electrically isolated interconnect through silicon, is one of the key technologies for the future's 3-D chip stacking package as shown in Figure 1.
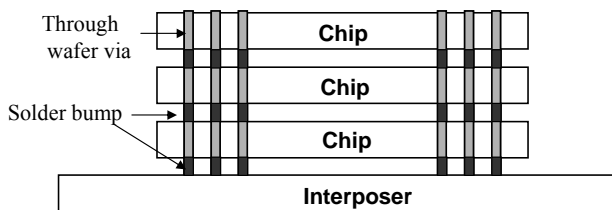

Fig. 1 Cross-section view of the through wafer via in 3-D chip stacking package.

Applications of through silicon wafer via technology of 3-D packaging offer excellent electrical performance and possibility of advanced wafer-level 3-D packaging or stacking of various types of micro-components directly on a CMOS chip [1-4].

To apply through wafer via technology to 3-D stacking package, electrical property of through wafer via should be characterized to estimate quality of the signal in 3-D stacking package. There has been effort to analyze electrical characteristics of through wafer via, and an equivalent circuit model of through wafer via was extracted from measured S-parameters [5]. Previous equivalent circuit model was extracted from a through via which has silicon substrate with high resisitivity 3000Ω·cm. And the through wafer via was modeled with series inductance and resistance [5]. However, in CMOS chips, through wafer via is fabricated in low resisitivity silicon substrate. Therefore an equivalent circuit model of the through wafer via should not be composed of series inductance and resistance simply.

In this paper, we propose an equivalent circuit model of a through wafer via of 10Ω·cm resisitivity silicon which is generally used in CMOS chips. The equivalent circuit model is fully composed of RLCG components, and it is developed based on the physical configuration of the through wafer via. Then, the parameter values of the equivalent circuit model are fitted to the measured S-parameters up to 20GHz by parameter optimization method [6]. And then, using the proposed equivalent circuit model, TDR/TDT and eye-diagram are acquired by simulation, and the characteristics of the through will be found analyzing simulation results. Finally, this paper shows how we can design through wafer via to improve performance of through wafer via using 3-D EM full wave simulation.

Fabrication of Through Wafer Via

To make Cu through wafer vias, via holes of 75μm diameter, 150μm depth, and 150μm pitch were formed on 550μm -thick p-type (100) Si wafer which has resisitivity of 10Ω·cm by using Deep RIE(Reactive Ion Etching). SiO_2 layer of 0.1μm thickness was formed on the surface of the Si wafer and via holes by using the dry oxidation method as an insulation layer between Si and Cu through vias. As a seed layer for electroplating of the Cu vias, 170 nm-thick Ta and 1μm-thick Cu were sequentially sputter-deposited on the surface of the via holes by using IMP (ionized metal plasma) system.

For Cu via filling into the via holes with the Ta/Cu seed layer, the electroplating solution was made by adding 300 ppm PEG (polyethylene glycol) and $CuCl_2$ 0.17 g/L as inhibitors and by adding small amounts of MPSA (3-mercapto-1-propanesulfonate) and SPS (sulfo-propyldi-sulfide) as accelerators into a solution composed of 0.25M $CuSO_4·5H_2O$ and 1M H_2SO_4. The solution was stirred at 200 rpm for 24 hours before electroplating. Si wafer was dipped into 10 vol% H_2SO_4 for 5~10 seconds just before Cu via filling process to remove the oxidation layer on the surface of the Ta/Cu seed layer. Before Cu via filling with electroplating process, the Si wafer was kept in the electroplating solution under a vacuum of 10^{-2} torr for 30 minutes to remove the air inside the via holes. Cu via filling was conducted by using the pulse-reverse pulse electroplating method with the ratio of the reduction current density(IC) to the oxidation current density(IA) as 1:3. After Cu via filling into the via holes, CMP (Chemical Mechanical Polishing) was performed on both sides of the Si wafer to thin it to 90μm thickness. Figure 2 shows a scanning electron microscope photograph of the fabricated through wafer via. To measure the electrical characteristics of the through wafer via, a test device was fabricated as shown in Figure 2.

To measure with a ground-signal-ground probe, we fabricated a coplanar waveguide on a ceramic substrate connected to a ground-signal-ground via with 150μm pitch. The coplanar waveguide was composed of three copper lines, and the width and length of the line were 100μm and 500μm, respectively. The pitch of the coplanar waveguide was same as that of the ground-signal-ground via, which was, 150μm.
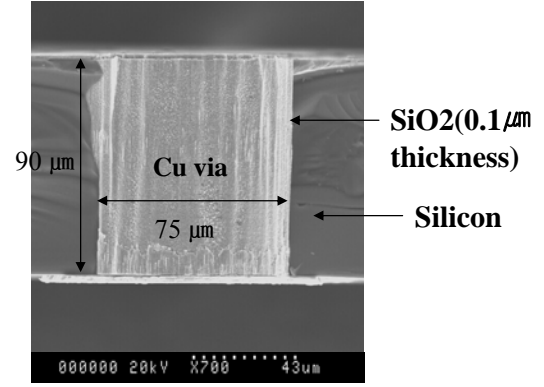

Fig. 2 Microphotograph of the fabricated through wafer via

To connect the ground-signal-ground via to the coplanar waveguide on the ceramic substrate, Cu/Sn bumps were fabricated under the vias. The diameter and height of the Cu/Sn bumps were 100μm and 3μm, respectively. On top of the via, soft tin which has a height of 1μm and a diameter of 100μm was plated for micro-probing.

Proposed Equivalent Circuit Model of Through Wafer Via

From the physical configuration of the through wafer via, a schematic of the equivalent circuit model is proposed as shown in Figure 3.
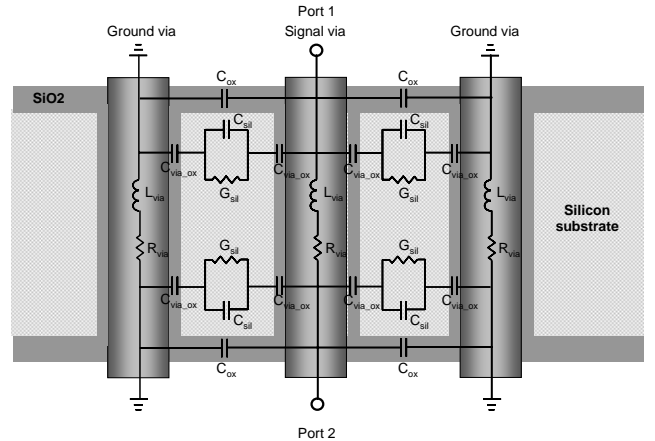

Fig. 3 An equivalent circuit model of the through wafer via.

The self-inductance of the via is characterized by L_{via}, and the resistance of it is represented by Rvia. The parameter C_{via_ox} represents the oxide capacitance between the via and the silicon, and C_{ox} represents the oxide capacitance and the fringing capacitance between the vias. Lossy characteristic of the silicon between the vias is represented by G_{sil},

and the capacitance between the vias is characterized by C_{sil}. In the equivalent model, each port represents signal input and output, and remaining two vias are connected to the ground. Therefore the equivalent circuit model of the through wafer via can be simplified as shown in Figure 4.
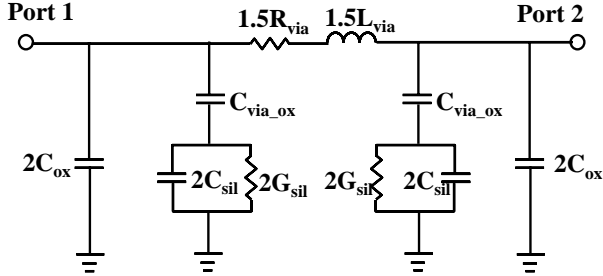

Fig. 4 The simplified equivalent circuit model of the through wafer via

The parameter values of the circuit model were extracted by fitting the measurement-based S-parameters up to 20GHz using parameter optimization method. For 2-ports S-parameter measurements, two micro-probe tips were used. One probe was placed on the top of the ground-signal-ground via and the other on the end of the coplanar waveguide as seen in Figure 5. The S-parameters were measured up to 20GHz using 150μm pitch G-S-G probe tips connected to a network analyzer.
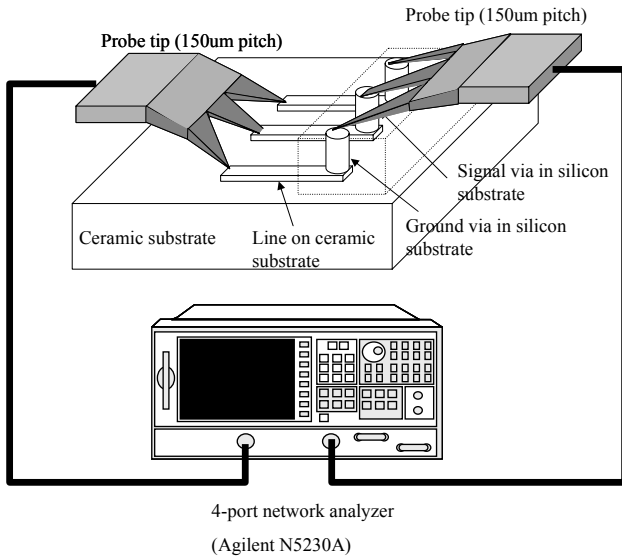

Fig. 5 Schematic of the test device for S-parameter measurement.

For de-embedding of the coplanar waveguide of the test device, we fabricated a replica of the coplanar waveguide of the test device on another substrate. Considering de-embedding of the coplanar waveguide, the following parameter values of the equivalent circuit model were extracted by fitting the measured S-parameters of the test device.

$$C_{ox\_via} = 0.8\,pF,\ G_{sil} = 1.92\,m/\Omega,\ C_{sil} = 9\,fF,$$

$$C_{ox} = 3\,fF,\ L_{via} = 15\,pF,\ R_{via} = R_{via0}\sqrt{1 + \frac{f}{f_0}}$$

where R_{via0} (4mΩ) is resistance of the via at 1GHz considering skin effect, and f_0 is 1GHz.

Figure 6 shows the measured S-parameters of the test device and the simulated S-parameter from the equivalent circuit model of the test device. The S11 and S21 with the magnitude and phase are plotted in Figure 6. The x-symbol lines show the measured S-parameters and the solid lines represent the equivalent circuit model based S-parameters, respectively. As seen in Figure 6, the parameters are reasonably matched up to 20GHz.

Observing the magnitude of S21 based on the measurement and simulation, the magnitude of S21 drops sharply under 1GHz because lossy characteristic of silicon starts to appear as the impedance of oxide capacitance of via decreases as frequency goes higher. At frequency over 1GHz, the impedance of oxide capacitance becomes very small, and the lossy characteristic of silicon becomes more dominant.

So the through wafer via causes inter-symbol interference (ISI) due to frequency dependent loss. It means signal integrity is hurt when data signals are transmitted through the via. In next chapter we will discuss how much the quality of a signal will be distorted by through wafer via.

Through wafer via shows lower series inductance compared to bonding wire of conventional 3-D packaging. It means that through wafer via can be used to provide excellent power ground network environment with low simultaneous switching noise (SSN).

Time-domain Simulation Results

From the proposed equivalent circuit model, we observed that the through wafer via has capacitive and resistive characteristics caused by thin oxide around the via and lossy silicon substrate, respectively. In this chapter, we will discuss how these parasitic characteristics of through wafer via affect signal waveforms.
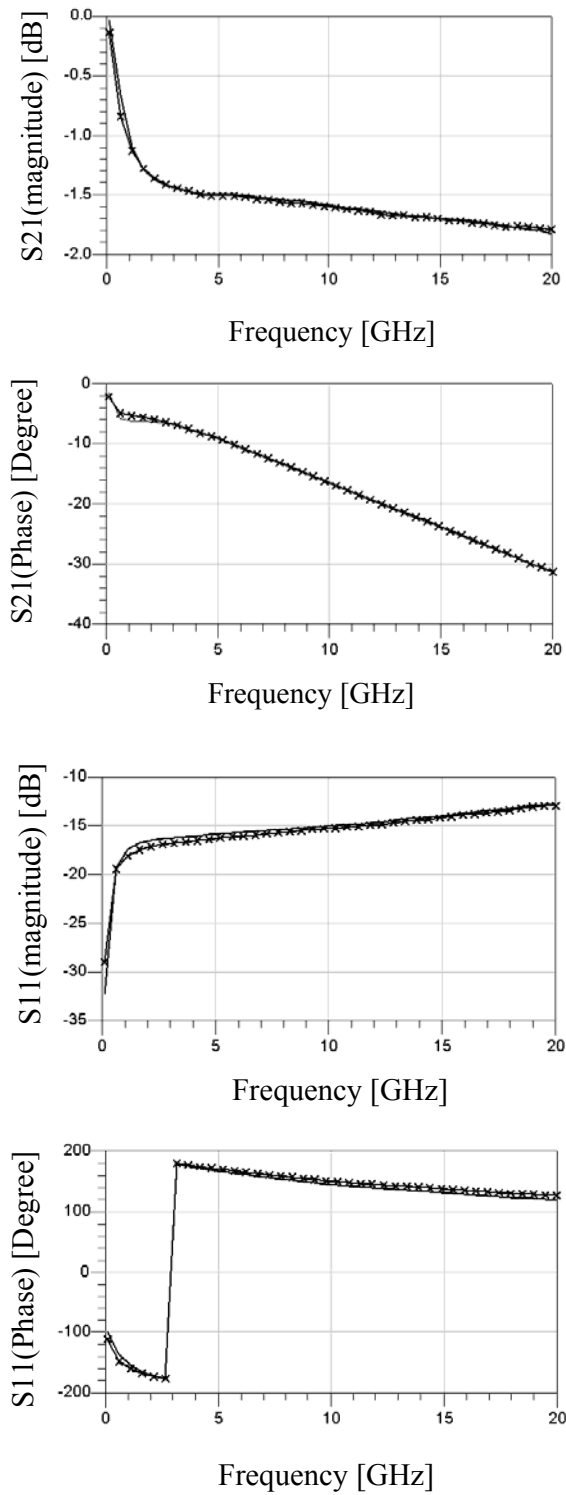
Fig. 6 Comparison of the S-parameters after the parameter fitting using the optimization method.

By using the equivalent circuit model of the through wafer via, Time Domain Reflectometry (TDR) / Time Domain Transmission (TDT) waveforms were gathered as plotted in Figure 7. In the TDR/TDT simulation, 0.5V step pulse which has 50 ps rising time was used. The TDR waveform

describes capacitive characteristic of the via, which comes from the thin oxide with 0.1μm thickness around the via. From the TDT waveform, it was found that the rising time of the transmitted signal becomes much slower than the rising time of the source. However, unlike to the most cases, the signal maintained its sharp rising feature for most of its rising time. But slightly before it reached its peak voltage, its slope decreased dramatically resulting slow rising time. It means the through wafer via will not distort signal severely. And through eye-diagram simulation, the parasitic effect of the through wafer via could be observed as Figure 8. For the eye-diagram simulation, 5 & 10 Gbps pseudo random bit sequence (PRBS) signal was applied to the circuit model of the through wafer via with 50 ps rising and falling time. As seen in Figure 8, the eye diagrams keep their opening well, and the timing and voltage margin do not decrease.
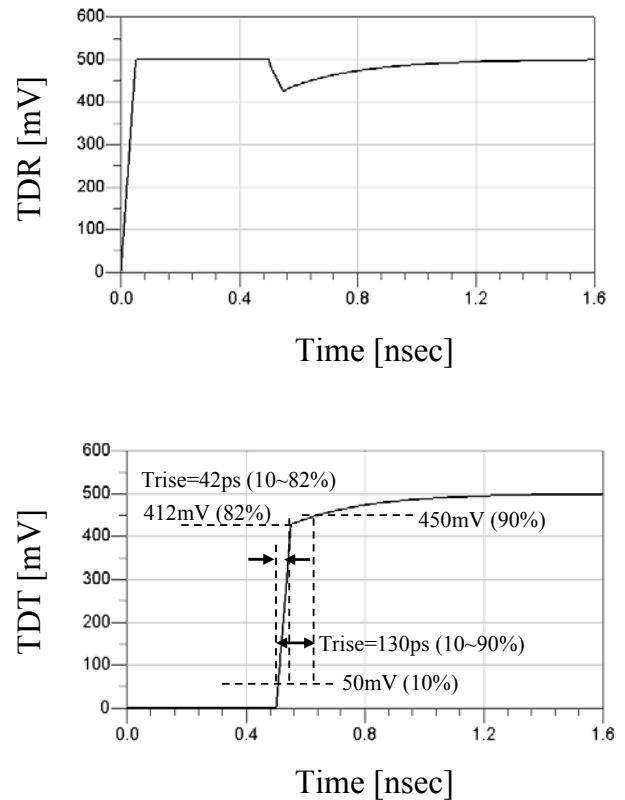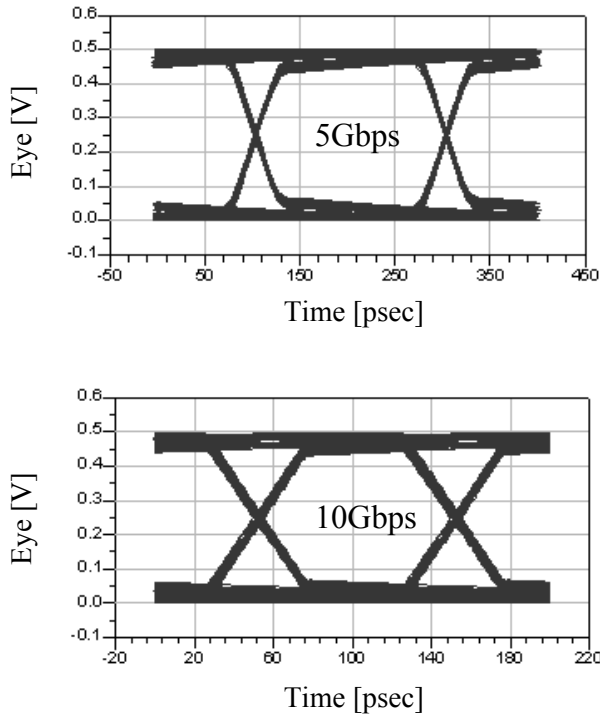

Fig. 7 Simulated TDR/TDT waveforms

5Gbps

10Gbps

Fig. 8 Simulated eye-diagram waveforms

Effect of the via structures

In the equivalent circuit model, we observed the parasitic effects of the through wafer via, and they reduced the magnitude of S21 with over GHz frequency range. And through time-domain results, we verified that the rising time of the signal became slow due to the parasitic effects of the via. Parasitic effect of through wafer via depends on the dimension of the via. In this chapter, we suggest optimal design of through wafer via to reduce the parasitic effects of via using 3-D EM full-wave simulation.

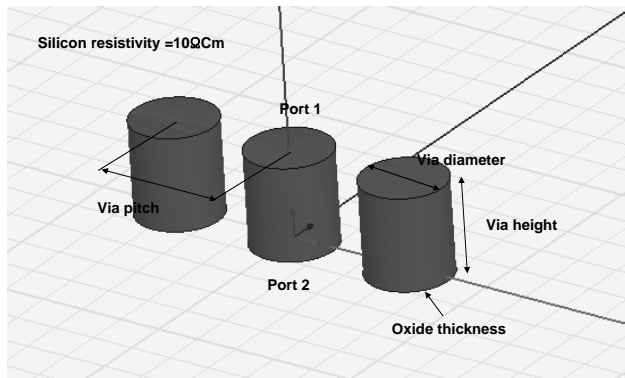Figure 9 shows full-wave simulation model of the through wafer via.

Fig. 9 3-D EM simulation model of the through wafer via using ansoft HFSS

In 3-D simulation model, the resisitivity of silicon substrate is 10 Ω·cm, the material property of the vias is copper. There is ground-signal-ground via, and the parameter values of the vias, such as diameter, height, pitch, oxide thickness are variables. Figure 10 shows the simulated magnitude of S21 of the through wafer via for various the parameter values. As shown in Figure 10, the magnitude of S21 can be increased by doing as follows.

- decrease diameter and height of the via

- increase pitch and oxide thickness of the via

As the diameter and height of the via decrease, the parasitics of the via are reduced. Therefore the magnitude of S21 becomes greater. When pitch of the via increase, the electric field between signal via and ground via will be placed in lossy silicon longer than before. This makes the effective resistance larger. In other words, the conductance of the model decrease, making S21 larger as a result. Increasing the thickness of oxide improves S21 by reducing its capacitance.
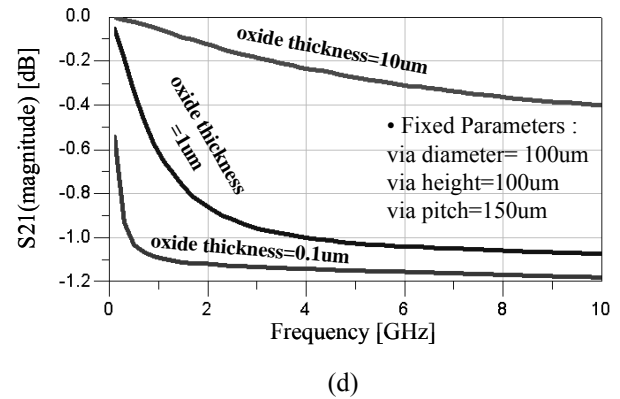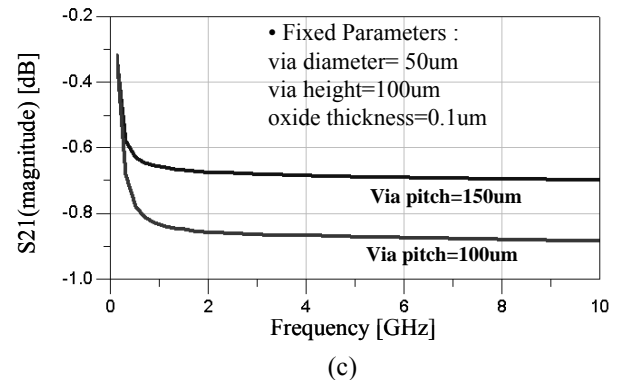

(c)

(d)

Fig. 10 3-D EM simulation results for various parameter values. (a) diameter of via, (b) height of via, (c) pitch of via, (d) oxide thickness

Conclusion

In this paper, we proposed an equivalent circuit model of through wafer via. The proposed circuit model consisted of RLCG lumped circuit elements, and the circuit model parameter values were extracted based on the measurement of S-parameters up to 20GHz. By using the proposed circuit model, TDR/TDT and eye-diagram simulations were performed. From time-domain simulation, it was found that the rising time of the signal becomes much slower. However, the slow rising time of the through wafer via will not degrade signal integrity severely as shown in simulated eye-diagram. At last, we showed the effect of dimension of through wafer via on performance of signal transmission using 3-D full wave simulation. As a result, the magnitude of S21 can be increased by reducing diameter and height of via and increasing pitch of via and oxide thickness.

Acknowledgments

References

1. S. Linder, H. Baltes, F. Gnaedinger, and E. Doering, "Fabrication technology for wafer through-hole hinterconnections and three-dimensional stacks of chips and wafers", in Proc. MEMS, 1994, pp. 349-354.
2. M. Koyanagi, H. Kurino, K. Lee, K. Sakmicrona, N. Miyakawa, H. Itani, "Future System-on-Silicon LSI Systems", IEEE Micro, Vol. 18, No. 4 , July-Aug. 1998, pp 17
3. K. Takahashi, M. Hoshino, H. Yonemura, M. Tomisaka, M. Sunohara, M. Tanioka, T. Sato, K. Kojima, H. Terao, "Development of Advanced 3-D Chip Stacking Technology with Ultra-Fine Interconnection", Proc. 51st Electronic Components and Technology Conf., Orlando, FL., May 2001, pp
4. G. Feng, X. Peng, J. Cai, and S. Wang, "Through-Wafer Via Technolgy for 3-D Packaging", 6th International Conference on Electronic Packaging Technology, pp 57-60, Sept. 2005
5. L. L. W. Leung, and K. J. Chen, "Microwave Characterization and Modeling of High Apect Ratio Through-Wafer Interconnect Vias in Silicon Substrates", IEEE Transation on Microwave Theory and Techniques, " Vol. 53, No. 8, pp 2472-2480, August 2005
6. S. Ahn, J. Lee, J. Lee, J. Kim, W. Ryu, B.-H. Kmicron, H.-S. Choi, C. K. Yoon, and J. Kim, " Over GHz Electrical Circuit Model of a High-Density Multiple Line Grid Array(MLGA) Interposer, IEEE transaction on advanced packaging, Vol. 26.