High-Frequency EMI Attenuation at Source with the Auxiliary Commutated Pole Inverter

Apollo Charalambous[1], Xibo Yuan[1], and Neville McNeill[2]

[1]Department of Electrical and Electronic Engineering, University of Bristol, Bristol, BS8 1UB, United Kingdom.
[2]Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, G1 1RD, United Kingdom.

Corresponding author:
Name: Xibo Yuan
Postal address: Department of Electrical and Electronic Engineering, Merchant Venturers Building, Woodland Road, Bristol, BS8 1UB, United Kingdom.
Telephone number: +44(0) 1179545186; **Fax:** +44(0) 1179545206; **E-mail:** xibo.yuan@bristol.ac.uk

This paper has not been submitted elsewhere previously.

***Abstract*—Fast-switching power converters are a key enabling technology for the More Electric Aircraft (MEA), but the generated Electromagnetic Interference (EMI) poses significant challenges to the electrification effort. To meet the stringent aerospace EMI standards, passive filters are commonly employed, despite the weight and size constraints imposed by the MEA. Alternatively, the EMI source, i.e., the high d*v*/dt and d*i*/dt slew rates, can be addressed through waveform-shaping techniques. For example, while most soft-switching converters can reduce switching loss, they do so by switching the semiconductor devices in a slower and smoother manner, resulting in the attenuation of high-frequency harmonics. This paper examines the Auxiliary Commutated Pole Inverter (ACPI) topology, and its first contribution is the attenuation of the high-frequency content of its EMI source, that is, the output voltage, in a predictable manner, through the active control of the resonant circuit. This is achieved by firstly discussing the time-domain characteristics of trapezoidal and S-shaped pulse-trains that lead to attenuated high-frequency harmonic content, and secondly, by analysing the equivalent LC circuit of the ACPI. The design of the inverter is then focused on the active control of the resonant parameters, for a predetermined and enhanced output voltage high-frequency response. The second contribution of this paper is the comparison of the EMI performance of hard switching and of three soft-switching modes, fixed-timing control, variable-timing control, and capacitive turn-offs, and how this informs important metrics like power efficiency, current stress, and implementation complexity. Lastly, the third contribution is on the trade-offs that arise when the primary design goal is enhanced EMI performance, as opposed to switching loss reduction. A 5-kW, 3-phase ACPI prototype is used for validating the high-frequency content attenuation at source. It is shown that the ACPI can achieve a 37-dB harmonic attenuation of its output voltage at 4 MHz, compared to a hard-switched inverter.**

***Index Terms*— auxiliary commutated pole inverter; EMI; fixed timing; frequency response; more electric aircraft; soft switching; variable timing.**

I. INTRODUCTION

Power electronic converters play a crucial role in the electrification of vehicles and aeroplanes. For example, they are among the key enabling technologies for the More Electric Aircraft (MEA) [1], where electrical systems are increasingly adopted for replacing actuation, fuel handling and cabin air pressurisation systems traditionally powered through hydraulic, pneumatic and mechanical means. MEA offers significant potential for reducing aircraft energy consumption, and consequently, for decreasing fuel burn and emissions. With on-board electrical power generation capacity reaching 1.5 MVA for new aircrafts and future forecasts showing an upward trend with electric propulsion, aggressive power density and efficiency targets are being set for new power electronic equipment to be installed, e.g. 15 kW/kg for power density and 95%+ for efficiency. For these goals to be achieved, the switching speed is pushed higher and higher for reducing the switching loss, thus improving the efficiency and reducing the cooling requirements, e.g. with the use of wide-bandgap power devices [2]. The switching frequency is also being increased for reducing the size of the passive components, such as filtering inductors and capacitors, and for improving the power density.

However, the fast switching action of power devices such as IGBTs and MOSFETs causes high-frequency Electromagnetic Interference (EMI) [3]. This is a major disadvantage, because EMI may disrupt the operation of surrounding electronic equipment [4,5]. Furthermore, common-mode EMI (CM EMI) from voltage-source converter (VSC) based motor drives can cause motor premature winding failure, ball bearing deterioration, and motor terminal overvoltages [6-8]. The electrification effort will thus be hindered if EMI remains unchecked. This is why the aerospace industry has stringent EMI standards such as the DO-160 [9] that defines the limits of conducted EMI in the range between 150 kHz and 152 MHz. The low-frequency EMI, i.e. from 150 kHz to 1 MHz is normally driven by PWM-associated harmonics and the high-frequency EMI from 1 MHz to 152 MHz is mainly driven by the switching transitions and the associated dv/dt and di/dt slew rates.

Conducted EMI is usually attenuated with the help of passive filters [3,10]. However, filters can add a significant portion to a converter's weight and size. This negates the effort to save weight and space that is pursued by the MEA concept, and increases overall cost as well.

Instead of adding filters, the EMI emissions can be attenuated at source. For low-frequency PWM-driven EMI (150 kHz to 1 MHz), this can be achieved by using specialised modulation schemes such as common-mode voltage cancelling [11] and random/chaotic switching [12], or even a lower switching frequency. For high-frequency switching transient-driven EMI (1 MHz to 152 MHz), solutions include the shaping of the converter/power device output waveforms such as through active gate driver control of the power devices [13], and the use of soft-switching topologies.

The active gate driver control method is not pursued in this work since the complexity of such circuits adds significant design effort, and the potential benefit of reducing both switching loss and EMI emissions is not possible.

As known, soft-switching topologies are commonly used for switching loss reduction by decoupling the transitioning edges of the current and voltage of the semiconductor devices [14,15,16]. This decoupling is usually realised with LC circuits that slow and smooth the edges in a resonant manner. When the voltage is manipulated like this, zero-voltage switching (ZVS) is performed. When the current is, zero-current switching (ZCS) is realised. Therefore, the switching transition can be effectively profiled with the di/dt and dv/dt rates controlled by the resonant circuit. As such, soft-switching converters are promising in reducing switching loss as well as the high-frequency content of the switching magnitudes. This is the main reason why soft switching is pursued in this paper.

Though there is a multitude of papers discussing topologies, modulation and control of soft-switching converters, the focus is on reducing the switching loss rather than EMI attenuation. In contrast, works such as [17-22] do indeed explore the viability of reducing EMI with soft-switching converters, both in simulation and in experiment, with encouraging results. An experimental 50-kW, 3-phase auxiliary commutated pole inverter (ACPI) prototype exhibits a 10-dB drop in conducted emissions in the 3 to 5 MHz range and a 5-dB drop from 8 to 12 MHz when compared to an equivalent hard-switched inverter [17]. In [21] a 70-W ZCS flyback converter exhibits a 16-dB conducted EMI attenuation in the frequency range of 5 to 20 MHz, when compared to its hard-switched counterpart. In these papers, it is recognized that some soft-switching topologies showcase an enhanced EMI performance because the di/dt and dv/dt slew rates are influenced directly by the soft-switching process. However, high-frequency harmonic attenuation is treated merely as a by-product of soft switching, or at best, when EMI attenuation is actively pursued, only simulation and experimental results are presented with no insight as to how the resonant process can be actively controlled for this specific task.

In contrast, the first contribution and the focus of this paper is a method of predetermining and attenuating the high-frequency content of an EMI source through the active control of the resonant circuit. The important time-domain characteristics of pulse-trains that lead to less high-frequency content are explored, and inform the design of a soft-switching converter for exhibiting an enhanced frequency response. This is done through analytical expressions for both the high-frequency response and the resonant circuit magnitudes. For this study, the auxiliary commutated pole inverter (ACPI) is chosen, a PWM-compatible soft-switching topology that highly resembles the standard VSC topology. VSCs are the industry standard in variable-speed motor drives, such as the Engine Starter Motor used for jet engine start-up on MEAs [1,23]. Due to this resemblance, the ACPI can be easily employed in motor drive applications.

The developed high-frequency attenuation method is based on the active control of the ACPI's resonant circuit for reducing the harmonic content of the output voltage, which is a significant source of EMI in VSCs. At the heart of this resonant circuit lies an equivalent series LC circuit, the study of which forms the basis for the second contribution of this

paper, namely the development and comparison of three ACPI soft-switching control schemes: fixed timing, variable timing, and capacitive turn-offs. The high-frequency response of these soft-switching schemes is discussed in depth, as well as how inevitably, the demand for attenuated harmonic content informs their performance regarding current stress, power efficiency, and implementation complexity. For example, while capacitive turn-offs can reduce current stress and auxiliary circuit loss by bypassing the auxiliary circuit, they generate linear output voltage edges that can potentially lead to increased high-frequency harmonics. Therefore in this paper, for the purpose of generating of an output voltage with only sinusoidal edges, capacitive turn-offs are initially ignored. All these trade-offs are also studied for the hard switching mode. Lastly, the third contribution of this work is on the trade-offs that arise when the ACPI is designed primarily for enhanced EMI performance, as opposed to when it is designed primarily for switching loss reduction.

This paper is structured as follows: Section II describes the operation of the ACPI. Section III presents the frequency response of trapezoidal and S-shaped pulse-trains, as the basis for an ACPI output voltage with attenuated high-frequency content. Section IV analyses the equivalent LC circuit, and explains how its resonant parameters, specifically the 'boost' currents, can actively control the duration and smoothness of the output voltage edges. Section V discusses and compares the fixed- and variable-timing control schemes with regards to implementation complexity, current stress, power loss, and crucially, output voltage edge shaping. Section VI details the ACPI design procedure for attaining an output voltage with attenuated high-frequency content. Lastly, Section VII presents the experimental results of the high-frequency attenuation, power efficiency, switching transients, and other special issues regarding the operation of the ACPI.

II. The Auxiliary Commutated Pole Inverter

A. Auxiliary Resonant Pole Inverters

This work primarily addresses high-frequency content attenuation at source for the VSC as an AC/DC rectifier, or a DC/AC inverter for motor drives in electromagnetically sensitive environments like the MEA, where it is imperative that the dv/dt of the output voltage is reduced [24]. The 6-switch, 2-level, 3-phase VSC is the standard configuration for AC/DC or DC/AC power conversion. Thus application-wise, the considered soft-switching topologies should be similar to the standard VSC. Given the focus is on the output voltage dv/dt and profile, only ZVS inverters are considered.

The topologies with the highest degree of PWM compatibility, independent phase-leg control, and efficiency, that most resemble the VSC are the auxiliary resonant pole inverter (ARPI) family of ZVS inverters [25]. The most popular ARPIs are the coupled-inductor ZVS inverters [26-29], and the auxiliary commutated pole inverter (ACPI) [30,31]. The coupled-inductor inverters are intended for adaptable control to any load level, and they exhibit the least amount of auxiliary circuit loss of all the ARPIs. However, they have a complicated design and high component counts. The ACPI on the other hand, might exhibit more auxiliary loss, but it has a lower component count, and its operation is simpler and more flexible. For this last reason, the ACPI is chosen as the subject of this study.

B. Operation of the ACPI

Fig. 1 shows an ACPI phase-leg, wherein a VSC phase-leg of main devices S_1/D_1 and S_4/D_4 is supplemented with an auxiliary branch between the DC midpoint O and the output node A. This branch consists of auxiliary devices S_{a1}/D_{a1} and S_{a4}/D_{a4}, in series with a resonant inductor L_r. C_{r1} and C_{r4} are snubber capacitors that are equal in value. Three such ACPI phase-legs comprise the 3-phase version, with all the auxiliary branches sharing O. The clamping diodes in grey, though not part of the topology, are essential for the protection of the auxiliary devices against overvoltages.

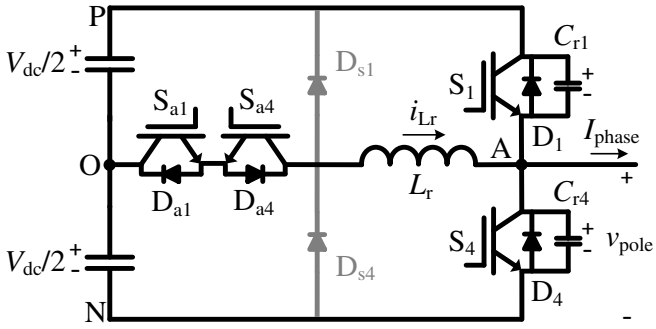

Fig. 1. The circuit schematic of the ACPI phase-leg.

Fig. 2 shows the waveforms of the inductor current i_{Lr}, the phase-leg output voltage v_{pole}, and the switching currents i_{S1} and i_{S4} of the main devices, during a switch turn-on transition (D_4 to S_1) in Fig. 2(a), a switch turn-off transition (S_1 to D_4) in Fig. 2(b), and a capacitive turn-off transition (S_1 to D_4) in Fig. 2(c). The phase current I_{phase} is considered positive and constant during a transition. The sub-circuits during each v_{pole} transition are also shown.

The turn-on transition of Fig. 2(a) starts with S_{a1} turning on first. During the t_{ramp_on} interval, i_{Lr} ramps up and L_r accumulates energy. As i_{Lr} surpasses I_{phase}, i_{S4} reverses through S_4. Then, i_{Lr} reaches I_{trip} and i_{S4} reaches I_{boost}. At this point, L_r starts resonating with C_{r1} and C_{r4}. During the resonant interval t_{res_on}, v_{pole} sinusoidally swings from the negative to the positive rail until it is clamped by D_1. Then i_{Lr} starts ramping down, and the incoming S_1 is gated on. As soon as i_{Lr} drops below I_{phase}, S_1 starts conducting. It is seen that a resonant turn-on transition always involves a swap between the antiparallel diode and its switch, as attested by the direction reversal of i_{S4} and i_{S1}. The swap from D_4 to S_4 allows for the controlled triggering of resonance, and a grace period is created as D_1 conducts during which S_1 is turned on under ZVS.

The turn-off transition of Fig. 2(b) starts with S_{a4} turning on first, and i_{Lr} ramping down in the negative direction, during the t_{ramp_off} interval. Meanwhile, the outgoing switch S_1 conducts the sum of $i_{Lr} + I_{phase}$. When i_{Lr} reaches the value of I_{boca}, and i_{S1} the value of I_{off}, S_1 is turned off and resonance commences. During the resonant interval t_{res_off}, v_{pole} swings down to the negative rail, and the edge is shaped in a sinusoidal fashion. Then, the incoming D_4 clamps v_{pole}, S_4 is gated on, and i_{Lr} starts ramping up to zero. Steady state is then established with D_4 conducting I_{phase}.

The resonant process performs ZVS turn-on and turn-off of the main devices, and ZCS turn-on and natural turn-off of the auxiliary ones. The voltage and the current are decoupled, with resonance slowing down v_{pole} and shaping it in a smooth, sinusoidal manner. Hence, the ACPI can reduce switching loss, while profiling the dv/dt of v_{pole}. However, with

hard switching no auxiliary circuit power loss exists [25,31]. Also, soft switching increases the current stress on the main devices, especially during the turn-off transition, because of the inductor current components I_{boost} and I_{off} that are imposed on i_{S1} and i_{S4}. Hard switching though cannot perform waveform shaping and smoothing, like soft switching can.

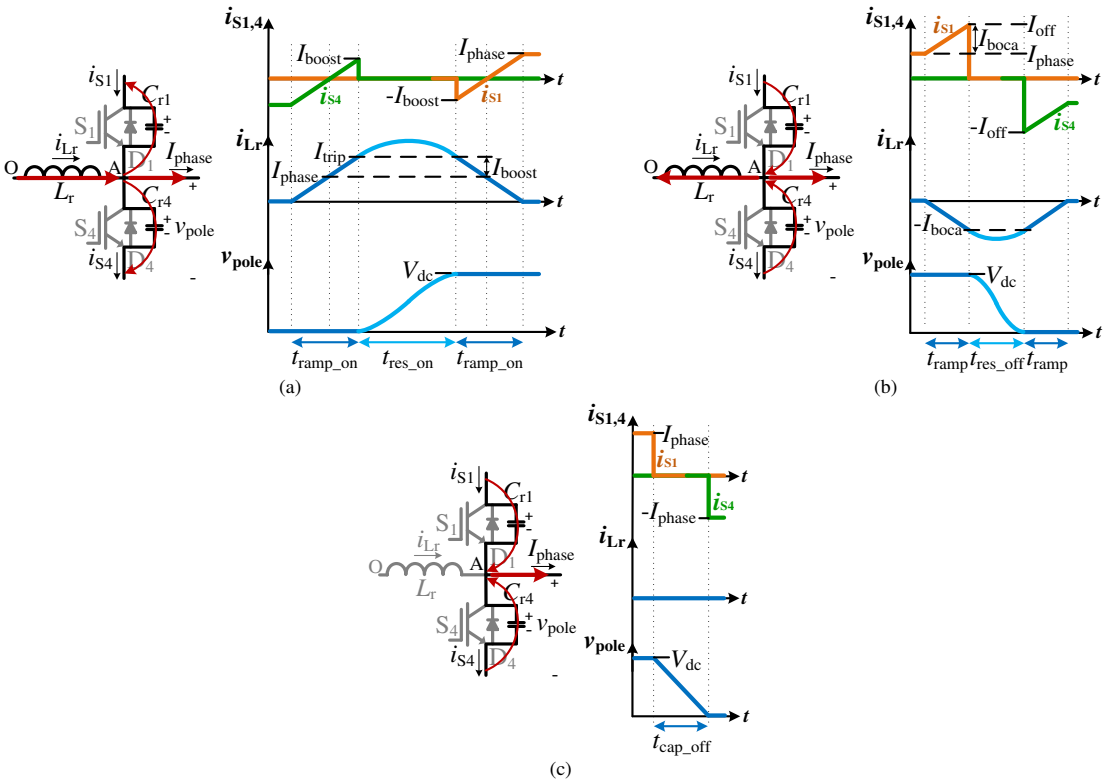

Fig. 2. Inductor current i_{Lr}, output voltage v_{pole}, switching currents i_{S1} and i_{S4}, and corresponding circuits during transitions of S_1: (a) a resonant turn-on, (b) a resonant turn-off, and (c) a capacitive turn-off, when $I_{phase} > 0$.

The main device current stress caused by the resonant turn-off transition can be avoided when a capacitive turn-off takes place, as seen in Fig. 2(c). Simply, I_{phase} alone discharges C_{r4} and charges C_{r1}, and v_{pole} transitions in a linear rather than a resonant manner, like a lossless turn-off snubber [14,32]. The auxiliary circuit is not utilized, which avoids the auxiliary loss and the extra current stress on the main devices. However, a capacitive turn-off is possible only at sufficiently high I_{phase} levels. Otherwise it will last too long, causing problems such as a current spike in the incoming device [33,34], and the drop of pulses if the PWM time constraints are violated.

In summary, the ACPI performs three kinds of transition: resonant switch turn-ons that occur during the entire fundamental cycle T_1, resonant switch turn-offs, and capacitive switch turn-offs. Resonant turn-off transitions can be utilized during the entirety of T_1, or at high I_{phase} levels, they can be replaced with capacitive ones. The way that each kind of transition occurs, influences the v_{pole} high-frequency, as well as the overall power loss and current stress of the ACPI.

III. Frequency Response of Pulse-Trains

The frequency response of pulse-trains commonly found in power converters is reviewed in this section, as it is the foundational theory for designing the ACPI for high-frequency attenuation purposes. Here, the frequency response of the trapezoidal, the S-shaped, and the sinusoidal pulse-train is briefly discussed. It is assumed that a hard-switched converter

has trapezoidal output voltage pulses, and that a soft-switching converter has S-shaped or sinusoidal voltage pulses.

Fig. 3 shows symmetrical trapezoidal and S-shaped pulses of a fixed pulse-width that are successively differentiated, until an impulse train appears [3,35,36]. This graphical representation serves the intuitive interpretation of their high-frequency content: the higher the derivative where the impulse train appears, the lesser the high-frequency harmonic content, and the larger the amplitude of the impulses, the higher that content is [36]. Also featured are the parameters of the pulse-width τ, the rise/fall time t_r, and the first-derivative rise time $t_{r(dv/dt)}$ of the corners of the S-shaped pulse.

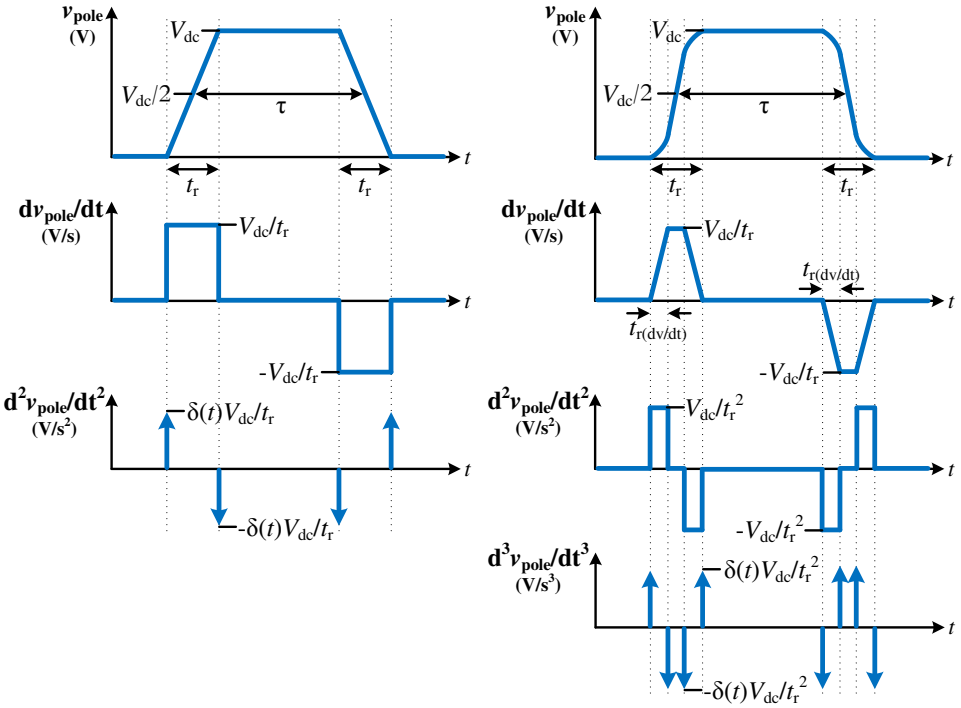

Fig. 3. Successive differentiations of (a) a symmetrical trapezoidal pulse, and of (b) a symmetrical S-shaped pulse.

The derivative order where the impulse train appears, corresponds to the number of corner frequencies on each symmetrical pulse-train's spectral envelope. This way, the trapezoidal spectral envelope has two corner frequencies as in (1) and (2): f_{c1} between the envelope slopes of 0 to -20 dB/dec, and f_{c2} between -20 to -40 dB/dec. The S-shaped envelope has three corner frequencies: while f_{c1} is the same, the $t_{r(dv/dt)}$ parameter defines f_{c2} and a third frequency f_{c3}, as in (3) and (4). The smooth corners of the S-shaped edges and the introduction of f_{c3} marks a slope change from -40 to -60 dB/dec. Hence, the pulse-width τ primarily influences the lower end of the spectrum, and t_r and $t_{r(dv/dt)}$ the higher end [3,35,36].

$$f_{c1} = 1/\pi\tau \tag{1}$$

$$f_{c2\_trap} = 1/\pi t_r \tag{2}$$

$$f_{c2\_S\text{-}shaped} = 1/\pi\left(t_r - t_{r(dv/dt)}\right) \tag{3}$$

$$f_{c3\_S\text{-}shaped} = 1/\pi t_{r(dv/dt)} \tag{4}$$

As described in Section II, if only resonant transitions are realised, the output voltage of the ACPI will consist of pulses with sinusoidal edges. If these pulses are assumed as symmetrical and of a fixed pulse-width, the v_{pole} pulse-train will only have two corner frequencies: the f_{c1} of (1) and an f_{c2} that marks a direct slope change from -20 to -60 dB/dec

[37]. However, the successive time-derivative method cannot be applied to sinusoidal edges, as they can be infinitely differentiated, yet they can be approximated as S-shaped, with a small error of about 4 dB, by defining that $t_r = 2 \cdot t_{r(dv/dt)}$ [36]. The result is an S-shaped pulse-train where $f_{c2} = f_{c3}$. This special S-shaped pulse maintains the sinusoidal property of the direct slope change to -60 dB/dec. Fig. 4 shows a simulation of trapezoidal, S-shaped, and 'sinusoidal' spectra of duty cycle $d = 0.5$, switching frequency $f_s = 20$ kHz, and symmetrical edges. It is clearly seen that the -60 dB/dec slope in the S-shaped and sinusoidal spectra results in less high-frequency harmonic content than the trapezoidal spectrum.

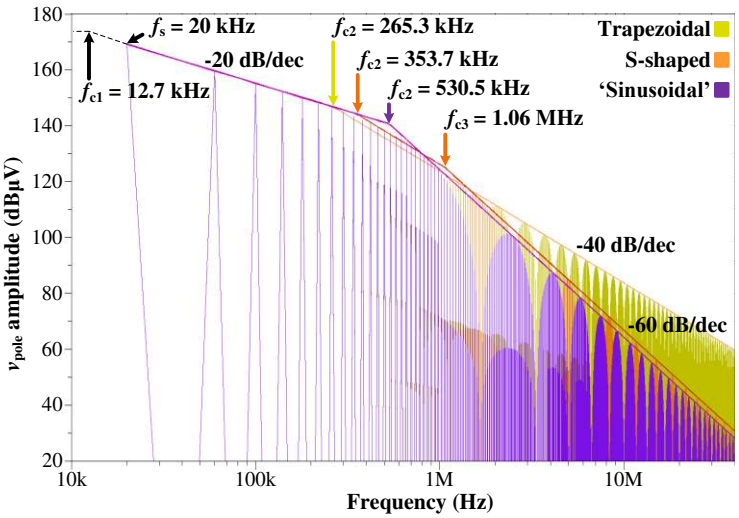

Fig. 4. Trapezoidal, S-shaped, and 'sinusoidal' spectra with $V_{dc} = 450$ V, $f_s = 20$ kHz, $\tau = 25$ μs, $d = 0.5$, $t_r = 1.2$ μs, $t_{r(dv/dt)} = 300$ ns for the S-shaped edges, and $t_{r(dv/dt)} = 600$ ns for the 'sinusoidal' edges.

In Fig. 4, d is fixed, although the v_{pole} pulse-train of the ACPI is modulated with Sinusoidal PWM (SPWM), where d varies during T_1 and is dictated by the amplitude modulation index m_A [38]. While in this case it is difficult to estimate the harmonic content, it will always be less than the pulse-train of a fixed $d = 0.5$, i.e., of $m_A = 0$ [39]. As such, the envelope under $m_A = 0$ is always the worst case for the envelope under $m_A \neq 0$, in the entire frequency range. If the pulses have identical edges between pulse-trains, the corner frequencies described in (2), (3), and (4) will not be affected.

This analysis highlights that the edges of an S-shaped/sinusoidal pulse can be manipulated in a flexible way, through their duration (t_r) and shape ($t_{r(dv/dt)}$), that is, their smooth corners. For the reasons discussed above, the frequency response of the sinusoidal v_{pole} pulses of the ACPI is treated as S-shaped. Based on this analysis, the ACPI resonance can be manipulated in a way that shapes the edges of the output voltage for an improved and more predetermined high-frequency attenuation.

IV. The Equivalent Series LC Circuit

In order to shape the edges of the v_{pole} pulses for an optimum frequency response, the ACPI resonant process has to be studied. Capacitive turn-offs are not considered in this section, since it is desirable that the v_{pole} edges be sinusoidal only.

A. The Free Oscillation of the Equivalent Circuit and the Quasi-resonant Action of the ACPI

Any resonant transition starts with a set of initial conditions that are dictated by its type (turn-on or turn-off), and by

the level and polarity of the phase current I_{phase}. This process is represented as an equivalent series LC circuit, whose solution is the inductor current i_{Lr} and the output voltage v_{pole}. Figs. 5(a) and (b) illustrate the LC circuits and their initial conditions for the turn-on and turn-off transitions, when I_{phase} is positive. These circuits are derived directly from the circuits in Fig. 2. It is seen that resonance is driven by half the DC-link voltage $V_{dc}/2$, while I_{phase} acts as a parallel DC load. The $2C_r$ capacitor between the output node A and the negative rail represents the two snubber capacitors.

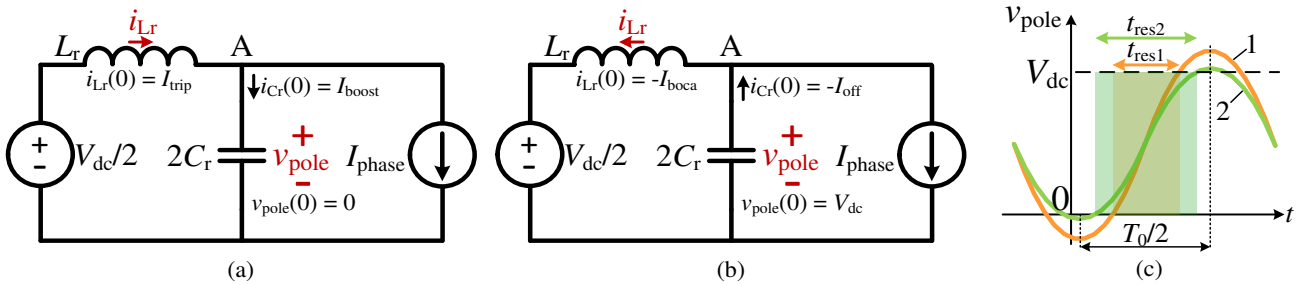

Fig. 5. Equivalent series LC circuit of (a) a switch turn-on transition, (b) a switch turn-off transition when $I_{phase} > 0$, and (c) ACPI quasi-resonant action applied to two v_{pole} sinusoids of the same frequency but of different amplitudes.

The step response of the LC circuits results in i_{Lr} and v_{pole} oscillating sinusoidally with a resonant period T_0, between a peak and a valley. The resonant energy available in the circuit depends on the level of V_{dc}, the properties of I_{phase}, and the initial conditions. If the energy increases by raising the $i_{Lr}(0)$ initial condition for example, the sinusoids will oscillate to more extreme peaks and valleys but with the same angular frequency ω_0. This is presented in Fig. 5(c), where two v_{pole} waveforms oscillate freely in response to the energy present in the circuit. Waveform 1 oscillates to more extreme values than waveform 2, since there is more energy in the circuit, while ω_0 is maintained.

It is important to note however, that the ACPI is a quasi-resonant topology. Resonance only happens when a main switch turns on or off. This contrasts with how other resonant DC-link inverters operate, where the ZVS transitions are realized by a continuously-resonating DC-link voltage. The basic resonant DC-link inverter [15,40] and its derivatives [41] operate in this manner. In the case of the ACPI however, only part of the free oscillation is experienced in the resonant circuit, as v_{pole} swings between the two DC rail values of (ideally) 0 and V_{dc}, during the resonant interval t_{res}. The two DC rail values are not necessarily at the extremes of the free oscillation, however. As seen in Fig. 5(c), the two v_{pole} waveforms oscillate between 0 and V_{dc}, only during the t_{res} intervals. Waveform 1 has a larger amplitude, meaning that its free oscillation reaches more extreme peaks and valleys than waveform 2. Hence, the t_{res} interval of waveform 1 is shorter, and the dv/dt gradient is larger. The reason for this behaviour is that the amount of energy present in the resonant circuit for waveform 1 is larger than for waveform 2. Consequently, the energy in the resonant circuit dictates the duration (t_{res}) and the shape of the v_{pole} edge between the DC rail values, impacting the high-frequency response.

B. Boost and Trip Currents

The main difference between the turn-on and the turn-off transitions is the role of I_{phase}. During the turn-on transition of Fig. 5(a), i_{Lr} flows into A to charge the capacitor, while I_{phase} flows out of it as to discharge it, thus inhibiting resonance.

When the $i_{Lr}(0)$ condition is kept constant, less energy is available to complete resonance, as I_{phase} increases during the fundamental cycle T_1. Conversely, in Fig. 5(b), both i_{Lr} and I_{phase} flow out of A and discharge the capacitor together. If $i_{Lr}(0)$ is kept constant, more energy is put into the circuit as I_{phase} increases. Under these conditions, the v_{pole} edge swings faster between the DC rails and becomes steeper during the turn-off transitions. The opposite trend applies for turn-ons.

At this point, a distinction concerning the initial conditions of the currents. I_{boost} and I_{off}, the currents denoted as the initial conditions $i_{Cr}(0)$ of the capacitor current in Figs. 5(a) and (b), are the values reached by the outgoing switch current right before resonance starts, as seen in Figs 2(a) and (b). I_{boost} and I_{off} are termed here as the boost currents and are controlled by the ramp time intervals t_{ramp}. The $i_{Lr}(0)$ conditions of a given turn-on or turn-off transition are also controlled by t_{ramp}. In Figs. 2(a) and (b), i_{Lr} ramps up to the values of I_{trip} and I_{boca}, which are termed here as the trip currents. Lastly, the relationship between the boost and the trip currents involves I_{phase}, as illustrated in Figs. 5(a) and (b).

The trip currents must be large enough to overcome the power loss incurred by the parasitic resistance of the auxiliary circuit [30,42]. The voltage that drives the ACPI resonance is always $V_{dc}/2$, and it does not provide enough energy to the resonant circuit for overcoming that power loss. Thus, additional inductor current is required to compensate the loss, and to allow v_{pole} to swing fully to the opposite rail and achieve ZVS. Conversely, the coupled-inductor inverters [26-29] raise the driving voltage to more than $V_{dc}/2$, allowing i_{Lr} to reach lower trip values. Customarily, $I_{trip} = I_{phase}$ is set for turn-ons, meaning that $I_{boost} = 0$. This reduces the auxiliary circuit loss. However, the coupled-inductor inverters suffer from high component counts and design complexity. While the boost currents in the ACPI increase the auxiliary circuit loss and the main device current stress, they allow flexibility in controlling resonance and the duration of the resonant intervals t_{res}. This is crucial, since the t_{res} intervals are the actual rise and fall times of v_{pole}. As such, this work investigates the ACPI for high-frequency content attenuation. Also of great interest are the trade-offs between the power efficiency and the output voltage high-frequency attenuation, due to the existence of the boost currents and the way they are controlled.

C. Analytical Expressions of the Equivalent Circuits

The equivalent circuits are described by ordinary differential equations that yield sinusoidal i_{Lr} and v_{pole} expressions, as in (5) and (6) for turn-ons, and (7) and (8) for turn-offs. A positive I_{phase} and no auxiliary circuit loss are assumed. Also during resonance, i_{Lr} is bounded by its trip values I_{trip} and I_{boca}, and v_{pole} swings between 0 and V_{dc}, like in Figs. 2(a) and (b).

$$i_{Lr} = I_{phase} + I_{boost}\cos(\omega_0 t) + \frac{V_{dc}/2}{Z_0}\sin(\omega_0 t) \tag{5}$$

$$v_{pole} = \frac{V_{dc}}{2}[1 - \cos(\omega_0 t)] + Z_0 I_{boost}\sin(\omega_0 t) \tag{6}$$

$$i_{Lr} = I_{phase} - I_{off}\cos(\omega_0 t) - \frac{V_{dc}/2}{Z_0}\sin(\omega_0 t) \tag{7}$$

$$v_{pole} = \frac{V_{dc}}{2}[1 + \cos(\omega_0 t)] - Z_0 I_{off}\sin(\omega_0 t) \tag{8}$$

Z_0 and ω_0 are the resonant impedance and the resonant frequency, respectively, and depend on the values of the resonant components L_r and C_r, as in (9) and (10). Z_0 and ω_0 are valid for both equivalent LC circuits.

$$Z_0 = \sqrt{L_r/2C_r} \tag{9}$$

$$\omega_0 = 1/\sqrt{2L_rC_r} \tag{10}$$

Solving (5) for $i_{Lr} = I_{trip}$ and (7) for $i_{Lr} = |I_{boca}|$, yields the expression for t_{res_on} in (11), and for t_{res_off} in (12).

$$t_{res\_on} = \frac{2}{\omega_0}\tan^{-1}\left[\frac{V_{dc}/2}{Z_0(I_{trip}-I_{phase})}\right] = \frac{2}{\omega_0}\tan^{-1}\left(\frac{V_{dc}/2}{Z_0 I_{boost}}\right) \tag{11}$$

$$t_{res\_off} = \frac{2}{\omega_0}\tan^{-1}\left[\frac{V_{dc}/2}{Z_0(|I_{boca}|+I_{phase})}\right] = \frac{2}{\omega_0}\tan^{-1}\left(\frac{V_{dc}/2}{Z_0 I_{off}}\right) \tag{12}$$

It is notable that the boost currents I_{boost} and I_{off} appear in (5), (6), (7), (8), (11) and (12). Hence, for given circuit conditions V_{dc} and I_{phase}, and for given L_r and C_r values, the boost currents affect the resonant magnitudes and the resonant intervals. By properly controlling the boost currents, v_{pole} can be profiled with slow and smooth edges for reduced high-frequency content, in a predetermined way, and in line with the theory of Section III.

V. Fixed-Timing and Variable-Timing Control

The thorough analysis of the equivalent LC circuit serves for deriving the ACPI control schemes. The two classic ACPI control schemes are fixed-timing and variable-timing control [33]. In [43,44] these terms refer to the inductor current ramp interval t_{ramp}. If these intervals are fixed throughout the fundamental cycle T_1, fixed-timing control is realised. If they vary, variable-timing control is realised. This terminology has also been applied to the conduction period t_{aux_sw} of the auxiliary devices [33]. Regardless of the parameter they refer to, these two schemes differ in ease of implementation, current stress, power loss, and most importantly, in high-frequency harmonic attenuation.

Fixed timing is simple to implement. The t_{ramp} intervals described by (13) and (14) are fixed and are manually set into the control algorithm. This means that for given L_r and V_{dc} values, the trip currents I_{trip} and I_{boca} are fixed throughout T_1.

$$t_{ramp\_on} = \frac{L_r I_{trip}}{V_{dc}/2} = \frac{L_r(I_{boost} + I_{phase})}{V_{dc}/2} \tag{13}$$

$$t_{ramp\_off} = \frac{L_r|I_{boca}|}{V_{dc}/2} = \frac{L_r(I_{off} - I_{phase})}{V_{dc}/2} \tag{14}$$

Moreover, the control algorithm uses the I_{phase} polarity information for selecting the appropriate auxiliary switch that for a given resonant transition: S_{a1} helps with turn-ons and S_{a4} with turn-offs, when I_{phase} is positive. When I_{phase} is negative, the auxiliary switches swap roles. However, this scheme can be greatly simplified if the t_{ramp} intervals are set equal, i.e., $t_{ramp\_on} = t_{ramp\_off}$. As such, $I_{trip} = I_{boca}$ and the control algorithm sees no distinction between a turn-on and a turn-off transition. This simplification results in no current and voltage sensing for the purpose of resonance.

The simple fixed-timing scheme comes at the expense of increased current stress and power loss [33]. Firstly, the i_{Lr} pulse currents are unnecessarily high, as seen in Fig. 6(a). This means that throughout T_1, the current stress in the

auxiliary devices is severe due to the large i_{Lr} peaks. Secondly, the RMS value I_{Lr_rms} of i_{Lr} is large, causing high auxiliary circuit loss. Thirdly, the main device current stress increases, especially during the resonant turn-offs when I_{phase} is near its peak value I_{phase_pk}. According to $I_{off} = I_{boca} + I_{phase}$, I_{off} becomes excessively large when I_{phase_pk} is reached, as I_{boca} is fixed throughout T_1. Hence, the peaks of the main switching currents i_{S1} and i_{S4} in Fig. 2(b), become very large at I_{phase_pk}. Lastly, due to both the I_{boost} and I_{off} contributions in i_{S1} and i_{S4}, the conduction losses of the main devices are increased.

Variable-timing control reduces current stress and power loss by varying the t_{ramp} intervals [33], which builds the trip currents and the overall i_{Lr} pulses according to the I_{phase} level. As seen in Fig. 6(b), the turn-on pulses are initially small, then turn larger as more i_{Lr} contribution is required at higher I_{phase} levels. The reverse trend holds for the turn-off pulses, since, as explained in Section IV, less i_{Lr} contribution is required as I_{phase} increases. Thus, I_{Lr_rms} and the peaks in the main device currents are reduced. However, this optimized scheme is more complex, because the V_{dc} value, and the I_{phase} level and polarity information are required for the online calculation of the t_{ramp} intervals of (13) and (14).

Most importantly, the fixed- and variable-timing schemes have a profound influence on how resonance transpires, which affects the high-frequency signature of v_{pole}. As (13) and (14) indicate, under fixed timing, the boost currents I_{boost} and I_{off} vary throughout T_1, since the trip currents I_{trip} and I_{boca} are fixed. In turn, the resonant intervals t_{res_on} and t_{res_off} vary during T_1, according to (11) and (12). As explained in Section IV, when the trip currents are fixed, the resonant energy increases for turn-offs and decreases for turn-ons, as I_{phase} increases. This erratic provision of energy means that from one switching cycle to the next, each v_{pole} pulse will be dissimilar to its adjacent ones in terms of edge duration and shape. As a result, the frequency response will not be as predictable as the spectra of Fig. 4.

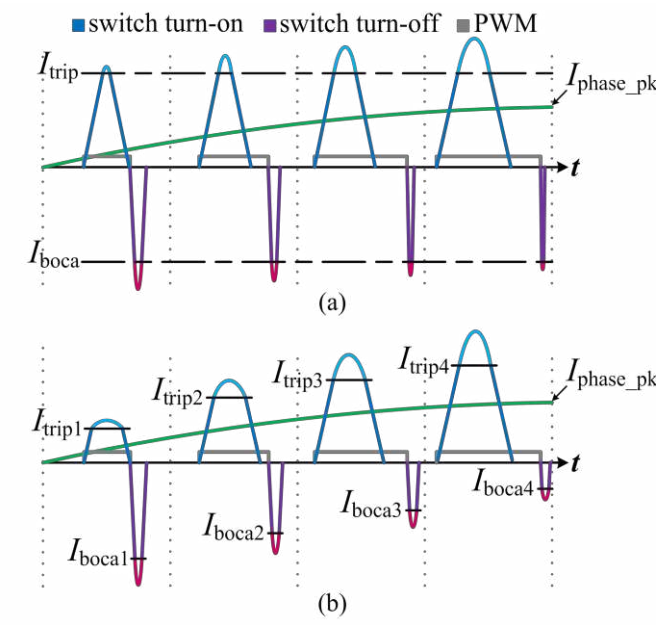

Fig. 6. Comparison of i_{Lr} pulses with (a) fixed-timing, and (b) variable-timing control during a fundamental quarter-cycle.

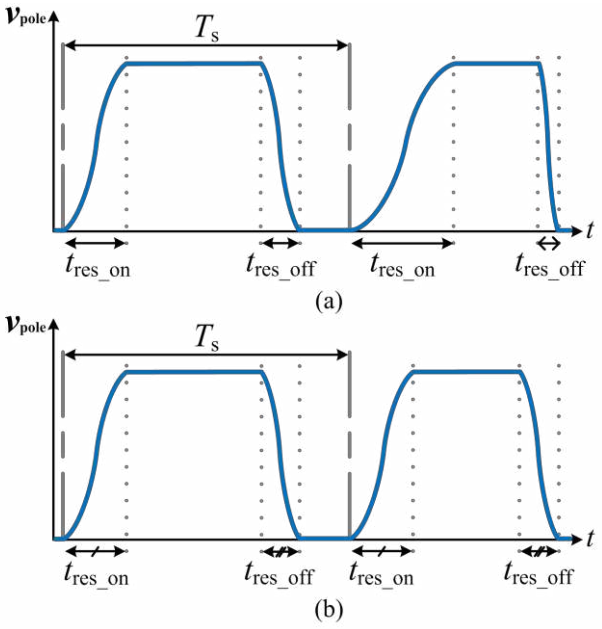

Fig. 7. Part of the v_{pole} pulse-train under (a) fixed-timing, and (b) variable-timing control when $I_{phase} > 0$.

In contrast, under variable-timing control, the fact that the t_{ramp} intervals of (13) and (14) vary, means that they can be controlled in a way that I_{boost} and I_{off} become fixed during T_1. In turn, the resonant intervals will become fixed throughout

T_1, as dictated by (11) and (12). This means that the energy put into resonance is more consistent as I_{phase} varies. The v_{pole} edges will then be shaped in a consistent manner from one switching cycle to the next, and the frequency response can become more predictable. This is preferable for high-frequency harmonic attenuation. The v_{pole} pulses generated by each scheme are shown in Fig. 7. In Fig. 7(a) it is seen that fixed timing produces edges that change from one switching cycle to the next, whereas in Fig. 7(b) the edges are consistent in duration and shape under variable timing.

In addition, the variable-timing control algorithm can be set up in such a way that the boost currents are both fixed and equal during the fundamental cycle, as in $I_{boost} = I_{off}$. Then, as dictated by (11) and (12), the resonant intervals will also be equal, that is, $t_{res\_on} = t_{res\_off}$. The consequence of this condition is the generation of v_{pole} pulses with the same rising and falling edges. In other words, the pulses can become symmetrical and the high-frequency response of the output voltage will be similar to the frequency response of a pulse-train with sinusoidal edges, as simulated in Fig. 4.

Conclusively, proper boost current control is essential to the active control of the ACPI resonant magnitudes [45,46], with the overall loss and current stress depending on the properties of the inductor current i_{Lr}, and the high-frequency attenuation capability depending on the edge properties of the output voltage v_{pole}. The two ACPI control schemes that were introduced in this section influence the way the boost currents inject energy into the resonant circuit during each switching cycle, and therefore have a direct effect on the resonant magnitudes.

VI. Designing the ACPI for High-frequency Content Attenuation

In this section, the design procedure for the experimental 3-phase ACPI prototype is presented. The timing constraints imposed by the soft-switching action are defined, and the boost current condition for symmetrical v_{pole} pulses is introduced, along with its advantages and disadvantages. Lastly, capacitive switch turn-offs are also considered.

A. Timing Constraints

Successful soft switching depends on two factors. Firstly, v_{pole} must swing fully to the opposite rail. This achieves ZVS, and v_{pole} edges that are completely shaped by resonance. If this does not happen, then an abrupt jump of high dv/dt will be experienced across the large snubber capacitors, and current spikes that are harmful to the main devices might appear.

Secondly, i_{Lr} must diminish to zero after a transition has ended and steady state is reached. If the auxiliary switch is turned off before i_{Lr} becomes zero, the slew rate di_{Lr}/dt of the inductor current will sharply increase, causing an overvoltage in the auxiliary branch. The clamping diodes in Fig. 1 will protect the auxiliary devices against this overvoltage, but the control should avoid this scenario, as the voltage spikes and the sharp di_{Lr}/dt can be secondary sources of EMI. To avoid this possibility, the conduction period of the auxiliary devices t_{aux_sw} is the first parameter to be set, and it is common to both the fixed-timing and the variable-timing schemes. The i_{Lr} pulse-width, denoted as t_{aux}, must be fully accommodated by t_{aux_sw} during any transition of T_1. As such, the t_{aux_sw} interval can be forced to vary along with

t_{aux}, but that would involve sensing the actual i_{Lr} pulses, which is a costly and difficult thing to do.

Instead, a fixed t_{aux_sw} is selected, a value that lies in the range of $t_{aux\_max} < t_{aux\_sw} < d_{min} \cdot T_s$. The lower limit t_{aux_max} is the pulse-width of the tallest and widest i_{Lr} pulse that appears during T_1. This specific pulse is built during the turn-on transitions at the phase current peaks $\pm I_{phase\_pk}$, and its width is defined as $t_{aux\_max} = 2t_{ramp} + t_{res\_on\_max}$ under fixed-timing control, and as $t_{aux\_max} = 2t_{ramp\_on\_max} + t_{res}$ under variable-timing control. The upper boundary $d_{min} \cdot T_s$ is the minimum pulse-width of the SPWM signal, with d_{min} the minimum duty cycle and T_s the switching period, and setting it as the upper boundary ensures that the auxiliary switch is gated off before the next transition begins. This boundary T_s shrinks if the switching frequency f_s and/or the modulation index m_A are increased. The modulation-imposed constraints on soft switching are more stringent since the transition times usually last an order of magnitude longer than with hard switching.

B. The Boost Current Condition

As discussed in Sections IV and V, the boost currents dictate the amount of energy provided to the resonant circuit per switching cycle. This in turn affects i_{Lr} and v_{pole}, as well as t_{res_on} and t_{res_off}, according to (5), (6), (7), (8), (11) and (12).

The main focus of the design procedure is the attenuation of the high-frequency content of v_{pole}. Essentially, its frequency response should be optimized compared to an equivalent hard-switched inverter, by exhibiting a corner frequency f_{c2} early in the spectrum and a -60 dB/dec roll-off at high frequencies, as discussed in Section III. Hence, the resonant intervals are demanded to be at least 5 or 10 times longer than the transition times under hard switching.

Theoretically, an optimised v_{pole} frequency response can be achieved more easily if it is demanded that $t_{res\_on} = t_{res\_off}$, as this will ideally generate a train of symmetrical pulses, and a frequency response that is as predictable as possible. This way, only one t_{res} value will have to be selected. This can only happen with variable-timing control, which is why it is the first control scheme to be designed. Symmetry in the v_{pole} pulses can theoretically be achieved by demanding that:

$$I_{boost} = I_{off} = I_{phase\_pk} \tag{15}$$

This boost current condition given in (15) means that during the longest turn-on transition at I_{phase_pk}, the maximum trip current will be $I_{trip\_max} = I_{phase\_pk} + I_{boost} = 2I_{phase\_pk}$. A maximum value for the ramp interval t_{ramp} is then selected that complies with (15), while respecting the $t_{aux\_max} < t_{aux\_sw}$ condition. Hence, (13) becomes:

$$L_r = \frac{V_{dc} \cdot t_{ramp\_on\_max}}{4 \cdot I_{phase\_pk}} \tag{16}$$

With t_{res} selected beforehand, the snubber capacitor C_r can be designed with the combination of (11), (9) and (10).

Now that the variable-timing scheme is designed, a fixed-timing scheme follows by demanding that the resulting $t_{res\_on\_max}$ interval, the longest that will appear, is equal to the t_{res} of the variable-timing scheme, while L_r and C_r are kept the same. Additionally, no current or voltage sensing is required, when the trip currents are set equal, that is, $I_{trip} = I_{boca}$. A SABER simulation of the simplified fixed-timing scheme provides a worst-case scenario for the current stress that will be

experienced in the inverter. The maximum I_{off} value defines the repetitive pulsed collector current of the main devices, and the I_{Lr_rms} value defines the auxiliary device continuous current. Finally, the peak of the tallest i_{Lr} pulse current defines the pulsed collector current rating of the auxiliary devices.

At this point, the significance of the boost current condition of (15) needs to be discussed. This discussion only applies to variable-timing control, since it is the only scheme that can result in fixed boost currents. The boost current condition ideally guarantees symmetry in the v_{pole} pulses and an optimised high-frequency response, but comes at the cost of increased current stress and power loss. Firstly, the i_{Lr} pulses during turn-ons will be too high, since $I_{trip} = I_{boost} + I_{phase}$ will increase from I_{phase_pk} when $I_{phase} = 0$, to $2 \cdot I_{phase\_pk}$ when $I_{phase} = I_{phase\_pk}$. Conventionally, I_{boost} must be just large enough to overcome the impact that the parasitic resistance of the auxiliary circuit has on resonance [43]. In other words, I_{boost} provides extra energy to the resonant circuit, so that v_{pole} can swing fully to the opposite DC rail. If the boost current condition is not applied, then I_{boost} can be reduced to a fixed value that is small enough for achieving ZVS, and at the same time decreasing the current stress and the power loss in the inverter.

The turn-on transition at I_{phase_pk} results in the tallest and widest i_{Lr} pulse during T_1. Its amplitude is described in (17):

$$I_{Lr\_pk\_max} = I_{phase\_pk} + \sqrt{\left(\frac{V_{dc}}{2 \cdot Z_0}\right)^2 + {I_{boost}}^2} \tag{17}$$

The $I_{Lr\_pk\_max}$ peak current is an indicator for the current stress and the power loss experienced in the auxiliary circuit. A larger value of L_r will increase the resonant impedance Z_0 and will reduce $I_{Lr\_pk\_max}$, but it will lead to a larger and bulkier resonant inductor [32]. Furthermore, it is not ensured that I_{Lr_rms} will decrease, since for a larger L_r, the t_{ramp} intervals will increase according to (13) and (14), and the i_{Lr} pulses will widen. Alternatively, I_{boost} can be reduced. An investigation of (17) however shows that $I_{Lr\_pk\_max}$ would not decrease dramatically if I_{boost} became smaller than I_{phase_pk}, not even if I_{boost} were zero. Therefore, undoing the boost current condition of (15) just for reducing the value of I_{boost}, would present slight gains in current stress and power loss reduction.

The greatest disadvantage of the boost current condition is not that I_{boost} becomes too large, but the demand that every turn-off transition must be resonant. This is desirable if every single v_{pole} pulse is to be sinusoidal and symmetrical in a controllable way. However, the I_{off} boost current cannot be smaller than I_{phase_pk}, if every turn-off is to be resonant. For example, the turn-off transition at I_{phase_pk} can only be resonant if I_{off} is at least equal to I_{phase_pk}, meaning that the trip current I_{boca} is 0 (since $I_{off} = I_{phase} + |I_{boca}|$). If, however $I_{off} < I_{phase\_pk}$, then $|I_{boca}| < 0$, which is impossible. This way the turn-off transitions around I_{phase_pk} will not be resonant. Consequently, the only way to examine any drastic trade-offs between power loss/current stress and high-frequency attenuation is to employ capacitive turn-offs that do not require the participation of the auxiliary circuit. As a final note, setting $I_{boost} = I_{off} > I_{phase\_pk}$ will not bring about any benefits to either the power loss/current stress, or the high-frequency attenuation.

An ACPI design that focuses primarily on achieving a predictable and attenuated high-frequency response for its

output voltage will result in increased power loss and current stress, as opposed to a design that focuses on decreasing switching loss. References [42] and [47] discuss how the boost currents can be selected not only for minimised power loss, but also for other important issues such as DC-link utilization, output voltage quality, and mid-point balancing.

C. Capacitive Turn-offs

Fig. 2(c) shows a capacitive switch turn-off, during which v_{pole} transitions in a linear fashion, rather than a sinusoidal one, since only the snubber capacitors are involved. While the turn-on transitions are always resonant, resonant turn-off transitions can be swapped for capacitive ones, but only when I_{phase} is sufficiently high. Therefore, a threshold I_{th} is introduced for I_{phase}. Above I_{th}, the auxiliary circuit is disabled during turn-offs and only the snubber capacitors are used. The control complexity increases this way [42], but current stress and power loss are alleviated, as several i_{Lr} pulses are dropped. However, the generation of linear v_{pole} edges is not controllable by the algorithm, but depends on the I_{phase} level and the value C_r of the snubber capacitors. As I_{phase} increases, the duration of the linear edges t_{cap_off} decreases, as in (18).

$$t_{cap\_off} = \frac{2C_r V_{dc}}{I_{phase}} \tag{18}$$

I_{th} should not be set too low, or else t_{cap_off} will become too long. Here, C_r was designed for the original variable-timing scheme and it cannot be altered. As such, I_{th} is constrained by the modulation scheme. The transition at $I_{phase} = I_{th}$ will occur at a specific point in the fundamental cycle. Therefore, the pulse-width of the SPWM signal at that point in T_1 must be considered. During the transitions around I_{th}, the longest capacitive turn-off transition of duration $t_{cap\_off\_max}$ will be followed by a resonant turn-on transition of duration t_{res}. The pulse-width of the SPWM signal must be large enough to accommodate both transitions. Otherwise, if $t_{cap\_off\_max}$ is too long, the v_{pole} pulse will be deformed or even dropped.

D. Selection of the Design Parameters

In this subsection, the design procedure for the experimental 3-phase ACPI prototype is presented. Firstly, a common SPWM modulation scheme is chosen for both the soft-switching and the hard-switching inverters with a fundamental frequency of $f_1 = 400$ Hz, a switching frequency of $f_s = 20$ kHz, and a modulation index of $m_A = 0.83$. The 3-phase load is in a star connection, with $R_{phase} = 10\ \Omega$ and $L_{phase} = 2$ mH. The above circuit conditions lead to a peak phase current of $I_{phase\_pk} = 18$ A, when the DC-link voltage is $V_{dc} = 500$ V.

Since the v_{pole} frequency response is to be optimised with respect to hard switching, a large enough t_{res} is demanded, during which the v_{pole} edges are shaped. Additionally, a symmetrical v_{pole} pulse-train is desired under the variable-timing scheme. Under these considerations, the resonant intervals are demanded to be $t_{res\_on} = t_{res\_off} = 1.2$ μs. At the same time, the boost current condition of (15) is applied for a symmetrical v_{pole} pulse-train. Thus, $I_{boost} = I_{off} = I_{phase\_pk} = 18$ A is set.

The SPWM scheme imposes a constraint of a minimum pulse-width of $d_{min} \cdot T_s = 4.2$ μs. The resultant pulse-width of the widest and tallest i_{Lr} current pulse is demanded to be quite smaller at $t_{aux\_max} = 2$ μs. With $t_{res} = 1.2$ μs, the maximum

ramp interval that will appear under the variable-timing scheme is $t_{ramp\_on\_max} = 400$ ns, since $t_{aux\_max} = 2 \cdot t_{ramp\_on\_max} + t_{res}$. The t_{aux_max} pulse-width can now be accommodated by a fixed auxiliary switch conduction period of $t_{aux\_sw} = 2.2$ μs.

Next, the values of the resonant components are estimated. Since $t_{ramp\_on\_max} = 400$ ns and the boost current condition is set as shown above, (16) results in $L_r = 2.7$ μH. Then, since $t_{res} = 1.2$ μs and $I_{boost} = 18$ A, (11) leads to $C_r = 47$ nF.

Fixed-timing control is then designed, while maintaining the values of L_r and C_r, and demanding that the maximum resonant interval that will appear during T_1 is $t_{res\_on\_max} = 1.2$ μs. Moreover, the fixed-timing scheme is simplified by setting the trip currents to a fixed value of $I_{trip} = I_{boca} = 36$ A, which can be achieved with a fixed $t_{ramp} = 400$ ns. Simulating this scheme in SABER predicts that the RMS value of i_{Lr} is $I_{Lr\_rms} = 15$ A, and that during the turn-on transition at I_{phase_pk}, the largest i_{Lr} peak is $I_{Lr\_pk\_max} = 68$ A. Furthermore, during the turn-off transition at I_{phase_pk} the largest boost current for turn-offs is $I_{off\_max} = 54$ A. These parameters are useful for selecting the device current ratings.

Finally, a phase current threshold of $I_{th} = 12$ A is introduced to the variable-timing scheme, above which the auxiliary circuit is disabled and the turn-off transitions are realised only by I_{phase} and the snubber capacitors. With $I_{th} = 12$ A, the longest capacitive turn-off that will appear during T_1 is $t_{cap\_off\_max} = 3.9$ μs according to (18).

In summary, a fixed t_{res} value is selected for generating a symmetrical output voltage pulse-train under variable-timing control, and the boost current condition is set. Then, a fixed auxiliary switch conduction period t_{aux_sw} is set, under both control schemes. Next, the resonant components L_r and C_r are calculated. A fixed-timing scheme is then designed for sizing the main and auxiliary devices. Lastly, capacitive turn-offs are introduced for examining any trade-offs that may arise between the decreased power loss/current stress, and the high-frequency content attenuation.

VII. Experimental Results

A 3-phase 5-kW ACPI prototype has been built for validating the proposed method of high-frequency harmonic attenuation. Fig. 8 shows a single-phase ACPI module. Two 1200V/40A IKW40N120T2 IGBT copacks from Infineon constitute the main devices (S_1 and S_4), and two 600V/35A NGTB35N60FL2WG IGBT copacks from ON Semiconductor the auxiliary ones (S_{a1} and S_{a4}). The resonant components can be easily disconnected for hard-switching tests. Three such modules form the 3-phase ACPI by being connected to a common DC link.

A Xilinx XC3S400 FPGA executes the PWM algorithm. Under hard switching it is input with a $t_{dead} = 1.2$ μs dead-time, and with a $t_{aux\_sw} = 2.2$ μs under soft switching. Variable timing relies on the online calculation of (13) and (14) by a TI F28335 DSP, which is based on the boost current condition of $I_{boost} = I_{off} = 18$ A (a manual input), and the V_{dc} and I_{phase} levels. These are sensed by AD7667 analog-to-digital converters. The I_{phase} polarity selects the appropriate auxiliary switch. In addition, capacitive turn-offs are realised by introducing a threshold of $I_{th} = 12$ A to the variable-timing scheme. Fixed timing requires only the input of $t_{ramp} = 400$ ns that leads to the condition of $I_{trip} = I_{boca} = 36$ A.

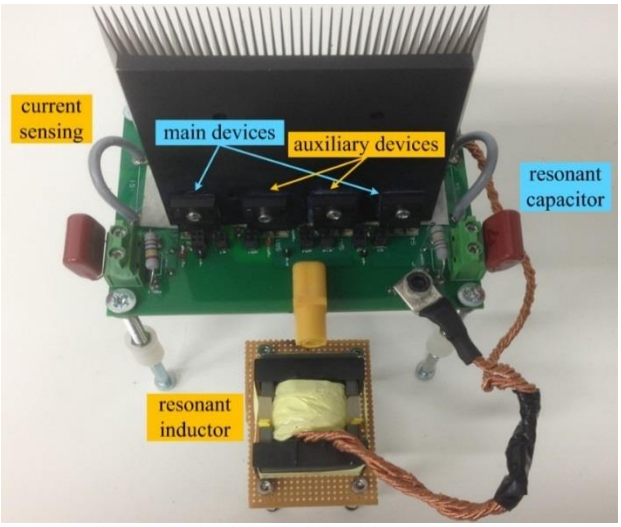

Fig. 8. A single-phase module of the ACPI prototype.

A modified gate driver based on a Schmitt trigger can sense the zero-crossing of the voltage across the main devices [48], for turning on the incoming switch at the end of t_{res}, making for load-adaptive control. This however will add more complexity. Instead, a fixed 1.2-μs delay is introduced to the PWM algorithm that starts as soon as the outgoing switch is gated off. After the delay, the incoming switch is gated on. Experimental trial and error is required for tuning this delay.

3-phase experiments are presented with a DC-link voltage of V_{dc} = 450 V, under hard switching, fixed timing, variable timing, and variable timing with capacitive turn-offs. Only phase A results are presented, due to the 3-phase symmetry.

A. Fundamental Cycle and ZVS

Fig. 9 shows the phase A current i_A, the output voltage v_{pole}, and the inductor current of phase A i_{LrA}, for two fundamental cycles under fixed timing in Fig. 9(a), variable timing in Fig. 9(b) and variable timing with capacitive turn-offs in Fig. 9(c). In Fig. 9(a), i_{LrA} does not vary much with i_A, as the current pulses are unnecessarily high, whereas in Fig. 9(b) the variation of i_{LrA} with i_A is stronger, as the pulse amplitudes get smaller in certain intervals. This way, the RMS value is I_{LrA_rms} = 11.2 A under fixed timing, and I_{LrA_rms} = 9.5 A under variable timing. In Fig. 9(c), the i_{LrA} turn-off pulses (negative pulses for $i_A > 0$, positive pulses for $i_A < 0$) above the I_{th} level are dropped. This way, I_{LrA_rms} is even smaller at 8.9 A. Overall, variable-timing control can decrease current stress and the auxiliary circuit loss, since the i_{LrA} pulses are built according to the phase current level. Capacitive turn-offs further reduce current stress and power loss.

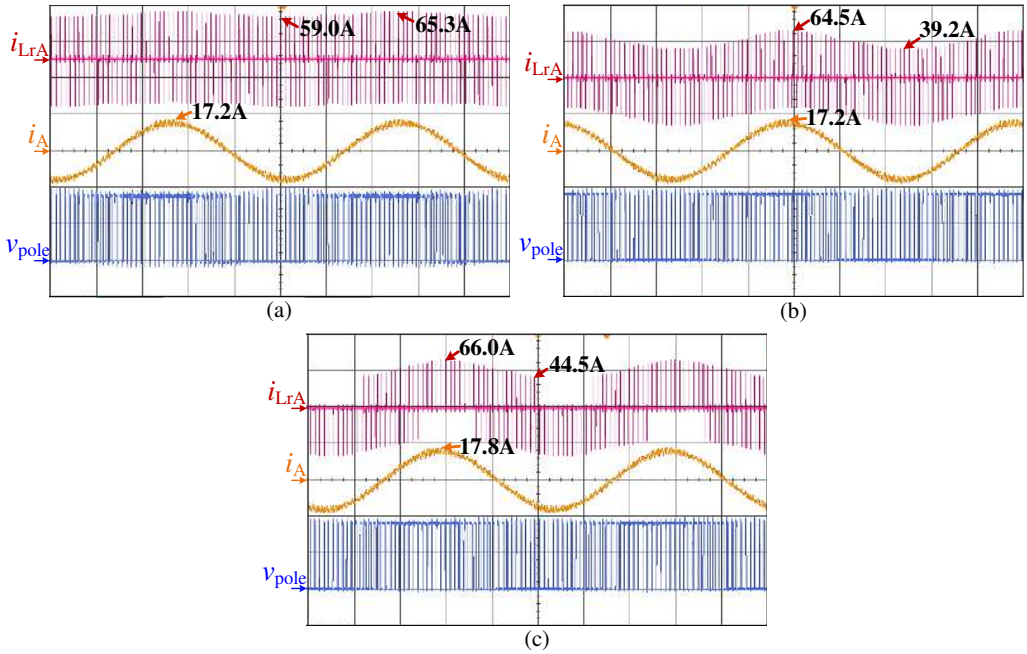

Fig. 9. Phase A current i_A, output voltage v_{pole}, and phase A inductor current i_{LrA} under (a) fixed timing, (b) variable timing, and (c) variable timing with capacitive turn-offs over two fundamental cycles. i_A 20A/div, v_{pole} 250V/div, i_{LrA} 50A/div, time 0.5ms/div.

Fig. 10 shows the ZVS transitions of the main switch S_1 at peak phase current I_{A_pk}. Current i_{S1} and voltage v_{S1} are shown during the turn-on and turn-off transitions under hard switching in Figs. 10(a) and (b), and under variable timing in Figs. 10(c) and (d). The capacitive turn-off transition is shown in Fig. 10(e). During the transition of Fig. 10(a), the reverse recovery current of the main diode D_4 causes i_{S1} to peak to double the i_A level. Also, the tail of i_{S1} in Fig. 10(b) worsens the hard-switching turn-off loss. In contrast, soft switching decouples the edges and minimize switching loss, as shown in Figs. 10(c), (d) and (e). Variable timing fully decouples the edges in Fig. 10(c). There is a large overshoot in i_{S1} though, due to the ringing caused by the parasitic inductance of the switching loop. In Fig. 10(d), i_{S1} peaks to 29.4 A due to the I_{off} component. Also, the edges in Fig. 10(d) are not decoupled fully due to the tail current bump of 6.6 A that i_{S1} exhibits. This peculiar bump occurs in IGBTs only when they turn off under ZVS [49]. Generally, more turn-off loss is incurred in the ACPI than turn-on loss [33], unless capacitive turn-offs are used, as in Fig. 10(e), in which case the ACPI operates as an almost lossless turn-off snubber. Overall, soft-switching decouples the transitioning edges and achieves ZVS, especially under resonant turn-ons and capacitive turn-offs, whereas hard switching does not, with the penalty of increased switching loss.

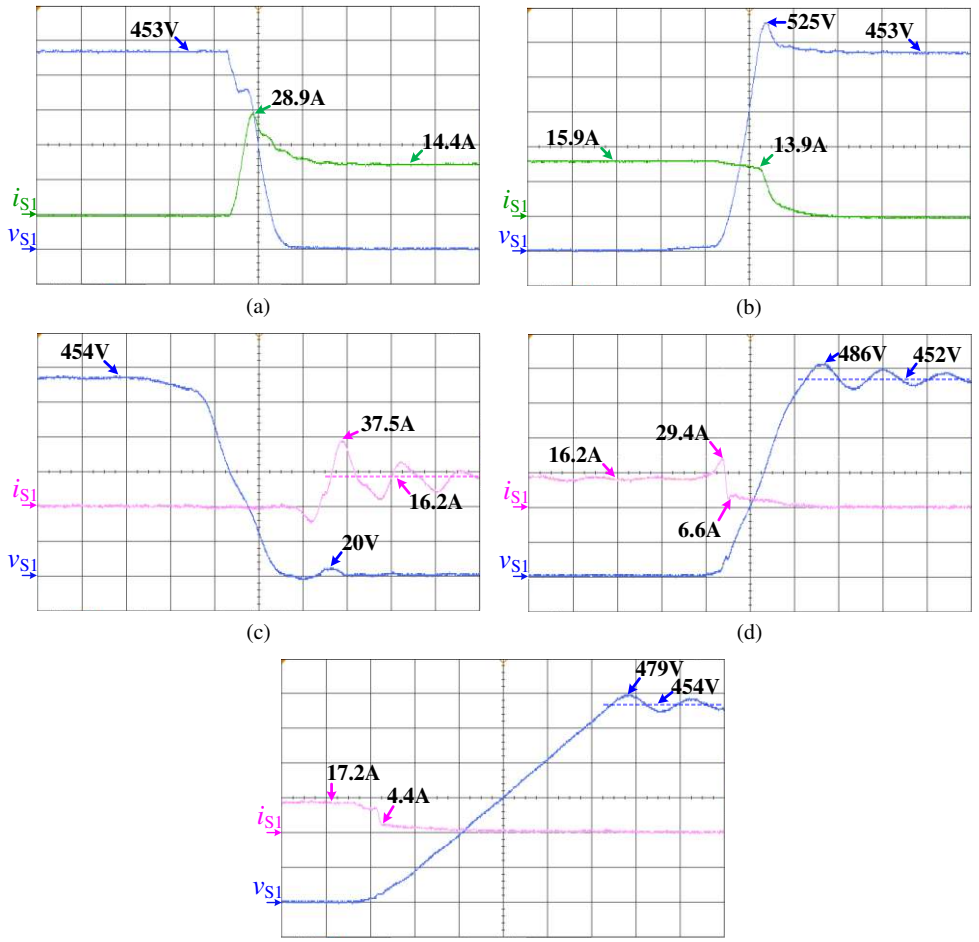

Fig. 10. Switching current i_{S1} and voltage v_{S1} during the transitions of S_1 at peak phase current I_{A_pk}. (a) Hard-switched turn-on and (b) turn-off, (c) variable-timing turn-on and (d) turn-off, and (e) variable timing with capacitive turn-off. Hard switching: v_{S1} 80V/div, i_{S1} 10A/div, time 200ns/div. Soft switching: v_{S1} 80V/div, i_{S1} 20A/div, time 500ns/div.

B. Resonant Transitions and Output Voltage Edge Generation

Of major importance in this work is how the four switching modes generate the output voltage edges. This comparison is shown in Fig. 11, where S_1 is shown to first turn off and then to turn on, at I_{A_pk}. The hard-switched edges in Fig. 11(a) transition quickly and linearly in a matter of 200 ns. In contrast, the soft-switched edges in Figs. 11(b), (c) and (d) are slower and smoother, with their duration spanning a range of 800 ns to 3 µs. However, the resonant soft-switched edges are not shaped in an ideal sinusoidal manner, nor are their corners completely smooth. In Fig. 11(b), fixed timing generates edges that are unequal in duration by 400 ns. As discussed in Sections IV and V, since the trip currents are fixed under fixed-timing control, the resonant energy is provided in an erratic way, and not according to the phase current level. As a result, the two i_{LrA} pulses are close in amplitude, even if the turn-off pulse need not be that large at I_{A_pk}. In contrast, variable timing in Fig. 11(c), generates edges of almost equal duration, as it provides the resonant energy according to the i_A level. Thus, the turn-off pulse drops by 20 A. When capacitive turn-offs are introduced in Fig. 11(d), the turn-off edge becomes linear and almost 2.5 times longer than the turn-on edge, since the snubber capacitors are quite large at 47 nF.

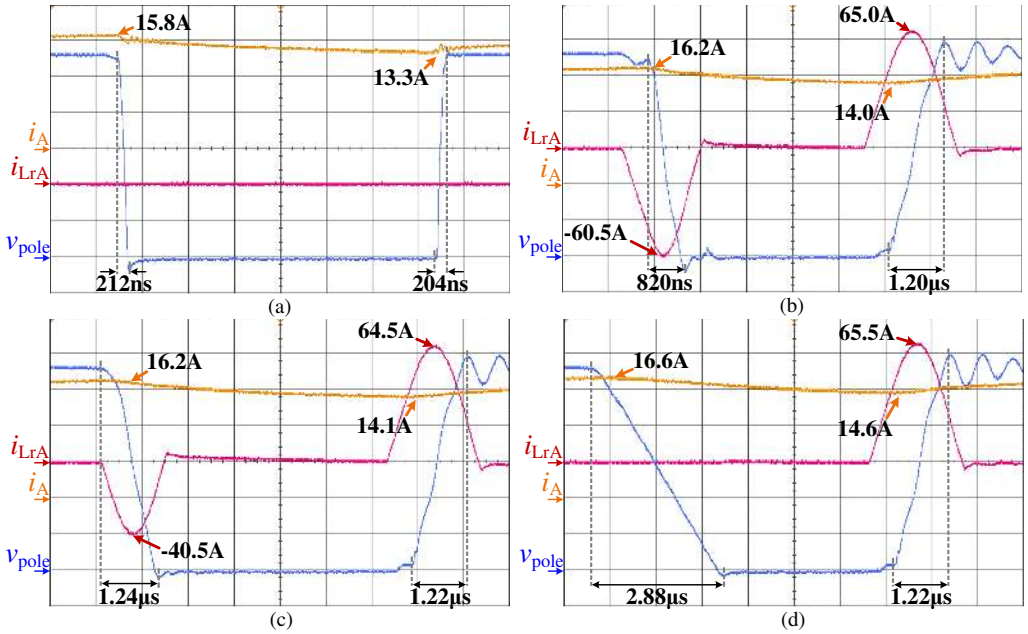

Fig. 11. Phase current i_A, output voltage v_{pole}, and inductor current i_{LrA} during the transitions of S_1 at I_{A_pk} under (a) hard switching, (b) fixed timing, (c) variable timing, and (d) variable timing with capacitive turn-offs. i_A 5A/div, v_{pole} 80V/div, i_{LrA} 20A/div, time 1µs/div.

All the linear v_{pole} edges differ in duration as they depend on the i_A level. They are not dictated by the control algorithm, as is the intention with the resonant edges. In addition, it is seen that these v_{pole} pulses that appear whenever the I_{th} threshold is exceeded, have a resonant and a linear edge. This introduces asymmetry in their duration and shape. The uncontrollability and asymmetry caused by the capacitive turn-offs can lead to an unpredictable high-frequency response, with the linearly-shaped edges potentially contributing to a higher harmonic content.

The resonant edges are not completely sinusoidal either. Fig. 12 examines the turn-on transition of S_1 at I_{A_pk} and under variable timing, where secondary effects take place before, during, and after resonance. As i_{S4} through the outgoing D_4 ramps up along with i_{LrA} during t_1, a di/dt-induced voltage drop across the negative rail parasitic inductance appears as a 16-V undershoot on v_{pole}. As i_{LrA} keeps ramping up, i_{S4} starts flowing through S_4 until it reaches 30.6 A. Then in a matter of 80 ns (interval t_2), i_{S4} abruptly drops to near zero, since the turn-off delay has transpired and the IGBT starts turning off [14]. At the same time, the i_{Cr4} capacitor current jumps to 28.5 A, as it takes up the I_{boost} current from S_4 to commence resonance. This swift change in i_{Cr4} forces v_{pole} to jump to 42 V, with a high dv/dt, at the end of t_2.

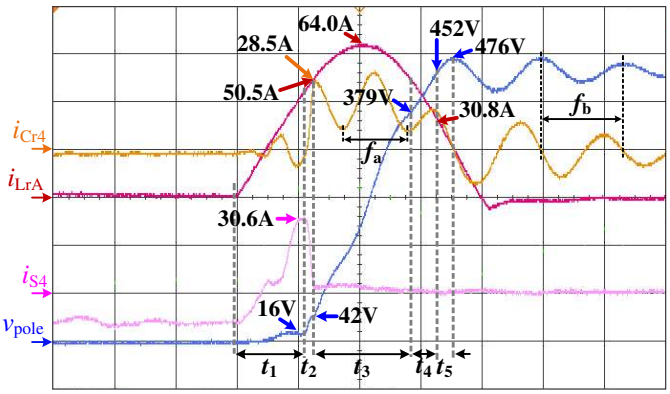

Fig. 12. Capacitor current i_{Cr4}, output voltage v_{pole}, inductor current i_{LrA}, and switching current i_{S4} during the turn-on transition of S_1 at I_{A_pk} under variable timing. i_{Cr4} 20A/div, v_{pole} 80V/div, i_{LrA} 20A/div, i_{S4} 20A/div, time 500ns/div.

The true I_{trip} value of i_{LrA} is 50.5 A for this turn-on transition. Ideally at I_{A_pk}, it should be near 36 A. The major reason for this discrepancy is the turn-off delay of S_4 that forces i_{LrA} to keep ramping up beyond the prescribed I_{trip}. Another reason is that the DSP estimates the t_{ramp_on} interval by using the i_A value of the previous switching cycle, due to the delay introduced by the AD7667 converters. This way, S_4 is gated off with a delay estimated for one i_A value, while resonance is happening under another i_A value. Thus, the I_{boost} value is altered, and the v_{pole} edges stray from their ideal duration and shape. This makes for a more unpredictable frequency response and for a harder estimation of the spectral envelope.

During the resonance of t_3, the parasitic inductance of the negative rail and the output node is in the path of i_{Cr4} and influences its oscillation. As such, i_{Cr4} does not look similar to i_{Lr} but oscillates with a frequency of f_a = 1.9 MHz. This causes undulations on the v_{pole} edge and alters its sinusoidal shape. After t_5, i_{Cr4} oscillates at f_b = 1.4 MHz, signifying that there is no L_r contribution anymore. This problem is specific to this prototype and is exacerbated by the presence of the snubber capacitors. Hard switching does not exhibit these oscillations. A better-engineered PCB could mitigate this issue.

The 770 ns of t_3 are the symmetrical portion of resonance, since i_{LrA} is bounded by I_{trip} = 50.5 A. However, v_{pole} does not reach the DC rail until 250 ns later, at the end of t_4, when i_{LrA} = 30.8 A. This is 20 A below I_{trip}. Therefore, full resonance lasts for $t_{res} = t_3 + t_4$ = 1020 ns and it is asymmetrical. This is due to the resonant circuit's parasitic resistance [31]. If a small R is considered in series with L_r in the LC circuits of Figs. 5(a) and (b), the resonant magnitudes will assume an underdamped waveform of the form $e^{-x}\sin(x)$. This R seems to be increased, and the reason can be traced in the inductor winding. The i_{LrA} waveform is expected to be rich in high-frequency harmonics, exacerbating the skin and proximity effects in the winding and increasing its AC resistance. Regardless, i_{LrA} keeps resonating with v_{pole} until the DC rail is reached at the end of t_4, and ZVS is achieved, with no jump in the dv/dt and no current spike in the incoming switch. Finally, it seems that the parasitic resistance counters the negative effect of the turn-off delay. The turn-off delay pushes resonance to transpire faster by increasing the value of I_{trip}, but the parasitic resistance slows it down.

130 ns later at the end of t_5, v_{pole} overshoots slightly to 476 V and starts oscillating at f_b = 1.4 MHz, along with i_{S4}. This overshoot and the subsequent oscillation are not considered part of the v_{pole} edge, as originally assumed in Figs. 11(b), (c), and (d). Rather, these phenomena are translated as increased harmonic content around the frequency of the ringing [3]. The 16-V undershoot during t_1 and the sudden jump during t_2 will similarly have their own contributions to the v_{pole} spectrum. As such, the v_{pole} edge actually lasts for $t_2 + t_3 + t_4$ = 1100 ns, with resonance shaping it for 1020 ns.

C. Effect of the Main Switch Gate Resistor on Resonance

Since the turn-off delay of the outgoing switch has such a strong influence on resonance, the effect of the main switch gate resistor R_{g_main} for devices S_1 and S_4 is investigated. Fig. 13 shows the variable-timing turn-on transition of S_1 at I_{A_pk}, for two R_{g_main} values. Similar results are observed for the turn-off transition, as well.

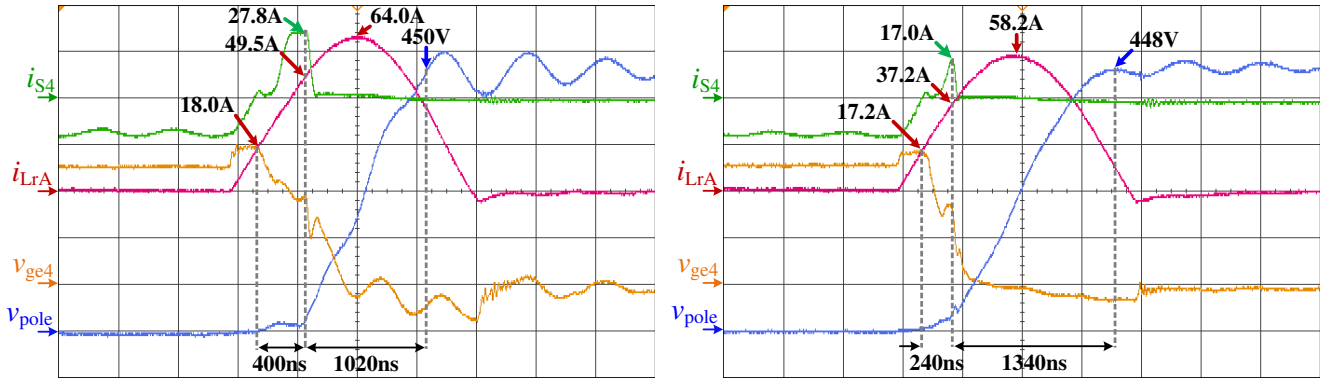

Fig. 13. Gate-emitter voltage of main device S_4 v_{ge4}, switching current i_{S4}, output voltage v_{pole}, and inductor current i_{LrA} for (a) R_{g_main} = 22 Ω, and (b) R_{g_main} = 11 Ω, during the turn-on transition of S_1 at I_{A_pk}, under variable timing. v_{ge4} 5V/div, i_{S4} 20A/div, v_{pole} 80V/div, i_{LrA} 20A/div, time 500ns/div.

In Fig. 13(a), R_{g_main} is 22 Ω. This value is chosen for minimizing any ringing exhibited under hard switching. The turn-off delay between the fall of the S_4 gate-emitter voltage v_{ge4} and the fall of i_{S4} is 400 ns. After the 400 ns, the values of 27.8 A and 49.5 A are assumed by i_{S4} and i_{LrA}, respectively, whereas they should ideally be 18 A and 36 A. In Fig. 13(b), R_{g_main} is halved to 11 Ω, and overall the transition progresses in a slower, smoother manner with dampened ringing. This is counter-intuitive. A lower R_{g_main} worsens ringing and accelerates the transitions, under hard switching.

The ACPI transitions however, are resonant. By reducing R_{g_main}, the turn-off delay is now 240 ns, i_{LrA} ramps up to a lower I_{trip} = 37.2 A, and i_{S4} peaks at 17 A. The energy put into resonance decreases, forcing the resonant magnitudes to swing to lower amplitudes, with i_{LrA} peaking at 58.2 A instead of 64 A. Also, the switching loop parasitic inductance is not energized as much, and the ringing in v_{pole} is suppressed. This way its edge is almost sinusoidal during resonance, and swings seamlessly from the negative to the positive rail with no undershoots or overshoots, in 1580 ns. Lastly, a smaller R_{g_main} reduces the overall current stress and power loss. With R_{g_main} = 11 Ω, I_{LrA_rms} decreases from 9.5 A to 8.4 A. Overall, a reduced main gate resistor puts less energy into the resonant circuit, resulting in a slower, nearly-sinusoidal edge, with smoother corners, and dampened ringing. All these are beneficial for an attenuated high-frequency response.

Fig. 13 suggests that the variable-timing scheme is not implemented perfectly. In both cases, i_{LrA} is near 18 A when v_{ge4} starts falling. This is half the intended I_{trip} value, which might not be enough for v_{pole} to completely swing to the opposite rail. This can be attributed to the delays associated with sensing the phase current and the DC-link voltage, translating that information into the appropriate t_{ramp} interval, and then applying the signals to the switches through the gate circuitry that also introduces its own delay. It seems that any outgoing switch turn-off delay is beneficial because it allows i_{LrA} to keep ramping up and inject more energy into resonance, despite the oscillations, and the fast, misshapen edges.

Lastly in Fig. 13(b), it is noted that even if I_{trip} is near the prescribed 36 A, the v_{pole} edge is longer than anticipated. Examining the 1340-ns interval of the edge, it is shaped by the symmetrical part of resonance for approximately 1 µs, which is closer to what the variable-timing design intended to do in the first place, i.e., to generate a resonant interval of t_{res} = 1.2 µs. The rest of the edge is shaped by the asymmetrical part of resonance. With less energy injected into the

resonant circuit, the damping due to the parasitic resistance is more pronounced. This further slows down the edge and makes resonance more asymmetrical than in Fig. 13(a). However, ZVS is still successful despite the increased damping.

D. Efficiency

The comparison of the four switching modes has yielded substantial differences in v_{pole} edge generation and ZVS. Also of interest is the efficiency exhibited by each mode. The input and output power of the inverter has been measured by Norma 4000 power analyzers connected at the DC input and the 3-phase output. The efficiency of each switching mode has been calculated based on these measurements, at intervals of 500 W. In addition to the default value of 22 Ω, the revised value of R_{g_main} = 11 Ω is also used, and the impact of the capacitive turn-offs is also considered.

Fig. 14 shows the efficiency η against the DC input power P_{in}. The first observation is that soft switching is less efficient than hard switching. From 3.5 kW onwards, only variable timing with capacitive turn-offs and R_{g_main} = 11 Ω is as efficient as hard switching. They both exhibit η = 97.6%, at 4.5 kW.

Soft switching can mitigate the switching loss of the main devices due to the decoupling of the switching magnitudes, but it incurs extra loss, mainly because of the auxiliary circuit. A hard-switching inverter does not exhibit this kind of loss. The auxiliary devices have increased conduction loss due to the I_{LrA_rms} value that is excessive under some schemes, especially fixed timing. The i_{Lr} pulses occur this way because the main purpose of this work is high-frequency content attenuation that can be predetermined within the confines of implementation, and not power loss reduction. Also, the resonant inductor is expected to exhibit increased AC resistance and winding loss. Moreover, the fringing effect around the large airgap of the inductor will cause eddy currents in the winding and contribute to its loss. Thus, an enhanced inductor design for coping with the uniqueness of the i_{Lr} waveform, and for reducing the loss should be considered [50].

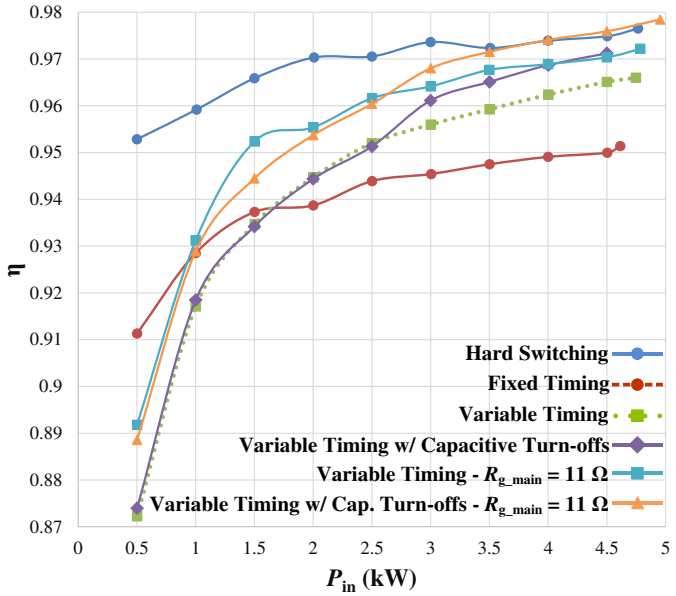

Fig. 14. Power efficiency η of the 3-phase ACPI against DC input power P_{in}, under all switching modes.

The main switches also exhibit increased conduction loss, especially resonant turn-offs, due to the I_{off} component imposed on the main switching currents. Since the soft-switching schemes have been designed for high-frequency

attenuation, I_{off} is comparable or even larger than the reverse recovery current observed under hard switching, as seen in Figs. 10(a) and (d). This is especially true for the simplified fixed-timing scheme with $I_{trip} = I_{boca}$, where I_{boca} is too high. For example, when the turn-off transition at I_{A_pk} happens, I_{off} = 54 A, which is three times the I_{A_pk} level.

The fact remains that the switching loss of the main devices is still worse under hard-switching, as attested by Figs. 10(a) and (b). It is important to note though that the decoupling during the resonant turn-offs, like the one shown in Fig. 10(d), is not entirely realised due to the tail-current bump exhibited by IGBTs, when they are switched under ZVS [49].

Variable timing generates smaller i_{LrA} pulses with decreased I_{LrA_rms} values and I_{off} components. This way, it is more efficient than fixed timing. Also, reducing R_{g_main} leads to less energy being put into any given resonant transition. This is a very simple way of reducing current stress and power loss. The most optimized scheme is variable timing that employs capacitive turn-offs, especially for reduced R_{g_main}. Not only are several i_{LrA} pulses dropped, but the decoupling during the capacitive turn-offs is enhanced with regards to a resonant turn-off, as seen in Fig. 10(e).

An ACPI design for purely reducing switching loss without introducing much loss anywhere else should exhibit higher efficiency than hard switching, especially at higher switching frequencies. A resonant inductor that is tailored to the demanding i_{Lr} waveform [50] can contribute to this. Capacitive turn-offs should also be employed with a I_{th} that is reasonably low, so that plenty i_{Lr} pulses are dropped. The remaining pulses should only be as large as necessary for achieving ZVS, without causing too much loss and current stress. Lastly, a reasonably small R_{g_main} should be employed.

E. Output Voltage Frequency Response

Fig. 15 shows the frequency response of v_{pole}, under hard switching, fixed timing and variable timing for a main gate resistor of R_{g_main} = 22 Ω, and the variable timing spectrum for R_{g_main} = 11 Ω. 20 fundamental cycles of the time-domain waveforms are captured at V_{dc} = 450 V with a Rohde & Schwarz RTO1024 oscilloscope. A resolution of 5 ns and a sample rate of 200 MSa/s give a record length of 10 MSa for each waveform. The noise floor at high frequencies is decreased by averaging the waveforms 5000 times. Then, Matlab performs an optimized Fast Fourier Transform on the time-domain data for obtaining the frequency-domain results.

The most important observation is that from near 600 kHz onwards, all soft-switching schemes exhibit less harmonic content than hard switching because of the longer and smoother v_{pole} edges. The PWM region below 600 kHz has an envelope slope of nearly -20 dB/dec that is common to all switching modes. However, the -40 dB/dec slope appears earlier under soft switching than hard switching. Moreover, a -60 dB/dec slope appears under soft switching, which further contributes to the high-frequency content attenuation. The existence of both the -40 and -60 dB/dec slopes means that the v_{pole} edges behave more like S-shaped ones, rather than sinusoidal ones that only exhibit the -60 dB/dec slope. This is a consequence of the ACPI's quasi-resonant action, which takes part of the free oscillation of the resonant circuit and applies it to the resonant magnitudes, as observed in Fig. 5(c). Hence, most of the middle stretch of the edges has an

almost fixed dv/dt rate that makes them S-shaped. Conversely, as expected, the hard-switched v_{pole} pulse-train behaves like a trapezoidal one, with only the -40 dB/dec slope observable up to 40 MHz, before the noise floor is reached.

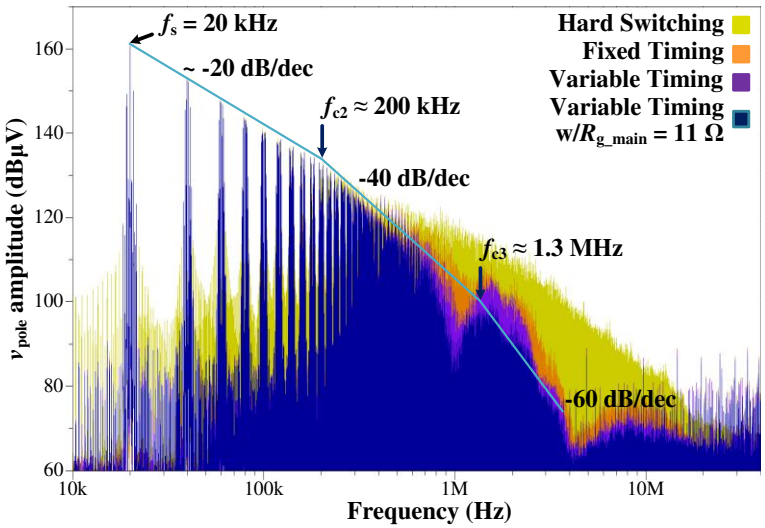

Fig. 15. Experimental output voltage frequency response under hard switching, fixed timing, variable timing, and variable timing for R_{g_main} = 11 Ω.

The frequency-domain results of the v_{pole} pulse-train with linear edges due to capacitive turn-offs are not shown here, because they are almost identical to the ones of their respective variable-timing scheme without the capacitive turn-offs. This means that the number of the linear edges is not large enough to convincingly influence the spectrum. Additionally, the linear edges are so long that they do not exacerbate the high-frequency content because of their shape. It is seen that in this work, capacitive turn-offs are useful for reducing current stress and power loss in the inverter without altering the high-frequency attenuation capability of the variable-timing scheme, albeit at the cost of increased control complexity.

Of all the schemes presented in Fig. 15, variable timing with a reduced R_{g_main} gate resistor of 11 Ω has the best performance, since it generates the longest and smoothest edges in the time domain, as seen in Fig. 13(b). With this simple alteration, gains in both the power efficiency and the high-frequency harmonic attenuation are achieved as attested by Figs. 14 and 15, respectively. This soft-switching scheme also has the most predictable frequency response, because the edges are shaped with no overshoots and undershoots, and because the ringing both during the transition and at steady state is suppressed. This is not the case with the default R_{g_main} = 22 Ω. The favourable edge shape when R_{g_main} = 11 Ω allows for the approximation of the spectral envelope and its corner frequencies, as shown in Fig. 15. It is assumed that every single edge of this pulse-train is the same as the one shown in Fig. 13(b), with a rise time of t_r = 1580 ns and a first-derivative rise time of $t_{r(dv/dt)}$ = 240 ns. With these parameters, the second corner frequency f_{c2} should be 237.5 kHz, according to (3). This is close to the observed f_{c2} = 200 kHz in Fig. 15. The third corner frequency f_{c3} should theoretically be 1.33 MHz, according to (4), a value that is very close to the observed 1.3 MHz.

Peaks of exacerbated harmonic content are seen between 1 and 3 MHz in the three soft-switching spectra, which interrupt the -60 dB/dec slope. As seen in Figs. 11(b), 11(c), 12 and 13, these peaks are due to the ringing observed in the time domain, under the soft-switching schemes. The first peak is concentrated around a frequency near 1.4 MHz, and the

second one, seen merging with the first, is centred on 2 MHz. The first peak is attributed to the 1.4-MHz ringing seen on the v_{pole} waveform as soon as it reaches steady state, while the second peak is due to the 1.9-MHz ringing of the capacitor current i_{Cr4} that is responsible for the undulation on the v_{pole} edges. As observed in Fig. 13(b), the ringing is attenuated when R_{g_main} = 11 Ω, and this is reflected in the corresponding spectrum. It is repeated here that these oscillations are inherent to the manufactured PCB used in this work. A better engineered PCB can mitigate these phenomena.

Nevertheless, the variable-timing scheme with R_{g_main} = 11 Ω results in a maximum harmonic content attenuation of 37 dB at 4 MHz, with regards to hard switching.

VIII. Conclusions

This paper has presented a method for designing ACPI converters mainly for attenuating high frequency EMI purposes. It has been shown that the generation of symmetrical v_{pole} pulses is made possible with variable-timing control, which allows for a frequency response with more predictable and predetermined spectral envelopes. Capacitive turn-offs, though adding to the control complexity, were shown to alleviate current stress and power loss even further, without altering the high-frequency response, since the linear v_{pole} edges they produced were long and low in number. Lastly, it was shown that reducing the main gate resistor value is a simple and effective way of reducing high-frequency harmonic content, power loss, and current stress under any soft-switching scheme. Thus, a 3-phase, 5-kW ACPI controlled under a variable-timing scheme with a reduced value of R_{g_main} = 11 Ω was shown to have the most optimized and predictable frequency response. At 4 MHz this control scheme achieved a harmonic content attenuation of 37 dB compared to an equivalent hard switching inverter. Thus, the ACPI can be employed for addressing the source of EMI in VSCs, with minimal to no impact on their efficiency.

References

[1] B. Sarlioglu and C. T. Morris, "More Electric Aircraft: Review, Challenges, and Opportunities for Commercial Transport Aircraft," *IEEE Transactions on Transportation Electrification,* vol. 1, no. 1, pp. 54-64, June 2015.

[2] G. Calderon-Lopez, A. J. Forsyth, D. L. Gordon and J. R. McIntosh, "Evaluation of SiC BJTs for High-Power DC-DC Converters," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2474-2481, May 2014.

[3] C. R. Paul, *Introduction to Electromagnetic Compatibility*, 2nd ed. Hoboken, NJ, Wiley, 2006.

[4] G. Skibinski, J. Pankau, R. Sladky, and J. Campbell, "Generation, control and regulation of EMI from AC drives," *IEEE Industry Applications Conference (IAS '97)*, 1997, vol. 2, pp. 1571-1583.

[5] A. Di Napoli and A. Ndokaj, "EMC and safety in vehicle drives," *IEEE Power Electronics and Applications Conference (EPE 2011),* 2011, pp. 1-8.

[6] J. Erdman, R. J. Kerkman, D. Schlegel and G. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Applied Power Electronics Conference and Exposition (APEC '95)*, 1995, vol.1, pp. 24-33.

[7] A. von Jouanne, P. Enjeti, and W. Gray, "The effect of long motor leads on PWM inverter fed AC motor drive systems," *IEEE Applied Power Electronics Conference and Exposition (APEC '95)*, 1995, vol.2, pp. 592-597.

[8] C. Jaeger, I. Grinbaum and J. Smajic, "Numerical simulation and measurement of common-mode and circulating bearing currents," *IEEE International Conference on Electrical Machines (ICEM '16)*, 2016, pp. 486-491.

[9] Radio Technical Commission for Aeronautics. DO-160G: Environmental Conditions and Test Procedures for Airborne Equipment. http://www.rtca.org (2010)

[10] C. R. Paul and K. B. Hardin, "Diagnosis and reduction of conducted noise emissions," *IEEE Transactions on Electromagnetic Compatibility,* vol. 30, no. 4, pp. 553-560, Nov. 1988.

[11] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 2, pp. 469-476, Mar.-Apr. 1999.

[12] A. Elrayyah, K. MPK Namburi and Y. Sozer and I. Husain. "An Effective Dithering Method for Electromagnetic Interference (EMI) Reduction in Single-Phase DC/AC Inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2798-2806, June 2014.

[13] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," *IEEE Energy Conversion Congress and Exposition (ECCE '12),* 2012, pp. 4754-4761.

[14] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics Converters*, *Applications and Design*, J. Wiley & Sons, Inc., 1995.

[15] V. Pickert, and C. M. Johnson, "Three-phase soft-switching voltage source converters for motor drives. I. Overview and analysis," *IEE Proceedings on Electric Power Applications*, vol. 146, no. 2, pp. 147-154, Mar. 1999.

[16] MA Ke, XU De-hong, ZHANG Tao, Seiki IGARASHI. "Divided-fixed Timing Control Method for Auxiliary Resonant Commutated Pole Soft-switching Inverter," *Proceedings of the CSEE*，2010，30(18)：23-27 (in Chinese).

[17] W. Dong, J. Y. Choi, Y. Li, D. Boroyevich, F. C. Lee, J. Lai et al., "Comparative experimental evaluation of soft-switching inverter techniques for electric vehicle drive applications," *IEEE Industry Applications Conference (IAS '01)*, 2001, vol. 3, pp. 1469-1476.

[18] Huibin Zhu, Jih-Sheng Lai, A. R. Hefner, Yuqing Tang and Chingchi Chen, "Modeling-based examination of conducted EMI emissions from hard and soft-switching PWM inverters," *IEEE Transactions on Industry Applications,* vol. 37, no. 5, pp. 1383-1393, Sep. 2001.

[19] J. Shao, R. L. Lin, F. C. Lee and D. Y. Chen, "Characterization of EMI performance for hard and soft-switched inverters," *IEEE Applied Power Electronics Conference and Exposition (APEC '2000)*, 2000, vol. 2, pp. 1009-1014.

[20] Y. Tang, H. Zhu, B. Song, J. S. Lai and C. Chen, "EMI experimental comparison of PWM inverters between hard- and soft-switching techniques," *Power Electronics in Transportation,* pp. 71-77, Oct. 1998.

[21] M. R. Yazdani, H. Farzanehfard and J. Faiz, "EMI Analysis and Evaluation of an Improved ZCT Flyback Converter," *IEEE Transactions on Power Electronics,* vol. 26, no. 8, pp. 2326-2334, Aug. 2011.

[22] M. Mohammadi, E. Adib and M. R. Yazdani, "Family of Soft-Switching Single-Switch PWM Converters With Lossless Passive Snubber," *IEEE Transactions on Industrial Electronics,* vol. 62, no. 6, pp. 3473-3481, June 2015.

[23] M.E. Elbuluk and M.D. Kankam, "Potential starter/generator technologies for future aerospace applications," *IEEE Aerospace and Electronic Systems Magazine,* vol. 12, no. 5, pp. 24-31, May 1997.

[24] F. Costa, C. Gautier, E. Laboure, and B. Revol, *Electromagnetic Compatibility in Power Electronics,* ISTE Ltd and J. Wiley & Sons, Inc., 2014.

[25] V. Pickert, and C. M. Johnson, "Three-phase soft-switching voltage source converters for motor drives. II. Fundamental limitations and critical assessment," *IEE Proceedings on Electric Power Applications*, vol. 146, no. 2, pp. 155-162, Mar. 1999.

[26] J. S. Lai, J. Zhang, H. Yu and H. Kouns, "Source and Load Adaptive Design for a High-Power Soft-Switching Inverter*," IEEE Transactions on Power Electronics,* vol. 21, no. 6, pp. 1667-1675, Nov. 2006.

[27] X. Yuan, and I. Barbi, "Analysis, designing, and experimentation of a transformer-assisted PWM zero-voltage switching pole inverter," *IEEE Transactions on Power Electronics,* vol. 15, no. 1, pp. 72-82, Jan 2000.

[28] I. Barbi, and D. C. Martins, "A true PWM zero-voltage switching pole, with very low additional RMS current stress," *Power Electronics Specialists Conference (PESC '91),* 1991, pp. 261-267.

[29] W. Yu, J. S. Lai and S. Y. Park, "An Improved Zero-Voltage Switching Inverter Using Two Coupled Magnetics in One Resonant Pole," *IEEE Transactions on Power Electronics,* vol. 25, no. 4, pp. 952-961, April 2010.

[30] R. W. De Doncker, and J. P. Lyons, "The auxiliary resonant commutated pole converter," *IEEE Industry Applications Society Annual Meeting*, 1990, vol. 2, pp. 1228-1235.

[31] W. McMurray, "Resonant snubbers with auxiliary switches," *IEEE Industry Applications Society Annual Meeting,* 1989, vol.1, pp. 289-834.

[32] N. Soltau, J. Lange, M. Stieneker, H. Stagge and R. W. De Doncker, "Ensuring soft-switching operation of a three-phase dual-active bridge DC-DC converter applying an auxiliary resonant-commutated pole," *IEEE European Conference on Power Electronics and Applications (EPE*

'14), 2014, pp. 1-10.

[33] K. Ma, D. Xu, T. Zhang, and S. Igarashi, "The evaluation of control strategies for auxiliary resonant commutated pole inverter," *IEEE Energy Conversion Congress and Exposition (ECCE 2009)*, 2009, pp. 810-816.

[34] Baoquan Kou, H. Zhang, Yinxi Jin and H. Zhang, "An improved control scheme for single-phase auxiliary resonant snubber inverter," *IEEE Power Electronics and Motion Control Conference (IPEMC-ECCE Asia '16),* 2016, pp. 1259-1263.

[35] Michigan State University. Electromagnetic Compatibility (EMC) Course Notes. http://www.egr.msu.edu/em/research/goali/notes/ (2007)

[36] N. Oswald, B. H. Stark, D. Holliday, C. Hargis, and B. Drury, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2154-2165, Sept.-Oct. 2011.

[37] A. Karvonen, T. Thiringer, P. Futane, T. Tuveson, and H. Holst, "Reduction of EMI in switched mode converters by shaped pulse transitions," *Society Automotive Engineers (SAE) World Congress,* 2007, Paper 2007-01-0361.

[38] D. G. Holmes and Thomas A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practices,* J. Wiley & Sons, Inc., 2003

[39] A. Nagel, and R. W. De Doncker, "Analytical approximations of interference spectra generated by power converters," *IEEE Industry Applications Conference (IAS '97)*, 1997, vol. 2, pp. 1564-1570.

[40] D. M. Divan, "The resonant DC link converter-a new concept in static power conversion," *IEEE Transactions on Industry Applications,* vol. 25, no. 2, pp. 317-325, March 1989.

[41] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Transactions on Industry Applications,* vol. 25, no. 4, pp. 634-643, July 1989.

[42] R. Teichmann, "Control parameter selection in auxiliary resonant commutated pole converters," *IEEE Industrial Electronics Society Conference (IECON '01)*, 2001, vol. 2, pp. 862-869.

[43] Wei Dong, Dengming Peng, Huijie Yu, F. C. Lee and J. Lai, "A simplified control scheme for zero voltage transition (ZVT) inverter using coupled inductors," *IEEE Power Electronics Specialists Conference (PESC '00),* 2000, vol. 3, pp. 1221-1226.

[44] Q. Yu, and R. M. Nelms, "State plane analysis of an auxiliary resonant commutated pole inverter and implementation with load current adaptive fixed timing control," *IEEE Industrial Electronics Society Conferece (IECON 02),* 2002, vol.1, pp. 437-443 vol.

[45] A. Charalambous, X. Yuan, N. McNeill, Q. Yan, and N. Oswald, "EMI reduction with a soft-switched auxiliary commutated pole inverter," *IEEE Energy Conversion Congress and Exposition (ECCE 2015)*, 2015, pp. 2650-2657.

[46] A. Charalambous, X. Yuan, N. McNeill, S. Walder, Q. Yan, and C. Frederickson, "Controlling the output voltage frequency response of the auxiliary commutated pole inverter," *IEEE Industrial Electronics Society Conference (IECON 2016),* 2016, pp. 3305-3310.

[47] R. Teichmann and H. Gueldner, "Analysis of transfer ratio limitations in auxiliary resonant commutated pole converters," *IEEE International Power Electronics Congress (CIEP 2000),* 2000, pp. 15-20.

[48] G. Rizzoli, M. Mengoni, L. Zarri, A. Tani, G. Serra and D. Casadei, "Experimental comparison of hard-switching, ZVT and SiC inverters*," IEEE International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM '16),* 2016, pp. 184-191.

[49] M. Trivedi, and K. Shenai, "Internal dynamics of IGBT under zero-voltage and zero-current switching conditions," *IEEE Transactions on Electron Devices,* vol. 46, no. 6, pp. 1274-1282, Jun. 1999.

[50] C. Du, W. G. Hurley and D. Xu, "Design Methodology of Resonant Inductor in a ZVS Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 3, no. 4, pp. 1142-1150, Dec. 2015.