High-Frequency Resonant SEPIC Converter With Wide Input and Output Voltage Ranges

High Frequency Resonant SEPIC Converter with Wide Input and Output Voltage Ranges

Jingying Hu, *Student Member, IEEE,* Anthony D. Sagneri, *Student Member, IEEE,* Juan M. Rivas, *Member, IEEE,* Yehui Han, *Student Member, IEEE,* Seth M. Davis, and David J. Perreault, *Senior Member, IEEE*

***Abstract*—This document presents a resonant Single-Ended-Primary-Inductor-Converter (SEPIC) converter and control method suitable for high frequency (HF) and very high frequency (VHF) dc-dc power conversion. The proposed design features high efficiency over a wide input and output voltage range, up-and-down voltage conversion, small size, and excellent transient performance. In addition, a resonant gate drive scheme is presented which provides rapid startup and low-loss at HF and VHF frequencies. The converter regulates the output using an on-off control scheme modulating at a fixed frequency (170 kHz). This control method enables fast transient response and efficient light load operation while providing controlled spectral characteristics of the input and output waveforms. A hysteretic override technique is also introduced which enables the converter to reject load disturbances with a bandwidth much greater than the modulation frequency, limiting output voltage disturbances to within a fixed value. An experimental prototype has been built and evaluated. The prototype converter, built with two commercial vertical MOSFETs, operates at a fixed switching frequency of 20 MHz, with an input voltage range of 3.6 V to 7.2 V, an output voltage range of 3 V to 9 V and an output power rating of up to 3W. The converter achieves higher than 80% efficiency across the entire input voltage range at nominal output voltage, and maintains good efficiency across the whole operating range.**

***Index Terms*—Resonant dc-dc converter, quasi-resonant SEPIC converter, high frequency, VHF integrated power converter, class E inverter, resonant gate drive, resonant rectifier, on-off control.**

I. Introduction

MANY portable electronic applications could benefit from a power converter able to achieve high efficiency across wide input and output voltage ranges at a small size. However, it is difficult for many conventional power converter designs to provide wide operation range while maintaining high efficiency, especially if both up-and-down voltage conversion is to be achieved. Furthermore, the bulk energy storage required at contemporary switching frequencies of a few megahertz and below limits the degree of miniaturization that can be achieved and hampers fast transient response. Therefore, design methods that reduce energy storage requirements and expand efficient operation range are desirable. In this paper, we exploit the use of resonant switching and gating along with fixed frequency control techniques to achieve these goals.

This paper introduces a quasi-resonant SEPIC converter, resonant gate drive and associated control methods suitable for converter designs at frequencies above 10 MHz. Unlike many resonant converter designs [1]–[4], the proposed approach provides high efficiency over very wide input and output voltage ranges and power levels. It also provides up-and-down conversion, and requires little energy storage which allows for excellent transient response. Unlike conventional quasi-resonant and multi-resonant converters [3], [4], no bulk inductor is used and the converter operates at fixed frequency and duty ratio. These attributes reduce passive component size, improve response speed, and enable the use of low-loss sinusoidal resonant gating. Furthermore, a new fixed-frequency on/off control is introduced which provides good control over input and output frequency content. The proposed design is discussed in the context of a prototype converter operating over wide input voltage ($3.6-7.2$ V), output voltage ($3-9$ V) and power ($0.3-3$ W) ranges. This design is suitable, for example, for a power supply to provide adaptive bias control of an RF power amplifier from a battery input. The wide output voltage and power reflect the requirements for adjusting bias to the power amplifier, while the wide input voltage reflects operation from a battery pack across the charge and discharge range. Section II presents the new proposed circuit design and discusses its operation. A low-loss resonant gate drive method suitable for this application is explained in detail in Section III, followed by a discussion of the converter control scheme in Section IV. Section V presents the design and experimental validation of a converter implementing the approach.

II. A New Resonant SEPIC Converter

Figure 1 shows the power stage of the proposed converter. The topology used here has some topological similarities with both the conventional SEPIC converter [5] and with the multi-resonant SEPIC converter proposed in [4]. However, the detailed component placement and sizing, operating characteristics, and control approach are all very different from previous designs.

First, consider the circuit topology. The conventional SEPIC converter has two bulk (ac choke) inductors, and yields hard switching of the switch and diode. Thus, in the conventional

J. Hu, A. D. Sagneri and D. J. Perreault are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (email: jyh@mit.edu, sagnea@mit.edu, djperrea@mit.edu).

J. M. Rivas is with GE Global Research, Niskayuna, NY 12309 USA (email: rivasd@ge.com).

Y. Han is with the Department of Electrical Engineering and Computer Science, University of Wisconsin-Madison, WI 02139 USA (email: yehui@engr.wisc.edu).

S. M. Davis is with the Charles Stark Draper Laboratory, Cambridge, MA 02139 USA (email: sethd@draper.com).

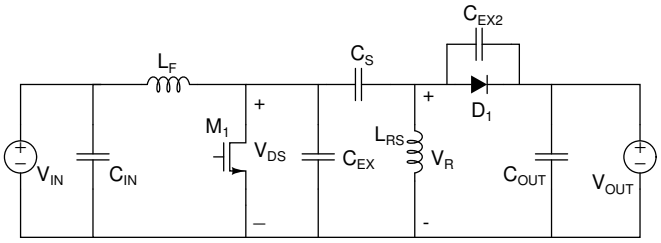


Fig. 1. Schematic of the proposed resonant SEPIC converter topology.

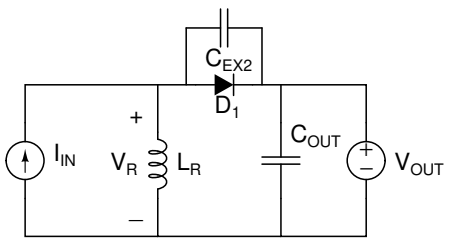


Fig. 2. Circuit model for tuning of the resonant rectifier.

quasi-resonant SEPIC converter L_F is a choke inductor, selected to provide nearly constant current over a switching cycle. The multi-resonant SEPIC [4] utilizes similar bulk inductors, but explicitly introduces capacitances in parallel with the switch and diode along with a resonant inductor in series with the coupling capacitor C_S to achieve zero-voltage soft switching of the switch and diode. The design introduced here also explicitly utilizes capacitances in parallel with the switch and diode. However, in contrast to previous resonant SEPIC designs [3], [4], the design here has no bulk inductors. Rather, it uses only two resonant inductors: one inductor, L_F, resonates with the net switch capacitance, $C_{OSS}+C_{EX}$, for resonant inversion, while the other inductor, L_{RS}, resonates with the rectifier capacitance, C_{EX2}, for resonant rectification. This design method leads to reduced magnetic component count, along with greatly increased response speed.

A further major difference between the converter proposed here and previous resonant SEPIC converters relates to control. The conventional resonant SEPIC converter regulates the output voltage by keeping the on-time pulse fixed while varying the off time duration, leading to variable-frequency, variable-duty-ratio operation. Unlike conventional designs which used variable frequency control to regulate the output [3], [4], the design here operates at fixed switching frequency and duty ratio. (As discussed in Section IV, output control is instead achieved through on/off control, in which the entire converter is modulated on and off at a modulation frequency that is far below the switching frequency [6]–[13].) Operation at a fixed frequency and duty ratio enables the elimination of bulk magnetic components (as described above) and facilitates the use of highly efficient sinusoidal resonant gating (as described in Section IV). Moreover, it enables zero-voltage soft switching to be maintained over wide input and output voltage ranges, and eliminates the variation in device stress with converter load that occurs in many resonant designs [3], [4].

Operation of this converter can be understood as a linking of two subsystems: a resonant inverter and a resonant rectifier. The design procedure for the proposed topology involves designing the rectifier and inverter individually, coupling the inverter and rectifier together, then retuning as necessary to account for nonlinear interactions between the inverter and rectifier. We treat these steps in the following subsections.

A. Rectifier Design

The design procedure of a full dc-dc converter starts with the rectifier. The particular resonant rectifier topology of interest here is illustrated in Fig. 2 (along with a sinusoidal drive source used in tuning the rectifier design). A similar rectifier structure was exploited in [7] but under different driving conditions. The rectifier utilizes a resonant tank comprising a resonant inductor L_R (which provides a dc path for the output current) and a capacitance including an external capacitor C_{EX2} along with additional parasitic junction capacitance from the diode.

To design the rectifier, we start by assuming that it is driven by a sinusoidal current source of magnitude I_{IN} at a given output voltage V_{OUT}, as illustrated in Fig. 2. (It is recognized that the actual drive waveform is not sinusoidal; this fact is addressed in a later tuning step.) For a desired output power level and operating frequency, the rectifier is tuned to appear resistive in a describing function sense by adjusting C_{EX2} and L_R. That is, we adjust C_{EX2} and L_R such that the fundamental component of V_R is in phase with the drive waveform I_{IN} (or alternatively has some phase shift, thus presenting an equivalent reactive component.) In doing this, we start by assuming a drive amplitude I_{IN}. We also adjust the values of L_R and C_{EX2} and/or the assumed drive level I_{IN} to ensure that the desired power is delivered through the rectifier. The equivalent rectifier impedance at the operating frequency is calculated as the complex ratio $Z_{EQV} = V_{R,1}/I_{IN}$, where $V_{R,1}$ is the fundamental of V_R. This equivalent impedance can be used in place of the rectifier for designing the resonant inverter, assuming that the majority of the output power delivered to the load is transferred through the fundamental.

The following design example of a 4 W rectifier at a nominal output voltage of 7 V illustrates the tuning procedure described above. The rectifier uses a commercial Schottky diode $DFLS230L$ (having an approximate capacitance of 70 pF) and is driven by a sinusoidal current source I_{IN} with an amplitude of 0.7A. The value of L_R of the resonant rectifier is selected in conjunction with C_{EX2} so that the fundamental rectifier input voltage V_R is in phase with rectifier input current I_{IN}. Figure 3 shows the input current and voltage of a resonant rectifier (like the one in Fig. 2) simulated using PSPICE. For the simulation shown, $L_R = 118$ nH, $C_{EX2} = 150$ pF, $V_{OUT} = 7$ V, and the sinusoidal input current $I_{IN} = 0.7$ A at a frequency of 20 MHz. The average power delivered to the load under these conditions is 4.12 W. In Fig. 3, the fundamental component of the input voltage and the current are in phase resulting in a rectifier with an equivalent resistance (at the fundamental) of approximately $17.14\,\Omega$. As the values of L_R and C_{EX2} are changed, output power level and the

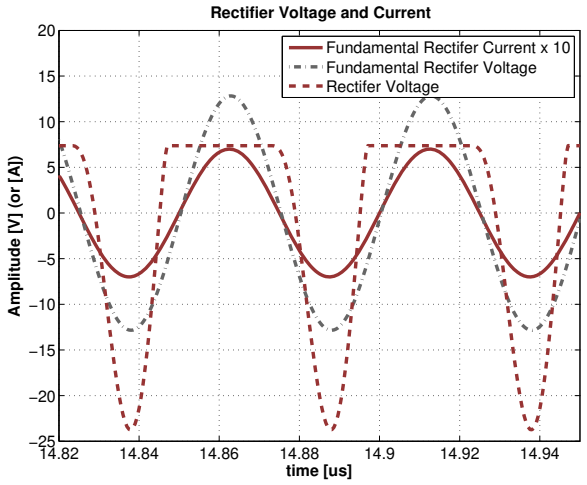


Fig. 3. Fundamentals of rectifier voltage, V_R and current, I_{IN} of the resonant rectifier of Fig. 2 tuned to look resistive at an operating frequency of 20 MHz. Simulation is for a rectifier built with a DFLS230L Schottky diode, L_R = 118 nH, C_{EX2} = 150 pF, and V_{OUT} = 7 V.

TABLE I
TUNED AND DETUNED RECTIFIER COMPONENT VALUES

L_R	90 nH	118 nH	118 nH
C_{EX2}	150 pF	50 pF	150 pF
$\|Z_{EQV}\|$	18.07 Ω	19.08 Ω	18.12 Ω
$\angle Z_{EQV}$	36.9°	47.69°	0
P_{OUT}	2.28 W	2.97 W	4.12 W
Efficiency	89.6%	90.6%	91.4%

phase relationship between V_R and I_{IN} change. As the phase difference between V_R and I_{IN} increases, the losses due to reactive currents rise, reducing the output power and the overall efficiency of the rectifier, as shown in Table I.

B. Inverter Design

Consider the inverter network of Fig. 4, which includes impedance matching from the inverter to the equivalent rectifier impedance. Inverter tuning begins by selecting appropriate matching components. (The matching inductance is later absorbed as part of the rectifier, with L_{RS} being the parallel combination of the inverter inductor L_S and the rectifier inductor L_R.)

Assuming that most power is transferred through the fundamental, the maximum equivalent resistance R_{MAX} needed to deliver an output power level of P_{OUT} with a fundamental voltage at the MOSFET drain, $V_{DS,1}$ can be calculated from $R_{MAX} = V_{DS,1}^2/(2 * P_{OUT})$,where R_{MAX} is the "transformed" resistance loading the drain-to-source port of the inverter. As Fig. 5 illustrates, the drain waveform of the resonant SEPIC converter is similar to that of a conventional Class-E inverter. Therefore, one possible starting point to obtain R_{MAX} is to approximate the fundamental voltage as in the Class-E inverter case, $V_{DS,1} = 1.6 * V_{IN}$, [14]. (It is recognized that the actual $V_{DS,1}$ of the resonant SEPIC converter is not exactly $1.6 * V_{IN}$, the effects of which can be addressed by adjusting output power when coupling the inverter and rectifier together.)

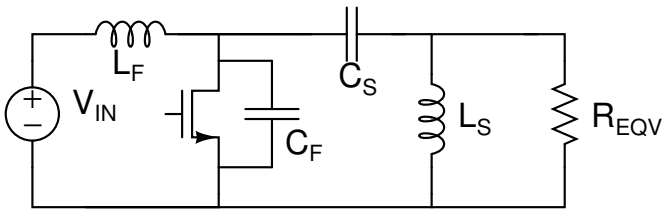


Fig. 4. Resonant inverter including a matching circuit and equivalent load resistance. This circuit model is used for tuning the inverter.

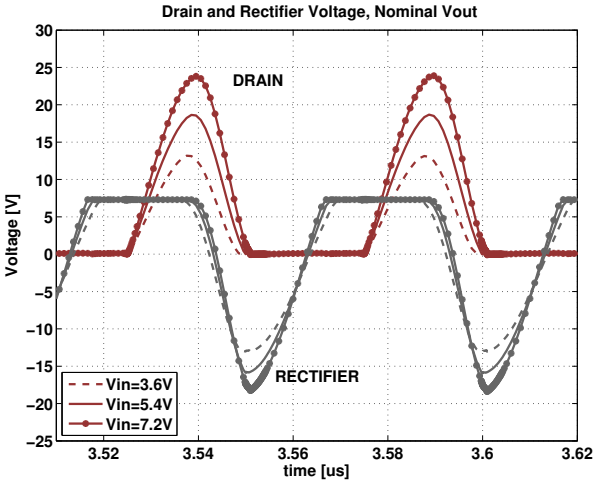


Fig. 5. Simulated drain (V_{DS}) and rectifier (V_R) voltages for a 20 MHz converter operating with V_{out} = 7 V, L_F = 22 nH, C_{EX} = 780 pF, C_{EX2} = 100 pF, C_S = 1270 pF, and L_P = 41 nH. Inductor Q of 70 and capacitor Q of 3000 is assumed. Two $SPN1443$ MOSFETs and a $DFLS230L$ diode are used.

When the rectifier equivalent resistance, R_{EQV}, is higher than the value R_{MAX} to meet the output power requirement, a matching network consisting of L_S and C_S is required to transform the load impedance to a lower value [7], [15], [16]. The approximate transformation ratio can be obtained as R_{MAX}/R_{EQV}. One possible starting point to selecting the component values for L_S and C_S is to design a matching network such that a transformation ratio R_{MAX}/R_{EQV} occurs at the desired operating frequency. Additional minor adjustments on these component values may be done later in conjunction with tuning C_F and L_F with a simulation tool (e.g. PSPICE) to achieve a resulting drain-to-source switching waveform V_{DS} that has ZVS and zero dv/dt at turn on. In practice, the resonance of L_S and C_S can be set to be exactly at the switching frequency, or slightly above or below the resonant frequency, all of which are typically viable and will lead to a working design. In a given application, one tuning may result in more achievable component values and therefore may be more favorable compared to the others. Once matching network components have been selected, inductance L_S may be absorbed into the rectifier inductance L_R.

The input resonant network, comprising L_F and C_F, largely shapes the frequency at which the drain waveform rings up and down. For an inverter operating at a 50% duty ratio, one possible starting point for L_F is to tune the input resonant

network such that its resonance frequency is at twice the switching frequency, as in (1). This tuning selection is similar to that of the "second harmonic" class E inverter in [17], [18].

$$L_F = \frac{1}{16\pi^2 f_{SW}^2 C_F} \tag{1}$$

Note that the capacitor C_F includes the parasitic capacitance of the semiconductor switch and possibly an external capacitor C_{EX}. In some applications where the packaging inductance of the semiconductor switch is significant, selecting C_F to be solely provided by the device capacitance may be a good choice, because it prevents waveform distortion caused by additional ringing between the external capacitance and the package inductance. In other cases where the circulating current is significant, it is a better choice to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the circulating current loss. One starting point for C_F is to assume it is comprised solely of parasitic capacitance of the semiconductor switch, allowing an initial value of L_F to be calculated. Since L_F significantly impacts the transient response speed, a small L_F is generally preferred. If the starting point of C_F leads to too large a value of L_F, additional parallel capacitance C_{EX} may be added until the value of L_F is in the desired range.

Once the initial values of L_F, C_F, L_S and C_S are determined from the procedure above, additional tuning can be made via minor adjustments of the component values along with the duty ratio until the resulting drain-to-source switching waveform V_{DS} achieves ZVS and zero dv/dt turn on, the so-called class E switching waveform.

Using the equivalent resistance $R_{EQV} = 17.14\ \Omega$ from the rectifier design discussed previously, a 20 MHz inverter utilizing two commercial vertical MOSFETs $SPN1443$ in parallel can be designed in the following manner: a matching network which transforms the equivalent rectifier impedance from $17.14\ \Omega$ to $4\ \Omega$ at about the operating frequency is required in order to deliver 4 W at an input voltage of 3.6 V. The component values for such a matching network are $L_S = 76$nH and $C_S = 1120$pF. If C_F is to be comprised solely of the parasitic capacitance of $SPN1443$ (about 160 pF), the resulting L_F is about 141 nH, a condition which deteriorates the transient response speed and overall closed-loop efficiency. In this design, it is found through time-domain simulations that it is desirable to add additional high-Q ceramic capacitance in parallel with the lossy device parasitic capacitance to reduce the overall loss and to reduce the component value (and size) of the input inductor L_F. A starting value for L_F is chosen to be 22 nH (so that the inductance is small enough to allow for fast transient response and large enough to not be significantly affected by low-Q board parasitic inductance), resulting in an external capacitor C_{EX} of 550 pF at a 50% duty ratio.

C. dc/dc Retuning

An entire converter design may be accomplished by connecting the tuned inverter to the resonant rectifier. When the inverter and rectifier are connected, the circuit waveforms and the output power level may be slightly different than that predicted by the inverter loaded with the equivalent impedance, due to the non-linear interaction between the inverter/matching network with the rectifier. Minor additional tuning may thus be required to achieve ZVS and the required power level. The final component values for a complete converter using the example rectifier and inverter design described in this section will be presented in Section V. A complete discussion of the tuning methodology for these components is found in [19].

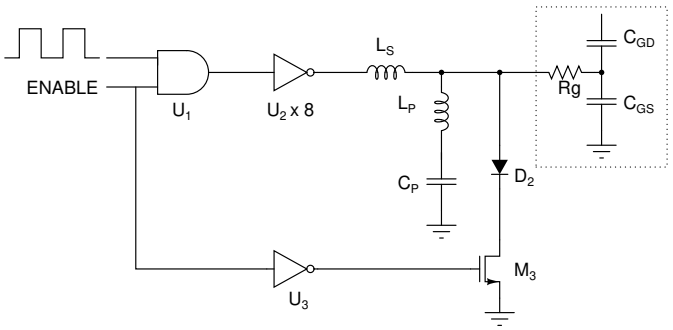


Fig. 6. Resonant sinusoidal gate drive circuit with MOSFET gate model.

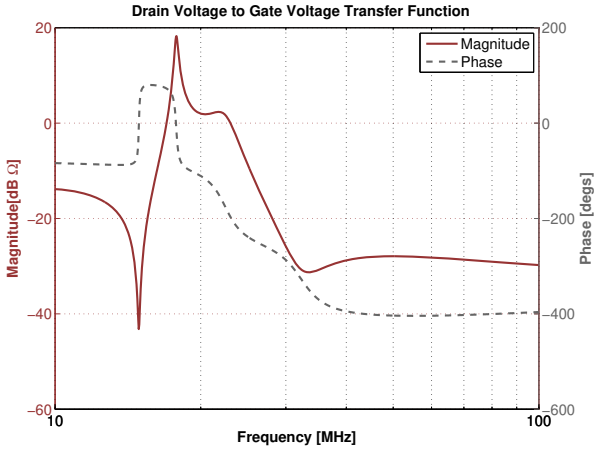
Figure 5 shows the idealized drain and rectifier voltage waveforms for the proposed design over a range of input voltages using the techniques outlined in previous subsections (the component values are included in the description of Fig. 5). It can be seen that zero-voltage soft switching is achieved at fixed frequency and duty ratio across a wide range of input voltages. In addition, while developing the design required tuning of the selected circuit component values, this tuning needed only to be performed once. The converter performance was found to be repeatable across several prototypes. Moreover, the converter is tolerant of the device non-linear capacitance variation with input voltage over the entire operating range.

III. Gate Driver

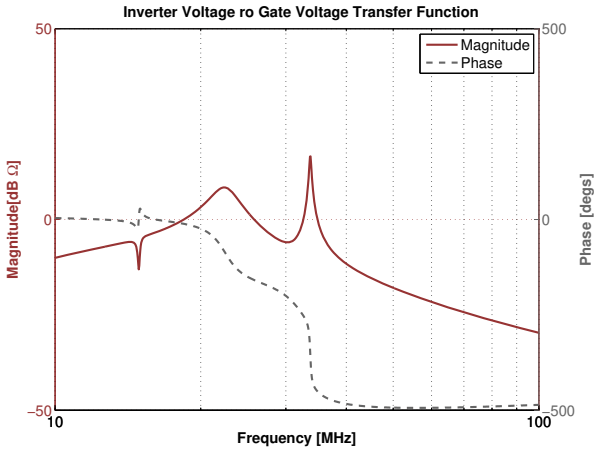
At HF and VHF frequencies, traditional hard-switched gate drives typically incur too much loss for acceptable efficiency, especially for low power converters. Resonant gating can reduce the gating loss significantly at these frequencies [7]–[9], [20]. By recovering a portion of the gate energy each cycle, much lower power is required to drive the gate, minimizing the impact that gating loss has on overall converter efficiency.

While use of fixed-frequency and fixed-duty-ratio operation reduces driver complexity, the use of on-off control of the output introduces some important requirements. In addition to achieving low power operation at steady state, a practical gate drive for our system must settle rapidly at startup and shutdown to maintain good converter transient response and high efficiency under modulation. A low-loss gate drive method is designed to meet these criteria for this converter. Figure 6 shows a schematic of the resonant driver circuit we have adopted. The detailed design approach and the operation of the gate drive is summarized as follows:

In the driver of Fig. 6, a bank of CMOS inverters drives the gate via a tuned resonant network. The shunt branch of L_P and C_P is inductive at the switching frequency (with C_P simply acting as a dc block). L_P is sized to partially cancel the gate admittance, leaving the parallel combination

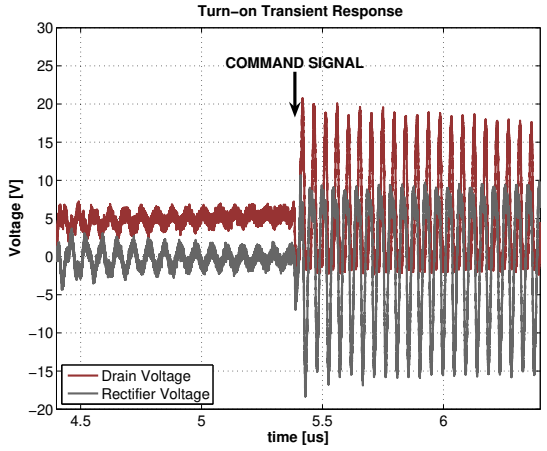


(a) Drain voltage to gate voltage transfer function V_{GATE}/V_{DRAIN}

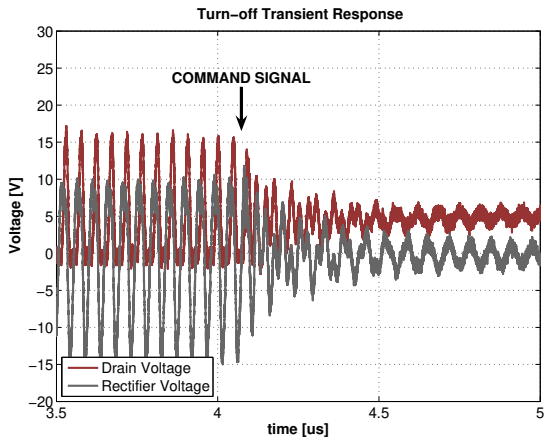


(b) Inverter voltage to gate voltage transfer function V_{GATE}/V_{INV}

Fig. 7. Gate drive transfer functions.



(a) Turn-on Transient Response



(b) Turn-off Transient Response

Fig. 8. Experimental On/Off transient response for the converter operating at $V_{IN} = 3.6$ V and $V_{OUT} = 5.2$ V.

of L_P and the gate capacitive, but with higher impedance than the gate capacitance alone. L_P thus provides some of the reactive power needed to charge and discharge the gate. L_G serves multiple functions. First, it is resonant with the parallel combination of the L_P and C_{GATE} near the switching frequency such that there is significant voltage gain from the CMOS inverter bank to the gate at the switching frequency. Second, it provides a high impedance to harmonic voltages applied by the CMOS inverter, reducing inverter loss.

The tuning method applied to the resonant gate drive is similar to that described in [9], with slight changes due to different device and overall system characteristics. In designing the gate drive, the feedback from the transistor drain to its gate is an important factor. Unlike [9], for the design parameters here, an optimal gate drive design cannot be achieved with the phase of a drain to gate transfer function close to $180°$. Achieving such a phase angle will either incur too much gating loss or require a large L_G and a small L_P which will slow the gate drive startup and deteriorate the overall system performance (The MOSFET used here present an equivalent R_g of 1.17Ω, C_{gs} of 550 pF and C_{gd} of 43 pF). Fortunately, for this application, the drain-to-gate feedback is not crucial to achieving the desired amplitude at the gate. A better overall efficiency is achieved with a drain-to-gate phase angle around $250°$. Figure 7 shows the drain-to-gate transfer function and driver-to-gate transfer function for such a gate drive design. Component values for this gate drive are shown in Table II. More details of the gate drive design appear in [19].

TABLE II
GATE DRIVE COMPONENT VALUES

U_1	NC7SZ08
U_2, U_3	NC7WZ04
L_G	110 nH
L_P	72 nH
C_P	0.1 μF
D_2	MA27D27
M_3	FDV303N

To provide on/off modulation capability, the CMOS inverter bank is driven by an oscillator signal that is gated by an enable input. The enable input provides on/off control. Moreover, an active pull-down network comprising a CMOS inverter (U_3), a MOSFET (M_3), and a diode (D_2) helps provide rapid shutdown at turnoff. This gate drive enables startup and shutdown of the converter (to steady state) within four switching cycles as shown in Fig. 8. This is sufficiently fast

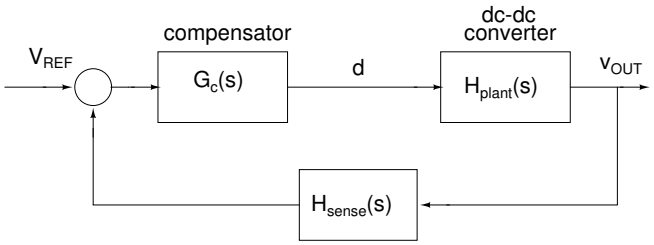


Fig. 9. Block diagram for the PWM on/off control method.

to maintain good efficiency under on-off modulation.

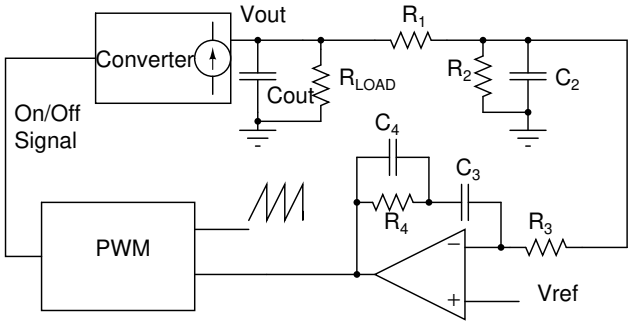
IV. Control Strategy

This control strategy employed is an on-off control scheme, in which switching of the converter is gated on and off to control the average power delivered to the output. The frequency at which the converter is modulated on and off is much lower than the converter switching frequency. In this approach, the power stage components are sized for the the very high switching frequency, while the converter input and output filters (e.g., capacitors) are sized for the lower modulation frequency.

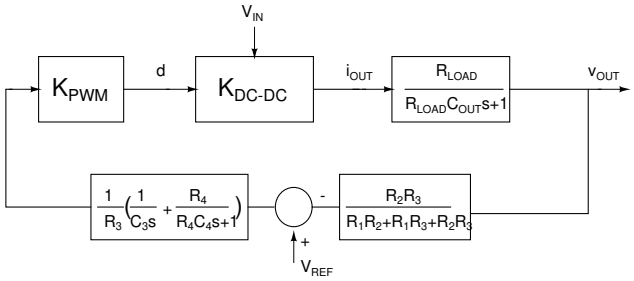
One on-off control method, voltage hysteretic control (or bang-bang control), has been implemented in previous resonant converter designs [6]–[11]. Voltage hysteretic on-off control offers advantages such as a well-controlled voltage band, good efficiency at very light load, and unconditional stability. However, the input and output waveforms have variable frequency content (owing to the variable-frequency modulation) making this control method undesirable in some applications (such as communication systems), and increasing the difficulty of designing input and output filters.

To address the variable frequency components residing in the input/output waveforms, a new approach, in which the on-time of the converter is pulse-width modulated within a fixed modulation period, is utilized to implement the on-off control method. Unlike hysteretic on-off control, PWM on-off control operates a fixed modulation frequency, leading to well-defined frequency content at the converter input and output. On the other hand, efficiency tends to decline at extreme light loads, when the converter may operate for only a few switching cycles each modulation period. The characteristics of this control method are similar in many regards to conventional fixed-frequency PWM. However, instead of modulating the voltage applied to a filter, the current delivered to the output capacitor and load is modulated.

The basic control approach is illustrated in Fig. 9, with a more detailed illustration of one particular circuit design and its control block diagram in Fig. 10. The controller in our prototype is implemented with a conventional PWM chip whose PWM output is the enable signal of the power stage gate drive. The converter power stage can be modeled as a one-pole system with the converter approximated as a controlled current source feeding the output capacitor and load C_{OUT} and R_{LOAD}, where R_{LOAD} is the effective load resistance of the converter. The transfer function of the plant,



(a) On/off PWM control of a resonant dc-dc converter.



(b) Block diagram model of the closed-loop system

Fig. 10. Implementation of PWM control for the prototype converter.

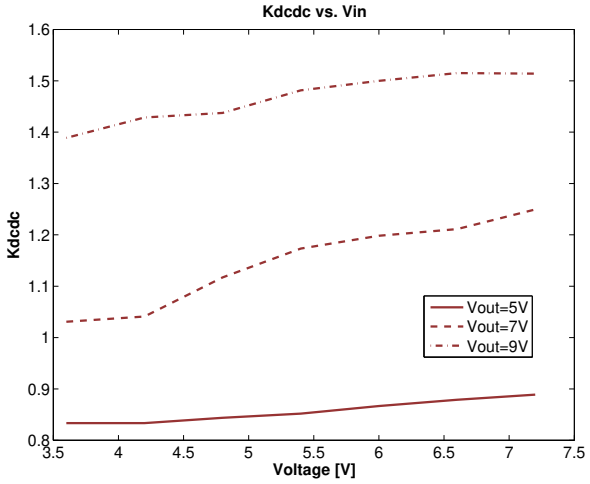


Fig. 11. K_{DCDC} for various operating conditions for the prototype converter.

$H_{PLANT}(s) = V_{OUT}(s)/d$, where d is the duty ratio of the enable signal, is given by

$$H_{PLANT}(s) = \frac{V_{OUT}}{d} = K_{DC-DC} * \frac{R_{LOAD}}{R_{LOAD}C_{OUT}s + 1}. \quad (2)$$

In (2), K_{DC-DC} is the dc converter output current under (constant) open-loop operation at a fixed input and output voltage. Values for K_{DC-DC} can be found by direct measurement or simulation of the converter power stage at different operating points V_{IN}, V_{OUT}. Figure 11 shows plots of K_{DC-DC} for the prototype converter for various operating conditions. The controller should be designed to be stable for all values of K_{DC-DC} in the operating range (Here between 0.8 A and

TABLE III
PWM CONTROLLER COMPONENT VALUES

R_1	22 kΩ
R_2	8.2 kΩ
C_2	5 pF
R_3	10 kΩ
C_3	5 pF
C_4	15 pF
R_4	470 kΩ

1.55 A). The transfer function for the duty ratio controller, including sensor gain, error amplifier/compensation gain, and PWM modulator K_{PWM}, are developed as is conventional in duty ratio control. The circuits and models in our particular prototype are as illustrated in Fig. 10.

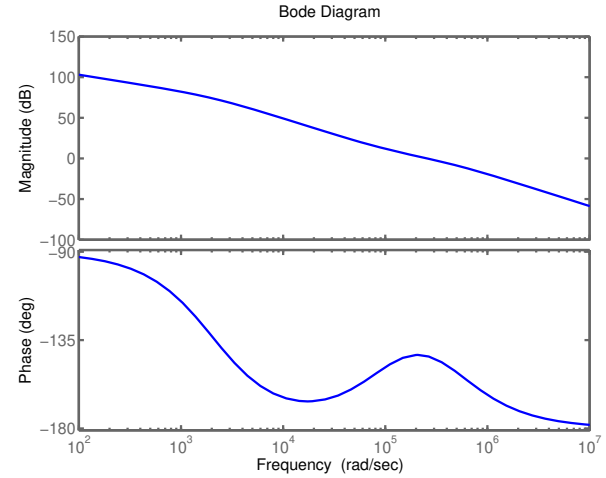
The PWM on-off control implementation utilizes a low-power Bi-CMOS PWM chip $UCC2813$. An error amplifier internal to the chip with a reference voltage of 2V is employed to implement a P-I controller. The P-I controller looks at the output voltage of the converter and integrates the error between the reference voltage and the output voltage to obtain an error voltage. The error voltage is then compared with the sawtooth voltage of the PWM chip to generate a command signal turning the converter cell on and off at a duty ratio such that the output remains regulated even as the load changes. The component values of the P-I controller are listed in Table III.

To design a stable controller across an entire operating range, the plant is modeled at its lightest load condition where the phase margin is the smallest (in this case, at the lowest input voltage and highest output voltage), using the open-loop output current and power measurements of the converter. Once the model for an open-loop converter is determined, a P-I controller can be designed using the block diagram in Fig. 10(b). In this model, K_{PWM} is a gain factor introduced by the PWM sawtooth waveform which converts an error voltage to a duty ratio (in this case, $K_{PWM} = 1/2.5$), and R_1, R_2, R_3, R_4, C_3 and C_4 are the components of the output voltage divider and the P-I controller in Fig. 10(a). The bode plot for the loop gain at $V_{OUT} = 7$ V and the step responses of V_{OUT}/I_{OUT} are shown in Fig. 12.

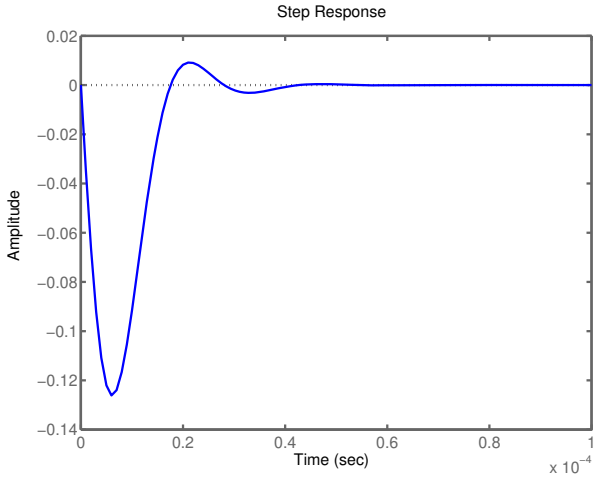
A. Fixed-Frequency PWM with Hysteresis Override

Note that the response speed illustrated in Fig. 12(b) and 12(c) is not limited by the inherent bandwidth of the plant (the power stage); instead it is limited by the bandwidth of the controller being a fraction of the PWM modulation frequency (in order to prevent feedthrough of the modulation ripple). A fixed-frequency PWM controller with hysteresis override in Fig. 13 can take advantage of the salient response speed of a hysteretic controller during load-step transient operation, while providing controlled frequency content at the converter input and output during steady-state operation. Such a controller can operate as follows:

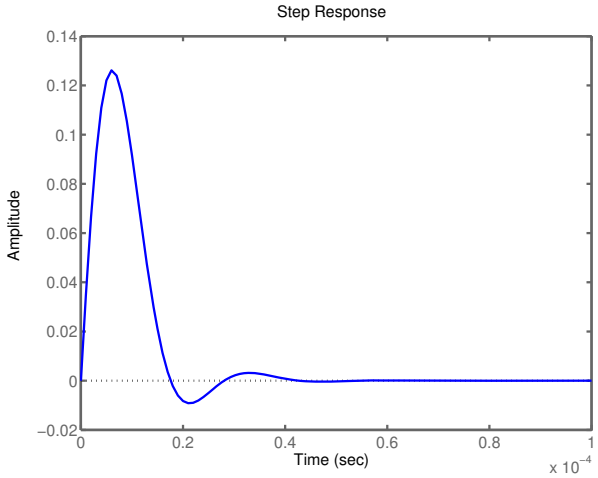
During a large load step where the transient output voltage exceeds the upper bound of a pre-determined hysteresis voltage band, the hysteretic controller output overrides the fixed-frequency PWM output, keeping the power stage off until the output voltage falls below the upper limit of the voltage band. Once the output voltage falls below the upper limit of the voltage band, the fixed-frequency PWM controller takes over and the controller operates as previously described. Similarly, during a large load step where the transient output voltage



(a) Loop gain bode plot

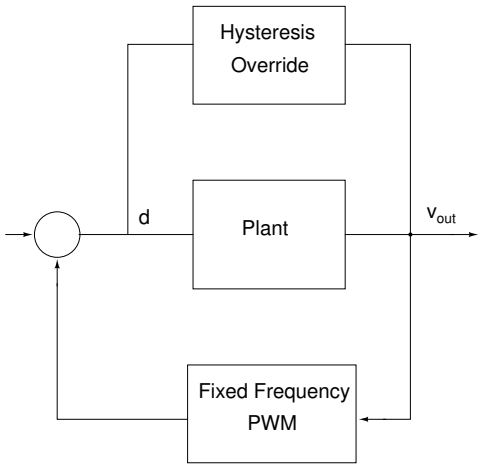


(b) Simulated 10 % to 90 % Load Step Response, ac component only.

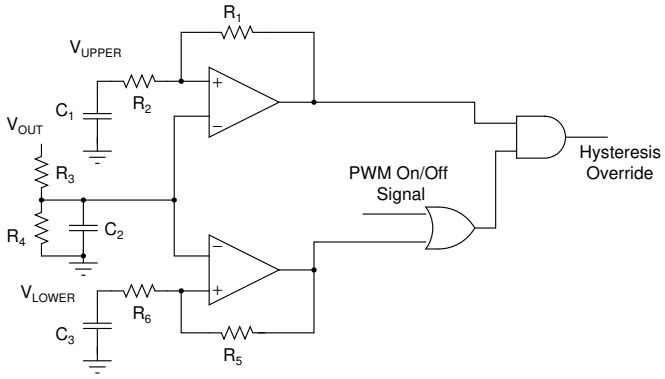


(c) Simulated 90 % to 10 % Load Step Response, ac component only.

Fig. 12. Bode plot and simulated step response for V_{OUT}/I_{OUT}.



(a) Block diagram model of the closed-loop system with a fixed-frequency PWM controller with hysteresis override



(b) Implementation of a fixed-frequency PWM controller with hysteresis override

Fig. 13. System block diagram and implementation of a fixed-frequency PWM controller with hysteresis override.

Fig. 14. Photograph of 20 MHz experimental prototype.

TABLE IV
EXPERIMENTAL DC-DC CONVERTER SPECIFICATIONS

Input Voltage Range	3.6 V - 7.2 V
Output Voltage Range	3 V - 9 V
Switching Frequency	20 MHz
Output Power	0.3 W - 3 W

TABLE V
POWER STAGE COMPONENT VALUES

L_F	22 nH
L_R	41 nH
C_{EX}	780 pF
C_{EX2}	100 pF
C_S	1270 pF
M_1	SPN1443 x 2
D_1	DSFL230L
C_{in}	0.9 μF
C_{out}	0.6 μF

drops below the pre-determined lower bound of the hysteresis voltage band, the hysteretic controller output again overrides the fixed-frequency PWM output, keeping the power stage on until the output voltage comes back above the lower limit of the hysteresis voltage band.

The fixed-frequency PWM with hysteresis override control scheme takes advantage of the small amount of energy stored in the passive components in the power stage, and combines that with the salient response speed of a hysteretic controller. This control scheme allows for faster response speed during large load-steps (as the hysteretic controller is enabled), while it keeps the frequency spectra of the input and output voltage well-defined during steady state operation and small load-step changes.

V. EXPERIMENTAL RESULTS

This section presents the design and experimental evaluation of the proposed resonant SEPIC converter. Table IV lists the converter specifications. The converter operates at 20 MHz and utilizes two commercial 30 V vertical MOSFETs in parallel.

A photograph of the prototype of a dc-dc converter, based on the topology introduced in Section II, is shown in Fig. 14. The values of the power stage components are given in Table V. Note that the capacitor C_{EX} is the external capacitance in parallel with the parasitic output capacitance of the MOSFETs, C_{OSS}. The control and gate drive circuitry is placed on the other side of the printed circuit board (not shown).

As can be seen in Table V, the largest inductor in the power stage is 41 nH, with both inductors implemented with CoilCraft Mini-Spring Series air-core inductors. The small sizes of the inductors are due both to the high operating frequency of the converter (20 MHz), and to the nature of the topology and its tuning procedure introduced in Section II.

Converter waveforms are presented in Fig. 15, which shows measured drain, gate and rectifier voltages for minimum V_{in} and maximum V_{in} at nominal V_{out}. From the experimental waveforms, the topology indeed provides good zero voltage switching characteristics. However, a degree of overlap loss due to device capacitance, C_{GD} can be observed in the design. Open-loop efficiency and power over the input voltage range are illustrated in Fig. 16, where the input voltage is swept from 3.6 V to 7.2 V, while the output voltage is kept at its nominal value, 7 V. In this open-loop efficiency measurement, a bank of Zener diodes are employed to maintain the converter's output voltage fixed at 7 V regardless of the output power level. A more complete open-loop efficiency plot taken over the entire

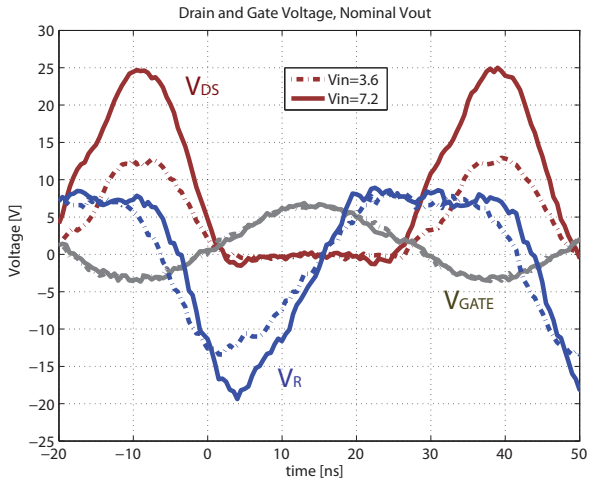


Fig. 15. Drain, rectifier and gate voltages for experimental 20 MHz converter operating with $V_{out} = 7$ V.

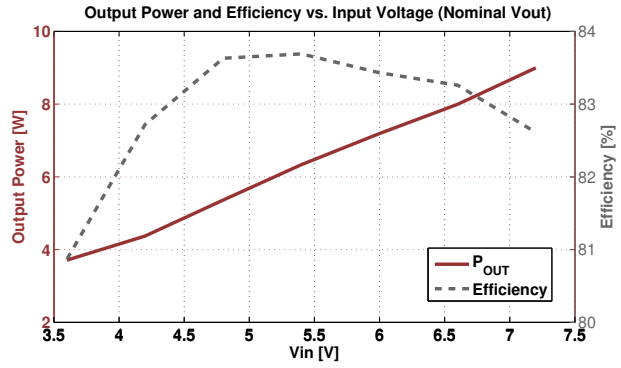


Fig. 16. Open-Loop output power and efficiency over the input range at $V_{out} = 7$ V.

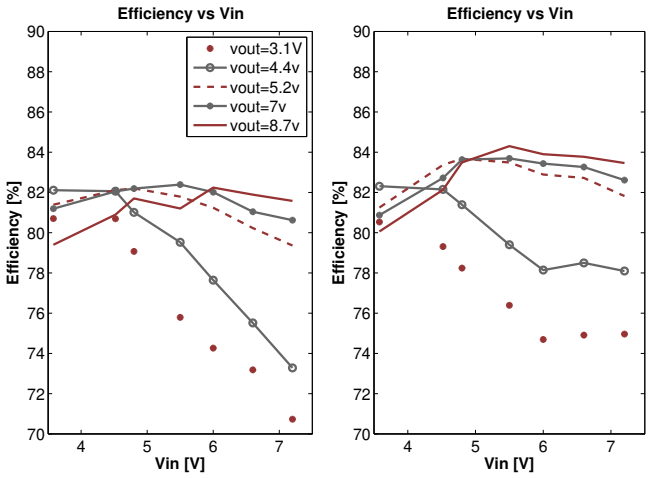


Fig. 17. Closed-loop (left) and open-loop (right) efficiency over the entire operating range.

operating range of the converter is shown in Fig. 17. It is clear from these two figures that this topology provides good efficiency across a very wide operating range and up and down voltage conversion. This and all following efficiency

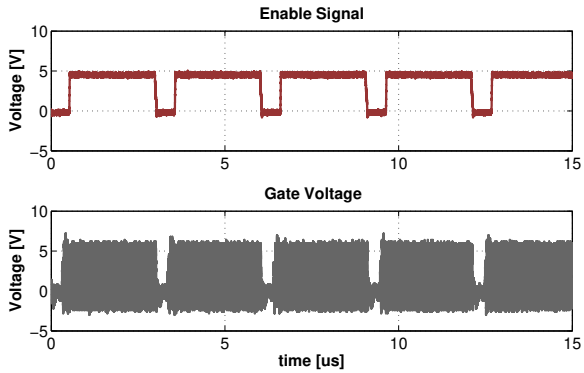


Fig. 18. Experimental controller output signal and gate drive.

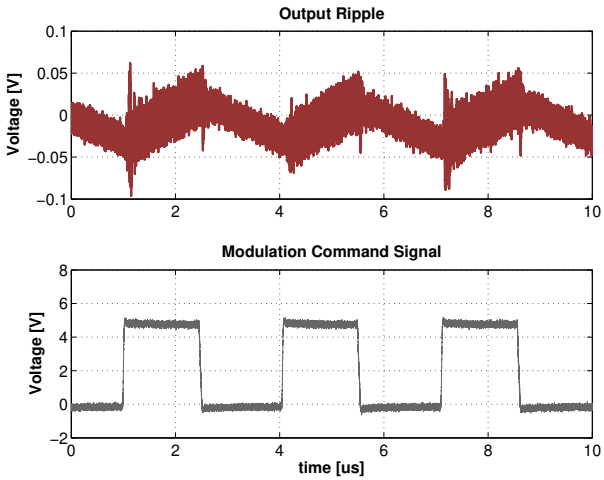
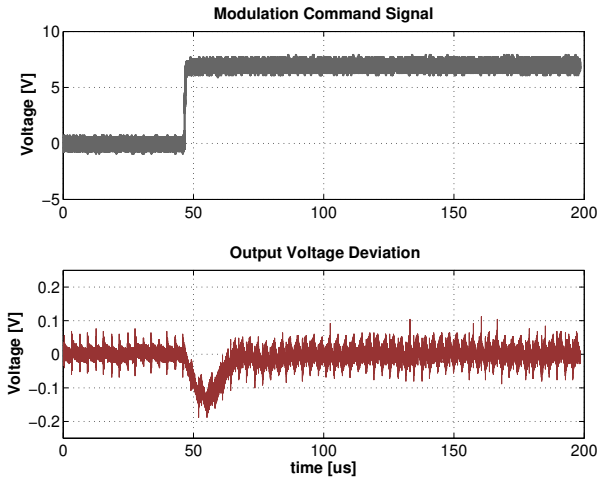


Fig. 19. Output voltage ripple during steady-state closed-loop operation at $V_{out} = 7$ V, $V_{in} = 5.2$ V, and $R_{LOAD} = 8\,\Omega$. One can see the 170 kHz ripple due to PWM on/off control. The 20 MHz "Hash" (undersampled) due to the 20 MHz switching operation when the converter is enabled can also be seen. Please note that the ripple waveforms contain ac components only.

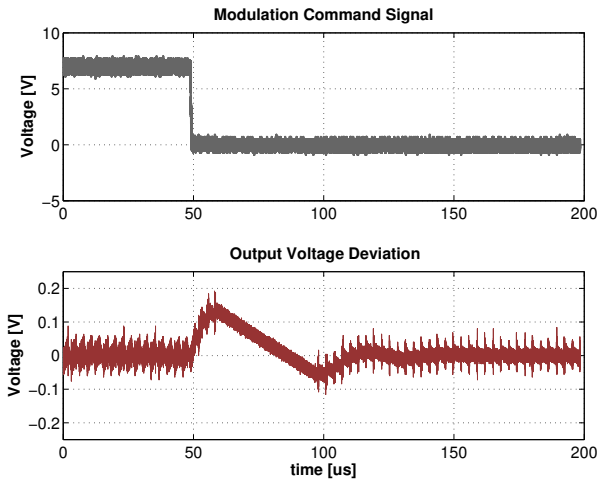
measurements include the losses of the gate driver and control circuitry.

Figure 17 also shows the efficiency under closed loop operation across the entire input and output voltage ranges for the rated 3 W output power. Ideally, when the converter is turned off, it consumes no power, and for the brief time when it is turned on, it operates in its most efficient state. In practice, there is quiescent loss in the control circuitry along with a small amount of power loss during the turn-on and turn-off transients, which explains the minor differences in efficiency under open-loop and closed-loop conditions.

The modulation frequency at which is the converter is turned on and off is 170 kHz. Figure 18 shows the gate voltage of the main switch, and illustrates how the converter is turned on and off as the output is regulated. Figure 8 shows the turn-on and turn-off transients. Figure 19 shows the output voltage ripple when the converter is regulating the output at 7.3 V. The approximately 100 mV ripple can be reduced (if so desired) by increasing the output capacitance. However, it is done at the expense of reducing the speed at which the output voltage can dynamically adjusted. The lower part of the figure shows the

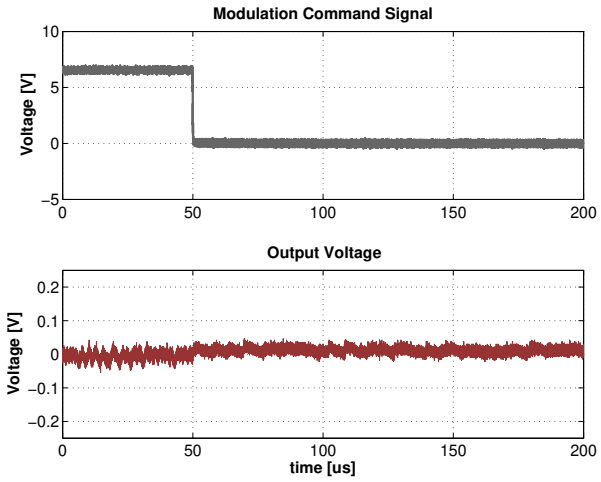


(a) 0.5 W to 3.5 W load step

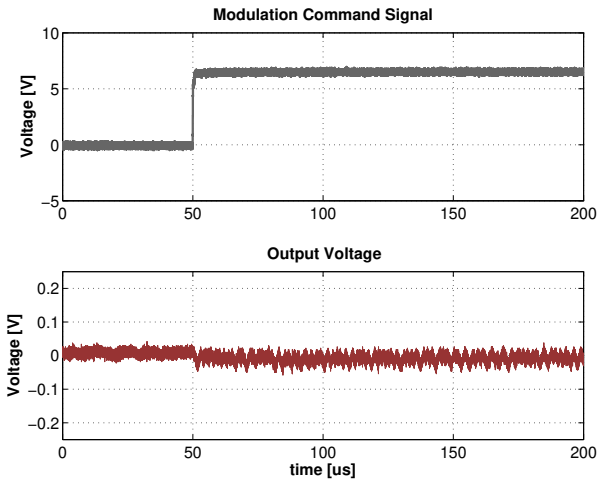


(b) 3.5 W to 0.5 W load step

Fig. 20. Experimental load step transient response with PWM controller alone. Conditions are for $V_{IN} = 4$ V and $V_{OUT,REF} = 7.3$ V.



(a) 0.5 W to 3.5 W load step



(b) 3.5 W to 0.5 W load step

Fig. 21. Experimental load step transient response with a fixed-frequency PWM controller with hysteresis override. Conditions are for $V_{IN} = 4$ V and $V_{OUT,REF} = 7.3$ V.

drain to source voltage of the main switch, and illustrate how the converter is modulated on and off as the output is regulated. It is important to note that while the modulation frequency in Fig. 18 is 170 kHz, the converter cell is operating at 20 MHz.

In conventional dc-dc converters, the total required output capacitance is determined by the allowed voltage ripple and the desired transient performance. It is often the latter condition that determines the minimum capacitance, calling for a larger capacitance than demanded by output ripple requirements alone. However, the resonant SEPIC converter, with its inherently fast transient response due to small valued inductors, does not have this problem. The output capacitor is sized solely based on the desired on/off modulation frequency and output ripple, not by transient response limitations.

In addition to the advantages in size, weight and cost realized from smaller passive components, in increase in switching frequency also leads to improved transient performance. Because of the small amount of energy stored in the passive components in each switching cycle, the converter can quickly adjust to changes in load conditions. To illustrate this, Fig. 20 shows the measured output voltage when the output power is changed from 0.5 W to 3.5 W, and from 3.5 W to 0.5 W by varying the load for a fixed-frequency PWM controller. As mentioned in the Section IV, the response speed in Fig. 20 is not limited by the inherent bandwidth of the power stage. Therefore, it can be tremendously improved by a fixed-frequency PWM controller with hysteresis override, as illustrated in Fig. 21. As can be seen by comparison of the responses in Figs. 20 and 21, the hysteresis override greatly reduces the voltage transient during a rapid load change. This salient transient response can be attributed to the small inductors and capacitors required for this topology at high frequency along with the control scheme.

VI. Conclusion

This document presents a resonant SEPIC converter suitable for extremely high frequency operation and for operating

across a wide input and output voltage range. The topology addresses several shortcomings of conventional resonant SEPIC converters through the development of topology, gate drive method and control scheme. The merits of these design methods are verified via a 20 MHz prototype with an input voltage range from 3.6 V to 7.2 V, an output voltage range of 3V to 9V and a rated output power of 3W. The converter utilizes a low-loss sinusoidal gate drive and an on-off control method modulating at fixed frequency, provides both fast transient response and good control over spectral characteristics of the input and output voltage. A hysteretic override technique is also introduced which enables the converter to reject load disturbances with a bandwidth much greater than the modulation frequency, limiting output voltage disturbances within a fixed value. This extremely rapid load disturbance rejection is enabled by the small passive component values and magnetic energy storage required. By contrast, the slew rate of the output voltage is limited by the output capacitance, which is sized by the desired modulation ripple voltage and modulation frequency. The achievable voltage slew rate is entirely appropriate for applications such as adaptive bias power supplies. As this paper has demonstrated, it is possible for resonant SEPIC converters to achieve a wide operating range, a small size and excellent transient response while maintaining good efficiency. It is hoped that these techniques will contribute to future development of low-power converters operating over wide ranges and extreme high frequencies to meet the increasing demands of modern portable electronics.

REFERENCES

[1] R. Redl, B. Molnar, and N. Sokal, "Class E resonant regulated dc/dc power converters: Analysis of operations and experimental results at 1.5 MHz," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 2, pp. 111–120, April 1986.

[2] R. Redl and N. Sokal, "A new class-E dc/dc converter family with reduced parts count: Derivation, topologies, and design considerations," in *Technical Papers of the Fourth International High Frequency Power Conversion Conference*, 1989, pp. 395–415.

[3] F. Lee, "High-frequency quasi-resonant converter technologies," in *Proceedings of the IEEE*, vol. 76, April 1988, pp. 377–390.

[4] W. Tabisz and F. Lee, "Zero-voltage-switching multiresonant technique-a novel approach to improve performance of high-frequency quasi-resonant converters," *IEEE Transactions on Power Electronics*, vol. 4, no. 4, pp. 450–458, Oct. 1989.

[5] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA: (Kluwer Academic Publishers), 2000.

[6] Y. Lee and Y. Cheng, "A 580 khz switching regulator using on-off control," *Journal of the Institution of Electronic and Radio Engineers*, vol. 57, no. 5, pp. 221–226, September/October 1987.

[7] J. Rivas, D. Jackson, O. Leitermann, A. Sagneri, Y. Han, and D. Perreault, "Design considerations for very high frequency dc-dc converters," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, 18-22 June 2006, pp. 1–11.

[8] J. Rivas, R. Wahby, J. Shafran, and D. Perreault, "New architectures for radio-frequency dc/dc power conversion," *IEEE Transactions on Power Electronics*, vol. 21, pp. 380–393, March 2006.

[9] R. C. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. I. Anderson, and D. J. Perreault, "Very high frequency resonant boost converters," in *Power Electronics Specialist Conference Proceedings*, June 2007.

[10] J. M. Rivas, "Radio frequency dc-dc power conversion," Ph.D. dissertation, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, September 2006.

[11] A. D. Sagneri, "Design of a very high frequency dc-dc boost converter," Master's thesis, Massachusetts Institute of Technology, Cambridge, MA, February 2007.

[12] J. Hu, A. D. Sagneri, J. M. Rivas, S. M. Davis, and D. J. Perreault, "High frequency resonant sepic converter with wide input and output voltage ranges," in *IEEE Power Electronics Specialist Conference Proceedings 2008*, June 2008.

[13] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Lietermann, R. Pilawa, A. Sagneri, and C. Sullivan, "Opportunity and challenges in very high frequency power conversion," in *24th Annual IEEE Applied Power Electronics Conference and Exposition, 2009. APEC 2009*.

[14] N. O. Sokal, "Class-E RF Power Amplifiers," *QEX*, pp. 9–20, Jan/Feb 2001.

[15] W. Everitt and G. Anner, *Communications Engineering*, 3rd ed. New York: (McGraw-Hill), 1956.

[16] Y. Han and D. J. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Transactions on Power Electronics*, vol. Vol. 21, No. 5, pp. pp. 1484–1491, Sept. 2006.

[17] H. Koizumi, I. M., and M. S., "Class E^2 dc/dc converter with second harmonic resonant class e inverter and class e rectifier," in *Third Annual Applied Power Electronics Conference Proceedings*, 1994, pp. 1012–1018.

[18] M. Iwadare, S. Mori, and K. Ikeda, "Even harmonic resonant class e tuned power amplifier without rf choke," in *Electronics and Communications in Japan*, vol. 79, no. 1, Jan. 1996, pp. 23–30.

[19] J. Hu, "Design of a low-voltage low-power dc-dc hf converter," Master's thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, 2008.

[20] J. R. Warren, III, K. A. Rosowski, and D. J. Perreault, "Transistor selection and design of a VHF dc-dc power converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, January 2008.

Jingying Hu (S'06) received B.S. degrees in electrical and computer engineering from the Illinois Institute of Technology, Chicago, IL, USA in 2005. She went on to receive the S.M. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA in 2007, where she is currently working toward the Ph.D. degree.

Anthony D. Sagneri (S'07) received the B.S. degree in 1999 from Rensselaer Polytechnic Institute, Troy, NY, and the S.M. degree in electrical engineering in 2007 from the Massachusetts Institute of Technology, Cambridge, where he is currently working toward the Ph.D. degree in the Laboratory of Electromagnetic and Electronic Systems.

From 1999 until 2004, he served in the U.S. Air Force. His current research interests include power electronics, resonant converters, soft-switching techniques, and semiconductor device and magnetics design for these applications.

Juan M. Rivas (S'01M'06) was born in Mexico City, Mexico. He received the B.A.Sc. degree from the Monterrey Institute of Technology, Monterrey, Mexico, and the S. M. and Sc.D. degrees from the Laboratory of Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge.

He currently works for the General Electric Company in the Electronic Power Conversion Laboratory, Niskayuna, NY. His current research interests include power electronics, RF power amplifiers, resonant converters, soft-switching topologies, and control of power converters.

Yehui Han (S'05-M'10) was born in Harbin, China. He received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, in 2000 and 2002, respectively and the Ph.D. degree from the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, in 2010.

In 2003, he was with DATEL, Inc, designing dc-dc converters. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Wisconsin-Madison, Madison, WI. His research interests are in power electronics, analog and digital circuit design, resonant converters, multilevel converters, and flexible ac transmission systems (FACTS).

Seth M. Davis

David J. Perreault (S'91M'97SM'06) received the B.S. degree from Boston University, Boston, MA, in 1989, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology (MIT), Cambridge, in 1991 and 1997, respectively.

In 1997, he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate. He became a Research Scientist in the Laboratory in 1999. In 2001, he joined the MIT Department of Electrical Engineering and Computer Science, where he is currently an Associate Professor of electrical engineering. His current research interests include design, manufacturing, and control techniques for power electronic systems and components, and their use in a wide range of applications.

Dr. Perreault received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society, an Office of Naval Research (ONR) Young Investigator Award, and the SAE Ralph R. Teetor Educational Award. He is the coauthor of two IEEE Prize Papers.