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High Frequency Substrate Technologies for the Realisation of Software Programmable Metasurfaces on PCB Hardware Platforms with Integrated Controller Nodes

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Abstract

The proposed work is performed in the framework of the FET-EU project "VISORSURF", which has undertaken research activities on the emerging concepts of metamaterials that can be software programmable and adapt their properties. In the realm of electromagnetism (EM), the field of metasurfaces (MSF) has reached significant breakthroughs in correlating the micro- or nano-structure of artificial planar materials to their end properties. MSFs exhibit physical properties not found in nature, such as negative or smaller-than-unity refraction index, allowing for EM cloaking of objects, reflection cancellation from a given surface and EM energy concentration in as-tight-as-possible spaces.

The VISORSURF main objective is the development of a hardware platform, the Hypersurface, whose electromagnetic behavior can be defined programmatically. The key enablers for this are the metasurfaces whose electromagnetic properties depend on their internal structure. The Hypersurface hardware platform will be a 4-layer build-up of high frequency PCB substrate materials and will merge the metasurfaces with custom electronic controller nodes at the bottom of the PCB hardware platform. These electronic controllers build a nanonetwork which receives external programmatic commands and alters the metasurface structure, yielding a desired electromagnetic behavior for the Hypersurface platform.

This paper will elaborate on how large scale PCB technologies are deployed for the economical manufacturing of the 4-layer Hypersurface PCB hardware platform with a size of 9"x12", having copper metasurface patches on the top of the board and the electronic controllers as 2mmx2mm WLCSP chips at 400µm pitch assembled at the bottom of the platform. The PCB platform designs have stemmed from EM modeling iterations of the whole stack of high frequency laminates taking into account also the electronic features of the controller nodes. The manufacturing processes for the realization of the selected PCB architectures will be discussed in detail.

Key words: Metasurfaces, metamaterials, software defined materials, High frequency substrates.

1. Introduction

Metasurfaces (MSs), the two dimensional versions of metamaterials, are ultrathin periodic structures with designed, subwavelength building blocks enabling exotic functionalities [1-2]. The building blocks can consist of metallic, dielectric, semiconducting, and 2D material inclusions. Tunable metasurfaces can be realized by modifying the properties of the meta-atoms via an external stimulus, leading to adjustable and, in some cases, reconfigurable functions. The available tuning schemes can be classified as "global" or "local" depending on the ability to tune the unit cells collectively or independently. Global control of the unit cells can, for example, enable tunable perfect absorption, whereas local control can provide more advanced functionalities such as wavefront manipulation, steering or focusing [3,4, 10-11]. An efficient control mechanism naturally suited to a *local* tuning scheme is that of *voltage-controlled* lumped electronic elements incorporated inside the meta-atom to provide control over the MS properties [5,6, 10-11]. In the framework of the VISORSURF project this is accomplished by specifically-designed integrated circuits (chips), embedded in the meta-atoms. The control of the circuits can be software-driven and the behavior of the metasurface can be

defined programmatically; this is the concept of the HyperSurface (HFS) [7]. In addition, the controllers can be nano-networked [7-9] enabling the broad vision of smart devices in the emerging Internet of Things paradigm. In this work, we present the concept of the Hypersurfaces with a focus on their electromagnetic aspects [10-11].

2. The Hypersurface Concept of The Visorsurf project

The functional and physical architecture of the Hypersurface tile is presented in Fig. 1(a) and it consists of a metasurface layer, an intra-tile control layer and a tile gateway controller. This paper focuses on the metasurface layer which realizes the electromagnetic functionalities. In the overall concept of the HFSs, there is a switch fabric design for operation in the microwave (GHz) regime.

The unit cell of the switch fabric is presented in Fig. 1(b). It consists of four copper patches (size is in millimeter range) residing on a low-loss dielectric substrate backed by a copper plate. A chip is attached in each unit cell, lying behind the copper plate, shown in Fig. 1(c), and its physical dimensions are also subwavelength. The chips are interconnected by means of communication tracks. The four patches are connected to the RF ports of the chip by means of through vias. When microwave radiation impinges on the chip-loaded unit cell, it induces local currents in the patches and the metallic substrate; in turn, the induced currents act as secondary electromagnetic sources modifying the scattered field which leads to the desired operation, when the aggregate effect of all unit cells of the metasurface is accounted for. Consequently, for the modification of the metasurface response, one needs to adjust dynamically the complex-valued surface impedance in each unit cell. This is achieved with the controller chip [Fig. 1(c)], which is judiciously placed behind the backplate in order to minimize interference with the impinging electromagnetic wave. By controlling the resistive and reactive contributions in each chip we can demonstrate an angle-tunable perfect absorber that can operate inside the 4.5-5.5 GHz range, and more advanced functionalities of wavefront manipulation such as anomalous reflection [10-11]. This paper describes in detail the manucturability of such large metasurface panels based on standard industrial PCB processes conducted in the Substrate line of Fraunhofer IZM.

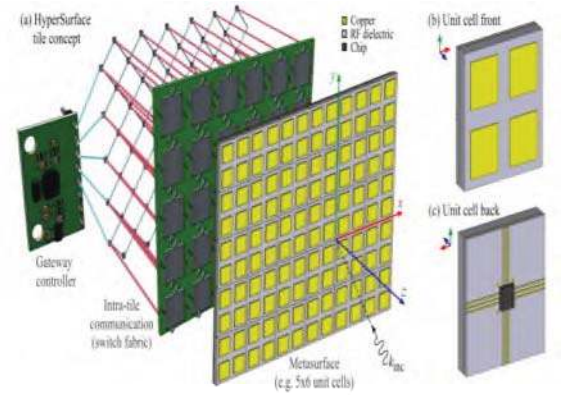
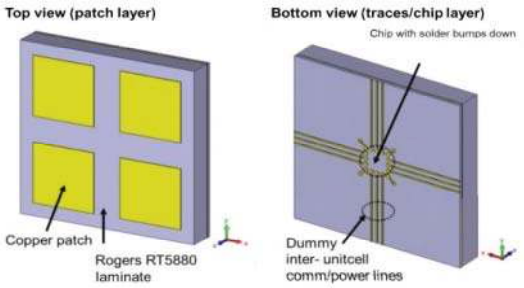


Figure 1:(a) The HyperSurface tile. The switch state configuration setup provides the desired function. A controller intra-network communicates the relevant commands and the inter-tile and external communication are handled by standard gateway hardware, such as an FPGA. Unit cell of the metasurface: (b) front side with periodic square 2x2 patches pattern and (c) back side with controller chip (dark grey box) and communication lines.

3. Manufacturing feasibility study on 3-layer HSF substrate

This Section presents the first manufacturing results of a 3-layer HSF substrate using a stack of a HF Rogers laminate material and a high-Tg FR4 material. The first 3-layer HSF substrate was constituted of a thick HF laminate based on Rogers RT5880 laminate and an underlying conventional high-Tg PCB prepreg. Figure 2 shows a perspective of a single unit cell from its top side which is the patch layer and its bottom side which is the chip layer. The copper patch is 4.2mm scquare; the space between them is 0.8mm. The HSF substrate consisted of 8 single unit cells with a final size of 96mmx96mm, and is shown in the bottom of Figure 2.



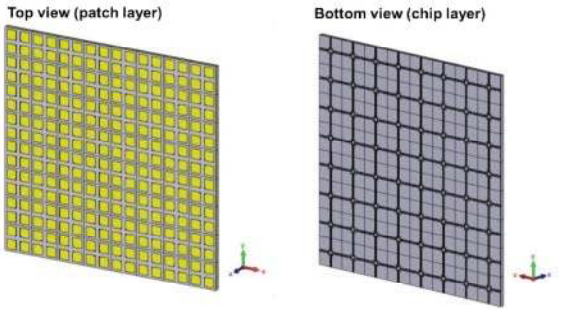


Figure 2: Perspective of a single unit cell and the whole HSF consisted of 8 single unit cells (96mmx96mm).

The geometrical design of the 3-layer board is shown in Figure 3 where the copper layer (1 st layer), the ground backplane layer (2nd layer) and the chip/copper trace layer (3rd layer) can be distinguished. The copper layers were 35µm thick and the high frequency RT5880 laminate was 1.575 mm whereas the underlying Hitachi 679FGS prepreg was 0.254mm. The whole thickness of the HSF substrate was targeted to be 1.934mm. There were 4 through vias from the patch layer to the chip layer which were mechanically drilled and had a diameter of 300µm.

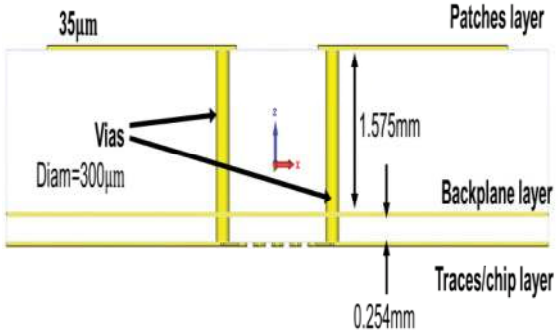


Figure 3: Geometrical cross section of the 3-layer HSF stack-up. Total estimated thickness is 1.934mm.

After the drilling of the vias, a typical permanganate desmear process was followed to clean the via from rest of the RT5880 material. However, such desmear process is not appropriate for RT5880 material and the copper has not really stuck to the via walls. No copper electroplating has taken place in the through vias.

Although repeated desmear processes were run with various parameters, the vias could not be cleaned efficiently and could not be electroplated at all. Therefore, the recommended process for Teflon based laminates was followed which is a plasma process. After 20 min plasma desmear, the through vias were cleaned efficiently and copper electroplating had been successful. Figure 4 shows cross sections of the 3-layer HSF after plasma desmear and electroplating. The copper wall thickness was increased to 20µm as shown in Figure 4. Figure 5 shows the corresponding X-Ray from the 3-layer HSF substrate from the chip layer with the vias filled with copper (dark contrast).

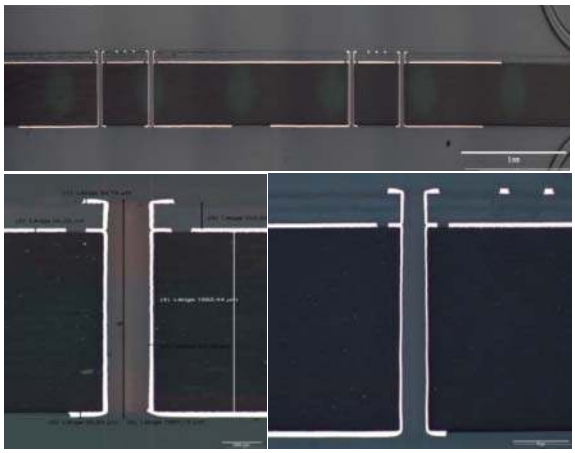


Figure 4: Cross-sections of the 3-layer HSF board with the bottom RT5880 laminate layer and vias filled with copper. Vias were cleaned with plasma desmear.

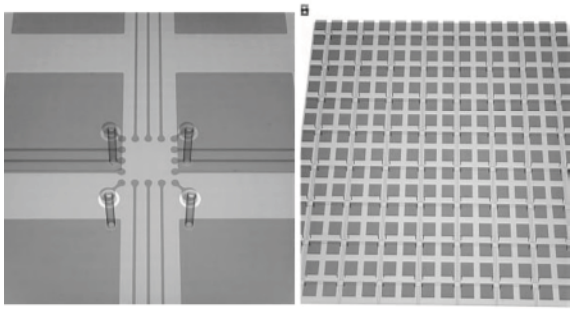


Figure 5: X-Ray of the 3-layer HSF stack-up from the chip layer side view. The Chip and the 4 vias can be seen filled with copper (dark contrast) due to used plasma desmear processes in the RT5880 laminate. On the right side, a X-Ray perspective of the whole HSF substrate (96mmx96mm) is provided from the chip side.

After structuring the first layer (patch layer) and the third layer (chip layer), 5µm Ni/80nm Au was applied on both layers whereas solder mask was also coated on the chip layer. Figure 6 shows pictures of the copper patches and the chip bottom side.

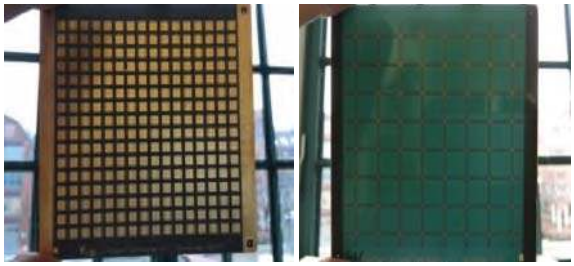


Figure 6: 3-layer HSF substrate 96mmx96mm in size.

The results provide ample evidence that the processing of RT5880 Teflon based laminate is quite challenging with conventional PCB processes and other alternative processes like plasma desmear should be employed, raising the cost of the process significantly. Furthermore, due to usage of different prepreg and laminate materials with respect to their thermal expansion coefficient, the 3-layer HSF board has shown a warpage of about 2mm, making the assembly of the controller chips on the third layer quite challenging. For these reasons, it was decided to deploy the Megtron 7N family of materials which are available both as laminates and prepregs. That would ensure the usage of uniform materials and the elimination of warpage at large production panels of 9"x12" (22cmx30cm) or 12"x12" (30cmx30cm) during the course of the project.

4. Manufacturing of 4-layer HSF substrate

After the experience gained in the feasibility studies with the 3-layer stack and having evaluated the pros and cons of employing the Rogers RT5880 Teflon based material, the Consortium decided to switch to Megtron 7N materials which could become readily available both as prepregs and laminates and could be potentially processed with conventional PCB processes. The Megtron 7N materials were available as R-5785(N) laminates with a thickness of d_1:750µm and d_2: 100µm and as prepreg R-5680(N) with a glass fiber of type 2116 and a thickness of 100µm. It was decided to build a symmetric and a slightly asymmetric stack-up to evaluate the final warpage effect on a 9"x12" board. The actual PCB process sequence is not differentiated whether a symmetric or asymmetric stack up is chosen.

○ *Symmetric and asymmetric laminate designs for 4-layer substrate*

Figure 7 shows the symmetric and asymmetric stack up next to each other for better comparison. The only slight difference between the two designs are the missing laminate (d_2) and a prepreg (t_1) on top of the asymmetric design which makes it eventually slightly thinner than the symmetric one. Figure 7 shows the stack-ups used and the main vias for interconnectivity among layers; namely the L2-L3 and L1-L4 through vias as well the L4-L3 blind vias.

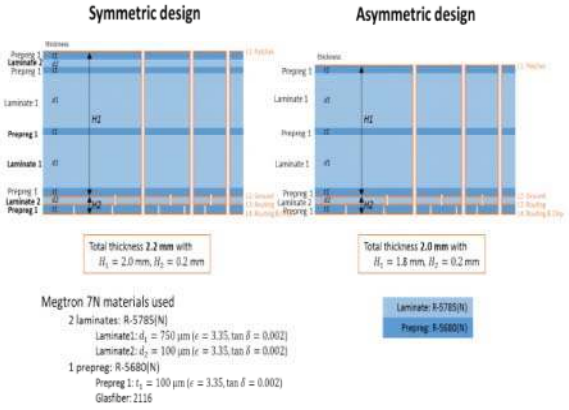


Figure 7: Symmetric and asymmetric stack-ups in comparison. Megtron 7N materials are being used.

○ *Process developments and flow for 4-layer substrate*

The process flow was decided based on the design requirements and especially the fine line L/S for the chip layer where a thin copper should exist at the end of the electroplating process so as to achieve the fine L/S under the chip area. Figure 8 provides the process flow and some dimensional via details.

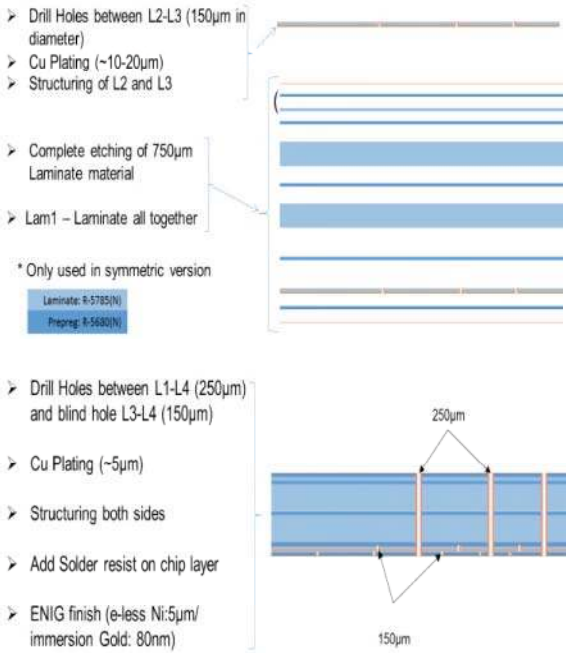


Figure 8: Process flow for 4-layer HSF substrate.

○ *Manufacturing process results and challenges*

The manufacturing of the 4-layer HSF substrate provided the first processing experience with Megtron 7N materials and yielded very good results and revealed the processing challenges that

need further developments before the launch of the next HSF substrates. Figure 9 shows a cross section of the symmetric 4-layer substrate after final processing. The thicknesses of the symmetric and asymmetric are 2.4 mm and 2.2 mm, respectively. Both values are 200µm higher than the estimated ones, mainly attributed to deviation in prepreg and lamination thicknesses in the stack compared to nominal ones and from slightly higher copper thicknesses after electroplating on the copper layers.

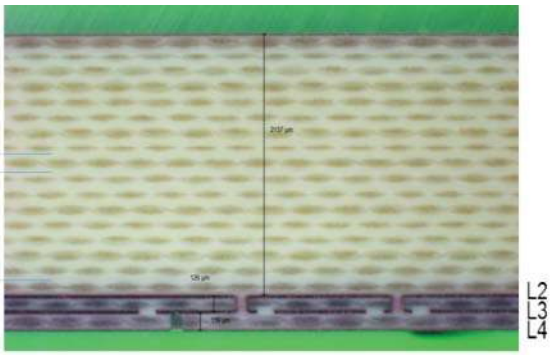
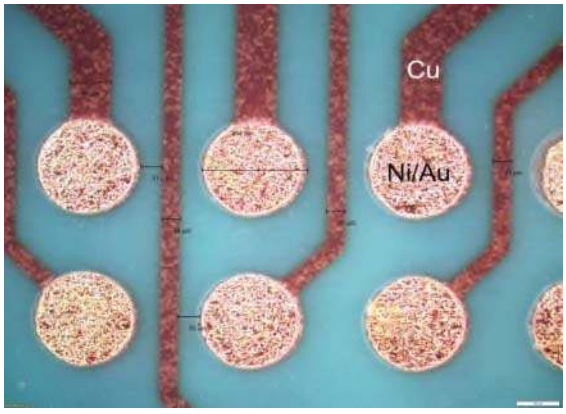


Figure 9: Cross section of the 4-layer stack.

The major challenges for the 4-layer HSF substrate are the fine line structuring of the bottom chip layer, the opening of the L4-L3 blind vias and the electroplating of all vias. As shown in Figure 10, very fine L/S of 45µm/55µm was successful with a copper thickness of 15µm. The application of solder resist and the deposition of 5µm Ni/80nm Au metallisation is also shown.

Figure 10 shows on the top the chip position where 45µm/55µm Line/Spacing was achieved and at the bottom the L3-L4 blind vias and the structuring around it. A 100µm line was structured. The results provide ample evidence that such fine copper structuring especially under the chip area is feasible.



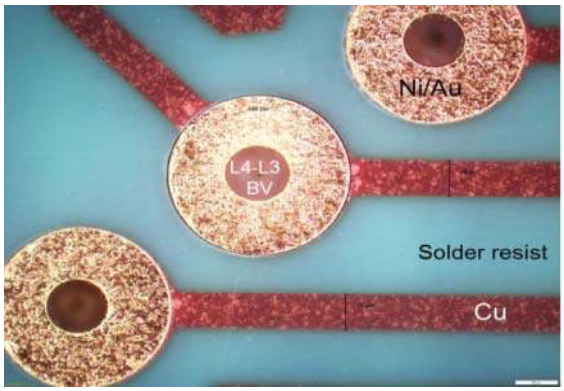


Figure 10: Bottom layer of HSF board at chip position. Fine line structures of 45µm/55µm L/S achieved. Structured bottom layer in proximity to L3-L4 blind vias.

Figure 11 shows X-Ray pictures of the 4-layer substrate where the copper filling of the L1-L4 vias, the L2-L3 vias and L4-L3 vias is witnessed with dark contrast. Via electroplating is successful.

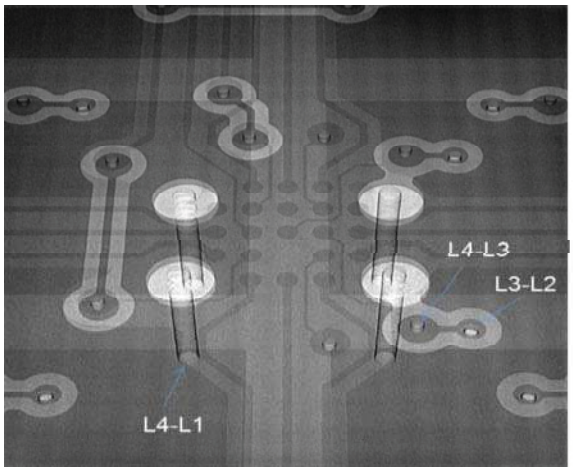


Figure 11: X-Ray of the 4-layer substrate. The dark contrast in all vias comes from the copper coating in the vias.

The through vias L4-L1 were successfully electroplated, as shown in Figure 12. It can be seen that inside the via 23µm were deposited and on the L1 and L4 layers the copper ring thickness was about 40µm and away from the ring the copper remained at about 11µm which is the ideal thickness for L1, L4 fine line structuring.

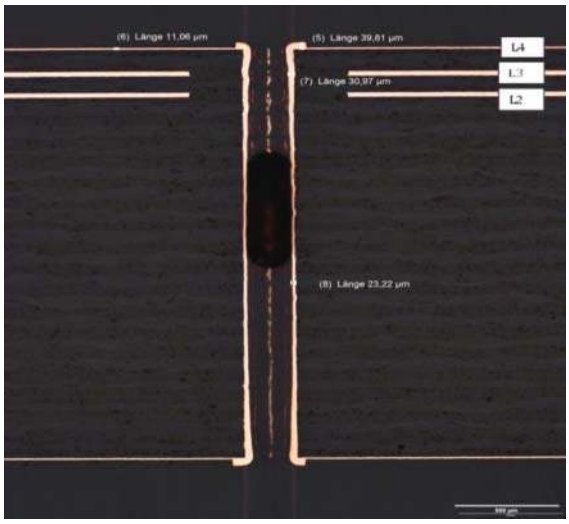


Figure 12: L4-L3-L2-L1 copper layers in a drilled through via of 250µm. Reinforced copper filling to achieve about 23µm in the via.

The blind vias L4-L3 were tried with the pico UV laser to reopen the blind vias which were initially opened by mechanical drilling. Some of the L4-L3 vias could not be efficiently opened by mechanical drilling. Few microns, around 10µm, were remaining to touch the L3 copper pad. That would be an ad-hoc solution for the boards, and mechanical drilling of all vias would be in any case preferable as a quick and economical industrial process. The laser was used to re-open and overshoot the blind vias and subsequently desmear and copper electroplating was performed. The results were very successful using the laser for the blind vias and the drilled board. In turn, the board was successfully electrically tested for continuity. Figure 13 shows the blind via, 150µm in diameter, opened with the UV laser to be also copper filled.

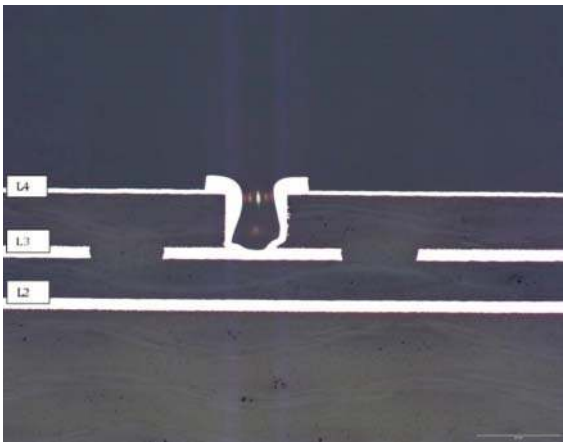


Figure 13: Blind via (L4-L3), 150µm in diameter, opened by UV laser and then copper coated.

The laser technology looks promising to solve the problem of drilled L4-L3 blind vias and is also compatible with filled Megtron 7N materials.

Figure 14 shows the 4-layer HSF substrate finished with solder resist on the bottom side. The warpage of the board, due to usage of uniform Megtron 7N materials, was less than 100µm, much smaller than the warpage of the 3-layer RT5880 board and is considered minimal from EM considerations.

The resultant HSF prototype has a net area of 6.2"x9.4" and containts 384 unit cells. It is electrically functionable and proves that the 4-layer HSF is manufacturable.

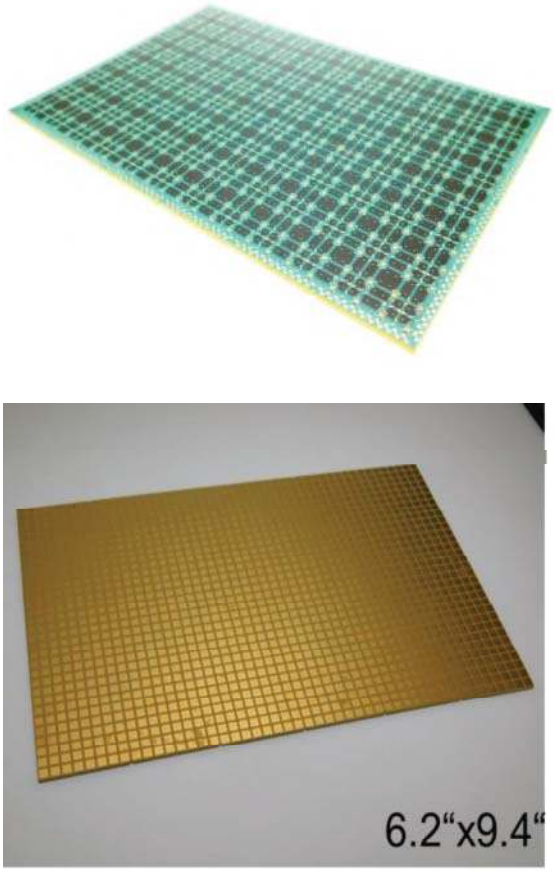


Figure 14: Bottom side (chip layer) and HSF unit cell area with Ni/Au metallization (top layer) of the 4-layer HSF substrate (net area of 6.2"x9.4", 384 unit cells)

Conclusions

This paper has presented the concept of Hypersurfaces, i.e., the approach of project VISORSURF to software-driven metasurfaces whose complex surface impedance can be locally modified with a set of programmable commands. The control is enabled by a network of voltage-driven electronic chips; they provide variable resistance and reactance values that modify the complex surface impedance of the metasurface in a

local or a global manner. This paper also provides the first manufactured Hypersurfaces on panels employing industrial PCB processes. Hypersurfaces were made on a 3-layer and a 4-layer PCB consustruction which will be finally the HSF design for the project. The 3-layer substrate was made of a RT5880 Teflon laminate outstanding for its HF properties, but it was difficult to process with conventional chemical desmear processes and therefore the electroplating did not work. The usage of plasma desmear has solved the problem. The 3-layer HSF substrate has shown high warpage due to usage of non-uniform laminates. Due to warpage and processability problems, it was decided to use Megtron 7N materials available as laminates and prepregs. A first version of the VISORSURF 4-layer substrate is already manufactured. Very fine structuring of 45μm/55μm L/S was successfully demonstrated at the chip level. Through vias were also successfully drilled and copper coated. Drilling of blind vias was not consistent and the results were not reliable. As a solution to solve the problem, pico UV laser has been employed successfully for the blind vias which were also copper coated. The warpage with the usage of uniform Megtron 7N materials remained under 100μm. Panels of 9"x12" were manufactured with a net area of 6.2"x9.4", consisted of 384 unit cells. The 4-layer HSF design is slightly modified and will be manufactured again in the next 2 months in the final size of 300mmx300mm (12"x12").

Acknowledgements

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