Lawrence Berkeley National Laboratory
Recent Work

Title
High-gain monolithic 3D CMOS inverter using layered semiconductors

Permalink
https://escholarship.org/uc/item/4fb626pb

Journal
Applied Physics Letters, 111(22)

ISSN
0003-6951

Authors
Sachid, AB
Desai, SB
Javey, A
et al.

Publication Date
2017-11-27

DOI
10.1063/1.5004669

Peer reviewed

eScholarship.org Powered by the California Digital Library
University of California

High-Gain Monolithic 3D CMOS Inverter using Layered Semiconductors

Angada B. Sachid, Sujay B. Desai, Ali Javey, Chenming Hu

Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA

We experimentally demonstrate a monolithic 3D integrated complementary metal oxide semiconductor (CMOS) inverter using layered transition metal dichalcogenide (TMD) semiconductor N- (NMOS) and P-channel (PMOS) MOSFETs, which are sequentially integrated on two levels. The two devices share a common gate. Molybdenum disulphide and tungsten diselenide are used as channel materials for NMOS and PMOS, respectively, with ON-to-OFF current ratio (I_{ON}/I_{OFF}) greater than 10^6, and electron and hole mobility of 37 and 236 cm^2/Vs, respectively. The voltage gain of the monolithic 3D inverter is about 45 V/V at supply voltage of 1.5 V and gate length of 1 µm. This is the highest reported gain at the smallest gate length and lowest supply voltage for any 3D integrated CMOS inverter using any layered semiconductor.

Device scaling has been essential to increase integration density in semiconductor circuits and systems with the accompanied benefits of higher speed and lower power dissipation [1]. With scaling, several second order effects like variability, parasitic resistance, and parasitic device and interconnect capacitance are limiting the performance of the devices, circuits and systems [2]. Monolithic 3-dimensional (3D) integration in which active device layers are sequentially fabricated can improve the circuit and system performance by reducing the average interconnect length and capacitance, thereby increasing the circuit speed and decreasing power dissipation [3]. 3D integration also enables the integration of heterogeneous active materials. To this effect, monolithic 3D integration of logic circuits, memory and sensors were demonstrated. Layered transition metal dichalcogenides (TMD) like molybdenum disulphide (MoS_2), tungsten diselenide (WSe_2) and so on show promising electronic and opto-electronic properties [4]. TMDs allow precise thickness control down to a monolayer thickness (less than a nanometer), which could potentially solve an important problem in scaled devices, i.e. variation in channel thickness in ultra-thin body devices [5]. Many of the TMD materials like MoS_2 and WSe_2 have a lower dielectric constant, which can reduce the drain-to-channel coupling and hence improve the short-channel performance of highly scaled devices [6]. The relative dielectric constant is ~10.7 for bulk and reduces to ~3.4 for monolayer thickness of MoS_2. The in-plane and out-of-plane dielectric constants of bulk MoS_2 are 7.43 and 15.4, respectively, and for monolayer MoS_2, they are 1.63 and 7.36, respectively [7]. Transistors using MoS_2 and WSe_2 have shown low mobility degradation with gate-to-channel electric field even at monolayer channel thickness [8-10]. Field-effect hole mobility as high as 300 cm^2/Vs was reported for monolayer WSe_2 MOSFET [10]. Hence, monolithic 3D integration using TMDs is interesting for further scaling.

In the planar complementary metal oxide semiconductor (CMOS) static logic gates, the NMOS and the PMOS transistors are placed on the same plane. The gate, source and drain electrodes are connected appropriately to form the inverter circuit as shown in Fig. 1(a). It can be seen that a pair of NMOS and PMOS devices are present in the circuit and electrically they share the same gate electrode. A typical layout for the inverter is shown in Fig. 1(b). The NMOS and the PMOS share the gate electrode. In many circuits like NAND, NOR, XOR, XNOR etc., the source and drain electrodes cannot always be shared, and must be electrically isolated in the generalized device structure as shown in Fig. 1(c). This type of shared gate 3D architecture was explored for silicon MOSFETs and FinFETs, and TMDs [11,12]. To date, the only monolithic 3D integration using TMDs showed a CMOS inverter voltage gain ($\Delta V_{OUT}/\Delta V_{IN}$) of about 10 V/V at supply voltage (V_{DD}) of 3 V [11]. In comparison to [11], in

this work we have added forming gas anneal, which is used as a cleaning step after the transfer of WSe_2. Forming gas anneal was used to reduce the output conductance of the WSe_2 PMOS device and hence improve the voltage gain of the CMOS inverter. In this work, we report a high-gain monolithic 3D integrated common-gate CMOS inverter using MoS_2 as NMOS and WSe_2 as PMOS with a peak switching gain of about 45 V/V at V_{DD} = 1.5 V, which is the highest reported gain at the smallest gate length and the lowest supply voltage for any reported 3D integrated CMOS inverter using any channel material.

Device fabrication was carried out on p+ doped silicon substrate with 260 nm of silicon dioxide (SiO_2). MoS_2 and WSe_2 flakes were transferred onto the substrate using mechanical exfoliation method. Flakes with 3 nm to 6 nm thickness were chosen for further device fabrication. The chosen MoS_2 flakes were etched into rectangular shapes using xenon difluoride (XeF_2) gas [13]. 40 nm of nickel (Ni) was evaporated and lifted-off to form the source/drain contacts to MoS_2 (Fig. 2(a)). 1 nm of SiO_x was evaporated as the seeding layer and 20 nm zirconium dioxide (ZrO_2) deposited using atomic layer deposition (ALD) at 110 ºC acts as the high-κ gate oxide (Fig. 2(b)). Fig. 2(c) shows the first layer MoS_2 MOSFET with 40 nm Ni metal common gate for the MoS_2 N-MOSFET in the first layer and the WSe_2 P-MOSFET that will be formed on top of the first layer. Next, 20 nm of ZrO_2 was deposited at 110 ºC using ALD (Fig. 2(d)). WSe_2 flake was transferred on top of the gate dielectric using a pick-and-place transfer method (Fig. 2(e)) [8]. The flake was etched into a rectangular shape using XeF_2 gas. At this stage, forming gas anneal was performed at 120 ºC for 30 minutes. Forming gas anneal is known to remove organic residues [14]. Forming gas anneal helps to clean the surface of WSe_2. 10 nm of platinum (Pt) and 30 nm of gold (Au) was evaporated and lifted-off to form the S/D contacts to WSe_2. Fig. 2(g) shows the device after the gate metal formation. Fig. 2(h) shows the final device after S/D contacts are formed on WSe_2.

Fig. 3 and Fig. 4 show the I_D–V_G and I_D–V_D characteristics of representative MoS_2 NMOS and WSe_2 PMOS devices, respectively. The threshold voltage (V_T) was extracted using constant current method with a current reference of 10^{-7} A/µm. For the MoS_2 NMOS, V_T was extracted to as -0.56 V. The drain current at V_D = 1 V and V_G–V_T = 1 V is about 10 µA/µm. The I_{ON}/I_{OFF} ratio is over 10^6. For the WSe_2 PMOS, V_T, drain current at V_D = -1 V and $|V_G–V_T|$ = 1 V, and I_{ON}/I_{OFF} ratio are about -1.48 V, 50 µA/µm, and 10^7, respectively. Electron field-effect mobility for MoS_2 was extracted as 37 cm^2/Vs and hole field-effect mobility for WSe_2 was 236 cm^2/Vs, which are commensurate with those reported in literature [8-10,15]. Contact resistance of MoS_2 MOSFET is 1.45 kΩ-µm and that for WSe_2 MOSFET is 1.04 kΩ-µm on each side. The peak transconductance (g_m) for MoS_2 and WSe_2 MOSFETs is about 15 µS/µm and 42

μS/μm, respectively. The devices show excellent output saturation. The output conductance (g_{ds}) at $|V_G–V_T|$ = 1 V for MoS_2 and WSe_2 MOSFETs is less than 1 nS/μm each. In [11], the output conductance of the reported WSe_2 PMOS device was about 5 μS/μm. Forming gas anneal step that was added after the transfer of WSe_2 helped to obtain a cleaner surface and improved the output conductance. The voltage gain for a CMOS inverter is $(g_{mn}+g_{mp})/(r_{on}||r_{op})$, where r_o is the output resistance of the device and the subscripts *n* and *p* refer to the NMOS and PMOS devices, respectively [16]. High g_m and r_o (=1/ g_{ds}) are required to achieve high switching voltage gain in a CMOS inverter. Fig. 5 shows the voltage transfer characteristics and peak gain of a representative monolithic 3D integrated CMOS inverter. Highest peak gain of about 45 V/V is observed at V_{DD} = 1.5 V and L_G = 1 μm, which is the highest gain reported at the smallest gate length and lowest supply voltage for a monolithic 3D CMOS inverter using any channel material. To use an inverter in a circuit, switching must be achieved between 0 and V_{DD}, preferably at around $V_{DD}/2$. The inverter shown in Fig. 5 does not switch between 0 and V_{DD} as the V_T of NMOS is negative. Hence, the noise margins for the inverter cannot be calculated. Methods like gate work function engineering [17], channel doping [9,16,18] and local back biasing [11,19] can be used to achieve the correct V_T for NMOS. Fig. 6 shows the impact of substrate back-biasing (V_B) on the performance of MoS_2 NMOS and inverter. By applying a more negative back bias, the V_T of the MoS_2 NMOS increases and becomes less negative. The V_T changes from -1.32 V to -0.45 V when the back bias is changed from -50 V to -70 V, respectively. The back-bias-coefficient ($\gamma = \delta V_T/\delta V_B = C_{oxb}/C_{oxf} = t_{oxf}/t_{oxb}$) is about 44 mV/V, where the subscripts *oxf* and *oxb* refer to the front and back oxides, respectively [20]. The low γ is due to the thick SiO_2 layer and can be increased by decreasing the thickness of the SiO_2 layer. Substrate back bias shifts the switching point (V_{IN} at $V_{OUT} = V_{DD}/2$) of the inverter to more positive values of V_{IN} as the V_T of NMOS increases (Fig. 6(b)). The switching point shifts by about 200 mV positive when the back bias changes from -50 V to -70 V. Voltage gain increases with increase in RBB (Fig. 6(c)). The voltage gains are 26 V/V, 31 V/V and 45 V/V at V_B = -50 V, -60 V and -70 V, respectively. This shows that MoS_2 NMOS with positive V_T can further improve the voltage gain of the monolithic 3D CMOS inverter. The inverter voltage gain is benchmarked against the other reported implementations of planar and 3D CMOS inverters [11,15,16,19,21,22]. Among all the reported monolithic 3D CMOS inverters using any channel materials, this work shows the highest voltage gain of 45 V/V, obtained at V_{DD} = 1.5 V and L_G = 1 μm (Fig. 7). Previously reported implementation of MoS_2-WSe_2 monolithic 3D CMOS inverter showed a voltage gain of 10 V/V at V_{DD} = 3 V [11]. Monolithic 3D CMOS inverter using InAs (NMOS) / Ge (PMOS) showed voltage gain of 45 V/V at V_{DD} = 4 V and L_G = 1.5 μm [23]. CNT-based 3D CMOS inverter showed a gain of about 8 V/V at V_{DD} = 5 V [22]. The gain of the

inverter increases with smaller channel length modulation parameter, λ, which is inversely proportional to the gate length (L_G). CMOS inverters with longer L_G will show higher gain. Hence, this work shows that highest gain at the smallest gate length for a 3D CMOS inverter using any channel material.

Monolithic 3D integration is essential to increase the integration density accompanied with higher speed and lower power dissipation. We demonstrate monolithic 3D integrated CMOS inverter using layered transition metal dichalcogenides. For a monolithic 3D CMOS inverter using any layered semiconductor, we report the highest voltage gain of about 45 V/V, which is achieved at a supply voltage of 1.5 V and gate length of 1 µm.

This work was funded by Applied Materials, Inc. and Entegris, Inc. through the I-RiCE program.

Figure Captions

Fig. 1. (a) Planar implementation of CMOS inverter. (b) Layout of a planar CMOS inverter. (c) Monolithic 3D CMOS inverter with common gate and electrically-isolated source/drain electrodes.

Fig. 2. Device fabrication flow: (a) MoS_2 flake (thickness = 3.5 nm) on Si/SiO_2 substrate after source/drain Ni contacts; (b) after ZrO_2 deposition using ALD; (c) Ni top gate is formed; (d) ZrO_2 is deposited using ALD; (e) WSe_2 flake (thickness = 2.8 nm) is placed on the gate stack using dry transfer; and (f) Pt/Au contacts are formed on WSe_2. Optical image of the device after (g) S/D contacts and gate formation to MoS_2; and (h) Pt/Au S/D formation on WSe_2. WSe_2 MOSFET is fabricated right on top of the MoS_2 MOSFET. Gate length for NMOS and PMOS is 1 µm.

Fig. 3. I_D–V_G and I_D–V_D characteristics of MoS_2 N-MOSFET

Fig. 4. I_D–V_G and I_D–V_D characteristics of WSe_2 P-MOSFET

Fig. 5. (a) Voltage transfer characteristics of the monolithic 3D CMOS inverter, and (b) Peak voltage gain as a function of supply voltage.

Fig. 6. (a) I_D–V_G characteristics as a function of V_B. (b) Voltage transfer characteristics of a monolithic 3D CMOS inverter as a function of V_B. (c) Voltage gain of the monolithic 3D CMOS inverter as a function of V_B. (d) Current drawn from the supply voltage as a function of V_{IN}.

Fig. 7. Benchmarking of our TMD monolithic 3D CMOS inverter against other reported 3D CMOS inverters. MoS_2-WSe_2 3D [11], InAs/Ge 3D [23], and CNT 3D [22].

Figure 1

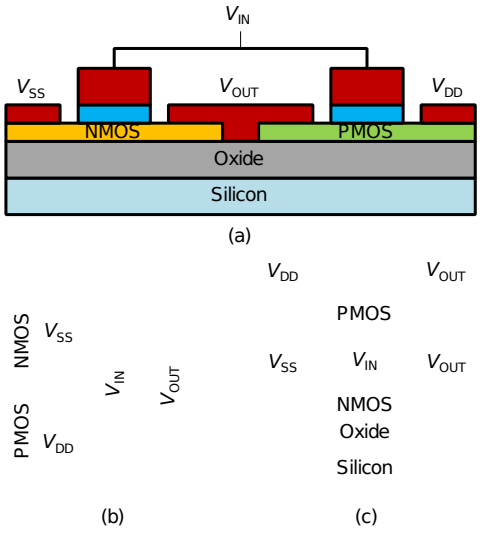

V_{IN}
V_{SS}
V_{OUT}
V_{DD}
NMOS
PMOS
Oxide
Silicon
(a)
NMOS
V_{SS}
V_{IN}
V_{OUT}
PMOS
V_{DD}
(b)
V_{DD}
V_{OUT}
PMOS
V_{SS}
V_{IN}
V_{OUT}
NMOS
Oxide
Silicon
(c)

Figure 2

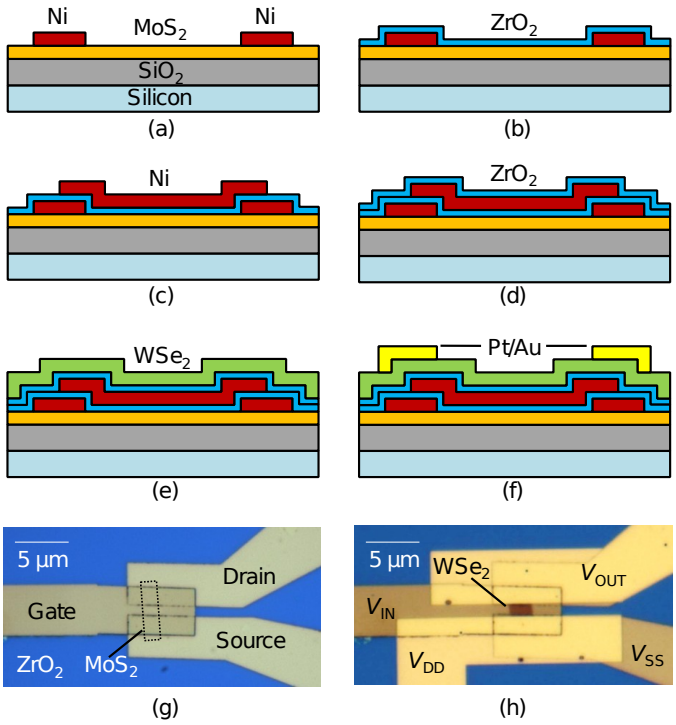

Ni
MoS2
Ni
SiO2
Silicon
(a)
ZrO2
(b)
Ni
(c)
ZrO2
(d)
WSe2
(e)
Pt/Au
(f)
5 µm
Drain
Gate
Source
ZrO2
MoS2
(g)
5 µm
WSe2
VOUT
VIN
VDD
VSS
(h)

Figure 3

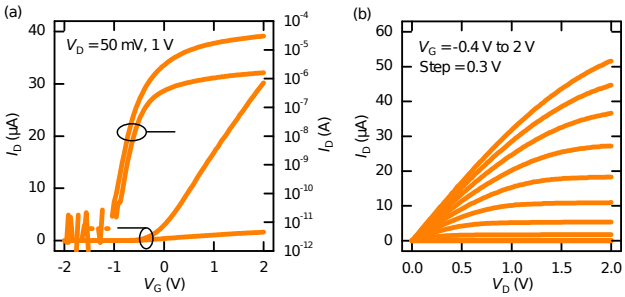


Figure 4

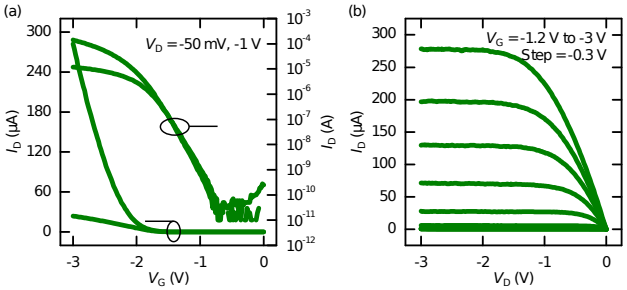


Figure 5

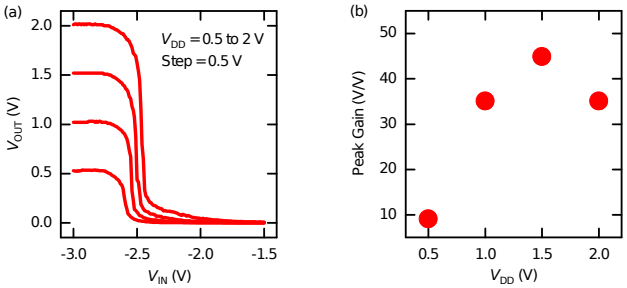

(a)
V_{DD} = 0.5 to 2 V
Step = 0.5 V
V_{OUT} (V)
V_{IN} (V)
2.0
1.5
1.0
0.5
0.0
-3.0
-2.5
-2.0
-1.5
(b)
Peak Gain (V/V)
V_{DD} (V)
50
40
30
20
10
0.5
1.0
1.5
2.0

Figure 6

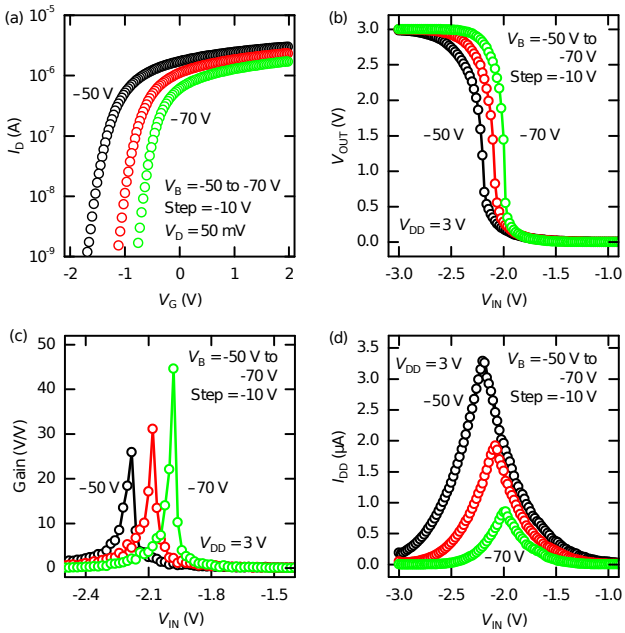
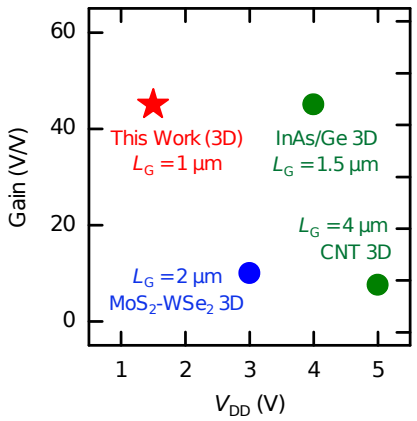

(a)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
I_D (A)
–50 V
–70 V
V_B = -50 to -70 V
Step = -10 V
V_D = 50 mV
-2
-1
0
1
2
V_G (V)
(b)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V_{OUT} (V)
V_B = -50 V to -70 V
Step = -10 V
–50 V
–70 V
V_{DD} = 3 V
-3.0
-2.5
-2.0
-1.5
-1.0
V_{IN} (V)
(c)
50
40
30
20
10
0
Gain (V/V)
V_B = -50 V to -70 V
Step = -10 V
–50 V
–70 V
V_{DD} = 3 V
-2.4
-2.1
-1.8
-1.5
V_{IN} (V)
(d)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
I_{DD} (μA)
V_{DD} = 3 V
V_B = -50 V to -70 V
Step = -10 V
–50 V
–70 V
-3.0
-2.5
-2.0
-1.5
-1.0
V_{IN} (V)

Figure 7


60
40
20
0
Gain (V/V)
1
2
3
4
5
V_{DD} (V)
This Work (3D)
L_G = 1 µm
InAs/Ge 3D
L_G = 1.5 µm
L_G = 4 µm
CNT 3D
L_G = 2 µm
MoS_2-WSe_2 3D

References

[1] David J. Frank, Robert H. Dennard, Edward Nowak, Paul M. Solomon, Yuan Taur, and Hon-Sum Philip Wong, Proceedings of the IEEE **89** (3), 259 (2001).

[2] Thomas Skotnicki, Claire Fenouillet-Beranger, Claire Gallon, Frederic Bœuf, Stephane Monfray, Fabrice Payet, Arnaud Pouydebasque, Melanie Szczap, Alexis Farcy, and Franck Arnaud, Electron Devices, IEEE Transactions on **55** (1), 96 (2008); Kelin J. Kuhn, Martin D. Giles, David Becher, Pramod Kolar, Avner Kornfeld, Roza Kotlyar, Sean T. Ma, Atul Maheshwari, and Sivakumar Mudanai, Electron Devices, IEEE Transactions on **58** (8), 2197 (2011).

[3] Anna W. Topol, D. C. La Tulipe, Leathen Shi, David J. Frank, Kerry Bernstein, Steven E. Steen, Arvind Kumar, Gilbert U. Singco, Albert M. Young, and Kathryn W. Guarini, IBM Journal of Research and Development **50** (4.5), 491 (2006); D. J. Young, V. Malba, J. J. Ou, A. F. Bernhardt, and B. E. Boser, presented at the Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International, 1997; C. C. Yang, J. M. Shieh, T. Y. Hsieh, W. H. Huang, H. H. Wang, C. H. Shen, T. T. Wu, Y. F. Hou, Y. J. Chen, Y. J. Lee, M. C. Chen, F. L. Yang, Y. H. Chen, M. C. Wu, and W. K. Yeh, presented at the 2015 IEEE International Electron Devices Meeting (IEDM), 2015; T. T. Wu, C. H. Shen, J. M. Shieh, W. H. Huang, H. H. Wang, F. K. Hsueh, H. C. Chen, C. C. Yang, T. Y. Hsieh, B. Y. Chen, Y. S. Shiao, C. S. Yang, G. W. Huang, K. S. Li, T. J. Hsueh, C. F. Chen, W. H. Chen, F. L. Yang, M. F. Chang, and W. K. Yeh, presented at the 2015 IEEE International Electron Devices Meeting (IEDM), 2015; T. T. Wu, W. H. Huang, C. C. Yang, C. D. Lin, H. H. Wang, C. H. Shen, and J. M. Shieh, presented at the 2015 International Symposium on VLSI Technology, Systems and Applications, 2015; Hai Wei, Max Shulaker, H. S. Philip Wong, and Subhasish Mitra, Electron Devices Meeting (IEDM), 2013 IEEE International, 2013; Hai Wei, Nishant Patil, Albert Lin, H. S. Philip Wong, and Subhasish Mitra, presented at the 2009 IEEE International Electron Devices Meeting (IEDM), 2009; Max M. Shulaker, Tony F. Wu, Asish Pal, Liang Zhao, Yoshio Nishi, Krishna Saraswat, H. S. Philip Wong, and Subhasish Mitra, presented at the Electron Devices Meeting (IEDM), 2014 IEEE International, 2014; M. M. Shulaker, K. Saraswat, H. S. P. Wong, and S. Mitra, presented at the VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on, 2014; Chang-Hong Shen, Jia-Min Shieh, Tsung-Ta Wu, Wen-Hsien Huang, Chih-Chao Yang, Chih-Jen Wan, Chein-Din Lin, Hsing-Hsiang Wang, Bo-Yuan Chen, and Guo-Wei Huang, presented at the Electron Devices Meeting (IEDM), 2013 IEEE International, 2013; Chang-Hong Shen, Jia-Min Shieh, Wen-Hsien Huang, Tsung-Ta Wu, Chien-Fu Chen, Ming-Hsuan Kao, Chih-Chao Yang, Chein-Din Lin, Hsing-Hsiang Wang, and Tung-Ying Hsieh, presented at the Electron Devices Meeting (IEDM), 2014 IEEE International, 2014; Chang Liu and Sung Kyu Lim, presented at the IEEE International Interconnect Technology Conference, 2012; Jin-Hong Park, Munehiro Tada, Duygu Kuzum, Pawan Kapur, Hyun-Yong Yu, H. S. Philip Wong, and Krishna C. Saraswat, presented at the Electron Devices Meeting, 2008. IEDM 2008. IEEE International, 2008; V. Deshpande, V. Djara, E. O' Connor, P. Hashemi, K. Balakrishnan, M. Sousa, D. Caimi, A. Olziersky, L. Czornomaz, and J. Fompeyrine, presented at the 2015 IEEE International Electron Devices Meeting (IEDM), 2015.

[4] Manish Chhowalla, Hyeon Suk Shin, Goki Eda, Lain-Jong Li, Kian Ping Loh, and Hua Zhang, Nature chemistry **5** (4), 263 (2013); Qing Hua Wang, Kourosh Kalantar-Zadeh, Andras Kis, Jonathan N. Coleman, and Michael S. Strano, Nat Nano **7** (11), 699 (2012).

[5] X. Wang, A. R. Brown, Cheng Binjie, and A. Asenov, presented at the Electron Devices Meeting (IEDM), 2011 IEEE International, 2011; A. B. Sachid, R. Francis, M. S. Baghini, D. K. Sharma, K. H. Bach, R. Mahnkopf, and V. R. Rao, presented at the 2008 IEEE International Electron Devices Meeting, 2008.

[6] Xunli Zhang, David O. Hayward, and D. Michael P. Mingos, Catalysis Letters **84** (3), 225 (2002); Youngki Yoon, Kartik Ganapathi, and Sayeef Salahuddin, Nano Letters **11** (9), 3768 (2011); Sunkook Kim, Aniruddha Konar, Wan-Sik Hwang, Jong Hak Lee, Jiyoul Lee, Jaehyun Yang, Changhoon Jung, Hyoungsub Kim, Ji-Beom Yoo, Jae-Young Choi, Yong Wan Jin, Sang Yoon Lee, Debdeep Jena, Woong Choi, and Kinam Kim, Nat Commun **3**, 1011 (2012).

[7] A. Molina-Sánchez and L. Wirtz, Physical Review B **84** (15), 155413 (2011).

[8] Tania Roy, Mahmut Tosun, Jeong Seuk Kang, Angada B. Sachid, Sujay B. Desai, Mark Hettick, Chenming C. Hu, and Ali Javey, ACS nano **8** (6), 6259 (2014).

[9] Hui Fang, Steven Chuang, Ting Chia Chang, Kuniharu Takei, Toshitake Takahashi, and Ali Javey, Nano Letters **12** (7), 3788 (2012).

[10] Angada B. Sachid, Hui Fang, Ali Javey, and Chenming Hu, in *Proceedings of Technical Program-2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)* (2014).

[11] Angada B. Sachid, Mahmut Tosun, Sujay B. Desai, Ching-Yi Hsu, Der-Hsien Lien, Surabhi R. Madhvapathy, Yu-Ze Chen, Mark Hettick, Jeong Seuk Kang, and Yuping Zeng, Advanced Materials (2016).

[12] J. F. Gibbons and K. F. Lee, Electron Device Letters, IEEE **1** (6), 117 (1980); J. P. Colinge and E. Demoulin, IEEE Electron Device Letters (10), 250 (1981); Wu Xusheng, P. C. H. Chan, Zhang Shengdong, Feng Chuguang, and M. Chan, IEEE Transactions on Electron Devices **52** (9), 1998 (2005).

[13] Yuan Huang, Jing Wu, Xiangfan Xu, Yuda Ho, Guangxin Ni, Qiang Zou, Gavin Kok Wai Koon, Weijie Zhao, A. H. Castro Neto, and Goki Eda, Nano Research **6** (3), 200 (2013).

[14] A. Hsu, H. Wang, K. K. Kim, J. Kong, and T. Palacios, IEEE Electron Device Letters **32** (8), 1008 (2011).

[15] Mahmut Tosun, Steven Chuang, Hui Fang, Angada B. Sachid, Mark Hettick, Yongjing Lin, Yuping Zeng, and Ali Javey, ACS Nano **8** (5), 4948 (2014).

[16] Lili Yu, Ahmad Zubair, Elton J. G. Santos, Xu Zhang, Yuxuan Lin, Yuhao Zhang, and Tomás Palacios, Nano letters **15** (8), 4928 (2015).

[17] Han Wang, Lili Yu, Yi-Hsien Lee, Yumeng Shi, Allen Hsu, Matthew L. Chin, Lain-Jong Li, Madan Dubey, Jing Kong, and Tomas Palacios, Nano letters **12** (9), 4674 (2012).

[18] Daisuke Kiriya, Mahmut Tosun, Peida Zhao, Jeong Seuk Kang, and Ali Javey, Journal of the American Chemical Society **136** (22), 7853 (2014); Kevin Chen, Daisuke Kiriya, Mark Hettick, Mahmut Tosun, Tae-Jun Ha, Surabhi Rao Madhvapathy, Sujay Desai, Angada Sachid, and Ali Javey, APL Materials **2** (9), 092504 (2014).

[19] Saptarshi Das, Madan Dubey, and Andreas Roelofs, Applied Physics Letters **105** (8), 083511 (2014).

[20] G. Tsutsui, T. Nagumo, and T. Hiramoto, IEEE Transactions on Nanotechnology **2** (4), 314 (2003).

[21] Jiang Pu, Kazuma Funahashi, Chang-Hsiao Chen, Ming-Yang Li, Lain-Jong Li, and Taishi Takenobu, Advanced Materials (2016); Han Liu, Adam T. Neal, Zhen Zhu, Zhe Luo, Xianfan Xu, David Tománek, and Peide D. Ye, ACS nano **8** (4), 4033 (2014); Atiye Pezeshki, Seyed Hossein Hosseini Shokouh, Pyo Jin Jeon, Iman Shackery, Jin Sung Kim, Il-Kwon Oh, Seong Chan Jun, Hyungjun Kim, and Seongil Im, ACS nano (2015); Pyo Jin Jeon, Jin Sung Kim, June Yeong Lim, Youngsuk Cho, Atiye Pezeshki, Hee Sung Lee, Sanghyuck Yu, Sung-Wook Min, and Seongil Im, ACS Applied Materials & Interfaces **7** (40), 22333 (2015); Saptarshi Das and Andreas Roelofs, presented at the Device Research Conference, 2014; Junghyo Nah, Hui Fang, Chuan Wang, Kuniharu Takei, Min Hyung Lee, E. Plis, Sanjay Krishna, and Ali Javey, Nano letters **12** (7), 3592 (2012); Ah-Jin Cho, Kee Chan Park, and Jang-Yeon Kwon, Nanoscale research letters **10** (1), 1 (2015); Zhiyong Zhang, Sheng Wang, Zhenxing Wang, Li Ding, Tian Pei, Zhudong Hu, Xuelei Liang, Qing Chen, Yan Li, and Lian-Mao Peng, ACS Nano **3** (11), 3781 (2009); Xiaolei Liu, Chenglung Lee, Chongwu Zhou, and Jie Han, Applied physics letters **79** (20), 3329 (2001); Li Ding, Shibo Liang, Tian Pei, Zhiyong Zhang, Sheng Wang, Weiwei Zhou, Jie Liu, and Lian-Mao Peng, Applied Physics Letters **100** (26), 263116 (2012); Ali Javey, Qian Wang, Ant Ural, Yiming Li, and Hongjie Dai, Nano Letters **2** (9), 929 (2002); Zhiyong Zhang, Xuelei Liang, Sheng Wang, Kun Yao, Youfan Hu, Yuzhen Zhu, Qing Chen, Weiwei Zhou, Yan Li, and Yagang Yao, Nano Letters **7** (12), 3603 (2007); Koungmin Ryu, Alexander Badmaev, Chuan Wang, Albert Lin, Nishant Patil, Lewis Gomez, Akshay Kumar, Subhasish Mitra, H. S. Philip Wong, and Chongwu Zhou, Nano Letters **9** (1), 189 (2008); Seong Jun Kang, Coskun Kocabas, Taner Ozel, Moonsub Shim, Ninad Pimparkar, Muhammad A. Alam, Slava V. Rotkin, and John A. Rogers, Nature nanotechnology **2** (4), 230 (2007); Dae-Hyeong Kim, Yun-Soung Kim, Jian Wu, Zhuangjian Liu, Jizhou Song, Hoon-Sik Kim, Yonggang Y. Huang, Keh-Chih Hwang, and John A. Rogers, Advanced Materials **21** (36), 3703 (2009); Dae-Hyeong Kim, Jong-Hyun Ahn, Hoon-Sik Kim, Keon Jae Lee, Tae-Ho Kim, Chang-Jae Yu, Ralph G. Nuzzo, and John A. Rogers, Electron Device Letters, IEEE **29** (1), 73 (2008); Dae-Hyeong Kim, Jong-Hyun Ahn, Won Mook Choi, Hoon-Sik Kim, Tae-Ho Kim, Jizhou Song, Yonggang Y. Huang, Zhuangjian Liu, Chun Lu, and John A. Rogers, Science **320** (5875), 507 (2008); Dae-Hyeong Kim, Won Mook Choi, Jong-Hyun Ahn, Hoon-Sik Kim, Jizhou Song, Yonggang Huang, Zhuangjian Liu, Chun Lu, Chan Ghee Koh, and John A. Rogers, Applied Physics Letters **93** (4), 044102 (2008); Myeongwon Lee, Youngin Jeon, Taeho Moon, and Sangsig Kim, ACS nano **5** (4), 2629 (2011); K. D. Buddharaju, N. Singh, S. C. Rustagi, S. H. G. Teo, L. Y. Wong, L. J. Tang, C. H. Tung, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, presented at the ESSDERC 2007 - 37th European Solid State Device Research Conference, 2007; K. D. Buddharaju, N. Singh, S. C. Rustagi, Selin H. G. Teo, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, Solid-State Electronics **52** (9), 1312 (2008); Dunwei Wang, Bonnie A. Sheriff, and James R. Heath, Small **2** (10), 1153 (2006); H. Wu, W. Wu, M. Si, and P. D. Ye, presented at the 2015 IEEE International Electron Devices Meeting (IEDM), 2015.

[22] Jong-Hyun Ahn, Hoon-Sik Kim, Keon Jae Lee, Seokwoo Jeon, Seong Jun Kang, Yugang Sun, Ralph G. Nuzzo, and John A. Rogers, science **314** (5806), 1754 (2006).
[23] SungWoo Nam, Xiaocheng Jiang, Qihua Xiong, Donhee Ham, and Charles M. Lieber, Proceedings of the National Academy of Sciences **106** (50), 21035 (2009).