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High Gain Transformer-Less Double-Duty-Triple-Mode DC/DC Converter for DC Microgrid

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ABSTRACT High-gain DC/DC converters with high efficiency are needed in dc microgrid owed to the low voltage of power sources, e.g., photovoltaic-cell and fuel-cell. This paper proposed a new high-gain double-duty-triple-mode (DDTM) converter for dc-microgrid applications. The proposed DDTM converter operates in three modes to achieve higher voltage gain without utilizing transformer, coupled inductor, voltage multiplier, and multiple voltage lifting techniques, e.g., triple, quadruple voltage lift. The modes of operation of the converter are controlled through three switches with two distinct duty ratios (double duty) to achieve wide range duty ratio. The operating principle, voltage gain analysis, and efficiency analysis of the proposed converter are discussed in detail and to show its benefits comparison is provided with the existing high-gain converters. The boundary operating condition for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is presented. The prototype of the proposed converters with 500-W power is implemented in the laboratory and experimentally investigated, which validate the performance and feasibility of the proposed converter. Due to double duty control, the proposed converter can be controlled in different ways and the thorough discussion on controlling of the converter is provided as a future scope.

INDEX TERMS DC/DC, double duty, high gain converter, dc microgrid, transformer-less, triple mode, wide duty range.

NOMENCLATURE

S_1, S_2, and S_3	Active switches
$R_{S1(ON)}$, $R_{S2(ON)}$, and $R_{S3(ON)}$	On state resistance of switches S_1, S_2, S_3
P_1 and P_2	Input and output power
η	Efficiency
P_{S1-SW}, P_{S2-SW}, and P_{S3-SW}	Switching power loss of switches S_1, S_2, S_3
P_{S-SW}	Total switching power loss
t_{f-S1}, t_{f-S2}, t_{f-S3}	Falling switching time for switches S_1, S_2, S_3
t_{r-S1}, t_{r-S2}, t_{r-S3},	Rising switching time for switches S_1, S_2, S_3
L_1 and L_2	Inductors
R_{L1} and R_{L2}	Effective series resistance of inductor L_1 and L_2. ($R_{L1} = R_{L2} = R_{L-ESR}$)
C_1, C_2, and C_3	Capacitors
D, D_1, and D_2	Diodes
R_{F-D1}, R_{F-D2}	Forward resistance of diode D_1 and D_2
V_{D1-TH} and V_{D2-TH}	Threshold voltage of diode D_1 and D_2
R	Load
T_S	Time required for one switching cycle.
f_S	Switching frequency

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d_1 and d_2	Duty ratio
α_1^I and α_1^{II}	Magnetizing angle of Inductor L_1 in mode I and II (CCM)
α_2^I and α_2^{II}	Magnetizing angle of Inductor L_2 in mode I and II (CCM)
β_1^{III} *and* β_2^{III}	Demagnetizing angle of Inductor L_1 and L_2 in mode III (CCM)
δ_1^I, δ_1^{II}	Magnetizing angle of Inductor L_1 in mode I and II (DCM)
δ_2^I, δ_2^{II}	Magnetizing angle of Inductor L_2 in mode I and II (DCM)
γ_1^{III} and γ_2^{III}	Demagnetizing angle of Inductor L_1 and L_2 in mode III (DCM)
i_{L1} and i_{L2}	Current through inductor L_1 and L_2
I_{L1} and I_{L2}	Average current through inductor L_1 and L_2
v_{L1} and v_{L2}	Voltage across inductor L_1 and L_2
$I_{L1}^{(max1)}$ and $I_{L1}^{(max2)}$	Peak of current through inductor L_1 in mode I and II
$I_{L2}^{(max1)}$ and $I_{L2}^{(max2)}$	Peak of current through inductor L_2 in mode I and II
$I_{L1}^{(min)}$ and $I_{L2}^{(min)}$	Lower peak of current through inductor L_1 and L_2
ΔI_{L1} and ΔI_{L2}	Peak to peak current ripples of inductor L_1, L_2
v_{C1} and v_{C2}	Voltage across capacitor C_1, C_2
V_{C1} and V_{C2}	Average voltage across capacitor C_1, C_2
v_{D1} and v_{D2}	Voltage across diodes D_1, D_2
V_{D1} and V_{D2}	Average voltage across diodes D_1, D_2
i_{S1}, i_{S2}, and i_{S3}	Current through switches S_1, S_2, S_3
v_{S1} and v_{S2}	Voltage across switches S_1, S_2
v_{AB}	Voltage across AB junction (diode D + switch S_3)
v_1 and v_2	Input and output voltage (average value of V_1 and V_2)
R_1	Series resistance of input voltage
i_1 and i_2	Input and output current
I_1 and I_2	Average value of Input and output current
v_{GS1}, v_{GS2}, and v_{GS3}	Voltage magnitude of gate pulse for switches S_1, S_2, S_3
I, II and *III* (in superscript)	Defines the values in Mode I, II and III
χ_B	Boundary normalized inductor time constant
χ	Normalized inductor time constant

I. INTRODUCTION

Due to penetration of renewable energy sources, the power converter configurations are gaining more attraction in DC microgrid [1]. Owing to the low terminal voltage of power sources e.g. photovoltaic-cell (PV cell) and fuel-cell, high gain DC/DC converters with high efficiency are needed in DC microgrid [2], [3]. Fig. 1 shows the typical block diagram of a DC microgrid system where DC-DC converter and proposed configurations are employed to uplift the low generated voltage (12-48V) to an adequate voltage level (200-400V) [4]. Practically, in present, the classical boost converter is not a suitable solution to accomplish high step-up voltage gain due to the effect of the series resistance of capacitor and inductor, effective electromagnet interference (EMI), and high rating components and semiconductor devices. Additionally, the reverse recovery of the diode problem is arising when the converter operates at a high duty ratio to achieve high voltage gain [5], [6]. In literature, to overcome these issues, several DC/DC converter configurations are recently proposed with high gain, high efficiency, and small volume etc., e.g. [7], [8]. The isolated DC/DC converters e.g. push-pull, half and full bridge, flyback, and forward converters are proposed in that high voltage gain is achieved by adjusting the turn of the transformer [8]–[11]. Nonetheless, due to the leakage inductance of the transformer, these configurations are suffered from high power dissipation and a high spike in voltage across switches [4]. Therefore, to overcome these issues, additional active clamping technique and snubber circuits are used [12], [13]. Nevertheless, high side driver and additional control switches increase the cost of the circuitry. Furthermore, transformer core saturation is the other problem associated with isolated converters. In [14], the interleaved converter technique is employed to achieve high gain, reduce filter size, and high efficiency using a reduced number of control switches. Nevertheless, complexity and drive circuitry is increased due to the parallel connection of several converters. Moreover, high loss of energy, high voltage/current stress, and complex switching control logic are other drawbacks of this technique. Therefore, transformer-less DC/DC converters can be a solution where galvanic isolation is not necessary and to achieve high voltage gain, reduced size and cost [15], [16]. The cascaded boost converters (CBC), quadratic boost converter (QBC), switched capacitor and switched inductor integration with classical converter,

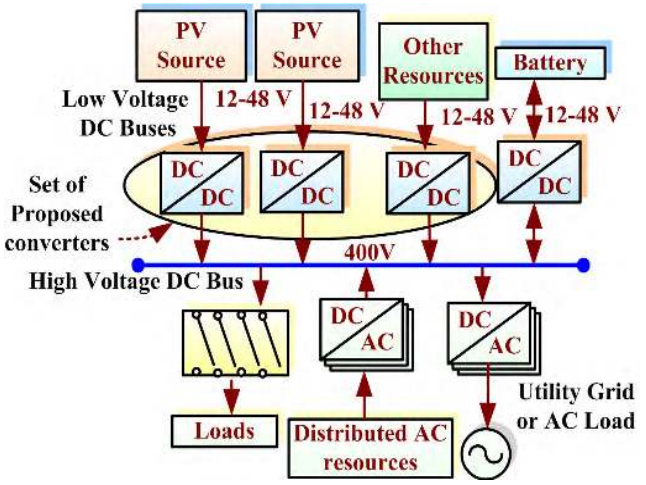

FIGURE 1. Typical blocks of 400V DC microgrid system using proposed converter.

voltage multiplier are utilized to achieve higher voltage gain [17]–[20]. However, a large number of reactive components, semiconductor, switched capacitor and switched inductors stages increase the complexity and price of the converter. In cascaded configurations, it is noteworthy that the requirement of high rating components is increased as the number of cascaded cells increases. Moreover, complex driver circuitry is required to control several switches [16], [21]. In [22], switch voltage stress is reduced by employing additional semiconductor devices and capacitor in a quadruple converter configuration. In [23], non-isolated coupled inductors based converter is proposed to achieve high efficiency and high voltage gain. Using this techniques energy recovery leakage inductance, high efficiency, high voltage, reduced switch stress is achieved by adjusting the turns and coupling factor of coupled inductors. Nevertheless, the large time is required for diode reverse recovery due to coupled inductor leakage inductance. Moreover, the complexity, size, and price of the converter circuitry are increased due to the utilization of coupled inductors. In coupled inductor based converters, the high ripple in the input current is a result of high turns ratio of coupled inductor. Therefore, the stage of the input filter is needed to minimize current ripples, which additionally increases the circuitry and cost of the converter [24]. In [25], capacitor and diode circuitry i.e similar to the switched capacitor is utilized to achieve higher voltage gain with a minimum number of inductor and control switches. In this technique, the capacitors perform similarly to serially connected voltage sources. Later, in [26] active network is combined with a switched capacitor with n cell structure to increase the voltage gain. However, the use of converter is restricted in practical application due to size, low efficiency, high cost, and several components in each cell. Moreover, complex control drive circuitry, additional inductor and active control switch are the other drawbacks of this configuration. Voltage-lift is another boosting technique in which the voltage gain is increased by utilizing the structure of capacitors and inductors, the technique is well presented in [27]. In this technique, inductors are serially discharged with a charged capacitor to increase the voltage at the output side. The main benefits of this structure are high power density, simple structure, less cost, minimum control switches (thus, simple control), small output voltage ripple, and higher efficiency. In [28], three different converters are proposed in that when switches are turned ON and OFF inductors are charged and discharged in parallel and series, respectively. Although using two switches and two inductors along with additional capacitor and diodes, the voltage gain is sufficiently high. In [29], the new non-isolated converter is proposed to achieve high gain for microgrid application. The voltage gain of this converter is adjusted by two duty ratios. However, the voltage gain is limited even though using three high voltage switches and two inductors. To increase the voltage gain, the inductor structure is replaced with stages of the switched inductor [30]. However, the voltage gain is restricted due to the use of several inductors and diodes. In this structure, the energy is transfer to load via multiple loops which degrade the efficiency and performance. Moreover, unequal inductances in the converter affect the characteristics of the converter.

In this paper, a new high gain Transformer-less Double-Duty-Triple-Mode (DDTM) converter is proposed for DC microgrid application. The proposed configuration is capable to provide high voltage gain with wide duty range and reduced switch voltage stress. Moreover, the converter is designed without using transformer, voltage multiplier, and multiple switched capacitor and switched inductor. The main benefits of the proposed configuration are flexibility in selection of duty ratios, the operating range is increased due to double duty ratio, and converter can be controlled in several ways when the input side voltage is perturbed. Moreover, the energy is transfer from input to output without using multiple energy transfer loops which increases the efficiency and performance. Wide duty range and high voltage gain with higher efficiency make proposed converter promising topology for DC microgrid applications.

The paper is organized as follows. Power circuitry of the proposed converters is explained in section II. The steady state analysis in CCM, DCM mode with boundary operating condition is given in section II. The effect of non-ideality of inductors and semiconductor devices on voltage gain and efficiency of the proposed configurations is analyzed in section III. The comparison of DDTM with existing converters is provided in section IV. The experimental investigation results are provided in section V. The thorough discussion on controlling of the converter is provided as a future scope in section VI. Finally, the conclusion is provided in section VII.

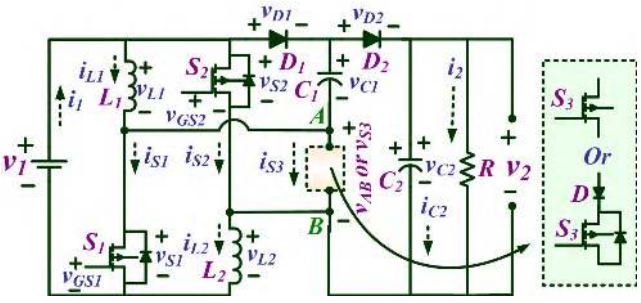

FIGURE 2. Power circuitry of the double-duty-triple-mode converter.

II. DOUBLE-DUTY-TRIPLE-MODE (DDTM) CONVERTER

A. POWER CIRCUIT

The power circuit of DDTM converter is depicted in Fig. 2. The power circuit is designed with the help of two switches S_1 and S_2, one unidirectional current switch S_3 (diode D is connected in series to make unidirectional), two identical inductors L_1 and L_2, two capacitors C_1 and C_2, and two diodes D_1 and D_2. The output voltage is taken across the capacitor C_2 and power is delivered to load (R). Based on the operation, both inductors L_1 and L_2 considered as identical inductors and have inductance L. Therefore, $L = L_1 = L_2$. Ideal components and semiconductors devices are considered

in order to explain the characteristics and operating principle. Let's consider, one switching cycle time period and switching frequency for all the switches are T_S and f_S, respectively. Switches S_1 and S_2 are controlled by the same gate pulse with duty ratio d_1 and the switch S_3 is controlled by gate pulse with duty ratio d_2 with time delay d_1T_S. Using these pulses, the converter is operates in three modes.

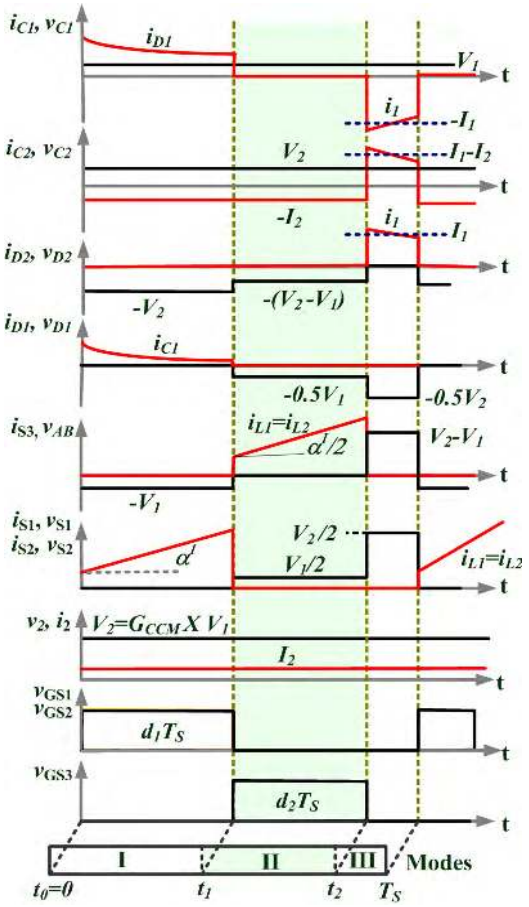

FIGURE 3. CCM characteristics waveforms of double duty triple mode converter (DDTM converter).

B. CCM OPERATION AND ANALYSIS

The CCM operation of the converter is explained as follows,

Fig. 3 depicts the typical characteristics of DDTM converter. Let's consider α_1^I, α_1^{II} and α_2^I, α_2^{II} are the inductor L_1 and L_2 magnetizing angles; where superscript is defines the mode of operation (I and II) and subscript defines the inductor. Also consider β_1^{III} and β_2^{III} are the inductor L_1 and L_2 demagnetizing angles in mode III. The typical inductor current and voltage waveforms are shown in Fig. 4. Due to same characteristics of inductor L_1 and L_2, the areas covered by both inductor voltage waveforms are same. In Fig. 4, A, B, and C are the areas under voltage waveform of inductor L_1 and L_2 for modes I, II, and III, respectively.

1) MODE I [t_0 TO t_1]

Fig. 5(a) depicts the mode I equivalent power circuit of DDTM converter in which switches S_1 and S_2 are turned ON

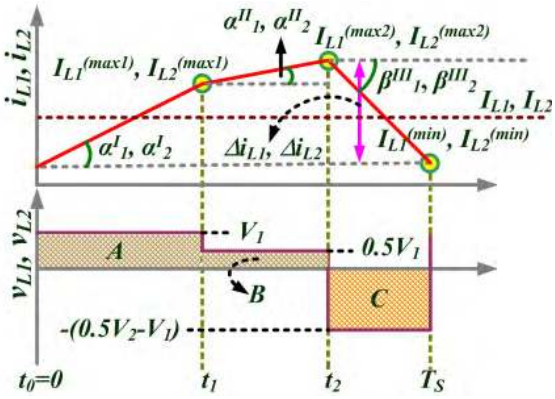

FIGURE 4. Typical voltage and current waveforms for inductor L_1 and L_2 in CCM.

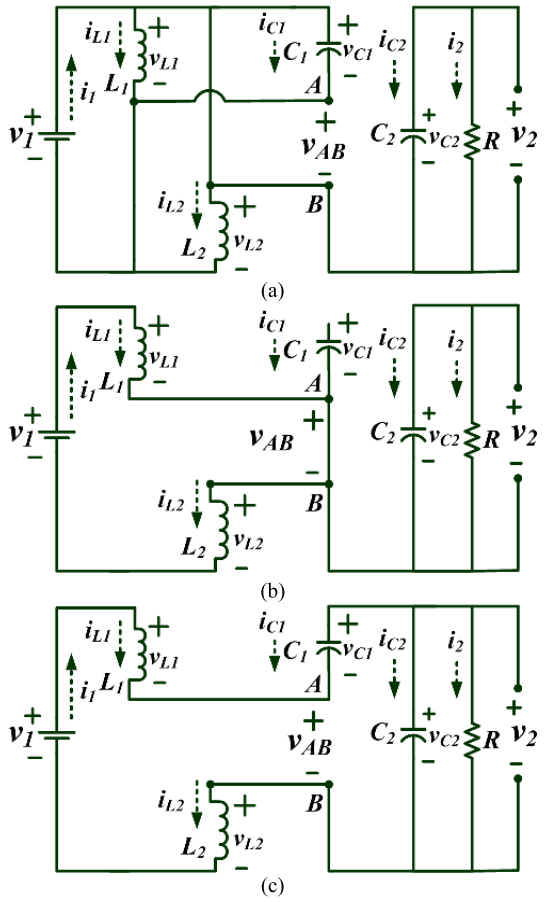

FIGURE 5. Equivalent circuitry of DDTM converter. (a) Mode I, (b) Mode II, (c) Mode III.

and the switch S_3 is turned OFF. In this mode, inductors L_1 and L_2 are magnetized by input voltage v_1 through switches S_1 and S_2, respectively. Also, capacitor C_1 is charged by the input voltage v_1 through diode D_1 and switch S_1. Throughout this mode, diodes D_1 and D_2 are forward biased and reversed biased, respectively and the capacitor C_2 is discharged through load (R). The average inductor L_1, L_2 and capacitor C_1, C_2 voltage and average input current can be

expressed as follows,

$$\begin{cases} V_L^I = V_{L1}^I = V_{L2}^I = V_1; \quad V_{C1}^I = V_1;\ V_{C2}^I = V_2 \\ I_1^I = I_{L1}^I + I_{L2}^I + I_{C1}^I \end{cases} \tag{1}$$

The "*I*" is expressed in the superscript for mode I. It is noteworthy that the current waveform of inductors L_1 and L_2 is linearly increased with slope tan (α_1^I) and tan (α_2^I). Moreover, the magnetizing angle of inductors L_1 and L_2 current is same and expressed as follows,

$$\begin{cases} \alpha_1^I = \tan^{-1}\left(\dfrac{I_{L1}^{(Max1)} - I_{L1}^{(Min)}}{d_1 T_s}\right) = \tan^{-1}\left(L_1^{-1} V_1\right) \\ \alpha_2^I = \tan^{-1}\left(\dfrac{I_{L2}^{(Max1)} - I_{L2}^{(Min)}}{d_1 T_s}\right) = \tan^{-1}\left(L_2^{-1} V_1\right) \\ we\ have\ L = L_1 = L_2, \quad \therefore\ \alpha = \alpha_1^I = \alpha_2^I \end{cases} \tag{2}$$

2) MODE II [t_1 TO t_2]

Fig. 5(b) depicts the mode II equivalent power circuitry of DDTM converter in which switches S_1 and S_2 are turned OFF and the switch S_3 is turned ON. In this mode, inductors L_1 and L_2 are magnetized in series by input voltage v_1 through switches S_3. In this mode, diodes D_1 and D_2 are reversed biased due to capacitor C_1 and C_2 voltages, respectively. Throughout this mode, the capacitor C_2 discharged through load (R). The average inductor L_1, L_2 and capacitor C_1, C_2 voltage and average input current can be expressed as follows,

$$\begin{cases} V_L^{II} = V_{L1}^{II} = V_{L2}^{II} = \dfrac{V_1}{2}; \quad V_{C1}^{II} = V_1;\ V_{C2}^{II} = V_2 \\ I_{L1}^{II} = I_{L2}^{II} = I_1^{II} \end{cases} \tag{3}$$

The "*II*" is expressed in the superscript for mode II. It is noteworthy that the current waveform of inductors L_1 and L_2 is linearly increased with slope tan (α_1^{II}) and tan (α_2^{II}). Moreover, the magnetizing angle of L_1 and L_2 current is same and expressed as follows,

$$\begin{cases} \alpha_1^{II} = \tan^{-1}\left(\dfrac{L_1^{-1} V_1}{2}\right) = \tan^{-1}\left(\dfrac{I_{L1}^{(Max2)} - I_{L1}^{(Max1)}}{d_2 T_S}\right) \\ \alpha_2^{II} = \tan^{-1}\left(\dfrac{L_2^{-1} V_1}{2}\right) = \tan^{-1}\left(\dfrac{I_{L2}^{(Max2)} - I_{L2}^{(Max1)}}{d_2 T_S}\right) \\ we\ have\ L_1 = L_2, \quad \therefore\ \alpha^I = 2\alpha_1^{II} = 2\alpha_2^{II} \end{cases} \tag{4}$$

3) MODE III [t_2 TO t_3]

Fig. 5(c) depicts the mode III equivalent power circuit of DDTM converter in which all the switches S_1, S_2, and S_3 are turned OFF. In this mode, the series connection of input voltage v_1, inductor L_1 and L_2, and capacitor C_1 supplied power to load (R) and also charges the capacitor C_2. Hence, inductor L_1 and L_2 are demagnetized and capacitor C_1 is discharged serially through load (R). Throughout this mode, diodes D_1 and D_2 are reversed biased and forward biased, respectively. The average inductor L_1, L_2 and capacitor C_1, C_2 voltage and average input current can be expressed as follows,

$$\begin{cases} V_L^{III} = V_{L1}^{III} = V_{L2}^{III} = \dfrac{V_1 - V_2 + V_{C1}}{2} = \dfrac{2V_1 - V2}{2} \\ V_{C1}^{III} = V_1; \quad V_{C2}^{III} = V_2,\ I_1^{III} = I_L^{III} = I_{L1}^{III} = I_{L2}^{III} \end{cases} \tag{5}$$

The "*III*" is expressed in the superscript for mode III. It is noteworthy that the current waveform of inductors L_1 and L_2 is linearly decreased with slope tan (β_1^{III}) and tan (β_2^{III}). Moreover, the demagnetizing angle of L_1 and L_2 current is same and expressed as follows,

$$\begin{cases} \beta_1^{III} = \tan^{-1}\left(\dfrac{V_1 - \frac{V_2}{2}}{L_1}\right) = \tan^{-1}\left(\dfrac{I_{L1}^{(Min)} - I_{L1}^{(Max2)}}{1 - d_1 T_S - d_2 T_S}\right) \\ \beta_2^{III} = \tan^{-1}\left(\dfrac{V_1 - \frac{V_2}{2}}{L_2}\right) = \tan^{-1}\left(\dfrac{I_{L2}^{(Min)} - I_{L2}^{(Max2)}}{1 - d_1 T_S - d_2 T_S}\right) \\ we\ have\ L_1 = L_2, \quad \beta = \beta_1^{II} = \beta_2^{II} \end{cases} \tag{6}$$

From Fig. 4, the area covered by the inductor L (i.e L_1 and L_2) voltage waveform in Mode I, II, III are relates as follows,

$$\begin{cases} \underbrace{\int_0^{d_1 T_S} V_L^I dt}_{A} + \underbrace{\int_0^{d_2 T_S} V_L^{II} dt}_{B} + \underbrace{\int_0^{(1-d_1-d_2)T_S} V_L^{III} dt}_{C} = 0 \end{cases} \tag{7}$$

By substituting (1), (3), and (5) in (7), the voltage gain for CCM is obtained as follows

$$\left\{ G_{CCM} = \frac{V_2}{V_1} = \frac{2 - d_2}{1 - d_1 - d_2} \right. \tag{8}$$

The plot of voltage gain versus duty ratio d_1 and d_2 is shown in Fig. 6. It is noteworthy that the proposed converter gives high voltage gain by selecting appropriate duty ratios d_1 and d_2. The region is shaded in which the proposed DDTM converter provides a voltage gain in the range 10 to 20. Further to explain Fig. 6, the effects of each duty ratio d_1 and d_2 on voltage gain are shown in Fig. 7(a) and 7(b). It is noteworthy that Fig. 6 is a combined version of Fig. 7(a) and Fig. 7(b). In Fig. 7(a), the plot of voltage gain in CCM versus duty ratio d_1 is given by considering the different values for the duty ratio d_2. It is observed that in each case the voltage gain is increased if duty ratio d_2 is constant and duty ratio d_1 is increased. When addition of duty ratios d_1 and d_2 i.e d_1+d_2 is constant in between 0 to 1, it is observed that the voltage gain is increased if duty ratio d_2 is decreased (The example is shown in Fig. 7(a) for $d_1 + d_2 = 0.8$ and $d_1 + d_2 = 0.9$). In Fig. 7(b), the plot of voltage gain in CCM versus duty ratio d_2 is given with considering the different values for the duty ratio d_1. It is observed that in each case the voltage gain is increased if duty ratio d_1 is constant and duty ratio d_2 is increased. When addition of d_1 and d_2 i.e $d_1 + d_2$ is constant in between 0 to 1, it is observed that the gain is decreased if duty ratio d_1 is decreased (The example is shown in Fig. 7(b) for $d_1 + d_2 = 0.8$ and $d_1 + d_2 = 0.9$).

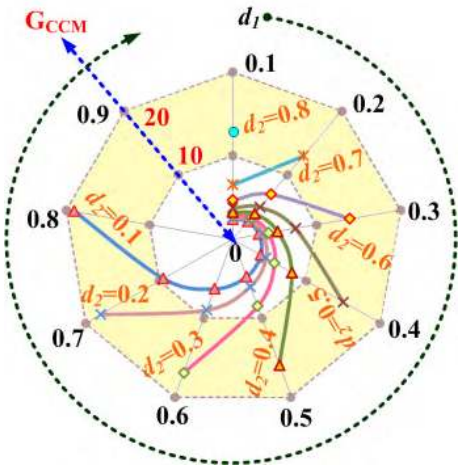

FIGURE 6. Plot of voltage gain in CCM versus duty ratio d_1 and d_2.

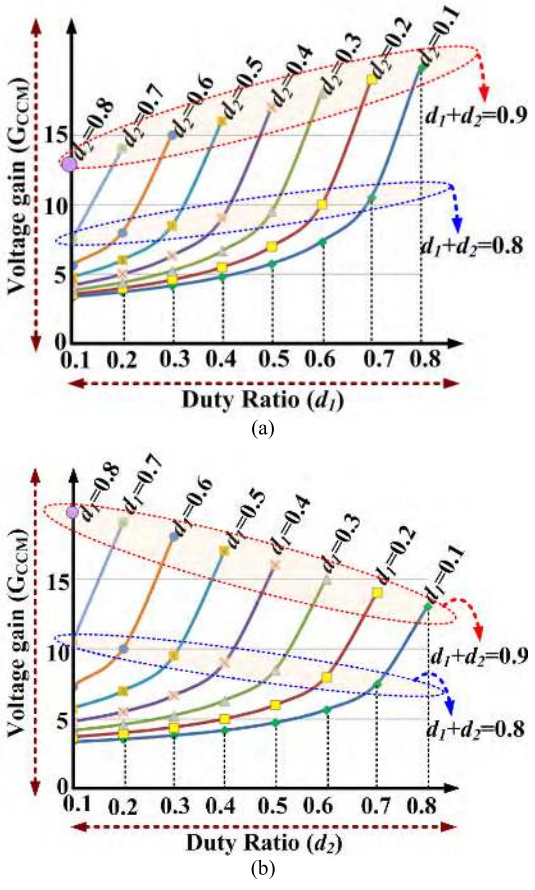

FIGURE 7. Effect of duty ratios on voltage gain (a)voltage gain versus duty ratio d_1 by considering the different values for duty ratio d_2, (b) voltage gain versus duty ratio d_2 by considering the different values for duty ratio d_1.

C. DCM OPERATION AND ANALYSIS

The DDTM converter DCM operation is divided in four modes. Fig. 8 depicts the typical DCM characteristics of DDTM converter. Let's consider δ_1^I, δ_1^{II} and δ_2^I, δ_2^{II} are the inductor L_1 and L_2 magnetizing angles; where superscript is defines the mode of operation (I and II) and subscript defines the inductor. Also consider γ_1^{III}, γ_2^{III} are the inductor

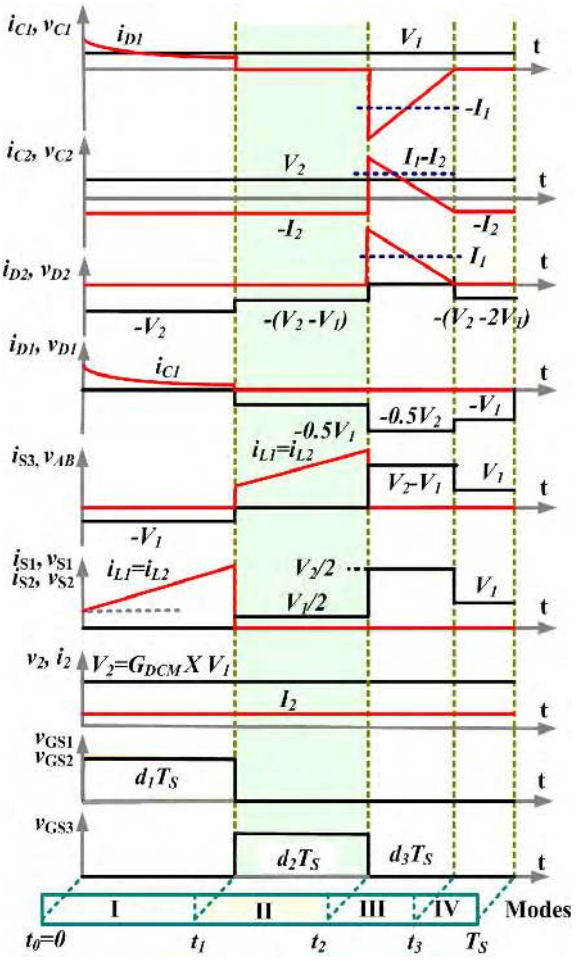

FIGURE 8. DCM characteristics waveforms of double-duty-triple-mode converter (DDTM converter).

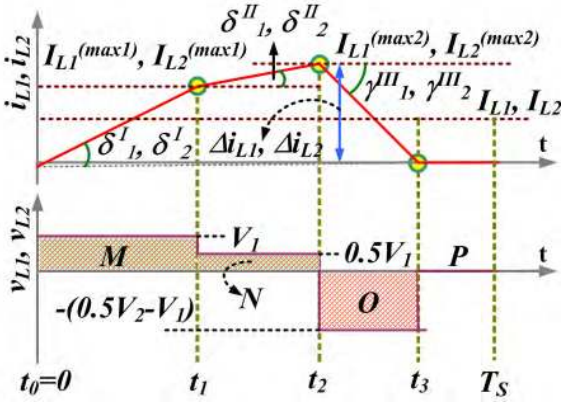

FIGURE 9. Typical voltage and current waveforms for inductor L_1 and L_2 in DCM.

L_1 and L_2 demagnetizing angles in mode III. The typical inductor current and voltage waveforms in DCM are shown in Fig. 9. Due to same characteristics of inductor L_1 and L_2, the areas covered by both inductors voltage waveforms are same. In Fig. 9, M, N, O and P are the areas under voltage waveform of inductor L_1 and L_2 for modes I, II, III, and IV, respectively. The DCM operation of the DDTM converter is explained as follows,

1) MODE I [t_0 TO t_1]

The equivalent circuit is same as mode I of CCM (Fig. 5(a)). In this mode, switches S_1 and S_2 are turned ON and the switch S_3 is turned OFF. For this mode, the maximum amplitude of current through inductor L_1 and L_2 can be expressed as follows,

$$\begin{cases} I_{L1}^{(max1)} = L_1^{-1} V_1 d_1 T_S = d_1 T_S \tan(\delta_1^I) \\ I_{L2^{(max1)}} = L_2^{-1} V_1 d_1 T_S = d_1 T_S \tan(\delta_2^I) \\ we\ know\ L = L_1 = L_2, \quad \delta^I = \delta_1^I = \delta_2^I \\ \therefore I_{L^{(max1)}} = I_{L1^{(max1)}} = I_{L2^{(max1)}} \end{cases} \tag{9}$$

2) MODE II [t_1 TO t_2]

The equivalent circuit is same as mode II of CCM (Fig. 5(b)). In this mode, switches S_1 and S_2 are turned OFF and the switch S_3 is turned ON. For this mode, the maximum amplitude of current through inductor L_1 and L_2 can be expressed as follows,

$$\begin{cases} I_{L1}^{(Max2)} \begin{cases} = I_{L1^{(Max1)}} + \left(\dfrac{L_1^{-1} V_1}{2}\right) d_2 T_S \\ = \left(L_1^{-1} V_1\right)\left(\dfrac{d_2}{2} + d_1\right) T_S \\ = d_1 T_S \tan(\delta_1^I) + d_2 T_S \tan(\delta_1^{II}) \end{cases} \\ I_{L2}^{(Max2)} \begin{cases} = I_{L2^{(Max1)}} + \left(\dfrac{L_2^{-1} V_1}{2}\right) d_2 T_S \\ = \left(L_2^{-1} V_1\right)\left(\dfrac{d_2}{2} + d_1\right) T_S \\ = d_1 T_S \tan(\delta_2^I) + d_2 T_S \tan(\delta_2^{II}) \end{cases} \\ we\ know\ L = L_1 = L_2, \quad \Rightarrow 2\delta_1^{II} = 2\delta_2^{II} = \delta_1^I = \delta_2^I \\ \therefore I_L^{(Max2)} = I_{L1}^{(Max2)} = I_{L2}^{(Max2)} \end{cases} \tag{10}$$

3) MODE III [t_2 TO t_3]

The equivalent circuit is same as mode III of CCM (Fig. 5(c)). In this mode, all the switches S_1, S_2 and S_3 are turned OFF and at the end of this mode (at $t = t_3$), the inductor L_1 and L_2 currents reached to zero. For this mode, the maximum amplitude of current through inductor L_1 and L_2 can be expressed as follows,

$$\begin{cases} I_{L1}^{(Max2)} \begin{cases} = \dfrac{(V_{C2} - V_{C1} - V_1)}{2} L_1^{-1} d_3 T_S \\ = \dfrac{(V_2 - 2V_1)}{2} L_1^{-1} d_3 T_S = d_3 T_S(\gamma_1^{III}) \end{cases} \\ I_{L2}^{(Max2)} \begin{cases} = \dfrac{(V_{C2} - V_{C1} - V_1)}{2} L_2^{-1} d_3 T_S \\ = \dfrac{(V_2 - 2V_1)}{2} L_2^{-1} d_3 T_S = d_3 T_S(\gamma_2^{III}) \end{cases} \\ we\ know\ L = L_1 = L_2, \quad \Rightarrow \gamma_1^{III} = \gamma_2^{III} \\ \therefore I_L^{(Max2)} = I_{L1}^{(Max2)} = I_{L2}^{(Max2)} \end{cases} \tag{11}$$

4) MODE IV [t_3 TO t_S]

In this mode, all the switches S_1, S_2 and S_3 are turned OFF and inductor L_1 and L_2 currents are zero. The equivalent circuitry for this DCM mode is shown in Fig. 10. Throughout this mode, the inductor L_1 and L_2 energy is zero and capacitor C_2 discharged through to load. Using (10) and (11), the value of d_3 is can be obtained as follows,

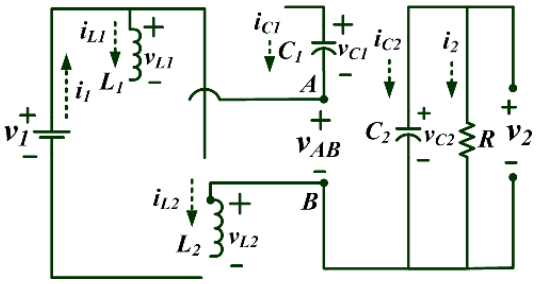

FIGURE 10. Equivalent circuit of DDTM converter in Mode IV (DCM) (Switches S_1, S_2, and S_3 are turned OFF).

$$d_3 = \left(\frac{V_1(2d_1 + d_2)}{V_2 - 2V_1}\right) \tag{12}$$

The average capacitor C_2 current can be expressed as follows,

$$\begin{cases} I_{C2} = \dfrac{I_{L1}^{(\max 2)} d_3 T_s - 2I_2 T_S}{2T_s} = \dfrac{I_{L1}^{(\max 2)} d_3}{2} - I_2 \\ I_{C2} = \dfrac{\left(\sqrt{L_1^{-1}} V_1\right)^2 (d_2 + 2d_1)^2 T_s}{4(V_2 - 2V_1)} - \dfrac{V_2}{R} \end{cases} \tag{13}$$

At steady state, the average current through any capacitor is zero. Therefore,

$$\begin{cases} \dfrac{V_1^2 (d_2 + 2d_1)^2 T_s}{4L(V_2 - 2V_1)} = \dfrac{V_2}{R} \end{cases} \tag{14}$$

Using (14), the voltage gain for DCM is obtained as follows

$$\begin{cases} G_{DCM} = \dfrac{V_2}{V_1} = 1 + \sqrt{1 + \dfrac{(d_2 + 2d_1)^2}{4\chi}}, \chi = L/RT_s \end{cases} \tag{15}$$

where, parameter χ is the normalized inductor time constant. The plot of voltage gain in DCM versus duty ratio d_1 and d_2 is shown in Fig. 11(a). It is noteworthy that the required voltage gain in DCM of proposed converter can be achieved by selecting appropriate duty ratio d_1 and d_2. The region is shaded in which the proposed converter provides a voltage gain in the range 8 to 12. Further to explain Fig. 11(a) more clearly, the effects of each duty ratio d_1 and d_2 on DCM voltage gain are shown in Fig. 11(b) and 11(c). It is noteworthy that Fig. 11(a) is combined version of Fig. 11(b) and Fig. 11(c). In Fig. 11(b), the plot of voltage gain in DCM versus duty ratio d_1 is given by considering different values for duty ratio d_2. It is observed that in each case of Fig. 11(b), the voltage gain is increased if duty ratio d_2 is constant and duty ratio d_1 is increased. When addition of d_1 and d_2 (i.e $d_1 + d_2$) is constant in between 0 to 1, it is observed that the voltage gain is increased if duty ratio d_2 is decreased (The example is shown for $d_1 + d_2 = 0.9$). In Fig. 11(c), the plot of voltage

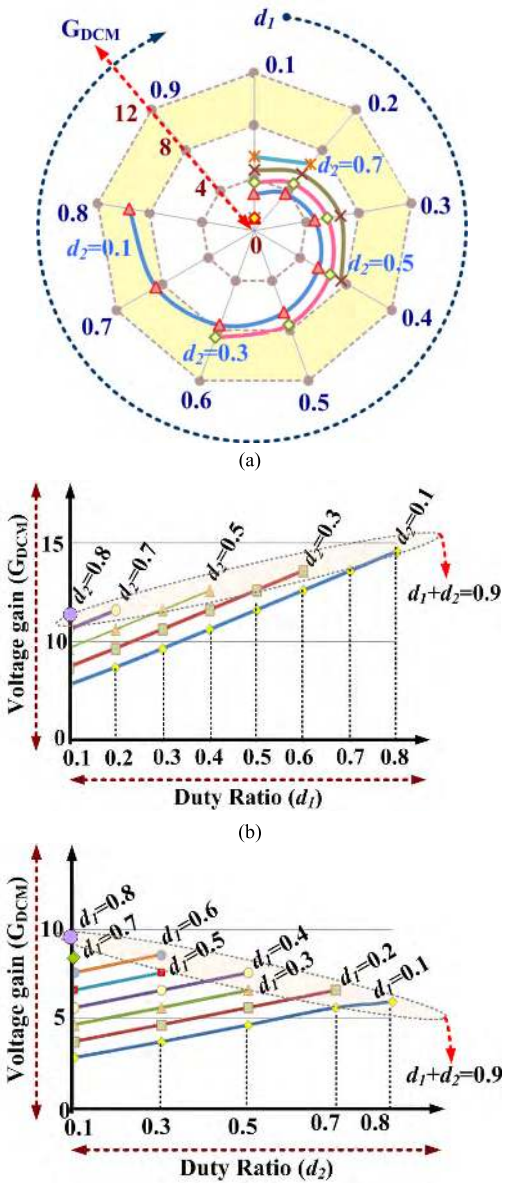

FIGURE 11. Plot voltage gain in DCM and effect of duty ratio (a) Plot of voltage gain versus duty ratio d_1 and d_2, (b) voltage gain versus duty ratio d_1 by considering the different values for duty ratio d_2, (c) voltage gain versus duty ratio d_2 by considering the different values for duty ratio d_1.

gain in DCM versus duty ratio d_2 is given by considering different values for duty ratio d_1. It is observed that in each case of Fig. 11(c), the voltage gain is increased if duty ratio d_1 is constant and duty ratio d_2 is increased. When addition of d_1 and d_2 (i.e $d_1 + d_2$) is constant in between 0 to 1, it is observed that the voltage gain is decreased if duty ratio d_1 is decreased (The example is shown for $d_1 + d_2 = 0.9$).

Using (8) and (15), the boundary for CCM and DCM can be obtained as follows,

$$\begin{cases} \chi_B = \dfrac{(d_2 + 2d_1)\,(1 - d_1 - d_2)^2}{4(2 - d_2)} \end{cases} \tag{16}$$

where boundary normalized inductor time constant is χ_B. In Fig. 12(a), the plot of χ_B versus duty ratio d_1 is shown by considering various value of duty ratio d_2. This graph

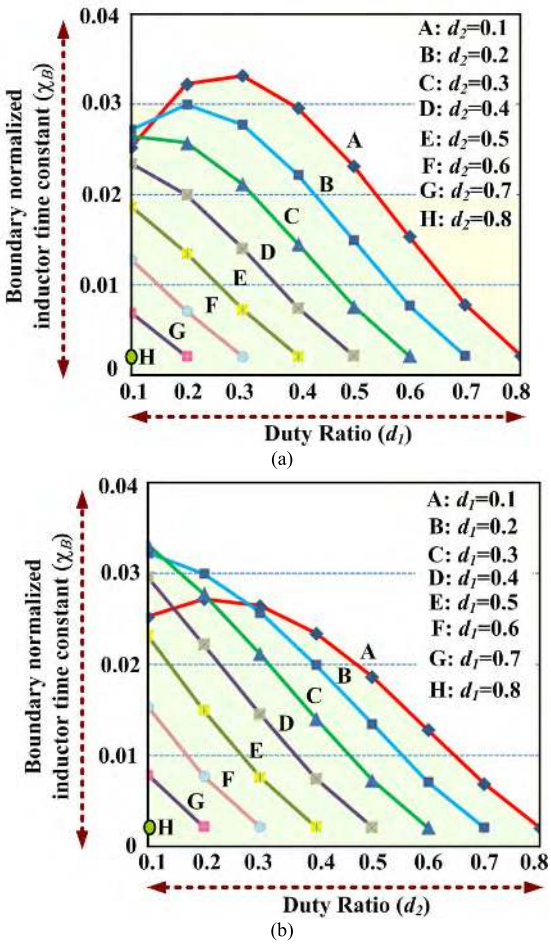

FIGURE 12. Plot of boundary normalized inductor time constant χ_B versus duty ratio (a) χ_B versus duty ratio d_1 with considering various value of duty ratio d_2, (b) χ_B versus duty ratio d_2 with considering various value of duty ratio d_1.

clearly explained the effect of duty ratio d_1 on χ_B. It is investigated that after attaining the peak value there is decrement in normalized inductor time constant χ_B when duty ratio d_1 is increased. Moreover, at constant d_1, the magnitude of χ_B is reduced when duty ratio d_2 is increases.

In Fig. 12(b), the plot of χ_B versus duty ratio d_2 is shown by considering various value of duty ratio d_1. This graph clearly explained the effect of duty ratio d_2 on χ_B. It is investigated that after attaining the peak value there is a decrement in normalized inductor time constant χ_B when duty ratio d_2 is increased. Moreover, at constant d_2, the magnitude of χ_B is reduced when duty ratio d_1 is increases.

The boundary surface of DCM and CCM is dependent on duty ratios d_1, d_2, and χ_B. Hence, to understand the combined effect of duty ratio d_1, d_2, and χ_B on boundary of DCM and CCM, the surface plot of χ_B versus duty ratios d_1 and d_2 is plot in Fig. 13(a). In Fig. 13(a), the area under the drawn surface is DCM region and area outside the surface is CCM region. Additionally, DCM region is shown in Fig. 13(b) by varying duty ratio d_1 for various values of duty ratio d_2. It is clearly visible that DCM region is reduced when the value of duty ratio d_2 is increased. It is also investigated that the DCM region becomes narrow when the duty ratio d_2

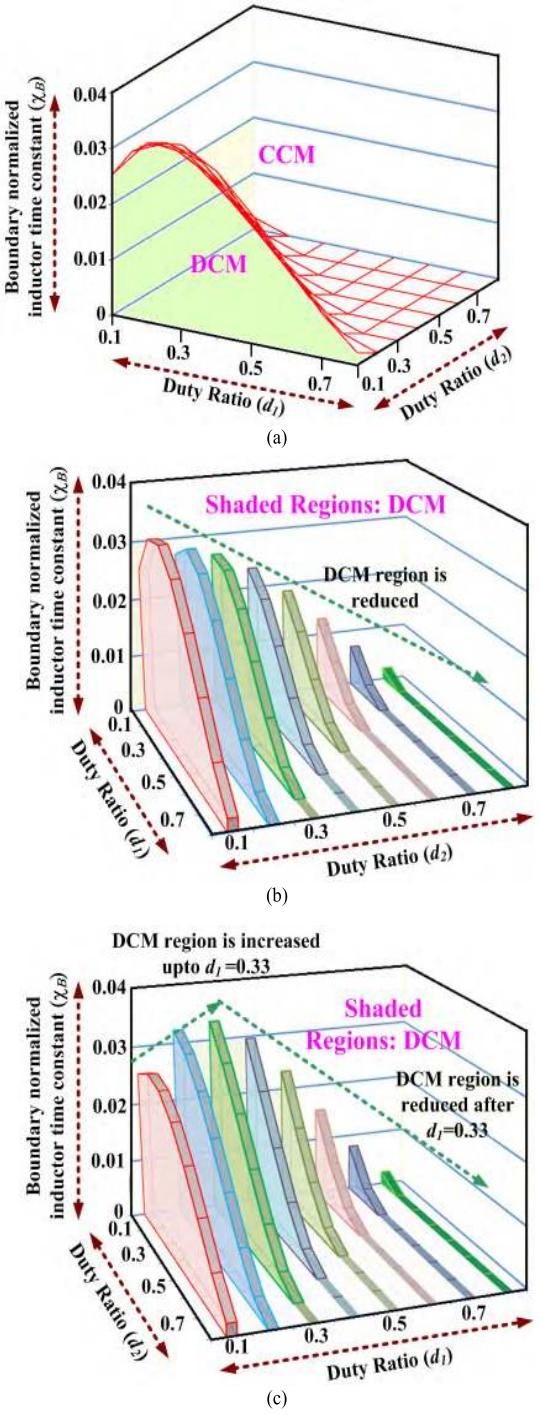

FIGURE 13. DCM and CCM boundary and regions (a) surface plot of normalized inductor time constant χ_B versus duty ratios d_1 and d_2, (b) DCM regions by varying duty ratio d_1 for various values of duty ratio d_2, (c)DCM regions by varying duty ratio d_2 for various values of duty ratio d_1.

is increased and duty ratio d_1 is constant. DCM region is shown in Fig. 13(c) by varying duty ratio d_2 for various values of duty ratio d_1. It is clearly visible that DCM region is increased when the value of duty ratio d_1 is increased from 0 to 0.33 and reduced when the value of duty ratio d_1 is increased beyond 0.33. It is also investigated that the DCM region becomes narrow when the duty ratio d_1 is increased

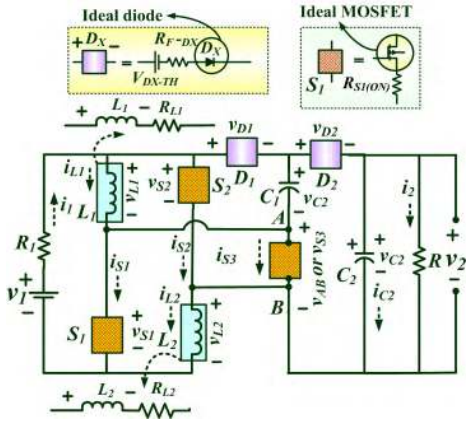

FIGURE 14. Equivalent circuit of DDTM converter with non-idealities.

and duty ratio d_2 is constant. Hence, the DCM operation is dependent on the both duty ratios d_1 and d_2, and χ_B. When χ_B is higher than χ then DCM occurs for DDTM converter. Nevertheless, the condition in order to operate converter in CCM is as follows,

$$\left\{\frac{(d_2+2d_1)\,(1-d_1-d_2)^2}{4(2-d_2)} < \left(\chi = \frac{L}{RT_s}\right)\right. \tag{17}$$

III. EFFICIENCY INVESTIGATION OF DDTM CONVERTER

The non-idealities are considered in order to analyze the efficiency of DDTM converter. The power circuit of DDTM converter is shown in Fig. 14 with non-idealities. The series resistances R_{L1} and R_{L2} are considered as non-ideality of inductor L_1 and L_2, respectively. The resistance R_1 is considered in series with input voltage as a non-ideality of input voltage source. The switches S_1, S_2 and S_3 non-ideality is shown by ON state resistance $R_{S1(ON)}$, $R_{S2(ON)}$, and $R_{S3(ON)}$, respectively. For simplicity, non-ideality of diode D is neglected. The diode D_1 and D_2 non ideality is shown by forward resistance R_{F-D1}, R_{F-D2} and threshold voltage V_{D1-TH} and V_{D2-TH}, respectively.

A. MODE I [t_0 TO t_1]

The average current and voltage through/across inductor and capacitor is obtained as follows,

$$\left.\begin{aligned} &I^I_{C1} \approx I^I_1 - I^I_{L1} - I^I_{L2}; \quad I^I_{C2} \approx -\left(V_2 R^{-1}\right) \\ &V^I_{L1} \approx V_1 - I^I_{L1}R_{L1} - I^I_{S1}R_{S1(ON)}) - I^I_1 R_1 \\ &V^I_{L2} \approx V_1 - I^I_{L2}(R_{L1} + R_{S2(ON)}) - I^I_1 R_1 \\ &V^I_{C1} \approx V_1 - I^I_1 R_1 - V_{D1-TH} - I^I_{D1}(R_{F-D1}) - I^I_{S1}R_{S1(ON)} \end{aligned}\right\} \tag{18}$$

B. MODE II [t_1 TO t_2]

The average current and voltage through/across inductor and capacitor is obtained as follows,

$$\left.\begin{aligned} &V^{II}_{L1} + V^{II}_{L2} = V_1 - I^{II}_{L1}(R_{L1} + R_{L2}) - I^{II}_1\left(R_1 + (R_{S3(ON)}\right) \\ &I^{II}_1 = I^{II}_{L1} = I^{II}_{L2}; \quad I^{II}_{C2} \approx -\left(V_2 R^{-1}\right) \end{aligned}\right\} \tag{19}$$

C. MODE II [t_2 TO t_3]

The average current and voltage of inductor and capacitor is obtained as follows,

$$\left.\begin{aligned} V_{L1}^{III}+V_{L2}^{III} &= V_1+V_{C1}-V_2 \\ &\quad -\begin{pmatrix} I_{L1}^{III}(R_{L1}+R_{L2}) \\ +I_1^{III}(R_1+R_{F-D2})+V_{D2-TH}\end{pmatrix} \\ I_1^{III} &= I_{L1}^{III}=I_{L2}^{III};\quad I_{C2}^{III}\approx I_1^{III}-\left(V_2R^{-1}\right)\end{aligned}\right\} \quad (20)$$

To design the DDTM converter, identical inductor L_1 and L_2 i.e ($L = L_1 = L_2$) are considered with same effective series resistance $R_{L1} = R_{L2} = R_{L-ESR}$. All the control switches are identical and ON state resistance of all the switches are same, that means $R_{S1(ON)} = R_{S2(ON)} = R_{S3(ON)} = R_{S(ON)}$. Identical diodes are considered with same forward resistance $R_{F-D1} = R_{F-D2} = R_{F-D}$ and same threshold voltage i.e means $V_{D-TH} = V_{D1-TH} = V_{D2-TH}$. Based on the consideration, (18)-(20) rewritten as follows,

$$\left.\begin{aligned} I_{C1}^{I} &\approx I_1^I-I_{L1}^I-I_{L2}^I;\quad I_{C2}^I\approx -\left(V_2R^{-1}\right) \\ V_{L1}^I &\approx V_{L2}^I\approx V_1-I_L^I(R_{L-ESR}+R_{S(ON)})-I_1^IR_1 \\ V_{C1}^I &\approx V_1-I_1^IR_1-V_{D-TH}-I_{D1}^I(R_{F-D})-I_{S1}^IR_{S(ON)}\end{aligned}\right\} \quad (21)$$

$$\left.\begin{aligned} V_{L1}^{II}+V_{L2}^{II} &= V_1-I_{L1}^{II}(2R_{L-ESR})-I_1^{II}\left(R_1+(R_{S(ON)}\right) \\ I_1^{II} &= I_{L1}^{II}=I_{L2}^{II};\quad I_{C2}^{II}\approx -\left(V_2R^{-1}\right)\end{aligned}\right\} \quad (22)$$

$$\left.\begin{aligned} V_{L1}^{III}+V_{L2}^{III} &= V_1+V_{C1}-V_2 \\ &\quad -\begin{pmatrix} I_1^{III}(2R_{L-ESR}) \\ +I_1^{III}(R_1+R_{F-D})+V_{D-TH}\end{pmatrix} \\ I_1^{III} &= I_{L1}^{III}=I_{L2}^{III};\quad I_{C2}^{III}\approx I_1^{III}-\left(V_2R^{-1}\right)\end{aligned}\right\} \quad (23)$$

The current through inductors L_1 and L_2 can be expressed as follows,

$$\left.\begin{aligned} &\int_0^{d_1T_S}\left(I_{C2}^I\right)dt+\int_0^{d_2T_S}\left(I_{C2}^{II}\right)dt+\int_0^{T_S(1-d_1-d_2)}\left(I_{C2}^{III}\right)dt=0 \\ &I_L=(1-d_1-d_2)^{-1}V_2R^{-1}\end{aligned}\right\} \quad (24)$$

The output voltage is obtained as follows,

$$\left.\begin{aligned} &\int_0^{d_1T_S}\left(V_L^I\right)dt+\int_0^{d_2T_S}\left(V_L^{II}\right)dt+\int_0^{T_S(1-d_1-d_2)}\left(V_L^{III}\right)dt=0 \\ &\frac{V_2}{V_1}=\frac{\left\{(1+d_1)-\frac{V_{D-TH}}{V_1}(1-d_1-d_2)\right\}}{\left\{\begin{matrix}\frac{2R_Sd_1+R_Sd_2+2R_{L-ESR}}{R(1-d_1-d_2)} \\ +R_{F-D}(1+d_1-d_2)\end{matrix}\right\}+(1-d_1-d_2)} \\ &\quad +\frac{V_{C1}}{V_1}\end{aligned}\right\} \quad (25)$$

where V_{C1}/V_1 is as follows,

$$\left.\begin{aligned} &\frac{V_{C1}}{V_1}\approx 1-\frac{I_1R_1+V_{D-TH}+I_{D1}(R_{F-D})+I_{S1}R_{S(ON)}}{V_1} \\ &I_1R_1=\text{voltage drop across resistance } R_1 \\ &V_{D-TH}+I_{D1}(R_{F-D})=\text{voltage drop across diode } D_1 \\ &I_{S1}R_{S(ON)}=\text{voltage drop across switch } S_1\end{aligned}\right\} \quad (26)$$

Let's assume, power loss due to switching of switches S_1, S_2, and S_3 is P_{S1-SW}, P_{S2-SW}, and P_{S3-SW}, respectively. The total switching power loss P_{S-SW} can be calculated as follows,

$$P_{S-SW}=\sum_{i=1,2,3}P_{Si-SW}=\frac{1}{T_S}\left(\begin{matrix}(t_{r1}+t_{f1})(V_{S1}\times I_{S1}) \\ +(t_{r2}+t_{f2})(V_{S2}\times I_{S2}) \\ +(t_{r3}+t_{f3})(V_{S3}\times I_{S3})\end{matrix}\right) \quad (27)$$

where falling and rising switching time for switches S_1, S_2, and S_3 are represented by t_{f-S1}, t_{f-S2}, t_{f-S3}, and t_{r-S1}, t_{r-S2}, t_{r-S3}, respectively. The average current and voltage through/across switches is represented by I_{S1}, I_{S2}, I_{S3} and V_{S1}, V_{S2}, V_{S3}, respectively. The total power at input and output port is obtained as follows,

$$\left.\begin{aligned} P_1 &= V_1\left(\begin{matrix}I_{L1}d_1+I_{L2}d_1+I_{C1}d_1+\frac{1}{2}I_{L1}d_2 \\ +\frac{1}{2}I_{L2}d_2+I_L(1-d_1-d_2)\end{matrix}\right)+P_{S-SW} \\ P_1 &= \frac{V_1V_2\,(1+d_1)}{R\,(1-d_1-d_2)}+V_1I_{C1}d_1+P_{S-SW}, P_2=V_2^2/R\end{aligned}\right\} \quad (28)$$

The efficiency of the DDTM converter is calculated as follows,

$$\eta=\frac{V_2/V_1}{\frac{(1+d_1)}{(1-d_1-d_2)}+\frac{2\pi V_1^2C_1d_1}{T_S}+P_{SW}} \quad (29)$$

IV. COMPARISON OF DDTM WITH EXISTING CONVERTER

Table-1 tabulates the detail comparison of proposed DDTM converter and existing converter. In [15], diode, capacitor and switched inductor network is used with SEPIC and ZETA converter to enhance the voltage gain. However, the voltage gain is not enhanced with high factor although using multiple capacitors and switched inductor network. In [28], three different converter circuitries (converter-1,2,3) are proposed by using two switches and diode-capacitor network. However, there is only slight improvement in voltage gain compared to switched inductor boost converter though using two inductor and capacitor network along with two switches. Moreover, these converters operation is dependent on the single duty. Therefore, these configurations are not suitable solution to achieve higher voltage gain with wide range of duty ratio. Compared to the proposed converter, the converter mentioned in case 7 of table 1 utilizing one additional capacitor to lift the voltage. If consider $d = d_1 + d_2$, theoretically, the gain of the converter of case 7 provides a higher voltage gain. However, in structure of the converter (case 7), extra clamping

TABLE 1. DDTM converter comparison with recently proposed DC-DC converter for higher voltage.

	$G_{CCM}=V_2/V_1$	Normalized intermediate capacitor voltage rating (V_c/V_2)	Normalized PIV of diode		Normalized switch voltage	Number of			
			Load side diodes (V_d/V_2)	Intermediate diodes (V_d/V_2)		N_S	N_C	N_I	N_D
1	$1/(1-d)$	-	-1	-	1	1	1	1	1
2	$(1+d)/(1-d)$	-	-1	$-1/G_{CCM}$, $-(G_{CCM}-1)/2G_{CCM}$	1	1	1	1	4
3	$(1+d)/(1-d)$	$-(G_{CCM}-1)/2G_{CCM}$	$-G_{CCM}+1)/2G_{CCM}$	-	$(1+G_{CCM})/2G_{CCM}$	1	3	1	3
4	$(2-d)/(1-d)$	$1/G_{CCM}$	$(G_{CCM}-1)/G_{CCM}$	-	$(G_{CCM}-1)/G_{CCM}$	1	4	2	3
5	$(1+d)/(1-d)$	-	$-(G_{CCM}+1)/2G_{CCM}$	$-(G_{CCM}+1)/2G_{CCM}$	$(G_{CCM}+1)/2G_{CCM}$	2	1	2	1
6	$2/(1-d)$	$1/G_{CCM}$	-1	$-1/2$	S_1 and $S_2=1/2$	2	2	2	2
7	$(3-d)/(1-d)$	$1/G_{CCM}$	$-(G_{CCM}-1)/G_{CCM}$	$-(G_{CCM}-1)/2G_{CCM}$	S_1 and $S_2=(G_{CCM}-1)/2G_{CCM}$	2	3	2	3
8	$(1-d_1)/(1-d_1-d_2)$	-	-1	$-1/G_{CCM}$	S_1 and $S_2=(G_{CCM}+1)/2G_{CCM}$, $S_3=1$	3	1	2	2
9	$(2-d_2)/(1-d_1-d_2)$	$1/G_{CCM}$	$-(G_{CCM}-1)/2G_{CCM}$	$-(G_{CCM}-1)/G_{CCM}$	S_1 and $S_2=1/2$, $S_3=(G_{CCM}-1)/G_{CCM}$	3	2	2	2+1*

1: Classical boost converter, 2: Boost converter with switched inductor [28], 3: Converter derived from ZETA converter 15], 4: Converter derived from SEPIC [15], 5: converter -1 [28], 6: converter-2 [28], 7: converter-3 [28], 8: converter in [29], 9: Proposed DDTM converter, N_S: Number of switches, N_C: Number of capacitors, N_I: Number of inductors, N_D: Number of diodes.
*additional one diode is required to make switch S_3 unidirectional for current.

stage (capacitor and diode) is utilized to boost the voltage; it's obvious utilization of additional reactive components offer higher gain. Moreover, practically increasing the reactive components and operate such a converter at a higher duty ratio is not a feasible solution. Theoretically, using classical boost converter (case 1) and existing converter (case 2 to 7) which uses single duty ratio, very higher voltage gain can be attained at duty ratio closer to unity (infinity at duty ratio = 1). However, practically the converter suffer to achieve high step-up voltage gain due to the effect of the series resistance of capacitor and inductor, electromagnet interference (EMI), and need high rating components and semiconductor devices. Moreover, the switches of the converter (case 1 to 7 in table 1) continuously ON when operates at higher duty ratio. Hence there is requirement of large heat sink.

In [29], high gain converter is proposed with two inductors, three switches and two types of duty ratios. However, the converter provides a low voltage gain compared to proposed DDTM converter. Moreover, among converters discussed in Table 1, the proposed DDTM converters provide high gain at given duty ratio and have higher duty range and required low voltage switches (except case 7; however, the converter mentioned in case 7 is restricted by duty ratio). It is noteworthy that the DDTM converter provides a option to adjust voltage gain by selecting appropriate duty ratios which is not possible from any converter (case 1 to 7) that is operated on single duty ratio.

V. EXPERIMENTAL RESULTS

A. PROTOTYPE DESCRIPTION

The prototype is developed in the laboratory to investigate and validate the performance and theoretical analysis of the DDTM converter. The designed prototype is shown in Fig. 15 and the parameters are shown in Table 2. The prototype is built with considering the parameters: power 500W, output/input voltage 400V/38V, and typical duty ratio $d_1 = 50\%$ and $d_2 = 35\%$. Two ferrite core identical inductor L_1 and L_2 with inductance 500μH, capacitor C_1 with 100μF/50V (two 50μF/50V capacitors in parallel), capacitor C_2 with 100μF/450V (two 50μF/450V capacitors in parallel), Flat-type heat sink for diodes (STTH30R04) and

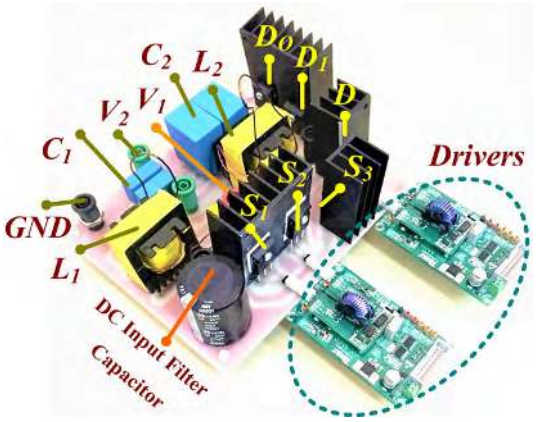

FIGURE 15. Designed prototype of proposed converter with power 500W. *DC input voltage is filter through capacitor 470uF/250V.

TABLE 2. Parameter of designed prototype.

Parameter	Value
Output and Input voltage	400V and 38 V
duty ratio*	d_1=50% and d_2=35%
Inductors L_1	500µH
Capacitors C_1	100 µF/50 V
Capacitors C_2	100 µF/450 V
Diodes D, D_1, D_2	STTH30R04
Switches (MOSFET)	FDP19N40
Pulse generation	FPGA
Gate driver	GDX-4A2S1

* Typical set of duty ratios to achieve desired output; however, the designed converter is tested at various set of duty ratios and investigated.

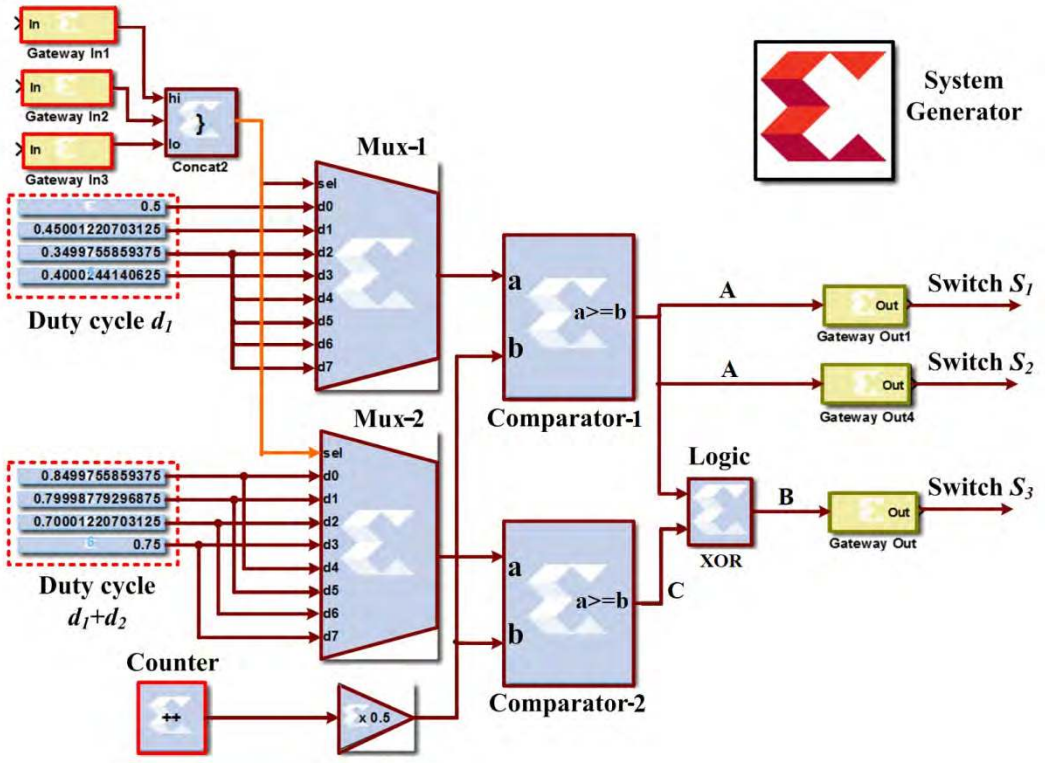

FIGURE 16. Block diagram of switching gate pulse generation scheme used for proposed DDTM converter.

switches FDP19N40 are used to design the circuitry of the DDTM converter.

B. PULSE GENERATION SCHEME AND LOGIC

Fig. 16 depicts the block diagram of switching gate pulse generation scheme which is used to test the performance of the proposed converter at different set of duty ratios. The switching gate pulse generation scheme is designed by using multiplexer, comparator, logic, constant, and counter blocks. The waveform associated with pulse generation scheme is shown in Fig. 17. Two 8:1 multiplexers (Mux-1 and Mux-2) are used to select the value of duty ratio. Four different values (50%, 45%; 40%, 35%) are provided for the duty ratio d_1 and the required value is selected through Mux-1. Mux-2 is used to select the value of d_1+d_2 from the given four different values (85%, 80%; 75%, 70%). Using counter block, sawtooth carrier waveform is generated and compared with output of Mux-1 to generate switching gate pulses (A in Fig. 17) for switches S_1 and S_2. The output of Mux-2 is compared with generated sawtooth carrier to generate pulse with duty ratio $d_1 + d_2$ (C in Fig. 17). Finally, the waveform A is XOR with waveform C to generate pulse (B in Fig. 17) for switch S_3. The 50kHz switching pulses with different 7 sets of duty ratios ($d_1 = 50\%$, $d_2 = 35\%$ (typical set); $d_1 = 45\%$, $d_2 = 35\%$; $d_1 = 40\%$, $d_2 = 35\%$; $d_1 = 35\%$, $d_2 = 35\%$; $d_1 = 35\%$, $d_2 = 35\%$; $d_1 = 35\%$, $d_2 = 40\%$; $d_1 = 35\%$, $d_2 = 45\%$; $d_1 = 35\%$, $d_2 = 50\%$) are

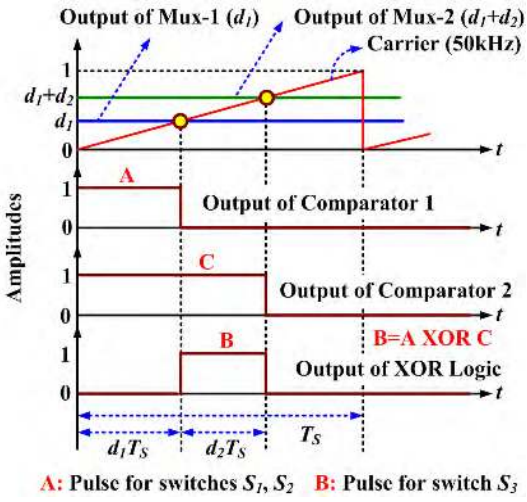

FIGURE 17. Waveform associated with pulse generation scheme.

generated using FPGA in order to investigate the effect duty ratios on voltage gain, performance, and efficiency of the DDTM converter. According to logic, switches S_1 and S_2 are turned ON with same switching pulse whereas switch S_3 is turned ON when switches S_1 and S_2 are turned OFF. Therefore, in mode I, switches S_1, S_2, and S_3 are turned ON, ON, OFF, respectively. In mode II, switches S_1, S_2, and S_3 are turned OFF, OFF, ON, respectively. In mode-III; all the switches S_1, S_2, S_3 are turned OFF.

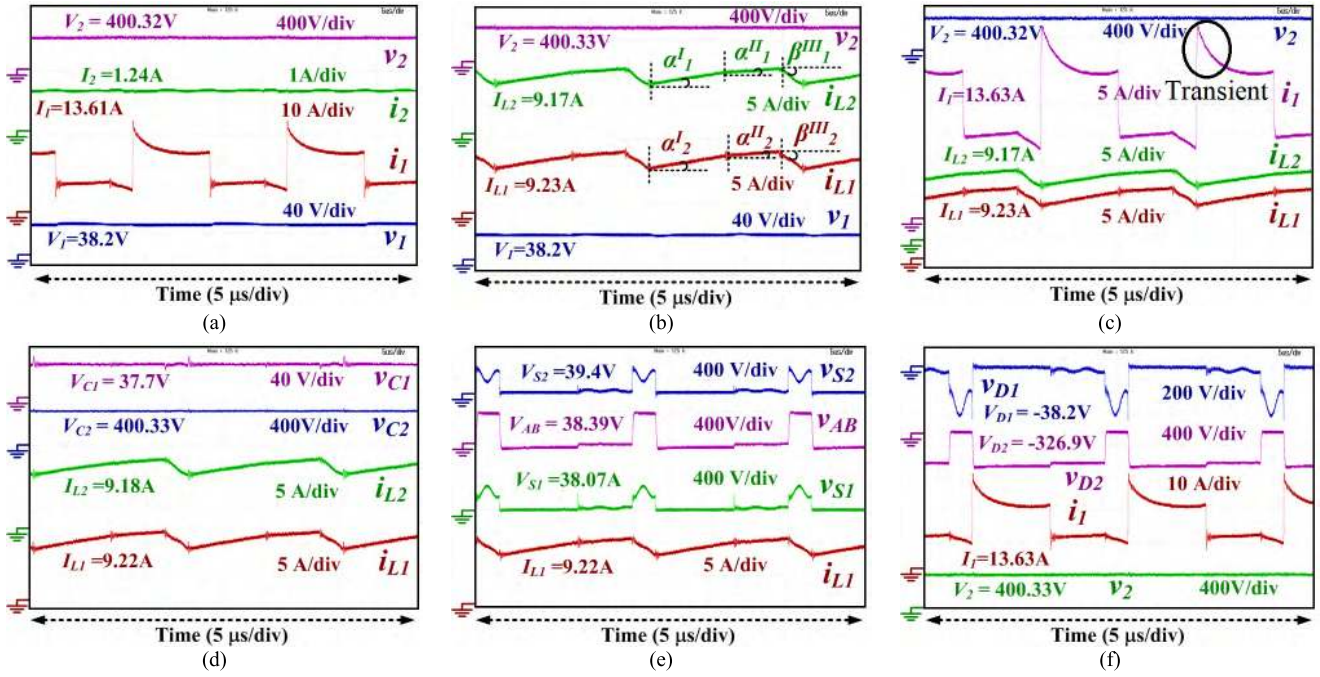

FIGURE 18. Experimental results (a) input, output voltage (v_1, v_2) and input, output current (i_1, i_2), (b) inductor L_1 and L_2 (i_{L1} and i_{L2}) currents and input, output voltage (v_1, v_2), (c) input current (i_1), output voltage (v_2), inductor L_1 and L_2 current (i_{L1} and i_{L2}), (d) capacitor C_1 and C_2 voltages, inductor L_1 and L_2 (i_{L1} and i_{L2}) currents, (e) voltage across switches S_1, S_2, S_3, and inductor L_1 current, (f) voltage across diode D_1 and D_2, input current (i_1), and output voltage (v_2).

C. EXPERIMENTAL RESULTS AT TYPICAL DUTY RATIO

The above discussed pulse generation scheme is utilized to generate two gate pulses; one for switch S_1 and S_2 with duty ratio 50% (d_1), and second for switch S_3 with delay 50% of T_S (d_1), and duty ratio 35% (d_2).

Fig. 18(a) shows experimental observed waveforms of input, output voltage (v_1, v_2) and input, output current (i_1, i_2). The observed average values of input voltage (V_1), output voltage (V_2), input current (I_1), and output current (I_2) is 38.2V, 400.32V, 1.24A, 13.61A, respectively. Fig. 18(b) shows experimental observed waveforms of inductor L_1 and L_2 (i_{L1} and i_{L2}) currents along with input, output voltage (v_1, v_2). The observed average value of inductor L_1 current (I_{L1}), inductor L_2 current (I_{L2}) is 9.23A and 9.17A, respectively. It is clearly visible that both inductors L_1 and L_2 are charged in mode I and mode II. In Fig. 18(b), it is practically seen that the magnetizing angles for both inductors in mode II are nearly half of the magnetizing angles for both inductors in mode I (i.e $\alpha_1^I = 2\alpha_1^{II} = \alpha_2^I = 2\alpha_2^{II}$) which is expected according to theory. It is noteworthy that both the inductors are charging with same magnetizing angles (i.e $\alpha_1^I = \alpha_2^I$ and $\alpha_1^{II} = \alpha_2^{II}$). It is clearly visible that both inductors L_1 and L_2 are discharged in mode III with same demagnetizing angle (i.e $\beta_1^{III} = \beta_2^{III}$).

Fig. 18(c) shows experimental observed waveforms of input current (i_1), output voltage (v_2), inductor L_1 and L_2 current (i_{L1} and i_{L2}). It is clearly visible that the both inductor currents (i_{L1} and i_{L2}) in mode II and III are same as input current. In starting mode I, the transient current observed in the input current due to charging of capacitor C_1 as shown in Fig. 18(c). Fig. 18(d) shows experimental observed waveforms of capacitor C_1 and C_2 voltages along with inductor L_1 and L_2 (i_{L1} and i_{L2}) currents. The observed value of capacitor C_1 voltage (V_{C1}), capacitor C_2 voltage (V_{C2}) is 37.7V, and 400.33V, respectively. It is notable that the voltage across capacitor C_1 is nearly equal to input and voltage across capacitor C_2 is equal to output voltage with is expected. Fig. 18(e) shows experimental observed waveforms of voltage across switches S_1, S_2 and S_3 along with inductor L_1 current. The total average voltage across switch S_1 is 38.07V. The total average voltage across switch S_2 is 39.4V. The total average voltage across switches S_3+diode D (V_{AB}) is 38.39V, respectively. The voltage across diode D_1 and D_2, input current and output voltage is shown in Fig. 18(f). The total average voltage across diode D_1 and D_2 is -38.2V and -326.9V, respectively. It is observed that the diode D_1 and D_2 are forwards biased during mode I and III, respectively.

D. EXPERIMENTAL RESULTS WITH REGULATION IN DUTY RATIO

At constant load $R = 320\Omega$, duty ratio $d_2 = 35\%$, and input voltage 38V; the duty ratio d_1 is regulated from 50 to 35% with the interval of 5% in order to investigate effect duty ratio on voltage gain, performance, and efficiency of the DDTM converter. The obtained waveform of input, output voltage (v_1, v_2) and input, output current (i_1, i_2) is shown in Fig. 19. When $d_1 = 50\%$ and $d_2 = 35\%$ (W in Fig. 19), the average output voltage, output current, input current are 400.32V, 1.24A, and 13.61A, respectively. When $d_1 = 45\%$ and $d_2 = 35\%$ (X in Fig. 19), the average output voltage,

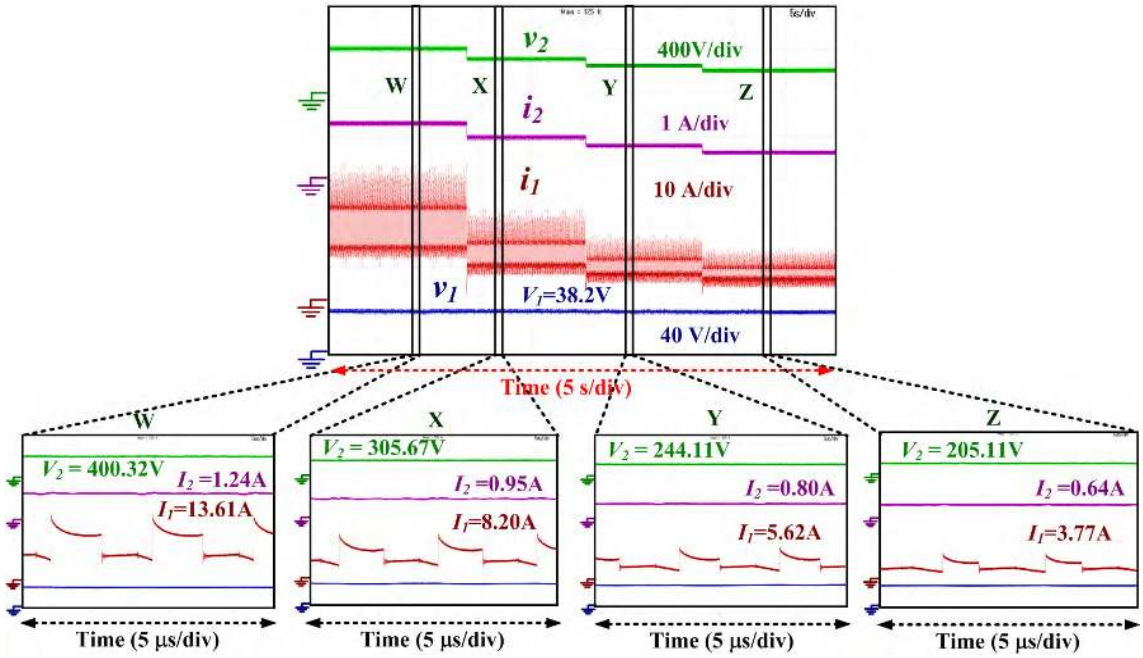

FIGURE 19. Experimental observed waveforms: input, output voltage (v_1, v_2) and input, output current (i_1, i_2), W: $d_1 = 50\%$, $d_2 = 35\%$, X: $d_1 = 45\%$, $d_2 = 35\%$, Y: $d_1 = 40\%$, $d_2 = 35\%$, Z: $d_1 = 35\%$, $d_2 = 35\%$.

output current, input current are 305.67V, 0.95A, and 8.20A, respectively. When $d_1 = 40\%$ and $d_2 = 35\%$ (Y in Fig. 19), the average output voltage, output current, input current are 244.11V, 0.80A, and 5.62A, respectively. When $d_1 = 35\%$ and $d_2 = 35\%$ (Z in Fig. 19), the average output voltage, output current, input current are 205.11V, 0.64A, and 3.77A, respectively.

At constant load $R = 320\Omega$, duty ratio $d_1 = 35\%$, and input voltage 38V; the duty ratio d_2 is regulated from 35 to 50% with the interval of 5% in order to investigate effect duty ratio on voltage gain, performance, and efficiency of the DDTM converter. The obtained waveform of input, output voltage (v_1, v_2) and input, output current (i_1, i_2) is shown in Fig. 20. When $d_1 = 35\%$ and $d_2 = 35\%$ (W in Fig. 20), the average output voltage, output current, input current are 205.11V, 0.64A, and 3.77A, respectively. When $d_1 = 35\%$ and $d_2 = 40\%$ (X in Fig. 20), the average output voltage, output current, input current are 236.97V, 0.73A, and 4.95A, respectively. When $d_1 = 35\%$ and $d_2 = 45\%$ (Y in Fig. 20), the average output voltage, output current, input current are 282.83V, 0.88A, and 7.06A, respectively. When $d_1 = 35\%$ and $d_2 = 50\%$ (Z in Fig. 20), the average output voltage, output current, input current are 358.2V, 1.08A, and 10.76A, respectively. Based on the experimental investigation, the efficiency graphs are plots by considering the regulation of duty ratio. Fig. 21(a) shows the plot of efficiency versus power of DDTM converter where duty d_1 is varying and d_2 is constant (35%). Fig. 21(b) shows the plot of efficiency versus power of DDTM converter where duty d_2 is varying and d_1 is constant (35%). Highest 95.47% efficiency is reported at $d_1 = 50\%$ and $d_2 = 35\%$. After conducting several tests, 93.43% is observed average efficiency of DDTM converter.

VI. FUTURE SCOPE-DIFFERENT CONTROL SCHEMES

The output voltage of proposed DDTM converter is based on the two duty ratios d_1 and d_2. Owing to advantages of two duty ratios, when the voltage changed the operation of proposed converter can be controlled in three possible ways 1) fixed duty ratio d_1 and variation in duty ratio d_2, 2) variation in duty ratio d_1 and fixed duty ratio d_2, and 3) variation in both duty ratio d_1 and d_2.

A. CONTROL SCHEME-1: FIXED DUTY RATIO d_1 AND VARIATION IN DUTY RATIO d_2

In this scheme, during perturbations of input voltage V_1, the output voltage V_2 is controlled at constant value by variation in duty ratio d_2. The pulses associated this operation is shown in Fig. 22, where duty ratio d_2 is changed by $+/-\Delta d_2$ to achieve required output voltage V_2. The value of $+/-\Delta d_2$ is based on the perturbation in input voltage $-/+\Delta V_1$.

B. CONTROL SCHEME-2: FIXED DUTY RATIO d_2 AND VARIATION IN DUTY RATIO d_1

In this scheme, during perturbations of input voltage V_1, the output voltage V_2 is controlled at constant value by variation in duty ratio d_1. The pulses associated this operation is shown in Fig. 23, where duty ratio d_1 is changed by $+/-\Delta d_1$ to achieve required output voltage V_2. It is noticeable that the duty ratio d_2 is constant; however position is changed according to new duty ratio d_1. The value of $+/-\Delta d_1$ is based on the perturbation in input voltage $-/+\Delta V_1$.

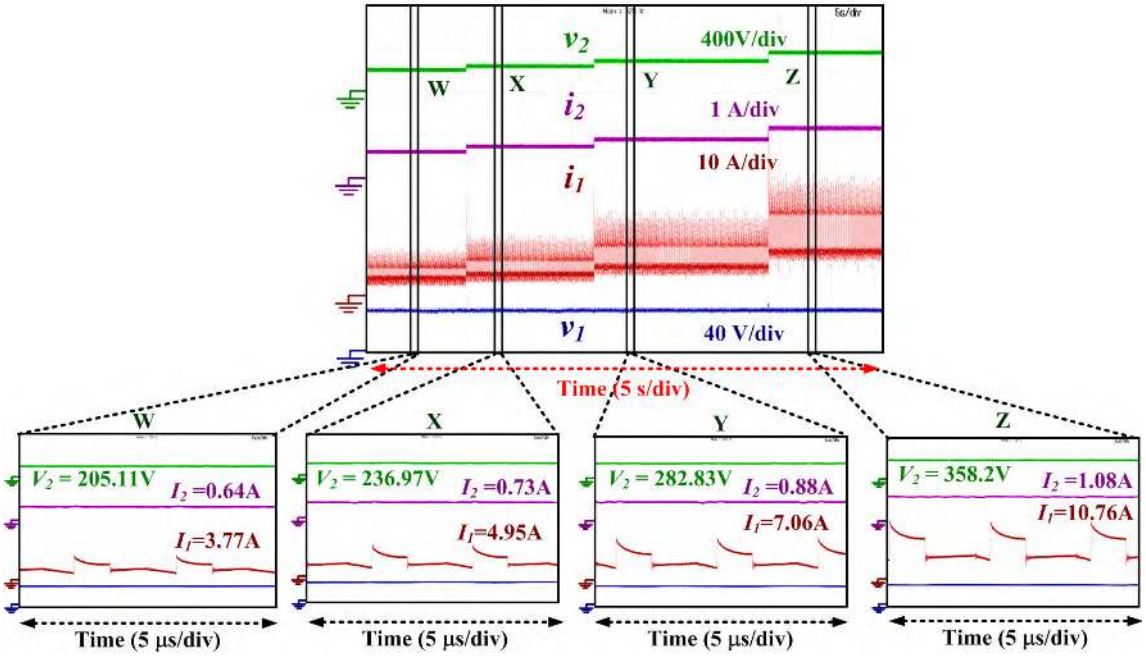

FIGURE 20. Experimental observed waveforms: input, output voltage (v_1, v_2) and input, output current (i_1, i_2), W: $d_1 = 35\%$, $d_2 = 35\%$, X: $d_1 = 35\%$, $d_2 = 40\%$, Y: $d_1 = 35\%$, $d_2 = 45\%$, Z: $d_1 = 35\%$, $d_2 = 50\%$.

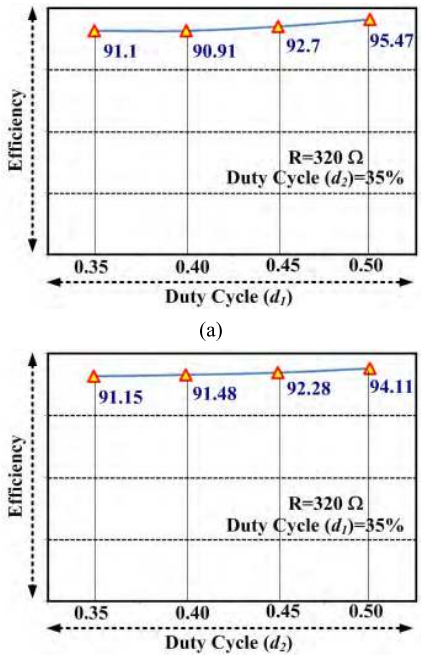

FIGURE 21. Efficiency of the DDTM converter at the different set of duty ratios (a) variation in duty ratio d_1 with maintain constant load and duty ratio $d_2 = 35\%$, (b) variation in duty ratio d_2 with maintain constant load and duty ratio $d_1 = 35\%$.

C. CONTROL SCHEME-3: VARIATION IN BOTH DUTY RATIOS d_1 AND d_2

In this scheme, during perturbations of input voltage V_1, the output voltage V_2 is controlled at constant value by variation in both duty ratios d_1 and d_2. The pulses associated

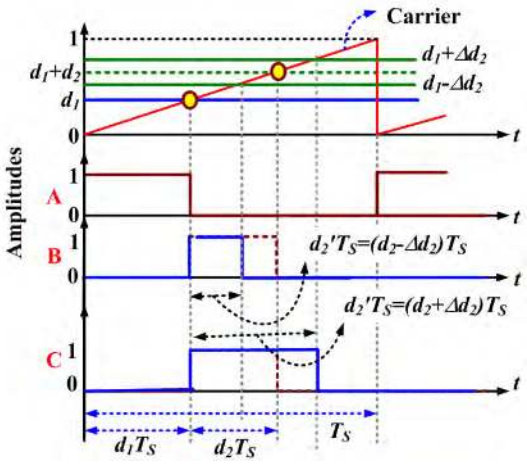

FIGURE 22. Gate pulses during control scheme-1 (A: gate pulse of switches S_1 and S_2, B: changed in gate pulse of switch S_3 when input voltage is increased, C: changed in gate pulse for switch S_3 when input voltage is reduced).

this operation is shown in Fig. 24, where duty ratios d_1 and d_2 are changed by $+/-\Delta d_1$ and $+/-\Delta d_2$ to achieve required output voltage V_2. It is noticeable that the duty ratios d_1 and d_2 is varied as well as the position of duty ratio d_2 is changed according to new duty ratio d_1. The value of $+/-\Delta d_1$ and $+/-\Delta d_2$ is based on the perturbation in input voltage $-/+\Delta V_1$. For this scheme, variation of both duty ratios d_1 and d_2 can be possible in six different ways (given in Table-3). It is noticeable that increment or decrement in one duty ratio and decrement or increment in another duty ratio also possible to achieved desired output voltage.

TABLE 3. Summery of possible control scheme during perturbation of input voltage.

Control Scheme	Perturbation in input voltage	Previous duty ratio (d_1)	New duty ratio (d_1')	Previous duty ratio (d_2)	New duty ratio (d_2')	changed in position of duty ratio (d_2)
1	$V_1+\Delta V_1$	d_1	d_1	d_2	$d_2-\Delta d_2$	No
	$V_1-\Delta V_1$	d_1	d_1	d_2	$d_2+\Delta d_2$	No
2	$V_1+\Delta V_1$	d_1	$d_1-\Delta d_1$	d_2	d_2	Yes
	$V_1-\Delta V_1$	d_1	$d_1+\Delta d_1$	d_2	d_2	Yes
3	$V_1+\Delta V_1$	d_1	$d_1-\Delta d_1$	d_2	$d_2-\Delta d_2$	Yes
		d_1	$d_1-\Delta d_1$	d_2	$d_2+\Delta d_2$	Yes
		d_1	$d_1+\Delta d_1$	d_2	$d_2-\Delta d_2$	Yes
	$V_1-\Delta V_1$	d_1	$d_1+\Delta d_1$	d_2	$d_2+\Delta d_2$	Yes
		d_1	$d_1-\Delta d_1$	d_2	$d_2+\Delta d_2$	Yes
		d_1	$d_1+\Delta d_1$	d_2	$d_2-\Delta d_2$	Yes

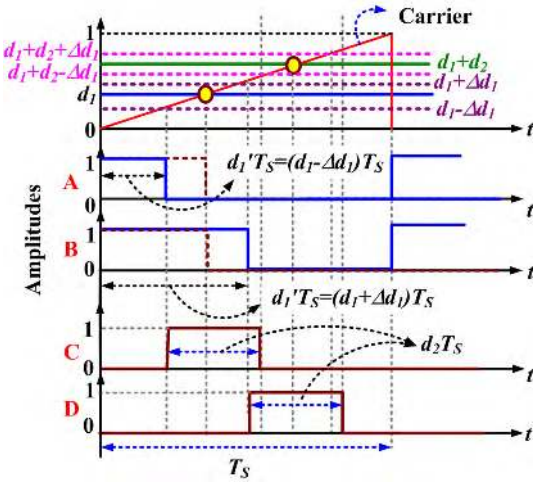

FIGURE 23. Gate pulses during control scheme-2 (A: changed in gate pulse of switch S_1 and S_2 when input voltage is increased, B: changed in gate pulse of switch S_1 and S_2 when input voltage is reduced, C: changed in position of gate pulse of switch S_3 when input voltage is increased, D: changed in position of gate pulse of switch S_3 when input voltage is reduced).

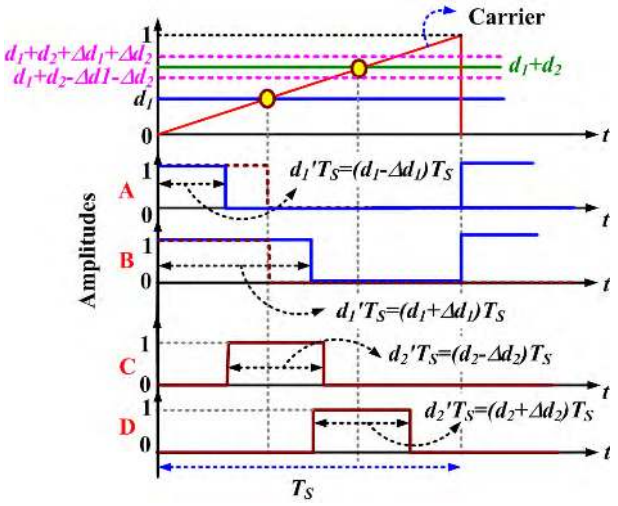

FIGURE 24. Gate pulses during control scheme-3 (A: changed in gate pulse of switch S_1 and S_2 when input voltage is increased, B: changed in gate pulse of switch S_1 and S_2 when input voltage is reduced, C: changed in position and duty ratio of gate pulse of switch S_3 when input voltage is increased, D: changed in position and duty ratio of gate pulse of switch S_3 when input voltage is reduced).

The control scheme-1 and scheme-2 can be called half or independent control schemes. Since during perturbation of input voltage v_1, only one duty ratio is varied to achieve required output voltage V_2 and the value of another duty ratio is fixed throughout the operations (d_1 is fixed in scheme-1 and d_2 is fixed in scheme-2). The control scheme-3 is called full or dependent control schemes. During perturbation of input voltage v_1, the value of both duty ratio d_1 and d_2 is varied and dependent on each other throughout the operation.

Due to high voltage gain, unidirectional power flow, wide duty range operation, and flexibility in control and selection of duty ratio, the proposed converter is more suitable and good choice for 400V DC microgrid PV application.

Additional advantages could be a scenario in that, in future the proposed converter provides an option that one may use one duty ratio for MPPT tracking and another to control output voltage.

VII. CONCLUSION

A new Double-Duty-Triple-Mode (DDTM) converter is proposed with high voltage gain for DC microgrid application. The proposed converter topology is transformer-less and has wide duty ratio range. The higher voltage gain is achieved without employing any complex techniques like multiplier, coupled inductor, and multiple lifting techniques. The operating principle, CCM and DCM characteristics waveform, and efficiency analysis is presented in detail. The main advantages of the DDTM converter is that the voltage gain is adjusted by controlling two different duty ratios and thus, offers wide operating duty range which is not possible through any single switch converter. The DDTM converter is compared with existing topologies and it is noteworthy that the proposed converter provides a good choice to attain high voltage with reduced voltage stress on semiconductor and component count. The future scope and advantages of two duty ratios in proposed circuit and its control is discussed. The experimental results are presented which validate the performance and theoretical analysis.

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