High-k Dielectric Double Gate Junctionless (DG-JL) MOSFET for Ultra Low Power Applications- Analytical Model

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High-k Dielectric Double Gate Junctionless (DG-JL) MOSFET for Ultra Low Power Applications- Analytical Model

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Abstract

This paper describes the impression of low-k/high-k dielectric on the performance of Double Gate Junction less (DG-JL) MOSFET. An analytical model of the threshold voltage of DG-JLFET has been presented. Poisson's equation is solved using the parabolic approximation to find out the threshold voltage. The effect of high-k on various performance parameters of N-type DG-JLFET is explored. The comparative analysis has been carried out between conventional gate oxide, multi oxide and high-k oxide in terms of Drain Induced Barrier Lowering (DIBL), threshold voltage, figure of merit (I_{ON}/I_{OFF}) and sub-threshold slope (SS). The high-k oxide has shown superlative performance as compared to others. The results are further analyzed for various device structures. The DG-JLFET with HfO_2 exhibits excellent attainment by mitigating the Short Channel Effects (SCEs). The significant reduction in off current makes the device suitable for ultra-low power applications. There is a 61.9 % and 34.29% improvement in the figure of merit and sub-threshold slope in the proposed device as compared to other devices. The simulation of DG-JLFET is carried out using the Silvaco TCAD tool.

Keywords: Junctionless MOSFET, Gate stack, DIBL, SS, SCEs.

1. INTRODUCTION

The MOSFET has been introducing in the field of electronics for more than 50 years. MOSFET is used to make an integrated circuit to act as a switch. Aggressive downscaling of gate oxide leads to more leakage current in the device. The scaling of MOSFET produces new challenges and opportunities for the device engineer. The short channel effects occur at a nanoscale size which mitigates the device performance. Many new device structures have been investigated to reduce the SCEs. Multi-gate devices have been preferred over single gate MOSFET due to their scalability. The necessity of abrupt p-n junctions between source/drain region and channel put the challenges in doping profile technique. Junctionless design is proposed by Colinge et al. [1] The absence of p-n junction between source/drain and the channel region is due to zero doping concentration gradient implies the presence of same doping in source/channel/drain regions increases effective channel length which reduces the short channel effects in Junctionless MOSFET [2-6].

To improve the performance in DG-JLFET for the parameters such as off current, on current, transconductance, DIBL and threshold voltage, many gate and channel engineering approaches are adopted [7-10]. The gate dielectric materials are required mainly for having good insulating properties and high capacitance value [11-13]. The gate dielectric materials should be able to prevent the diffusion of dopants. It should have good thermal stability and very good interface adhesion with the substrate.

However, the utilization of high-k materials improves the control of the gate and results in the reduction of SCEs along with all the above qualities [14-15]. The Lombardi CVT, Shockley-Read-Hall and Drift-diffusion model is utilized for the mobility, recombination and energy transport during the simulation. The Newton method is used for the numerical solution.

An analytical model of DG-JLFET is presented in Section 2. The numerical solution of DG-JLFET using TCAD is described in Section 3. The comparative analyses of DG-JLFET with SiO_2, Multi oxide and HfO_2 have been portraits in Section 4.

2. ANALYTICAL MODELING

The cross-sectional view of short channel DG-JLFET is shown in Figure 1.

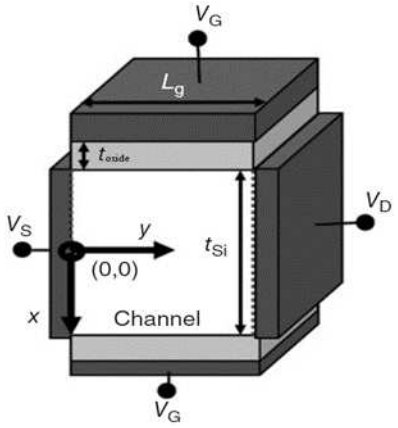
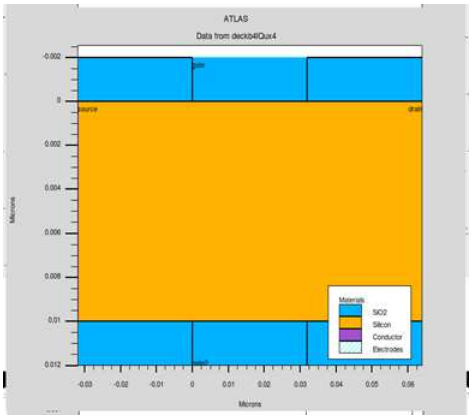
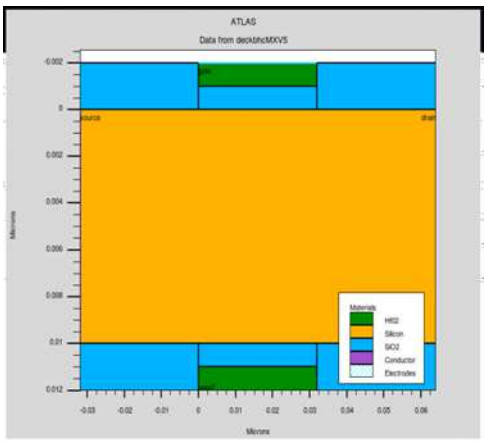


Fig. 1 –Short-channel DG-JLFET.

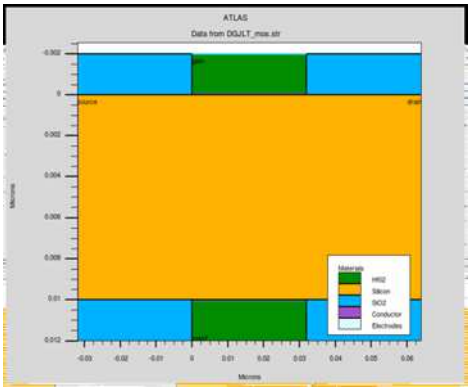


(a)

The N-type DG-JLFETs at 32nm with (a) SiO_2 as dielectric material (b) Multi oxide (SiO_2+HfO_2) as dielectric material and (c) HfO_2 as dielectric material are shown in Figure 2.



(b)



(c)

Fig. 2- The N-type DG-JLFETs at 32nm with a dielectric material as (a) SiO_2 (b) Multi oxide (SiO_2+HfO_2) and (c) HfO_2

The Poisson's Equation for the short-channel DGJLFETs is given as.

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=-\frac{\rho}{\epsilon_{Si}} \quad (1)$$

The parabolic potential approximation is taken in x-direction [16].

$$\Psi(x,y)=\alpha_0(y)+\alpha_1(y)x+\alpha_2(y)x^2 \quad (2)$$

The value of a2 can be found assuming continuity of electric displacement vector we have

$$-C_{OXIDE}\left(V_G-V_F-\Psi_{S,b}\right)=-\epsilon_{Si}\frac{d\Psi\left(\frac{t_{Si}}{2},y\right)}{dx}=-\epsilon_{si}t_{Si}\alpha_2(y) \quad (3)$$

Equation (2) was modified by putting the value of α2.

$$\Psi(x,y)=\Psi_0(y)+\frac{C_{OXIDE}}{\epsilon_{Si}t_{Si}}\left(V_G-V_F-\Psi_s(y)\right)y^2 \quad (4)$$

The relation between the central potential and the surface potential can be represented as

$$\Psi(\frac{t_{Si}}{2},y)=\Psi_S(y)=\Psi_0(y)+\frac{C_{OXIDE}t_{Si}}{4\epsilon_{Si}}\left(V_G-V_F-\Psi_s(y)\right) \quad (5)$$

The surface potential can be obtained by simplifying the above equation as

$$\Psi_S(y)=\frac{\Psi_0(y)+\frac{C_{OXIDE}t_{Si}}{4\epsilon_{Si}}(V_G-V_F)}{1+\frac{C_{OXIDE}t_{Si}}{4\,\epsilon_{Si}}} \quad (6)$$

By putting the value of ΨS from equation (6) to equation (4) we get

$$\Psi(x,y)=\Psi_0(y)+\frac{C_{OXIDE}}{\epsilon_{Si}t_{Si}}\left(V_G-V_F-\frac{\frac{t_{Si}C_{OXIDE}}{4\epsilon_{Si}}(V_G-V_F)+\Psi_0(y)}{1+\frac{t_{Si}C_{OXIDE}}{4\epsilon_{Si}}}\right)y^2 \quad (7)$$

Modifying the equation (1) from the value obtained in equation (7) as

$$\frac{\partial^2\Psi_0(y)}{\partial y^2}-\frac{8C_{OXIDE}}{C_{OXIDE}t_{Si}^2+4\epsilon_{Si}t_{Si}}\left(\Psi_0(y)-V_G-V_F+\frac{qN_Dt_{Si}}{2C_{OXIDE}}+\frac{qN_Dt_{Si}^2}{8\epsilon_{Si}}\right)=0 \quad (8)$$

The equation (8) can be simplified by considering $1/L_2^2=8C_{oxide}/(4\epsilon_{Si}*t_{Si}+C_{oxide}t_{Si}^2)$, $\xi_0=V_G-\gamma_2$ and $\gamma_2=V_F-[(qN_At_{Si})/2C_{oxide}]-(qN_Dt_{Si}^2)/8\epsilon_{Si}$ Here L_2 is the natural length of DG-JLFET, ξ_0 is long channel central potential. The above equation can be simplified as

$$\frac{\partial^2\Psi_0(y)}{\partial x^2}-\frac{1}{L_2^2}(\Psi_0(y)-\xi_0)=0 \quad (9)$$

The solution of this differential equation is as

$$\Psi_0(y)=\xi_0+a_1e^{\frac{y}{L_2}}+a_2e^{-\frac{y}{L_2}} \quad (10)$$

The value of a_1 and a_2 can be obtained by using boundary conditions which state that the surface potential is the potential at the Silicon-silicon oxide interface, the electric field at the center of the DG-JLFET should be zero due to its symmetric nature and the electrical displacement vector is continuous near to the top and bottom gate at the silicon-silicon oxide interface hence we have

$$\Psi_0(y=0)=V_S=0 \quad (11)$$

$$\Psi_0(y=L_g)=V_D=V_{DS} \quad (12)$$

Hence the value of a_1 and a_2 are

$$a_1=\beta_1V_G+\beta_2 \quad (13)$$

$$a_2=\beta_3V_G+\beta_4 \quad (14)$$

Here the value of β_1, β_4, β_3 and β_4 can be specified as

$$\beta_1=\frac{e^{-\frac{L_g}{L_2}}-1}{2\sinh\left(\frac{L_g}{L_2}\right)} \quad (15)$$

$$\beta_2=\frac{V_{DS}-\gamma_2\left(e^{-\frac{L_g}{L_2}}-1\right)}{2\sinh\left(\frac{L_g}{L_2}\right)} \quad (16)$$

$$\beta_3=\frac{1-e^{\frac{L_g}{L_2}}}{2\sinh\left(\frac{L_g}{L_2}\right)} \quad (17)$$

$$\beta_4=\frac{-V_{DS}+\gamma_2\left(e^{-\frac{L_g}{L_2}}-1\right)}{2\sinh\left(\frac{L_g}{L_2}\right)} \quad (18)$$

After calculating the value of a_1 and a_2, the expression for analytical relation can be solved. The minimum central potential location can be found by differentiating equation (10). The y_{min} is the location of the minimum central potential can be found as [17]

$$y_{min}=\frac{L_2}{2}\ln\left(\frac{a_2}{a_1}\right) \quad (19)$$

By putting the value of y_{min} in equation (10), the minimum central potential is

$$\Psi_0(y_{min})=\sqrt{a_1a_2}+\xi_0 \quad (20)$$

As in JLFET, when a gate voltage is equal to threshold voltage the channel starts to open [18-20]. Hence at threshold voltage the $\Psi_0(y_{min})=0$. For short-channel DG-JLFETs threshold voltage is given as

$$V_{Th}=\frac{2(\beta_2\beta_3+\beta_1\beta_4)+\gamma_2+\sqrt{(2(\beta_2\beta_3+\beta_1\beta_4)+\gamma_2)^2-(1-4\beta_1\beta_3)(\gamma_2-4\beta_2\beta_4)}}{(1-4\beta_1\beta_3)} \quad (21)$$

The analytical modeling solution for the threshold voltage for short channel DG-JLFETs is given by Equation (21). In the case of long channel DG-JLFETs, the value of β and $\gamma=0$. Hence, the thresh-old voltage for short channel DG-JLFET tends to ω_2, which is equal to the threshold voltage obtained

for long channel DG-JLFET. The effect of high-k material on Threshold voltage in DG-JLFET has been analyzed.

3. RESULTS & DISCUSSION

The numerical simulation of DG-JLFET at 32nm technology node is carried out using the Silvaco TCAD tool. The performance of the DG-JLFET device can be further enhanced by introducing high-k dielectric gate materials. The structures considered for numerical simulations are having the gate oxide as SiO_2, HfO_2 and stack architecture of SiO_2 and HfO_2. These numerical simulations are done with the intention to analyse the characteristics of the device. The physical thickness of oxide is taken as 2nm (in the case of multi oxide 1nm for SiO_2 and 1nm for HfO_2). The work function of both gate materials is taken as 5.2ev. The silicon material is uniformly doped with n-type material with the doping density in the range of 1.5e-19 cm^{-3}. The permittivity of the HfO_2 is taken as 21 and the permittivity of the SiO_2 is taken as 3.9. The results were obtained using the Atlas device simulator and plotted on Tonyplot [21].

3.1 TRANSFER CHARACTERISTICS

Figure 3 depicts the characteristics of drain current in saturation (high V_{DS}) on a logarithmic scale for different oxide materials. The characteristics of SiO_2 as the dielectric for gate oxide are shown with the red line, the green line shows the characteristics of multi-oxide as a dielectric material for the gate oxide and the blue line shows the characteristics of HfO_2 as a dielectric material for the gate oxide. It can be seen from Figure 3 that N-type DG-JLFETs architecture having HfO_2 (oxide permittivity=21) as dielectric material (blue line) has the lowest value of off current. The multi oxide has better off current properties than a device made only with SiO_2. It can also be observed that the on-current of all the devices is of the same order. The sub-threshold slope of the device can also be deduced from Figure 3 and the device having HfO_2 as a gate dielectric has the minimum sub-threshold slope among all compared here.

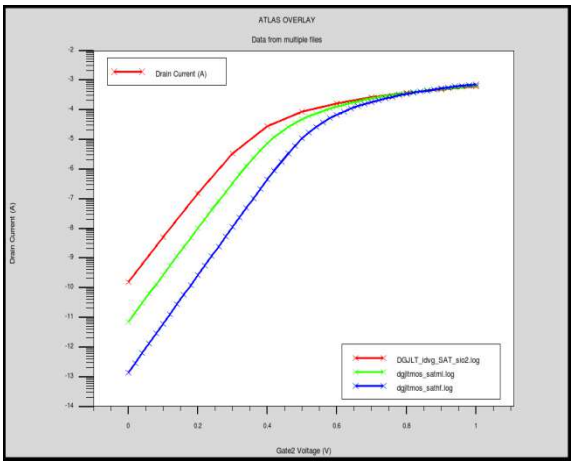


Fig. 3- 32nm N-type DG-JLFETs transfer characteristics with SiO_2, Multi oxide and HfO_2 as gate dielectric materials.

The detailed comparisons for the different dielectric materials obtained from numerical simulation are given in Table 1.

Table 1: 32nm N-type DG-JLFETs Characteristics with Different Oxide

Device	**DG JLT with SiO_2**	**DG JLT with Multi oxide**	**DG JLT with HfO_2**
V_{tsat}	0.293049	0.367348	0.456414
SS_{sat}	0.0661216	0.0628691	0.06094
I_{on}	0.000613	0.00066889	0.000737
I_{off}	1.587 e-10	7.08627 e-12	1.4025 e-13
I_{on}/I_{off}	3.86 e+6	9.4 e+7	5.25 e+9
V_{tlin}	0.324705	0.3987	0.474328
SS_{lin}	0.0664907	0.0632479	0.0611267
DIBL	0.033322	0.03302	0.0188568

3.2 Effect of High-k Material on Various Parameters for N-type DG-JLFETs

Table 1 shows the effects of high-k materials/ high-k materials in stack architecture for N-type DG-SOI MOSFET at 32nm. Some of the variations of characteristics parameters are analyzed as under.

3.2.1 DIBL

The Drain Induced Barrier Lowering or DIBL is given by equation (22).

$$\text{DIBL} = \frac{V_{Th_{lin}} - V_{Th_{sat}}}{V_{sat} - V_{lin}} \tag{22}$$

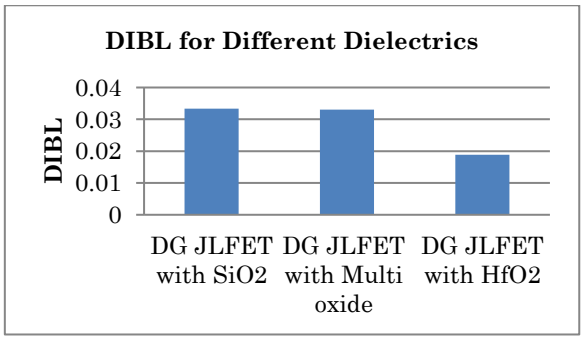


Fig. 4- DIBL for 32nm N-type DG-JLFETs with different dielectric materials.

DG-JLFET with HfO_2 as gate dielectric indicates a lower value of DIBL because of its high value of dielectric constant which in turn enhances the control of gate over the channel and provides low leakage current resulting in lower DIBL.

3.2.2 Threshold Voltage

In JLTFETs when the gate voltage is increased from zero, the channel starts to open. At a particular voltage, the un-depleted region in the middle of the channel vanishes due to the merging of the depleted region; this voltage is called threshold voltage for JLTFETs. It has been observed that at the threshold

voltage the inversion layer carrier density is equal to the bulk carrier concentration. The threshold voltage can be represented by equation (21). Figure 5 depicts the threshold voltage variation for the different dielectric. The percentage enhancement in threshold voltage is 31.54 % for DG-JLFET with HfO_2 compared to DG-JLFET with SiO_2 and 15.94% compared to DG-JLFET with Multi oxide. The device with more value of threshold voltage will produce a low leakage current and will be useful for low power applications.

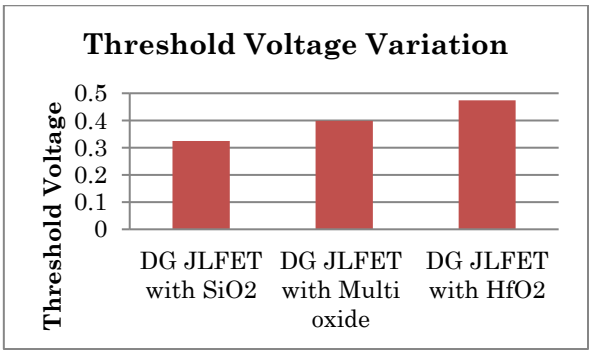


Fig. 5- Threshold voltage variation with different dielectrics.

3.2.3 Sub-threshold Slope

The sub-threshold slope (SS) is a significant design parameter related to MOSFET, it is usually described how fast a device can turn off from the on-state. The SS can be calculated as given by equation (23)

$$SS = \left(\frac{kT}{q}\right) ln_{10}\left(1 + \left(\frac{C_D}{C_{oxide}}\right)\right) \quad (23)$$

SS depends on the first term only and has a value of 60 mV/decade [22]. The effect of high- k materials on the sub-threshold slope of the 32nm DG-JLFETs is shown in Figure 6. The percentage improvement in SS is 8.06 % for DG-JLFET with HfO_2 compared to DG-JLFET with SiO_2 and 3.35% compared to DG-JLFET with Multi oxide. The value of SS is very low points out to a diminution in SCEs.

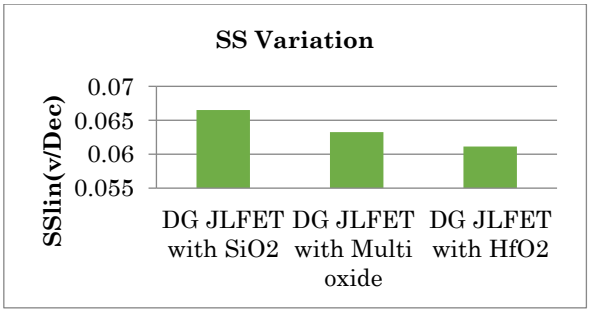


Fig. 6- Sub-threshold slope variation with different dielectrics.

3.2.4 I_{ON}/I_{OFF} Ratio

The I_{ON}/I_{OFF} ratio is also known as the figure of merit. I_{ON} means the current driving capability of the device and I_{OFF} contribute to the power dissipation. The variation of I_{ON}/I_{OFF} with different dielectric materials for 32nm N-type DG-JLFETs is shown in Figure 7. Figure 7 depicts DG-JLFETs with SiO_2

dielectric have a smaller value of I_{ON}/I_{OFF} ratio as compared to DG-JLFETs with high-k dielectric materials which can be attributed to the fact that strong depletion of a channel occurs with higher barrier potential in high-k devices [23].

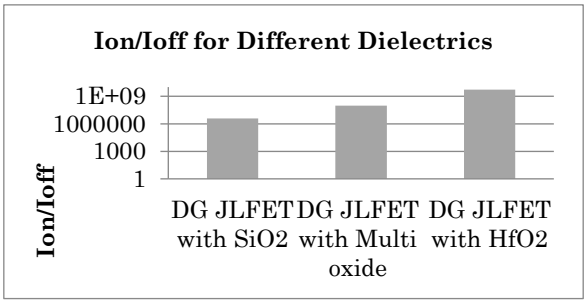


Fig. 7- Variation of I_{ON}/I_{OFF} for DG-JLFETs with different dielectric materials

The high-K dielectric mitigates the leakage current in MOSFET. The DG-JLFETs provide better electrostatic control of the gate on the channel. This will enhance the on-current of the device. So overall, it will increase the I_{ON}/I_{OFF} value as compared to low dielectric constant materials.

4. COMPARATIVE ANALYSIS

The comparisons of transfer characteristics for all the structures of MOSFET viz. Bulk MOSFET, DG-SOI MOSFET and DG-JLTFET for various oxide viz. SiO_2, Multi oxide and HfO_2 are shown in Figure 8.

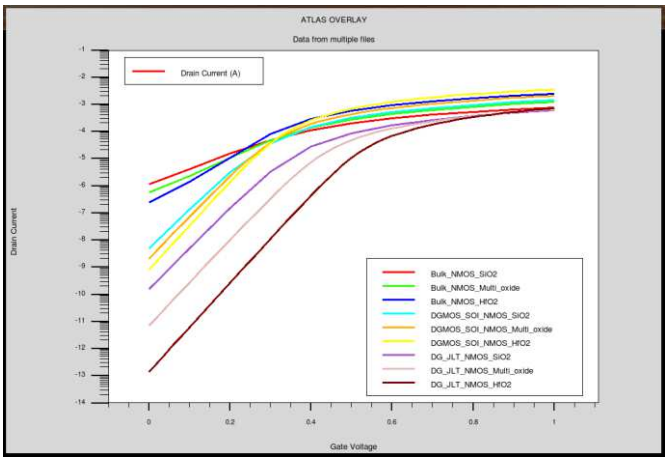


Fig. 8- Transfer characteristics for all the structures for various oxides

Comparison of simulation results in Figure 8 was plotted on the Tonyplot tool of Silvaco. It can be seen from Figure 8 that the MOSFET made using DG-JLTs will give minimum off current and best slope among all compared for about the same order of on current. The DG-JLT MOSFET having gate dielectric is showing the best characteristics for the off current. Hence, the circuit made with DG-JLT MOSFET is expected to give minimum power dissipation. Figure 9 depicts the I_{on}/I_{off} ratio for various structures having different oxides as a gate dielectric.

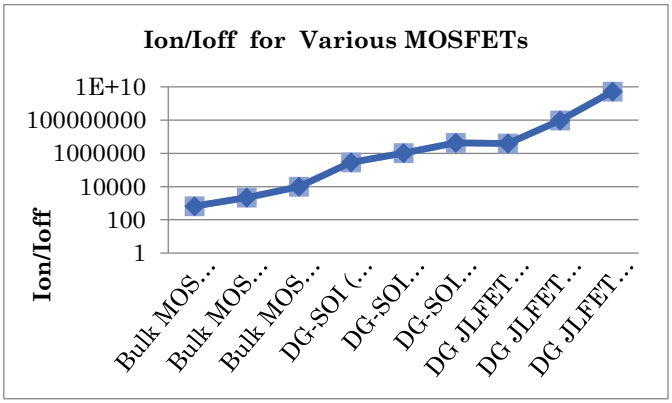


Fig. 9- I_{on}/I_{off} ratio for all the MOS structures

It can be seen from Figure 9 that the MOSFET made with DG-JLT having HfO_2 as dielectric giving a maximum on to off current ratio. A 61.9% enhancement in I_{on}/I_{off} ratio is envisaged in DG-JLT with HfO_2 in contrast to conventional junction less DG-MOSFET [24].

Figure 10 depicts the DIBL for various structures having different oxides as a gate dielectric. MOS structure made with DG-JLT and DG-SOI having almost the same minimum DIBL among the compared structures. DG-JLT reveals significant mitigation in DIBL as compared to DIBL reported as 0.4965 V by Mohd. Bavir [25] and 0.24 V by P. Wang [26]. This makes the device suitable for ultra-low-power range applications. The results are validated by comparing with existing results.

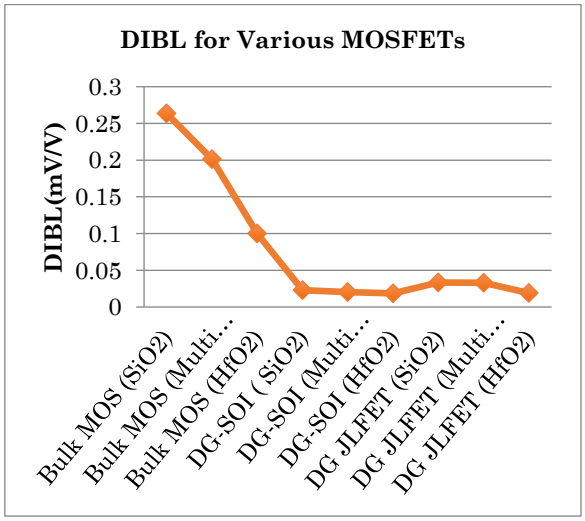


Fig. 10- DIBL for various MOSFETs structures

Figure 11 depicts the sub-threshold slope for various structures having different oxides as a gate dielectric. MOS structure made with DG-JLT and DG-SOI having almost the same minimum sub-threshold slope close to perfect (60mv/Decade) among the compared structures. DG-JLT depicts a significant improvement of 7.4 % in SS as compared to SS reported by Mohd. Bavir [25] and 34.29 % by P Wang [26]. It is a clear indication of improvement in the short channel behavior of the device.

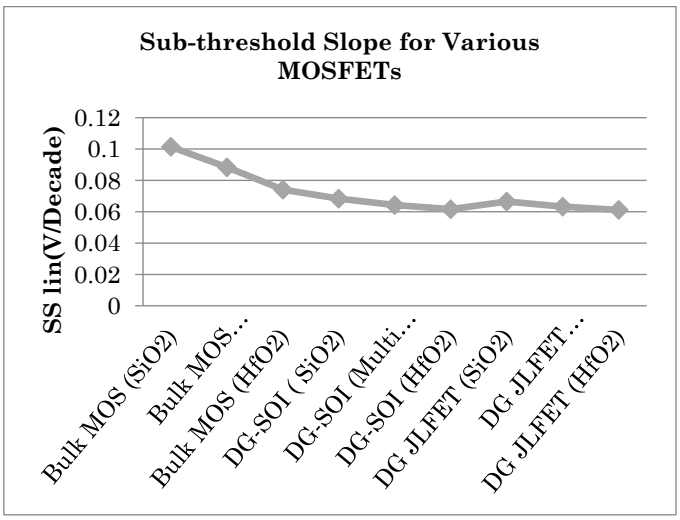


Fig. 11- Sub-threshold slope for various MOSFETs structures

5. CONCLUSION

The analytical modeling for threshold voltage is developed using parabolic approximation in this paper. The numerical simulation of JLFET is also carried out using TCAD Silvaco. The simulation includes the application of SiO_2, HfO_2 and multi-oxide (SiO_2+HfO_2) as gate dielectric to analyze the characteristics of JLTs. The behavior of DG-JLT was found to be very interesting as compared to bulk and DG-SOI MOSFET. In bulk MOSFET with SiO_2, I_{on}/I_{off} ratio is 661.86. This ratio increases with an increase in dielectric constant due to the reduction in leakage current. It is scrutinized that the substitution of SiO2 with high-k dielectric materials in DG-JLT is beneficial for future devices. Moreover, the consequences of SiO_2, HfO_2 and multi-oxide on DG-JLT short channel parameters are studied. HfO_2 as gate oxide reveals a lower value of DIBL and SS as compared to other gate dielectrics on the application of high drain bias. Further, a comparison has been carried out between bulk, DG-SOI and DG-JLT MOSFET to evaluate the performance of the devices with SiO_2, HfO_2 and multi-oxide. DG-JLT with HfO_2 exhibits excellent immunity against SCEs. The leakage current is a very crucial factor in power dissipation. The leakage current is very less for DG-JLT with HfO_2 that makes it a more appropriate device for ultra-low power applications.

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Not applicable

Declarations

Funding

No funding was received for conducting this study.

Conflicts of interest/Competing interests

The authors declare that there is no conflict of interest regarding the content of this article.

Availability of data and material

The datasets generated and analyzed during the current study are not publicly available but may be available from the corresponding author on reasonable request.

Code availability

The code used during this work is not available.

Authors' contributions

The idea of the research was conceptualized by Prashant Kumar and Neeraj Gupta carried out the analytical modeling and simulation of Junctionless MOSFET. The formal analysis and resources for the research were arranged by Munish Vashisht and Rashmi Gupta. Prashant Kumar also prepared the original draft of the paper and Neeraj Gupta did the review, proofreading and necessary editing in the article.

Ethics approval

Not applicable

Consent to participate

All authors are agreed.

Consent for publication

There are no details on an individual reported in the manuscript.

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