High-κ perovskite membranes as insulators for two-dimensional transistors

Ultrahigh-κ single-crystalline perovskite dielectric membranes for two-dimensional transistors

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The dimension and power consumption scaling of Si metal-oxide-semiconductor field-effect transistors (MOSFET) has followed Moore's Law for decades but now faces the challenges associated with the physical thinning limit of Si at sub-10 nm technology nodes[1]. Two-dimensional (2D) layered semiconductors, with an atomic thickness allowing superior gate-field penetration, are potential for future channel materials[2,3]. Advancements for 2D transistors have been achieved such as wafer-scale monocrystalline growth of materials[4] and reduction of metal-2D contact resistance[5]. However, it remains challenging to explore high-κ dielectrics to well couple with 2D transistors and continue scaling their capacitance

equivalent thickness (CET). Here, we propose to use the transferrable ultrahigh-κ single-crystalline perovskite $SrTiO_3$ membrane as gate dielectric that exhibits a desirable sub-1 nm CET with a low leakage current (J_{leak} < 10^{-2} A/cm^2) under 2.5 MV/cm. The van der Waals (vdW) gap between $SrTiO_3$ and 2D semiconductors mitigates the unfavorable fringing-induced barrier lowering (FIBL) effect resulting from the use of ultrahigh-κ dielectrics[6]. Typical transistors made of scalable chemical vapor deposition (CVD) MoS_2 and $SrTiO_3$ dielectrics exhibit steep subthreshold swings (SS) down to ~70 mV dec^{-1} and ON/OFF current ratios up to 10^7, matching low-power specifications suggested by the latest International Roadmap for Devices and Systems (IRDS)[7].

For the sub-10 nm technology nodes in Si MOSFETs, a sub-nanometer CET and flawless interface with the channel are essential for gate dielectric to maintain the gate controllability[6]. Therefore, the development of reliable high-κ dielectrics (CET < 1 nm), which are adaptable to 2D MOSFETs for future nodes, is eagerly awaited. Typically used high-κ dielectrics in silicon technology (i.e., SiO_2, Al_2O_3, and HfO_2) have been integrated with 2D transition metal dichalcogenide (TMD) materials[8]. Nevertheless, their amorphous nature and imperfect dielectric/TMD interfaces make the elimination of charge scatters/traps difficult, not to mention the direct damages of 2D channels caused by dielectric deposition processes[9,10]. Although several interfacial passivation layers have been developed, such as organic molecules and atomically thin hexagonal boron nitride (hBN), these layers would reduce the overall gate capacitance[4,10-12]. Another attractive approach is to adopt crystalline dielectric materials such as multilayer hBN and epitaxial calcium fluoride (CaF_2), where the atomically flat surfaces result in smoother dielectric/semiconductor interfaces than conventional amorphous oxides despite their relatively lower dielectric constant retarding CET shrinkage[13-15]. The perovskite $SrTiO_3$ exhibits high static permittivity ($\varepsilon_{bulk} \approx 300$ at room temperature[16]), which makes it a promising gate dielectric for electrostatic modulation of silicon[17,18], graphene[19,20], or two-dimensional electron gas (2DEG) of complex-oxide heterointerface[21,22]. Moreover, recent advances in synthesizing single-crystal freestanding perovskite oxide membranes[23,24] establish a feasible route to integrate the ultrahigh-κ crystalline $SrTiO_3$ films with 2D semiconductors to form high-quality dielectric/channel interfaces for surmounting the present limit of gate control.

In this work, the reflection high-energy electron diffraction (RHEED) assisted pulsed-laser deposition (PLD) technique is adopted to prepare freestanding $SrTiO_3$ dielectric layers (see **Methods** for details)[23]. The water-soluble sacrificial $Sr_3Al_2O_6$ layer is epitaxially grown on top of a single-crystalline $SrTiO_3$ (001) substrate and then serves as the template for the subsequent epitaxy of single-crystalline $SrTiO_3$ dielectric films with various thicknesses. The as-deposited $SrTiO_3$ films exhibit atomically flat surfaces with clear atomic step-terraces (**Extended Data Fig. 1a, b**). The X-ray diffraction (XRD) pattern (**Extended Data Fig. 1c**) and X-ray reflectivity (XRR) analysis (**Extended Data Fig. 1d, e**) of the as-prepared $Sr_3Al_2O_6/SrTiO_3$ heterostructure clearly indicates the formation of single-crystalline phase and the atomically sharp interface with limited interdiffusion at the interface. Next, the $SrTiO_3$ layer is coated by a polymer support and delaminated in the deionized water after the $Sr_3Al_2O_6$ sacrificial layer was dissolved. With the polymer support layer, the released single-crystalline freestanding $SrTiO_3$ membranes are transferred onto the target substrates as illustrated in **Fig. 1a**. The photo of the as-released $SrTiO_3$ layer with the dimensions of 5×5 mm^2 on the pre-patterned Si/SiO_2 substrate is shown in **Fig. 1b**. The optical micrographs in **Fig. 1c** display that optical contrast gradually increases with the increasing $SrTiO_3$ thickness. Furthermore, the thickness measurement by atomic force microscopy (AFM) is consistent with the results of RHEED (**Extended Data Fig. 2**). Representative reciprocal space maps (RSM) of the transferred $SrTiO_3$ membrane around (002), (103), and (013) planes confirm the single-crystallinity, and the extracted average in-plane and out-of-plane lattice parameters are 0.3908 nm and 0.3907 nm, respectively (**Extended Data Fig. 3a, b**), which are within the measurement errors of the theoretical values of 0.3905 nm[23]. The plan-view dark-field transmission electron microscopy (TEM) images (**Fig. 1d, e**) and the selected area electron diffraction (SAED) (**Fig. 1f**) of 5 unit-cell (u.c.) thick $SrTiO_3$ prove its high crystallinity. Moreover, X-ray photoelectron spectroscopy (XPS) results (**Extended Data Fig. 3c, d**) suggest the good atomic stoichiometry of $SrTiO_3$ film.

The metal-insulator-metal (MIM) capacitor structure is employed to evaluate the dielectric property of the as-prepared $SrTiO_3$ membranes through capacitance-voltage (C-V) measurements[4,25], where the $SrTiO_3$ layer is sandwiched between the Pt-coated Si substrate and a top Ti/Au electrode (**Fig. 2a**). **Fig. 2b** shows that the measured capacitance density moderately decreases with the voltage and frequency, which is ordinarily observed in paraelectric ceramic

and asymmetric electrode configuration[26]. The effective permittivity ε_{eff} is related to capacitance as described by the equation[25]:

$$C_{eff} = \frac{A\varepsilon_0\varepsilon_{eff}}{t}$$

where C_{eff} is the measured capacitance, A is the area of top electrodes, t is the thickness of the $SrTiO_3$ layer, and ε_0 is the vacuum permittivity. The inset of **Fig. 2c** plots the thickness dependence of ε_{eff}, where the result for a particular thickness is obtained from the measurements conducted on at least 17 individual devices made of $SrTiO_3$ membranes with the same thickness. The ε_{eff} as a function of thickness can be well described by the typical "dead layer" model emerging in high-κ nanocapacitor (refer **Extended Data Fig. 4** for more details) as follows[25]:

$$\frac{t}{\varepsilon_{eff}} = \frac{t}{\varepsilon_{bulk}} + D$$

where ε_{bulk} is the bulk permittivity of dielectric material, and D is the derived constant resulted from the interfacial dead layers. **Fig. 2c** shows that CET exhibits a near-linear relationship with the $SrTiO_3$ thickness, implying that sub-1 nm CET can be achieved with ease while the oxide thickness is thinner than 26 nm (~ 65 u.c.). The CET is calculated by[6]:

$$\mathrm{CET} = \frac{3.9t}{\varepsilon_{eff}}$$

where 3.9 is the dielectric constant of silicon oxide. Besides, the extracted ε_{bulk} is ~270 approaching the ideal value ($\varepsilon_{bulk} \approx 300$) of bulk single-crystal $SrTiO_3$, pledging the quality and ultrahigh dielectric constant nature of prepared $SrTiO_3$ membranes.

On the other hand, low leakage current and high breakdown strength of dielectric materials are critical criteria responsible for the power consumption and reliability of electronic devices[6,10,27]. **Fig. 2d** demonstrates the leakage current characteristic of the as-prepared $SrTiO_3$ membranes with thicknesses of 10, 20, 40, and 80 u.c., respectively. For the applied field of 2.5 MV/cm, the leakage currents of 40 and 80 u.c. thick $SrTiO_3$ membranes are far below the low-power limit ($J_{leak} < 1.5\times10^{-2}$ A/cm^2), and all investigated sorts meet the requirement of MOSFET gate limit (< 10 A/cm^2)[28]. Moreover, **Fig. 2e** summarizes the breakdown field versus effective permittivity for the dielectrics used in the state-of-art Si and 2D semiconductor technologies for comparison[26,27,29-32]. Our optimized $SrTiO_3$ membranes (20, 40, and 80 u.c., **Extended Data Fig. 5**) tolerate analogous electric-field strength with the widely used Al_2O_3 and HfO_2 while

possessing much higher effective permittivities. Noteworthy that compare with the high-κ dielectrics built by deposition processes, the freestanding $SrTiO_3$ membranes possess well-defined surfaces to interface with metal contacts and 2D channel materials, greatly diminishing the interfacial imperfections and reinforcing dielectric strength[8,26]. Also, the presence of the vdW gap plays an important role in suppressing leakage current via the decrease of carrier tunneling probability[8,10]. Hence, freestanding single-crystalline $SrTiO_3$ membranes manifest superb capabilities of being an ideal building block for future short-channel FETs.

To examine the gate dielectric performance, a $SrTiO_3$ membrane with the thickness of 40 u.c. is transferred onto the SiO_2 substrate with pre-defined gate metals. A monolayer CVD MoS_2 thin film is then transferred on top of the $SrTiO_3$ and the quality of MoS_2 is verified by Raman and photoluminescence (PL) spectroscopies (**Extended Data Fig. 6**). Finally, the MoS_2 channels are patterned to form local back-gate MoS_2 FETs (**Fig. 3a**) and the photo for the FET arrays is shown in **Fig. 3b**. The cross-sectional structure of the FET is revealed by scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) mapping (**Fig. 3c**). The transfer (I_D-V_G) and output (I_D-V_D) characteristics of long-channel monolayer MoS_2 FET (W_{CH}/L_{CH} = 10/3.5 μm) are plotted in **Fig. 3d** and **Fig. 3e**, respectively. The transfer curves at different V_D show a steep increase in drain current at the subthreshold region with a SS value of 71.5 mV dec^{-1}, and typical output characteristics also show promising current control and saturation. **Fig. 3f** further presents I_D-V_G curves of 50 MoS_2 FETs, and **Fig. 3g** shows the correlation between the ON/OFF current ratio and SS value from these devices. A number of devices approach 10^7 ON/OFF current ratio; meanwhile, the best SS values are close to 70 mV dec^{-1}, which is among the best record values ever attained by MoS_2 FETs. **Fig. 3h** summarizes SS values achieved by the reported CVD-prepared MoS_2 long-channel FETs coupled with sub-10 nm CET high-κ dielectrics, where the crystalline interfaces generally exhibit better switching behavior than the amorphous interface (see **Extended Data Table 1** for details). Note that some reports only estimate the gate capacitance by adopting ideal dielectric permittivity without performing C_{eff} measurements, which may lead to underestimation of the equivalent oxide thickness (EOT). Thus, we re-estimated these EOTs with the scope of both ideal and practical permittivities derived from the nanocapacitors to ensure an impartial judgment. Notably, the $SrTiO_3$ dielectric yields extremely low SS values among published results based on CVD-grown

MoS_2, already meeting the microelectronic technology metrics 2028 (shaded red corner) projected by IRDS[7]. To further probe the interface properties, the trap density (D_{it}) at the $SrTiO_3$-MoS_2 interface is estimated using the expression[8]:

$$SS = \ln(10)\frac{k_B T}{q}\left(1 + \frac{qD_{it}}{C_G}\right)$$

where C_G is the gate capacitance obtained from MOS capacitance measurements (**Extended Data Fig. 7a**). The extracted $D_{it} \approx 4.3\times10^{-12}$ $cm^{-2}eV^{-1}$ is lower than the values typically obtained from CVD-grown MoS_2 channels (**Extended Data Table 2**), consistent with the low SS values from our devices. We anticipate further optimization of the nanofabrication process and interface engineering could lead to improvements in SS values.

With the scaling of channel length, the drain-induced barrier lowering (DIBL) becomes pronounced; consequently, the electrostatic control of the gate degrades, leading to the higher subthreshold current and poor SS values. Such a phenomenon can be mitigated via reducing CET[6,33]. Hence, we fabricated short-channel (**Fig. 4a**, L_{CH} ~ 35 nm; **Extended Data Fig. 7b,** L_{CH} ~ 55 nm) MoS_2 FETs to demonstrate the gate-to-channel control with the as-developed ultrahigh-κ $SrTiO_3$ dielectrics. The transfer characteristic of 35 nm short-channel MoS_2 FET (**Fig. 4b**) shows a near 10^6 ON/OFF current ratio and a steep SS value of 79 mV dec^{-1}, and output curves (**Fig. 4c**) exhibit promising current control and saturation. The benchmark results of the SS values for the reported short-channel MoS_2 FETs fabricated with different gate dielectrics are summarized in **Fig. 4d**, where SS values achieved by the $SrTiO_3$ gate dielectrics are lowest among the reported CVD-prepared MoS_2 FETs with similar device geometries. Despite these achievements, we are aware that the acknowledged selection criteria of gate dielectrics for further scaling MOSFETs suggest a proper permittivity of around 20~30[6]. The benefits of using a very high-permittivity dielectric to slim the CET are limited because the fringing field originating from the drain penetrates into the channel through the physically thicker gate dielectric, which sinks the source-to-channel potential barrier. Therefore, resembling DIBL, this fringing-induced barrier lowering (FIBL) effect degrades the subthreshold characteristics of MOSFET[6]. However, dissimilar from the conventional 3D bulk semiconductors, the native existence of a few-angstrom thick vdW gap between 2D semiconductor and adjacency plays an important role in the suppression of FIBL. To elaborate this, we performed the technology

computer-aided design (TCAD) simulation, where **Extended Fig. 8a, b** reveal the simulated equipotential contours of 10 nm short-channel MoS_2 FET without and with the involvement of a 5 Å vdW (vacuum) gap, respectively. The presence of the vdW gap redirects most of the fringing field lines through itself, which greatly restrains the drain-to-channel coupling. The calculated conduction band diagrams (**Extended Fig. 8c**) also imply that FIBL is apparently moderated in the $SrTiO_3$ dielectric with the vdW gap. Correspondingly, the simulated transfer characteristics reflect vast differences between the interfaces with and without the vdW gaps, especially in the ultrahigh-κ $SrTiO_3$ dielectric (**Extended Fig. 8d, e**). Note that the degradation occurring in the condition of SiO_2 with vdW gap is ascribed to the physically 1 nm thick SiO_2, where the overall gate capacitance severely decreases when introducing a comparable thickness-level vdW gap. The simulation results reveal the concealed advantage of vdW integration of 2D semiconductors and further expand the selection criteria of high-κ gate dielectric for the ultra-scaling 2D electronics.

In brief, the high-permittivity characteristic of freestanding single-crystalline $SrTiO_3$ membranes facilitates the CET shrinking into sub-1 nm scales. Moreover, the crystalline surface and well-defined vdW interfaces with 2D semiconductors exhibit the scaling potential for future transistor technologies. The $SrTiO_3$ dielectric membranes, with the elastic and slim nature[34], have also enabled the accomplishment of flexible and transparent electronics using MoS_2 as the transistor channel as demonstrated in **Extended Data Fig. 9**. Meanwhile, considering the exquisitely controlled and scalable growth techniques already established in the perovskite oxide field[18,23,24], the capability to freely integrate functional perovskite oxide membranes with 2D materials offers a new route to laminate assembly for monolithic 3D integration[1,2,35].

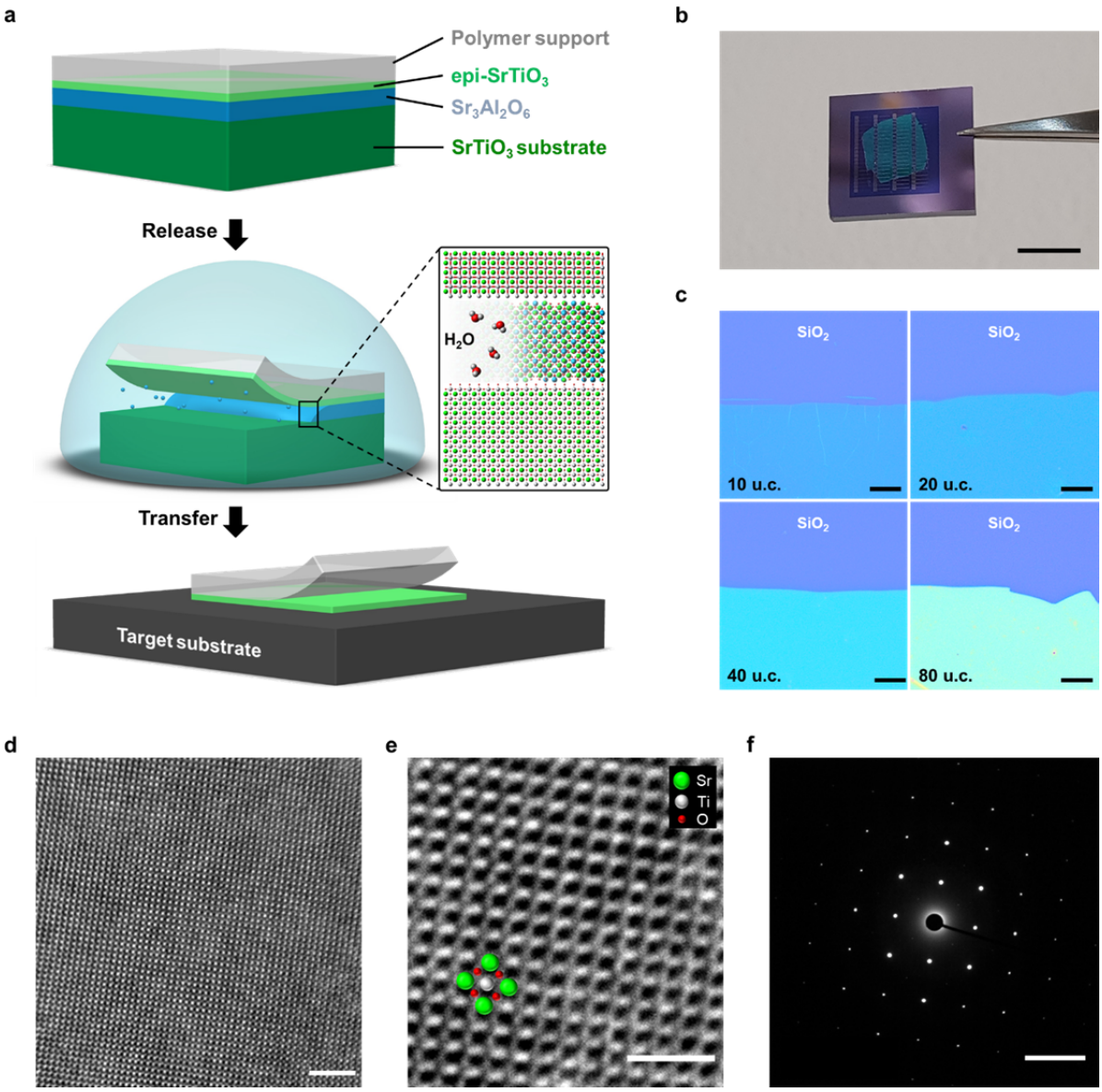

Fig. 1 Preparation and characterizations of freestanding single-crystalline $SrTiO_3$ layers. a, Schematic illustration of lift-off and transfer processes for epi-$SrTiO_3$ thin films onto the target substrate. **b,** Photograph of the transferred millimeter-scale freestanding $SrTiO_3$ membrane onto pre-pattern Si/SiO_2 substrates. The scale bar indicates 5 mm. **c,** Optical micrographs of $SrTiO_3$ films with various unit-cell (u.c.) thicknesses on 300 nm Si/SiO_2 wafers. The scale bars are 25 μm. **d, e,** Plan-view dark-field TEM images of 5 u.c. thick $SrTiO_3$ membrane. The scale bars are 2 nm and 1 nm, respectively. **f,** The corresponding SAED pattern, where the scale bar indicates 5 nm^{-1}.

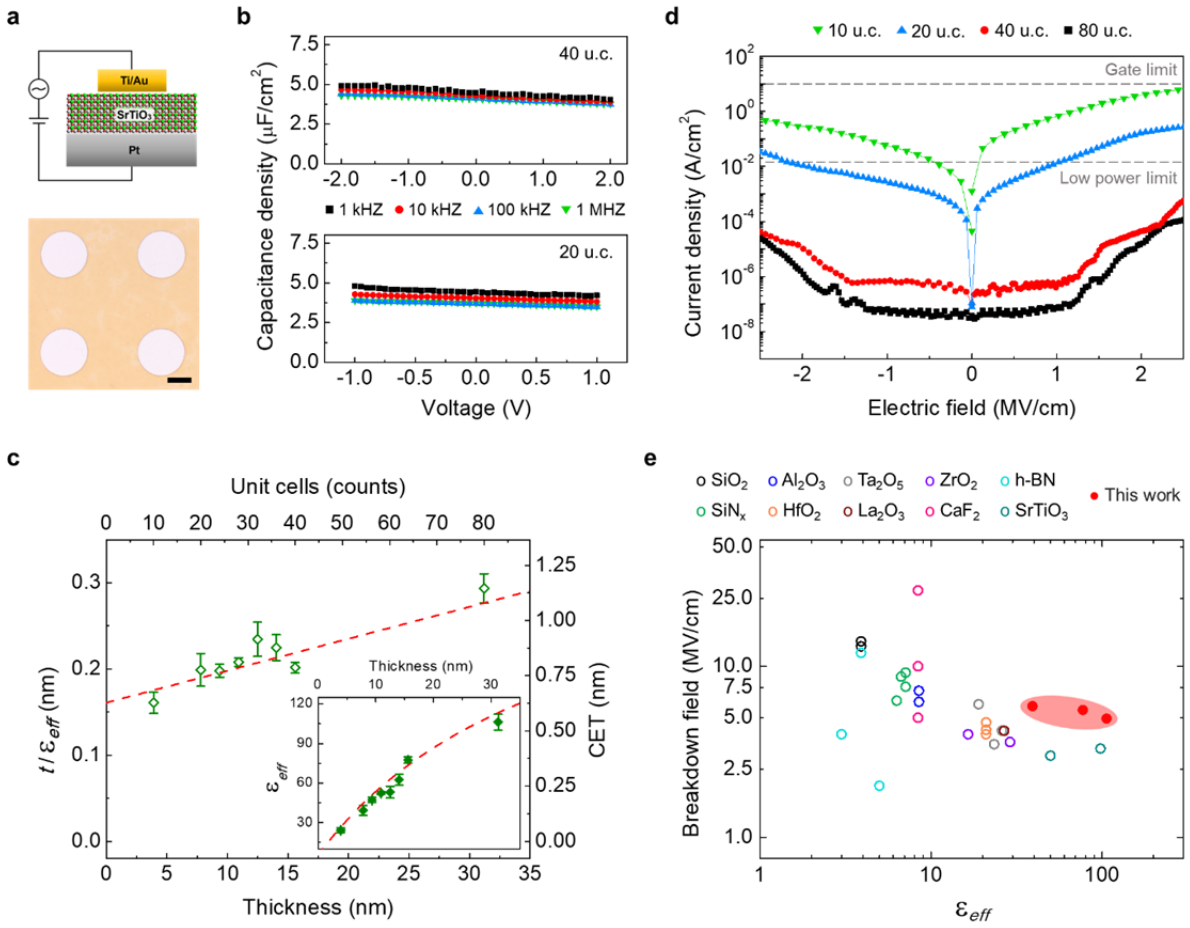

Fig. 2 Dielectric properties of single-crystalline $SrTiO_3$ membranes. a, The structure and optical micrograph of the MIM device. The scale bar is 100 μm. **b,** Voltage-dependent capacitance density (C-V) for MIM devices of 40 u.c. and 20 u.c. $SrTiO_3$ thin films at four different frequencies. **c,** t/ε_{eff}, and CET as a function of various $SrTiO_3$ thicknesses measured from MIM capacitors. The inset displays ε_{eff} as a function of $SrTiO_3$ thickness. Both red dashed lines are theoretical fitting using the dead layer model. **d,** Electric field-dependent leakage current density of $SrTiO_3$ films with various unit-cell thicknesses. Gray dashed lines mark the limits for relative applications. **e,** The breakdown field versus effective dielectric constant of our $SrTiO_3$ membranes, in comparison to the published literature.

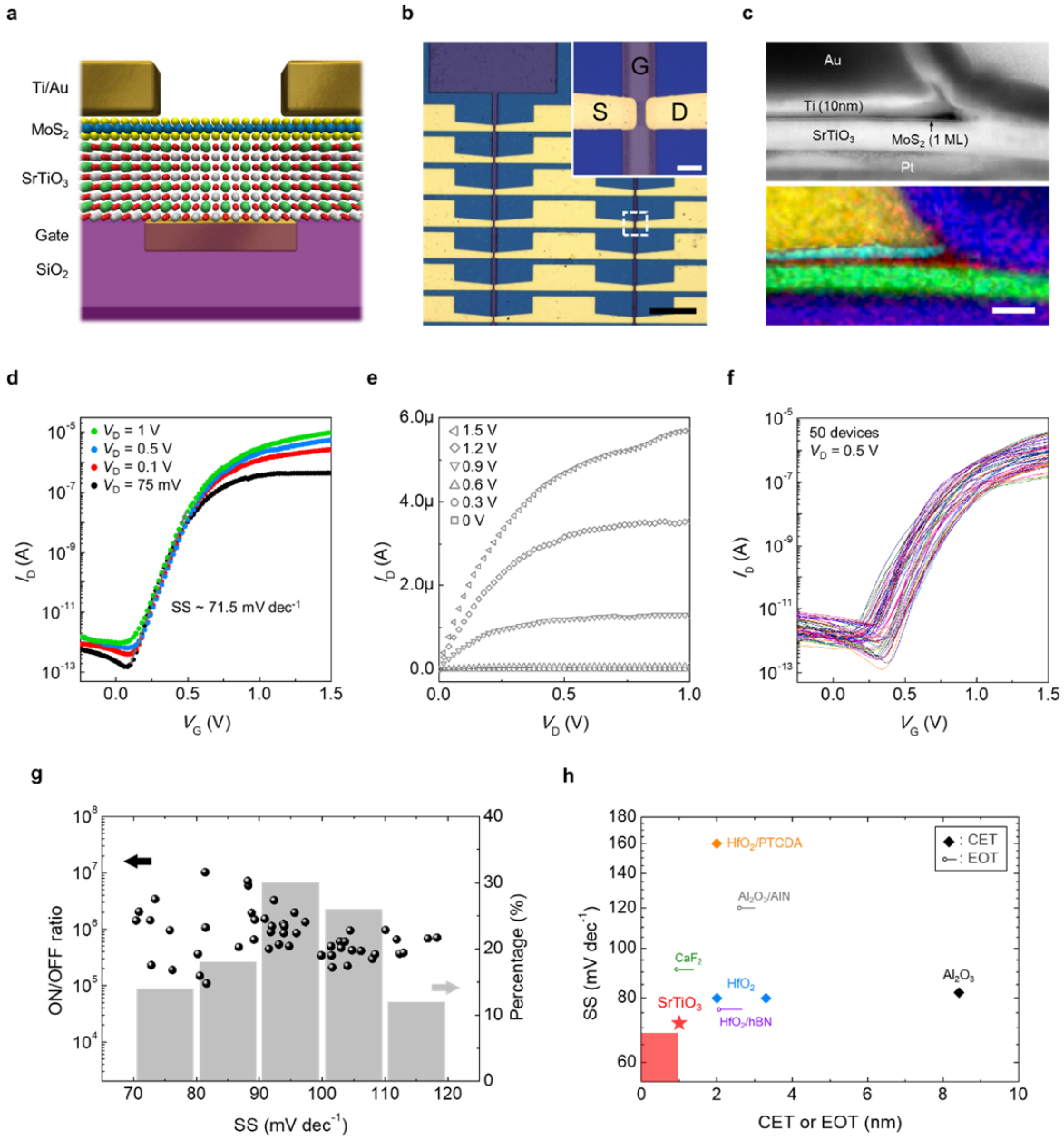

Fig. 3 Local back-gated MoS_2 FETs with ultrahigh-κ $SrTiO_3$ dielectrics. a, Structure of the local back-gated FETs, where a vdW interface exists between $SrTiO_3$ and MoS_2 in the channel region. **b,** Optical micrograph of batch-fabricated FET arrays. Inset shows the magnified image of the white square. The scale bars are 100 μm and 10 μm (inset) respectively. **c,** Cross-sectional STEM image and corresponding EDS mapping obtained in the contact-channel area. The colors represent as follows: blue (Pt), yellow (Au), cyan (Ti), red (S), green (Sr). Scale bar: 25 nm. **d,** Transfer characteristics (I_D-V_G) of monolayer MoS_2 FET, showing steep subthreshold slopes. **e,** Output characteristics (I_D-V_D) of the same device. **f,** I_D-V_G curves of 50 $SrTiO_3$/MoS_2 FETs. **g,** Scatter distribution (black) of recorded ON/OFF current ratios and SS values, and statistical histogram (gray) of SS from 50 devices. **h,** Comparison of SS values achieved by state-of-the-art

CVD-prepared MoS_2 FETs with the CET < 10 nm. The ball-stick symbol represents EOT, where ball is theoretical value while stick is EOT range extracted from practical permittivity in general nanocapacitor. SS values were extracted within the V_D range of 0.1 ~ 1 V and L_{CH} range of 0.1 ~ 5 μm. The shaded red corner is the IRDS low-power specification for 2028.

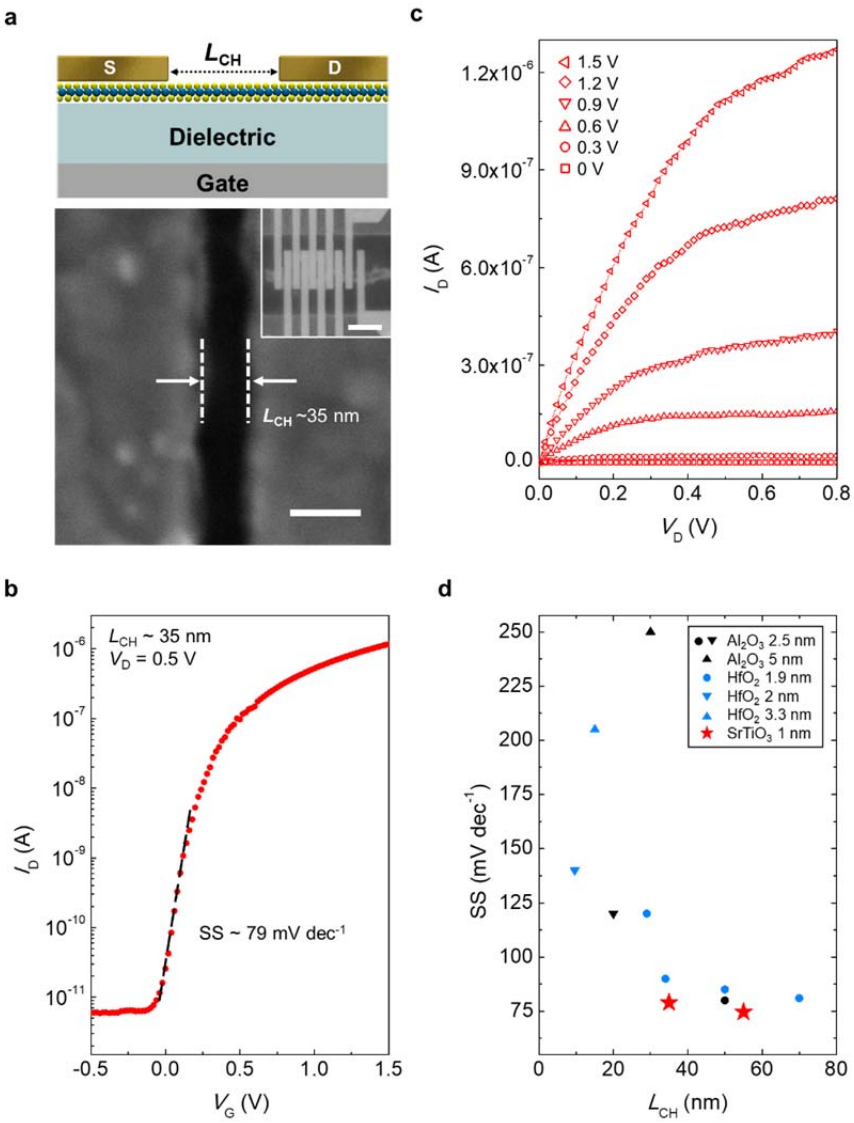

Fig. 4 Electrostatics of short-channel MoS_2 FETs based on ultrahigh-κ $SrTiO_3$ dielectrics. a, Schematic illustration of the structure and SEM image of the device with a channel length of 35 nm. Inset shows the optical micrograph of the associated devices. Scale bars indicate 50 nm and 1μm (inset). **b,** I_D-V_G characterization of the device shown in **a**. **c,** I_D-V_D output curves of the same device. **d,** Benchmark of SS in reported short-channel ($L_{CH} \leq 100$ nm) 2D FETs coupled with different CET gate dielectrics. For a fair comparison, only the devices with single-gate geometry are shown.

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Author contributions

S.L. and L.-J.L. supervised the project. J.-K.H. conceived and directed the project. J.Z., W.W., N.Y., and Y.L. performed the synthesis and characterization of perovskite oxide heterostructures. J.-K.H. and Y.W. synthesized MoS_2 monolayer. J.S., X.G., and L.H. carried out microscopy characterization. J.-K.H., C.-H.L., and T.W. performed Raman and PL analyses. J.S. and J.-K.H. contributed to the device fabrication. J.-K.H. conducted electrical measurements and analyses of devices. Z.W. contributed to the TCAD simulation. J.Y., D.W, V.T., K.K.-Z, X.Z. and L.Q. provided constructive opinions and suggestions. All the authors discussed and contributed the results. J.-K.H., L.-J.L., and S.L. drafted the manuscript.

Competing interests

J.-K.H., J.S., J.Z., and S.L. are co-inventors on a patent application (Australian provisional filling number: 2021902514) related to the research presented in this paper.

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