

HIGH-LEVEL MULTI-STEP INVERTER OPTIMIZATION, USING A MINIMUM NUMBER OF POWER TRANSISTORS.

Juan Dixon (SM)

Department of Electrical Engineering
Pontificia Universidad Católica de Chile
Casilla 306, Correo 22, Santiago, Chile
fax 56-2-552-2563

e-mail jdixon@ing.puc.cl
(corresponding autor)

Luis Morán (F)

Department of Electrical Engineering
Universidad de Concepción
Casilla 53-C, Concepción, Chile
fax 56-41-246-999

e-mail lmoran@renoir.die.udec.cl

ABSTRACT

Multilevel inverters with a large number of steps (more than 50 levels) can generate high quality voltage waveforms, good enough to be considered as suitable voltage template generators. Many levels or steps can follow a voltage reference with accuracy, and with the advantage that the generated voltage can be modulated in amplitude (AM) instead than PWM. The main disadvantage of this type of topology is the large number of power supplies and semiconductors required to obtain these multi-step voltage waveforms. This paper is focussed in minimizing the number of power supplies and semiconductors (transistors or GTOs) for a given number of levels. Different combinations of topologies are presented, and the corresponding mathematical relations have been derived. The paper shows optimized curves to obtain the relation between minimum number of power semiconductors required for a given number of levels. Experimental results obtained from an optimised prototype, capable to generate 81 levels of voltage with only four power supplies and sixteen transistors per phase are shown.

I. INTRODUCTION

Power electronics devices contribute with important part of harmonics in all kind of applications, such as power rectifiers, thyristor converters, and static *var* compensators (SVC). Even updated PWM techniques used to control modern static converters such as machine drives, power factor compensators or active power filters, do not produce perfect waveforms, which strongly depend on the semiconductors switching frequency. Normally, with voltage or current converters, as they generate discrete output waveforms, forcing the use of machines with special isolation, and in some applications large inductances connected in series with the respective load are required. In other words, neither the voltage nor the current waveforms are as expected. Also, it is well known that distorted voltages and currents waveforms produce harmonic contamination, additional power losses, and high frequency noise that can affect not only the power load but also the associated controllers. All these unwanted operating characteristics associated with PWM converters can be overcome with multi-level converters, with the addition that higher voltage levels can be achieved [1-5].

Multi-level inverters can operate not only with PWM techniques but also with amplitude modulation (AM), improving significantly the quality of the output voltage waveform. With the use of amplitude modulation, low frequency voltage harmonics are perfectly eliminated, generating almost perfect sinusoidal waveforms, with a THD lower than 5 %. Another important characteristic is that each converter operated at a low switching frequency, reducing the semiconductor stresses, and therefore reducing the switching losses [6, 7]. The principal objective of this paper is to determine the simplest converter topology in terms of number of power semiconductors, for a given number of levels. The “redundant” levels are minimized,

and the combination of bridges to maximize the number of levels [8,9] and minimize power sources and semiconductors are analyzed.

II. MULTILEVEL CONVERTERS CHARACTERISTICS

The principal function of the inverters is to generate an ac voltage from a dc source voltage. If the dc voltage is composed by many small voltage sources connected in series, it becomes possible to generate an output voltage with several steps. Multilevel inverters include an arrangement of semiconductors and *dc* voltage sources required to generate a stair case output voltage waveform. Figure 1 shows the schematic diagram of voltage source-inverters with different number of levels. As it is well known, a two level inverter, as the one shown in Fig. 1(a), generates an output voltage with two different values (levels), V_C and “zero”, with respect to the negative terminal of the *dc* source (“0”), while a three level module, Fig. 1(b) generates three different voltages at the output ($2 \cdot V_C$, V_C and “zero”). The different positions of the ideal switches are implemented with a number of semiconductors that are in direct relation with the output voltage number of levels.

Multilevel inverters are implemented with small *dc* sources, used to form a stair case *ac* waveform, which follows a given reference template. For example, having 10 dc sources with magnitude equals to 20 V each one, a composed 11 level waveform can be obtained (five positive, five negatives and zero with respect to the middle point between the ten sources), generating a sinusoidal waveform with 100 V amplitude as shown in Fig. 2, and with very low THD.

It can be observed that the larger the number of the inverter dc supplies, the greater the number of steps that can be generated, obtaining smaller harmonic distortion. However, the number of dc sources is directly related with the number of levels through the equation:

$$n = m - 1 \quad (1)$$

where n is the number of dc supplies connected in series and m is the number of the output voltage levels. In order to get a 51-level inverter output voltage, 50 voltage supplies would be required which is too much for a simple topology.

Besides the problem of having to use too many power supplies to get a multilevel inverter, there is a second problem which is also important, the number of power semiconductors required to implement the commutator, as shown in Fig. 1. Technical literature has proposed two converter topologies for the implementation of the power commutator, using force-commutated devices (transistors or GTOs): a) the Diode-Clamped, and b) the Capacitor-Clamped Converter [2].

2.1 Diode-Clamped Inverter

This inverter consists on a number of semiconductors connected in series, and another identical number of voltage sources, also connected in series. These two chains are connected with diodes at the upper and lower semiconductors as shown in Fig. 3 a). For an m -level converter, the required number of transistors T is given by the following equation:

$$T = 2(m - 1) \quad (2)$$

Then, for the example of 51-level converter, 100 power transistors would be required, which is an enormous amount of switches to be controlled. One of the most utilized configurations with this topology is that of the three-level inverter, which is shown in Fig. 3 b).

The capacitors act like two dc sources connected in series. Thus, in the diagram, each capacitor accumulates $\frac{1}{2}V_{dc}$, giving voltages at the output of $\frac{1}{2}V_{dc}$, 0 or $-\frac{1}{2}V_{dc}$ with respect to the middle point between the capacitors.

2.2 *Capacitor-Clamped Inverter.*

This inverter has a similar structure to the Diode-Clamped, but it can generate the voltage steps with capacitors connected as shown in Fig. 4. The problem with this converter is that requires a large number of capacitors, which translates in a bulky and expensive converter as compared with the Diode-Clamped Inverter. Besides, the number of transistors becomes the same as the Diode-Clamped inverter, and therefore, for a 51-level inverter, again 100 power transistors are required. In order to overcome all these problems, a third topology, which will be called “Transistor-Clamped Inverter” will be presented and analyzed.

2.3 *Transistor-Clamped Inverter.*

The transistor-clamped inverter has the advantage of requiring the same number of power transistors as the levels generated, and therefore, the semiconductors are reduced by half with respect to the previous topologies. A 51-level converter requires 51 instead of the 100 transistors. The Figure 5 shows the circuit topology of a m -level Transistor Clamped Inverter, which satisfies (3):

$$T = m \tag{3}$$

In this topology, the control of the gates is very simple because only one power transistor is switched-on at a time. Then, there is a direct relation between the output voltage, V_{out} , and the transistor that has to be turn-on. However, and despite the excellent characteristics of this

topology, the number of transistors is still too large to allow the implementation of a practical converter with more than 50 levels.

One solution to increase the number of steps could be the use of “H” converters, like the one shown in Fig. 6, which consists on connecting two of the previously discussed topologies in series (two legs). If Transistor-Clamped inverters are used to build an “H” converter, the number of transistors required for a m -level inverter is $m+1$, which means only one more transistor than the required for a simple leg configuration. However, the number of dc sources is reduced in 50 %, which is the most important advantage of “H” converters.

Another characteristic is that the “H” topology has many redundant combination of switches position to produce the same voltage levels. As an example, the level “zero” can be generated with switches in position S(1) and S(2), or S(3) and S(4), or S(5) and S(6), and so on. Another characteristic of “H” converters is that they only produce an odd number of levels, which ensures the existence of the “zero volt” level at the load.

For example, a 51-level inverter using an “H” configuration with Transistor-Clamped topology requires 52 transistors, but only 25 power supplies instead of 50 required using a single leg. Therefore, the problem related with increasing the number of levels and reducing the size and complexity has been partially solved, since power supplies have been reduced to 50 %.

III. SCALING OF MULTILEVEL CONVERTERS

Like binary numbers, which are scaled in power of two using two bits, an association between bits and levels can be realized. A 2-level inverter can be scaled in power of “2” with another 2-level inverter in the same way as binary systems do. In the same way, a 5-level converter can be scaled in power of “5” with another 5-level converter, and so on. The scaling

can be implemented in practice using many m -level inverters with their respective power supplies being multiplied by m , as shown in Fig. 7, where a cascade of *three* 4-level converters ($m=4$) is displayed. In this example, a *three* digits, “quaternary” number is obtained. The “*three*” digits is because there are three inverters in the chain, and the “quaternary” denomination is because each inverter can produce *four* levels output voltage.

It can be noticed from Fig. 7 a) that **64 levels of voltage** are obtained, starting from the level $V_{out}=0$, to the level $V_{out}=63 \cdot V_c$ ($63V_c=3 \cdot [16V_c+4V_c+V_c]$). Then, with a few number of transistors, a large number of levels is available using power combination of converters. For a symmetrical **Vout** ($|V_{MAX}|=|-V_{MAX}|$) the power supplies located at the center of each converter are divided in two, in order to allow the “middle point” connection between converters, as shown in Fig. 7 b). This division is not required when the level of individual converters is an odd number.

In the example of Fig. 7 a), only 12 transistors (if the Transistor-Clamped topology is used) and 9 power supplies are required to obtain the 64 levels in the output voltage. However, for a symmetrical **Vout**, as the one shown in Fig. 7 b), 12 power supplies are required due to the reasons mentioned before. The equation that relates the number of levels with the number of m -level inverters used in the chain is:

$$M = m^k \quad (4)$$

M is the total number of levels that can be generated, using a cascade of “ k ” m -level inverters. Now the question is how to find the best combination of converters in cascade with a given number of levels, in order to obtain the highest number of steps with the minimum amount of power transistors (and also minimum power supplies). Following the example of Fig. 7, where 12 power transistors were used to get 64 levels, it is also possible to build a cascade of *six* 2-

level inverters using the same amount of transistors (12). The total number of levels (M) are the same ($2^6=64$), but the power supplies are reduced from 9 to only 6. However, in this case the six power supplies are floating one from each other as compared with the example of Fig. 7 where only three packs of power sources are floating.

Searching for the minimum number of power transistors to obtain at list 51 levels of voltage, Fig. 8 shows a relation between number of transistors used, and the number of levels obtained, assuming cascades based on Transistor-Clamped topologies. It can be seen that it is possible to obtain **81 voltage levels** with only **12 transistors**, if a chain of *four* 3-level converters are used ($3^4=81$), which is the highest number of levels that can be achieved with 12 transistors. With 10 transistors it is possible to build a cascade of *one* 10-level inverter, or *two* 5-level inverters, or *five* 2-level inverters. In the first case 10 levels are obtained (10^1); in the second, 25 levels (5^2); and in the third 32 levels (2^5). It becomes clear that with 10 transistors it is not possible to get 51 levels, so the maximum number of levels that can be achieved, in this example, is 32.

The question that must be answered is, what happens with a cascade of converters with different number of levels?. If a 51-level inverter is the target, 11 transistors may be the solution, because 10 transistors is not enough ($M_{MAX}=32$) and 12 is too much ($M_{MAX}=81$). Using a combination of inverters of different levels, for example, *three* 3-level inverters plus *one* 2-level inverter, and using Transistor-Clamped topologies, with **11 transistors, 54 levels** can be obtained ($M=3\cdot3\cdot3\cdot2=54$). This 54-level inverter using 11 transistors for a Transistor-Clamped topology can be implemented in four different ways, two of them are shown in Fig. 9.

These two 54-level inverters generate 27 positive levels and 27 negative levels at the output voltage, scaled by one unit of V_{DC} , and with peak values of $\pm 26.5V_{DC}$ in both the cases.

Since the number of levels is even, the level “zero Volt” can not be generated. One important difference between the two configurations is that, even though the levels of voltages generated are the same, the values of power supplies for each one are different. In Fig. 9 b), the voltage escalation decreases faster than in Fig. 9 a). This characteristic becomes an advantage when the small floating power supplies from the top converters are generated from the large one in the bottom of the circuit, using bi-directional DC-DC supplies.

By using multi-level bridges with different number m it is also possible to find a combination with 10 transistors, which can result in more than the $M_{MAX}=32$, shown in Fig. 8 which uses *five* 2-level converters (2^5). For example, 36 levels are obtained with a cascade of *two* 3-level inverters plus *two* 2-level inverters ($M=3 \cdot 3 \cdot 2 \cdot 2=36$). In general, the total number M of levels that can be reached with k converters of different number m is given by:

$$M = \prod_{i=1}^k m_i \quad (\text{with } m_i \geq 2) \quad (5)$$

and the number of power transistors required, T , when Transistor-Clamped topology is used is given by:

$$T = \sum_{i=1}^k m_i \quad (\text{with } m_i \geq 2) \quad (6)$$

Another important issue in the simplification of multilevel inverters, is the number of power supplies needed for their implementation. It can be noticed for example that the multilevel inverter shown in Fig. 9 needs 4 independent and floating power supplies, each one with middle point to allow generation of symmetrical voltages. As it has been demonstrated, multi-level converters with m =even, need to have a source with middle point to get the symmetrical condition for \mathbf{V}_{out} ($|V_{MAX}|=|-V_{MAX}|$). With m =odd, this is not required because the

number of power sources is even. On the other hand, the amount of floating supplies is equal to k , which represents the quantity of m -level inverters in the cascade (or chain). Therefore, the total number of power supplies can be expressed as follows:

$$n_T = \sum_i k_{odd}^i (m_{odd}^i - 1) + \sum_j k_{even}^j \cdot m_{even}^j \quad (7)$$

where k_{odd}^i is the number of odd-level converters (each one with is m_{odd}^i levels). Similar explanation is valid for k_{even}^j and m_{even}^j . On the other hand, the number of floating power supplies is given by:

$$n_F = \sum_i k_{odd}^i + \sum_j k_{even}^j = k_{odd} + k_{even} = k \quad (8)$$

In the example shown in Fig. 9 there are four converters in cascade, and hence $n_F=k=4$. Besides, there are *three* 3-level inverters and *one* 2-level inverter, which defines a total number of supplies $n_T=3(3-1)+1\cdot2=8$. On the other hand, in the example of Fig. 7 b), which corresponds to a symmetrical 64-level converter, the total number of power supplies is $n_T=k_{even}\cdot m_{even}=3\cdot4=12$. Considering a more complex cascade of converters, like for example the one shown in Fig. 10, which has from top to bottom, *three* 2-level converters plus *one* 4-level converter, plus *one* 3-level converter and plus *two* 5-level converter, the number of floating supplies is $n_F=3+1+1+2=7$, and the total number of sources is $n_T=3\cdot2+1\cdot4+1(3-1)+2(5-1)=20$. The number of levels would be, according with (5), $M=5\cdot5\cdot3\cdot4\cdot2\cdot2=2400$, and the number of transistors, using Transistor-Clamped Topologies, would be $5+5+3+4+2+2+2=23$. It can be noticed that the number of levels has increased more than 100 times, with the same number of transistors used in each phase. However, this is not the maximum number of levels that can be obtained with 23 transistors per phase.

3.1 *Output Voltage Generation.*

In Figs. 9 and 10, the scaling of voltages seems quite unclear. However, they are scaled according with the particular level of each inverter. To start the process of escalation, a base voltage must be selected from either, the upper level inverter (on the top of the chain), or the lower level inverter (at the bottom of the chain). Starting from the voltage V_C of the converter on the top of the chain, the value of the voltage supply of the next converter is obtained by multiplying the level m of this top converter by its base voltage V_C . This rule can be applied in every step of the chain, multiplying the level m_i of the forefront inverter for one of their respective voltages $V_C^{(i)}$, to obtain the value of the voltage supplies of the next converter located at the backside, no matter the particular level of this converter. The mathematical relation is as follows:

$$V_C^{(i+1)} = m_i \cdot V_C^{(i)} \quad (9)$$

where $(i+1)$ represents the inverter located below the inverter (i) . The explanation of this rule is as follows: the new converter located at the backside, has to start generating a voltage that is one more step larger than the maximum voltage obtained with the previous converter. The previous converter can generate m_i levels starting from zero, which means that the higher voltage with this converter is $(m_i-1) \cdot V_C^{(i)}$. Then, the next voltage step has to be the one given by (9).

3.2 *Optimizing the Number of Levels.*

In order to optimize the number of levels for a given number of power transistors, eq.(5) has to be maximized. To do that, a special combination of numbers of converters k and particular levels m_i has to be found. Once this combination is obtained, the optimum number of levels can be known. Figure 11 shows the maximum number of levels that can be obtained with

different number of power transistors. This figure assumes that the converters use the Transistor-Clamped topology. It can be noted that the maximum number of levels that can be achieved increases very rapidly, making possible to have more than 8700 levels with only 25 transistors. Despite most of real applications, 81 levels is more than enough for getting an almost perfect voltage waveform, special medical or military applications could require a large number of levels. The optimization process was obtained using a small computer simulation where only integer numbers were evaluated.

3.3 Minimizing the Number of Power Supplies.

To minimize the number of power supplies the number of converters k has to be minimized because they are in direct relation with the number of voltage sources. On the other hand, and for similar reasons, the number of levels of each converter also needs to be minimized. The three-level “H bridge” converter has the particular advantage of requiring only **one** power supply, which is obviously the minimum. When they are scaled in power of three (three-level converters), they reach a high number of levels rapidly with few power sources. Unfortunately, power supplies and transistors cannot be minimized simultaneously, which becomes clear because three-level H-bridges need four transistors and one power source instead of the three transistors and two supplies required by transistor clamped bridges.

IV. PRACTICAL APPROACH

An optimized arrangement with 81 levels of voltage has been built using 4 power supplies and 16 transistors per phase, enough to get almost perfect voltage waveforms for power applications. However, it is important to say that the paper was not focused on implementing

particular arrangements, but on the way special topologies can be built to get a high number of levels with few transistors and power supplies. The idea behind the description of this practical approach is to show how problems related with large number of power supplies can be solved.

The Figure 12 shows the main components of the 81-level multiconverter, which has been built in two different topologies: 8a) using four individual voltage sources for each module [8], and 8b) using one single voltage source for all modules and voltage escalation through output transformes [9]. The first topology is suitable for machine drives applications, and the last configuration is useful for constant frequency applications such as active front-end rectifiers, active power filters and reactive power compensation. In this last case, the power supply could also be a voltage regulated dc capacitor. This arrangement has also been successfully implemented.

One important characteristic of multilevel converters using voltage escalation is that electric power distribution and switching frequency present advantages for the implementaion of these topologies. Figure 13 shows the switching frequency and power distribution for each one of the four bridges used for the implemetation of the 81-level multiconverter. It can be seen that 80% of the power is controlled by one of the four converters, which is called “Main Converter”. The Main Converter is also switched at the fundamental frequency, minimizing switching losses and improving efficiency. It can also be seen that the two converters with small voltages only manage 5% of the total power. This characteristic has a significant effect on the design of machine drives, because two of the four converters can be fed with small DC-DC bi-directional power supplies with galvanic isolation. The figure 14 shows an example of machine drive for a small electric vehicle, using different solutions for their power supplies. As can be seen, 12 dc power supplies have been reduced to only four batteries, some small DC-DC

converters, and a special battery charger. Solutions like the one shown in figure 14 are many, but this work is not focused in this matter.

The active power filter of ref [9] was implemented with a *dc* link capacitor and output transformers like the example showed in Fig. 8b). The figure 15 shows the high quality waveforms obtainable with this kind of active power filter when compared with conventional PWM technologies. Another application example of multilevel converters is as power rectifier [10].

It is interesting to mention that, because of the low switching frequency of the Main Converter, efficiency remains high. Another good characteristic of this kind of converter is that they are connected in series at the ac side, reducing protection problems.

As a final comment, it is important to mention that the quality of the voltage waveform deteriorate with low amplitudes, but this depends on the number of levels of the particular converter. With 81 levels, the THD remains low even with 25% of amplitude. For smaller amplitudes, it is recommended to use a combination of AM and PWM.

V. EXPERIMENTAL RESULTS

Figure 16 shows a detail of a half-wave voltage, and the voltages of the three phases of the 81-level converter descried above, which is feeding an induction motor. The power configuration is as shown in Fig. 14. The current of one of the phases is also displayed, which is almost perfectly sinusoidal. This high quality current has many benefits in the operation of the machine: smooth torque, low noise, reduced losses and better controllability. Evidently, the overall operation of the machine becomes improved. Similar results with active power filters or

power rectifiers implemented with high-level multilevel converters have been obtained (see Fig. 15).

VI. CONCLUSIONS

Multilevel inverters with a large number of steps or levels have been analyzed. The problem has been focused in minimizing the number of power transistors for a given number of levels. The optimization process shows that the number of levels increases very rapidly as the number of power transistors increases. Different combinations and topologies were presented, and some mathematical relations were developed. The paper shows experimental results obtained from an optimised prototype, able to generate 81 levels output voltage with only four power supplies and sixteen transistors per phase.

VII. ACKNOWLEDGEMENTS

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Figure captions

Fig. 1. Basic multilevel inverters (a) two levels, (b) three levels y (c) m levels.

Fig. 2. Voltage waveform from an 11-level inverter.

Fig. 3. a) m -level, and b) three-level Diode-Clamped Inverter topology.

Fig. 4. m -level Capacitor-Clamped Inverter.

Fig. 5. m -level Transistor-Clamped Inverter.

Fig. 6. m -level inverter using an “H” bridge.

Fig. 7. 64-level inverter built with three, 4-level inverters
a) negative reference (only positive values of **V_{out}**)
b) middle point reference for symmetrical **V_{out}**

Fig. 8. Total number of levels related with the number of bridges and transistors

Fig. 9. 54-level inverters with only 11 transistors, using Transistor-Clamped topology
a) The 2-level inverter at the bottom
b) The 2-level inverter on the top

Fig. 10. 2400-level inverter, using a series of different m -level bridges.

Fig.11. Maximum number of levels reachable with a given number of transistors

Fig. 12. Main components of an 81-level multiconverter.
a) four individual voltage sources for each module.
b) one single voltage source for all modules, series connection via output transformes.

Figure 13: a) frequency modulation in each converter, b) power distribution in each converter.

Figure 14: Special 81-level arrangement for electric vehicle.

Fig. 15. Active power filter waveforms: a) PWM technique; b) 81-level technique

Fig.16. a) half-wave voltage waveform at the output of the experimental 81-level converter
b) current in one phase and voltages at the three phases of an induction motor

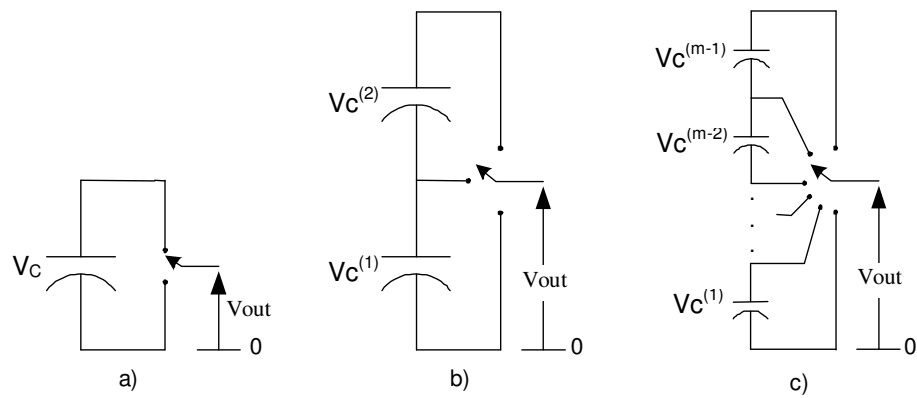


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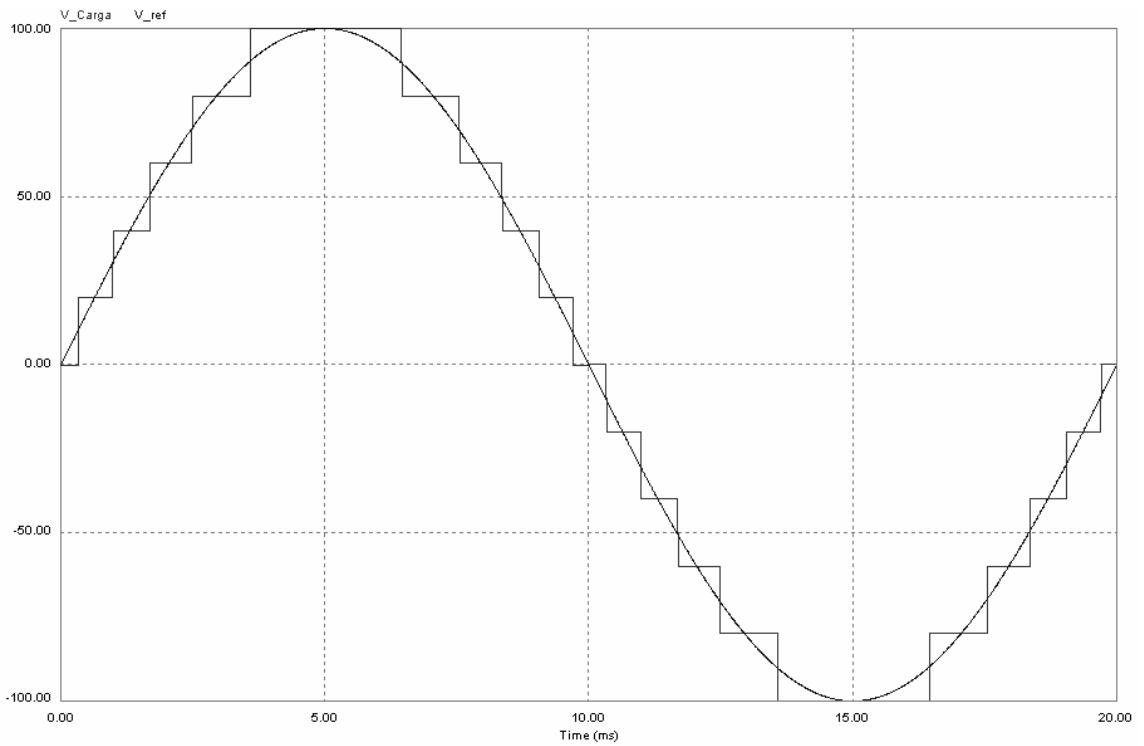


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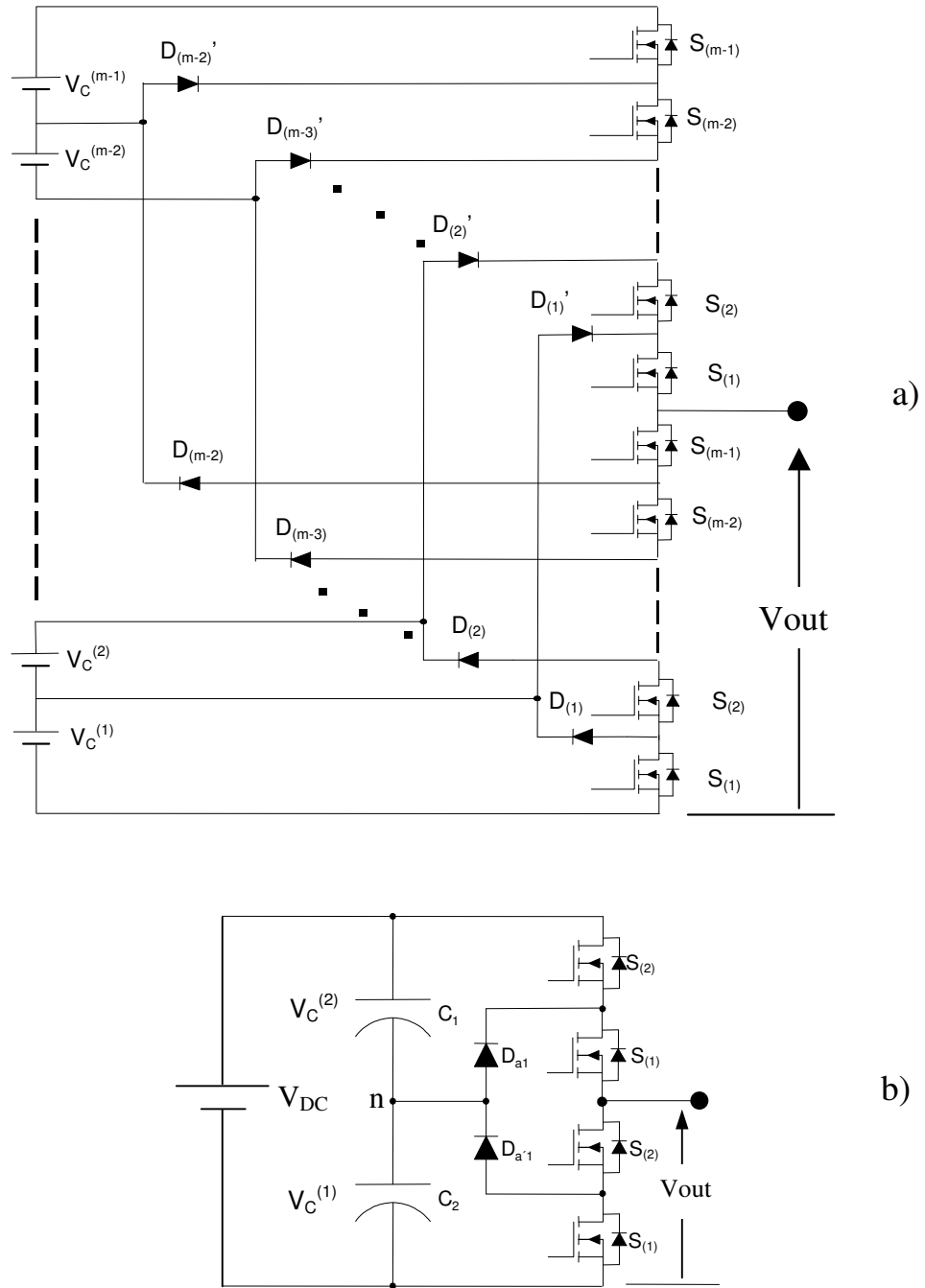


Fig. 3. a) m -level, and b) three-level Diode-Clamped Inverter topology.

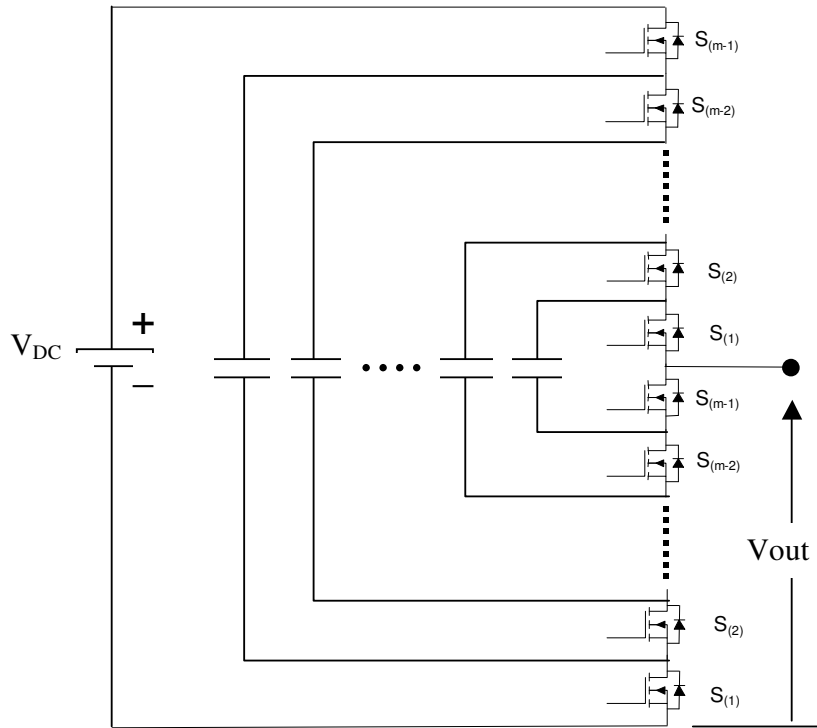


Fig. 4. m -level Capacitor-Clamped Inverter.

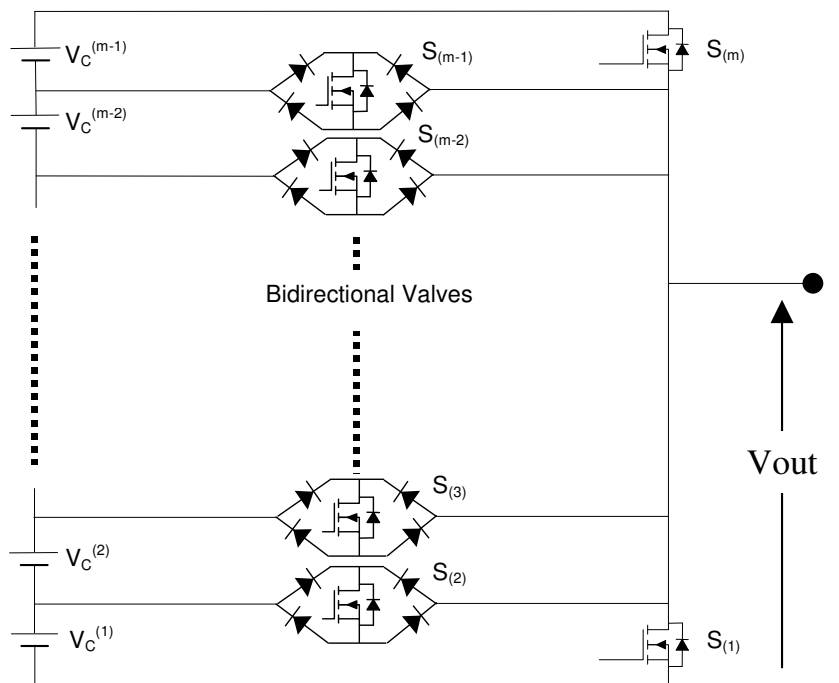


Fig. 5. m -level Transistor-Clamped Inverter.

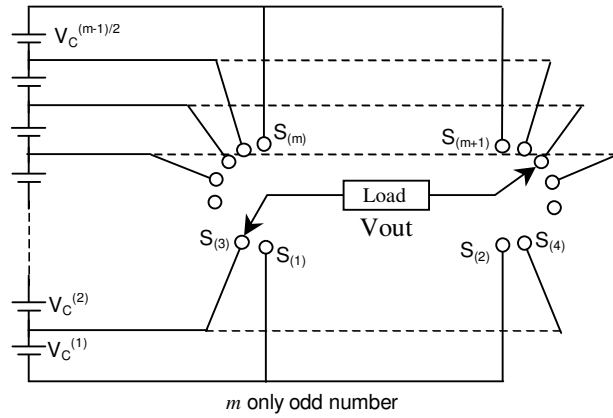


Fig. 6. m -level inverter using an “H” bridge.

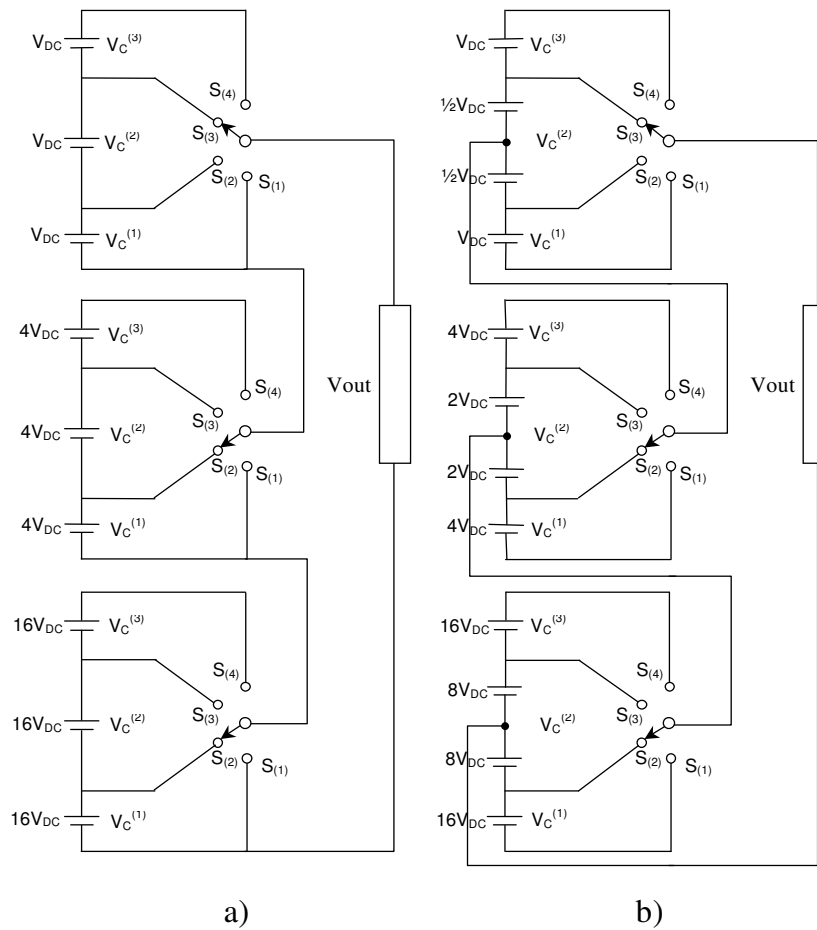


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 b) middle point reference for symmetrical V_{out}

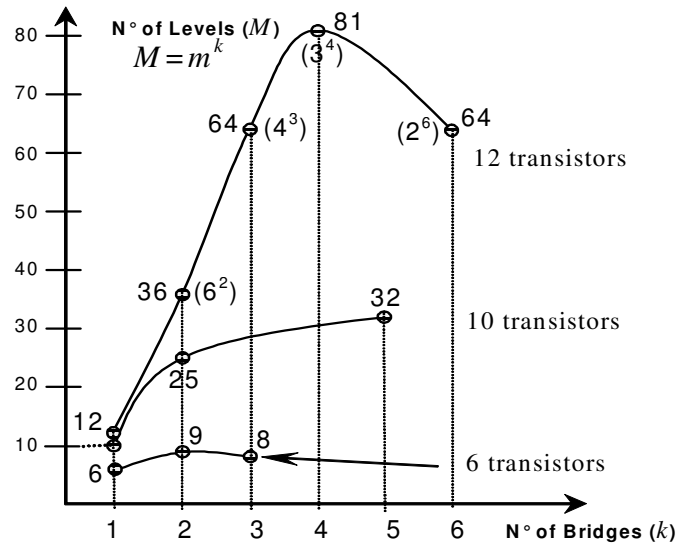


Fig. 8. Total number of levels related with the number of bridges and transistors

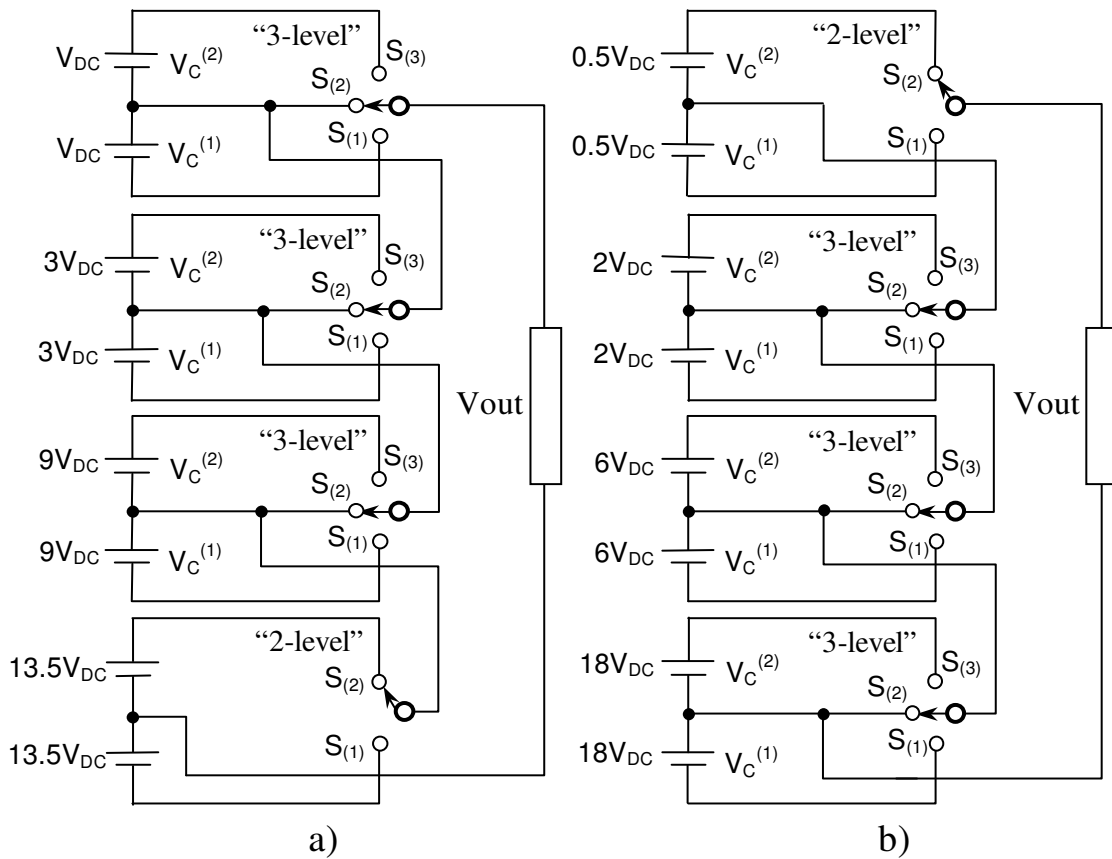


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 a) The 2-level inverter at the bottom
 b) The 2-level inverter on the top

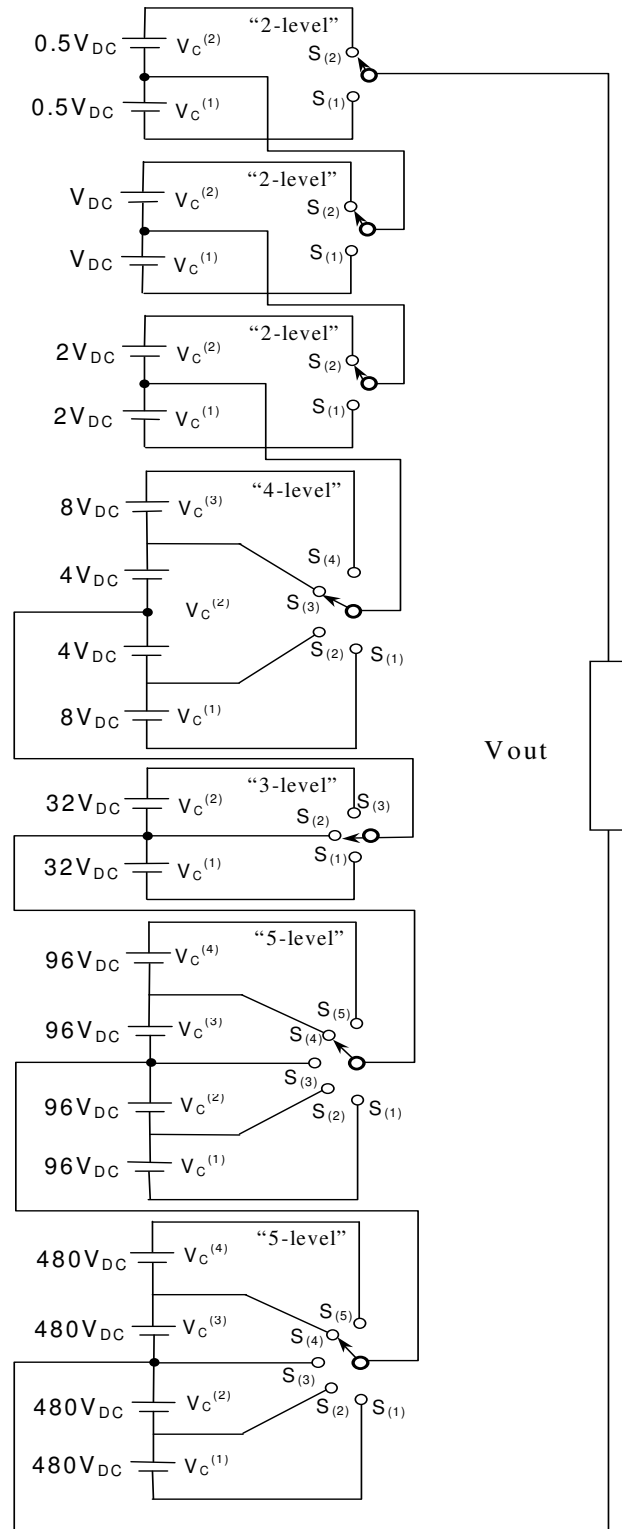


Fig. 10. 2400-level inverter, using a series of different m-level bridges.

Trans.	Levels
2	2
3	3
4	4
5	6
6	9
7	12
8	18
9	27
10	36
11	54
12	81
13	108
14	162
15	243
16	324
17	486
18	729
19	972
20	1458
21	2187
22	2916
23	4374
24	6561
25	8748

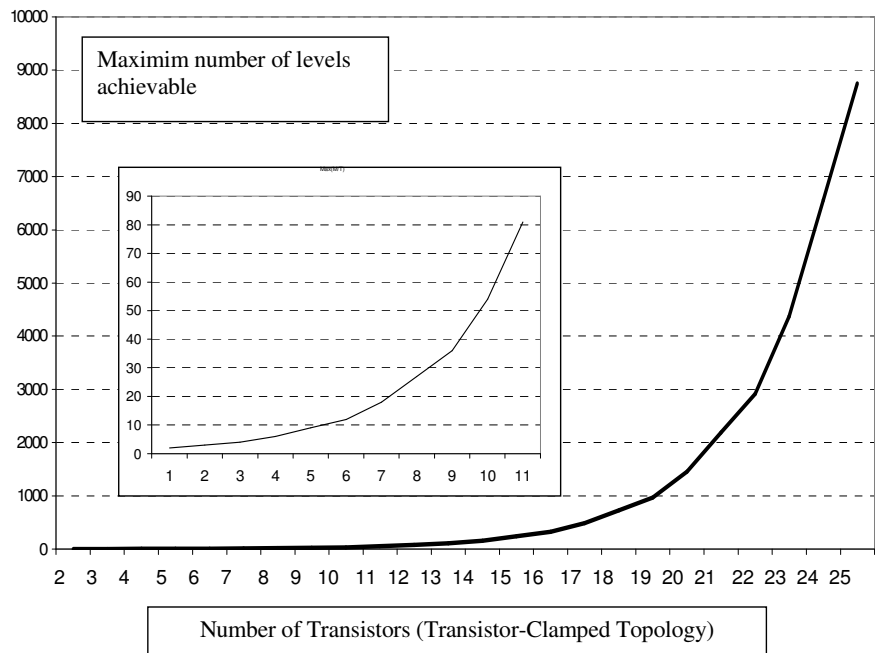


Fig.11. Maximum number of levels reachable with a given number of transistors

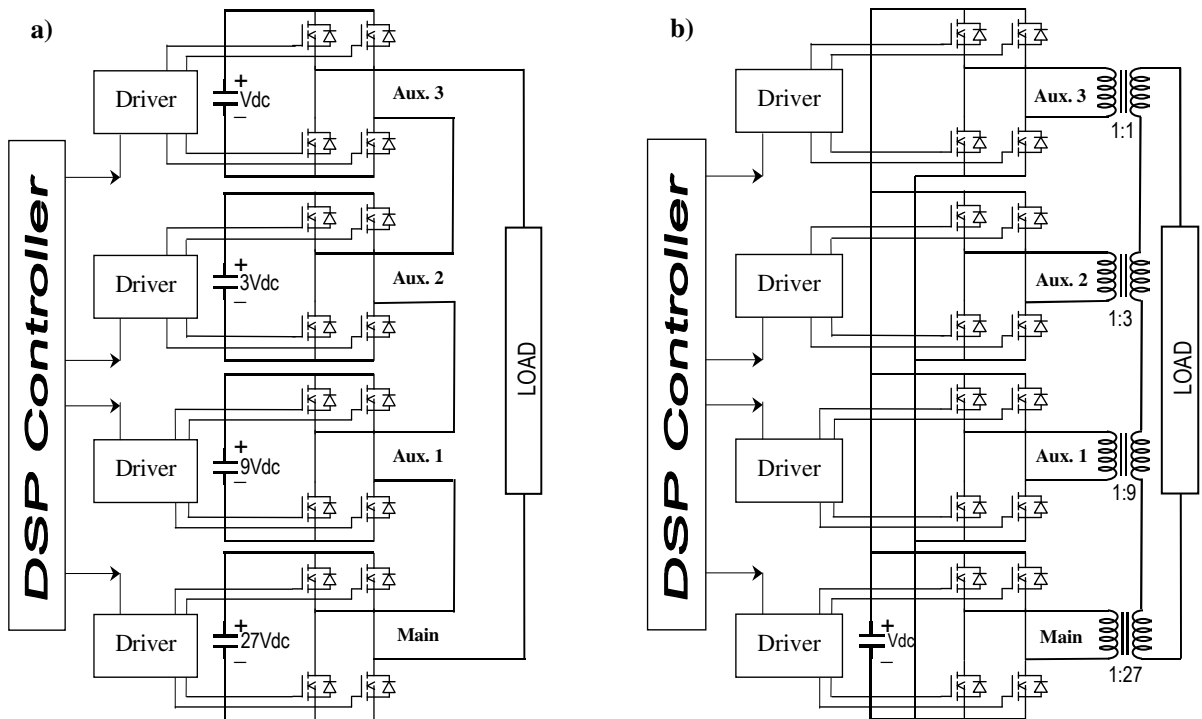


Fig. 12. Main components of an 81-level multiconverter.

a) four individual voltage sources for each module.

b) one single voltage source for all modules, series connection via output transforms.

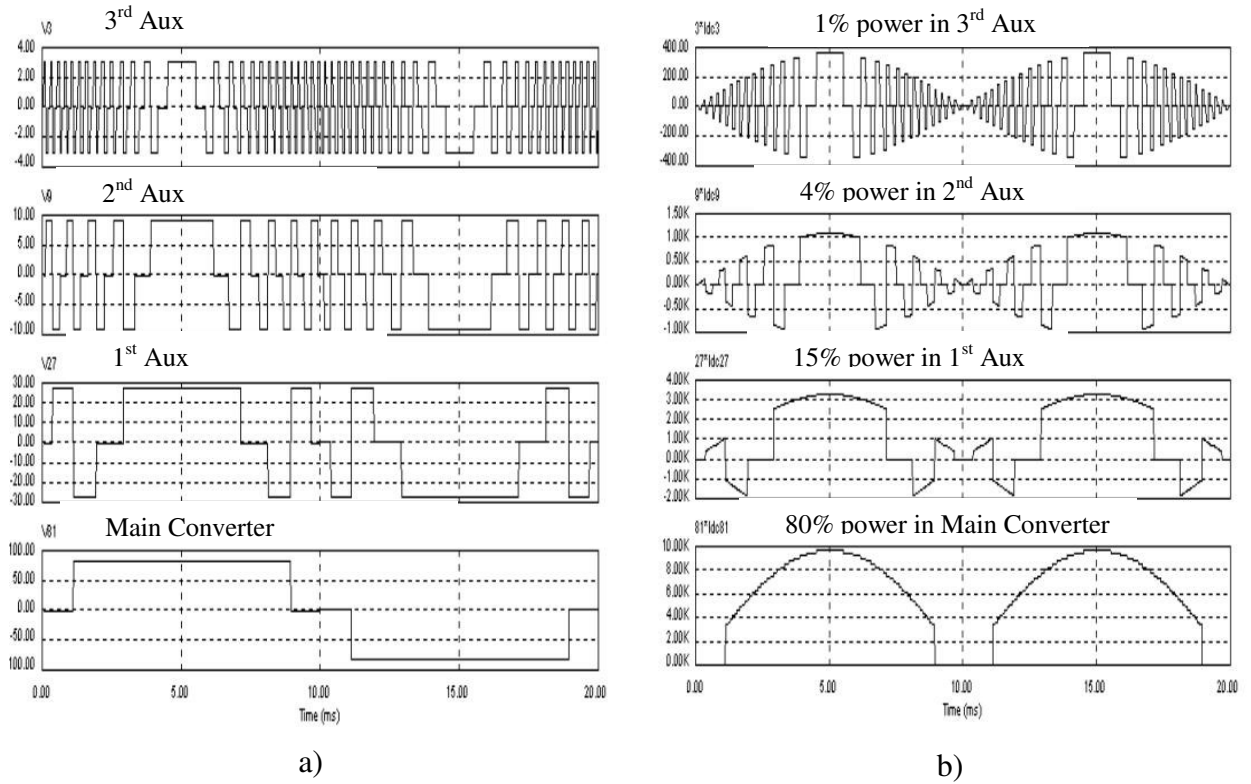


Figure 13: a) frequency modulation in each converter, b) power distribution in each converter

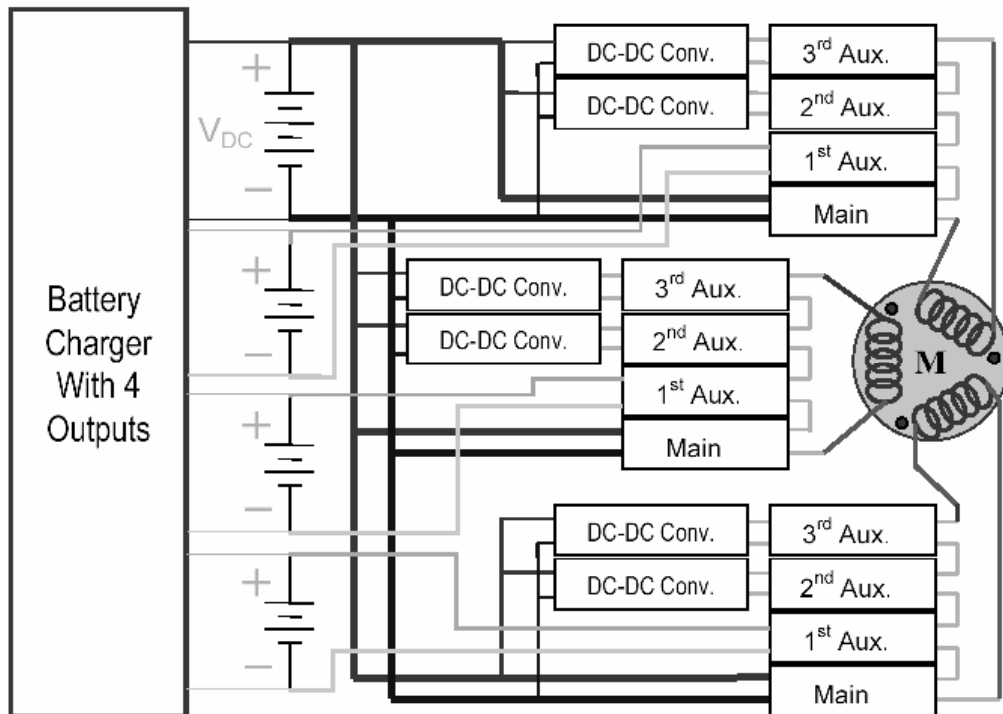


Figure 14: Special 81-level arrangement for electric vehicle

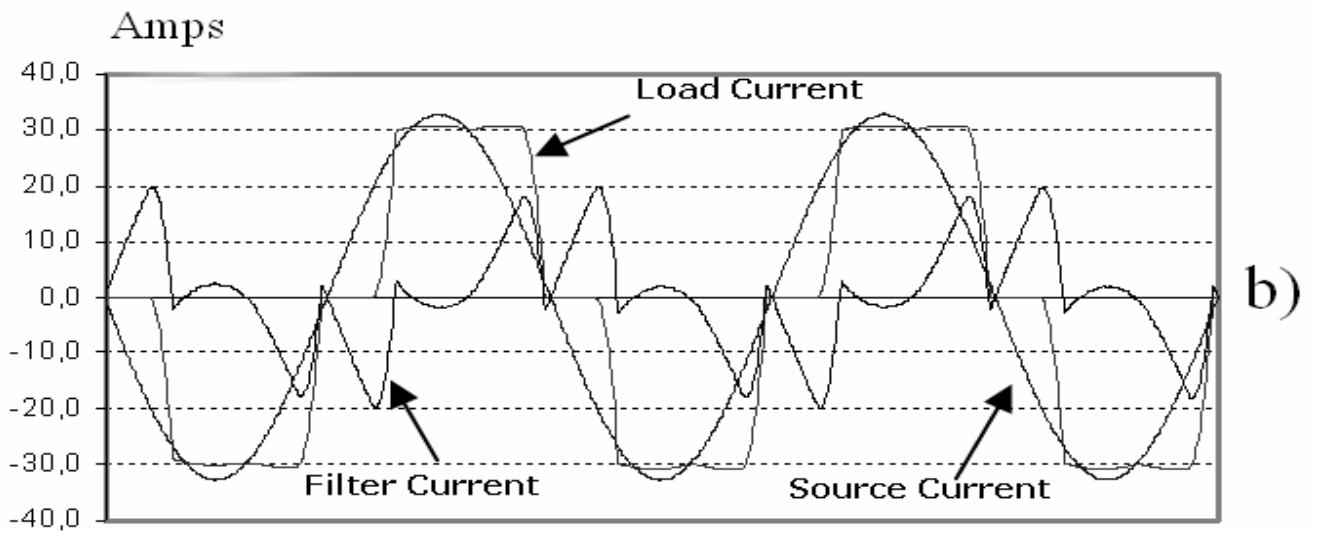
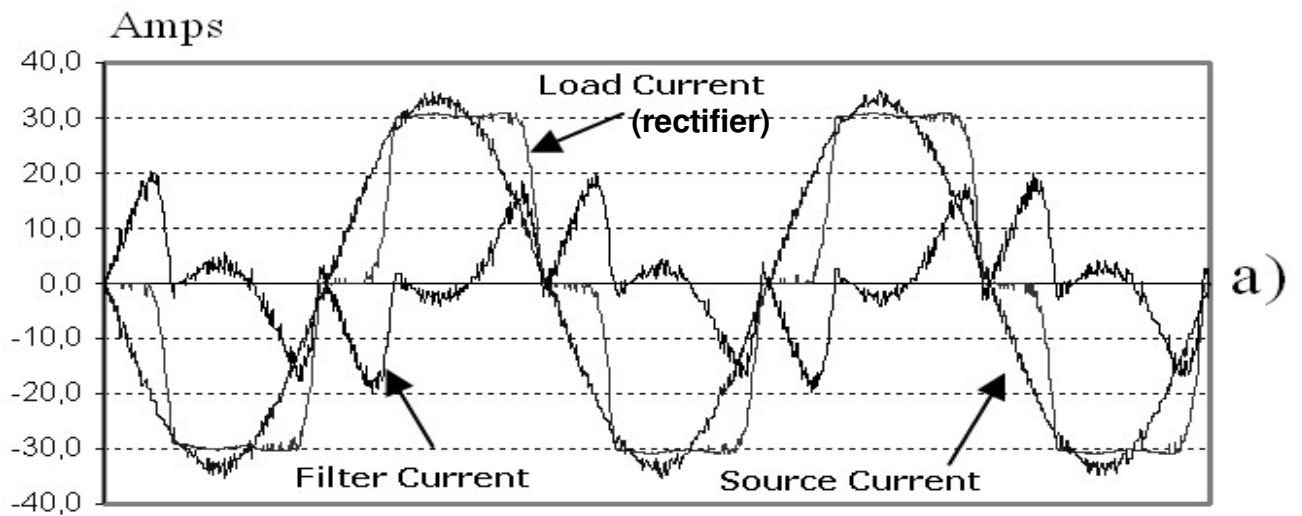


Fig. 15. Active power filter waveforms: a) PWM technique; b) 81-level technique

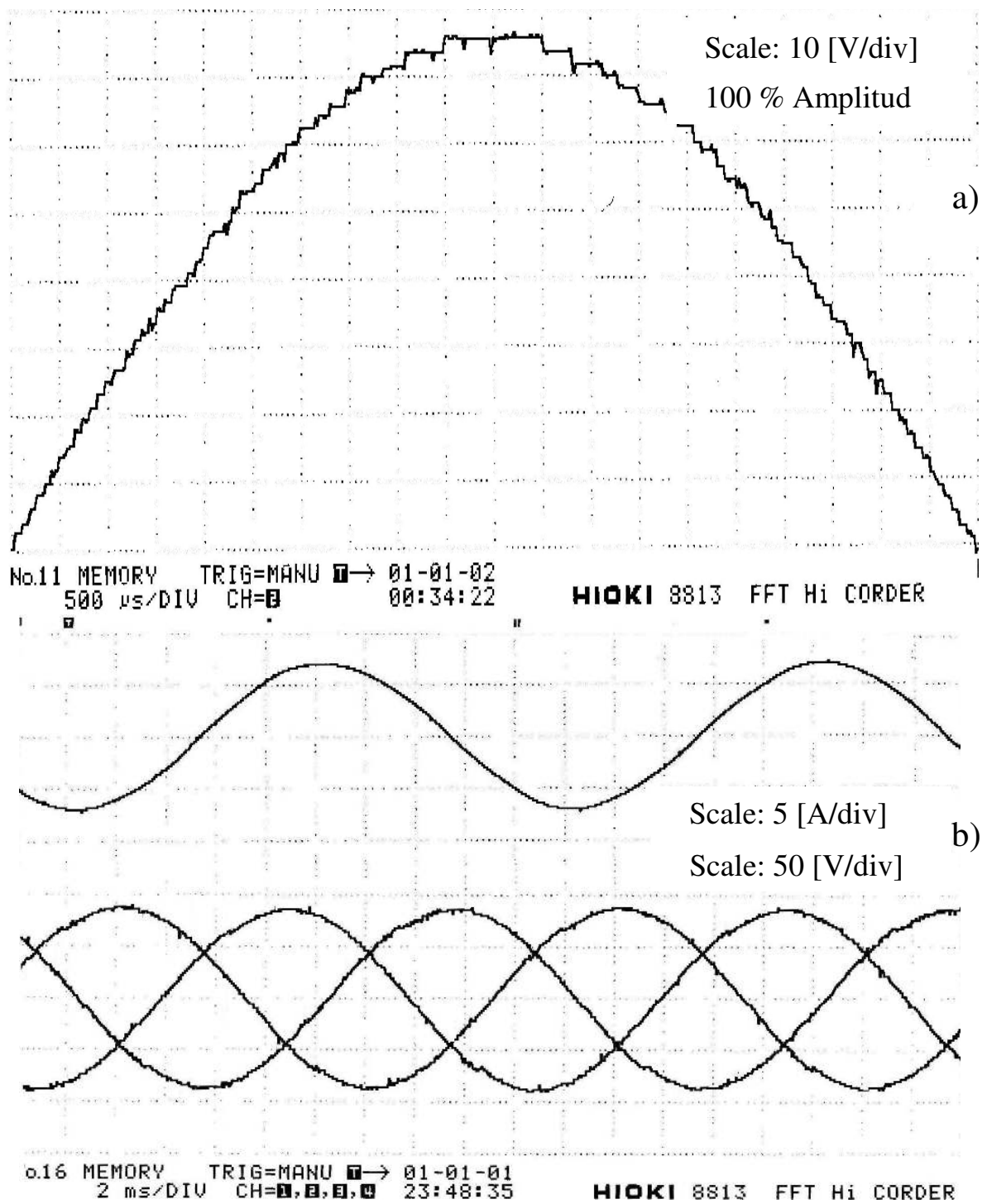


Fig.16. a) half-wave voltage waveform at the output of the experimental 81-level converter
b) current in one phase and voltages at the three phases of an induction motor