High-Level Simulation of Substrate Noise Generation Including Power Supply Noise Coupling

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Abstract

Substrate noise caused by large digital circuits will degrade the performance of analog circuits located on the same substrate. To simulate this performance degradation, the total amount of generated substrate noise must be known. Simulating substrate noise generated by large digital circuits is however not feasible with existing circuit simulators and detailed substrate models due to the long simulation times and high memory requirements. We have developed a methodology to simulate this substrate noise generation at a higher level. Not only does this methodology take noise coupling from switching gates into account, but also noise coupling from the power supply is included. This paper describes this simulation methodology. In the paper it is shown that the high-level simulations correspond very well with SPICE simulations and that a large gain in simulation speed is obtained. This high-level simulation methodology makes it possible to predict substrate noise generation of large digital circuits in a very efficient way, early in the design flow of mixed-signal ASICs.

1 Introduction

There is a trend to integrate more and more functionality on one single chip. Also analog circuits, for example analog-to-digital converters, are integrated on the same silicon substrate as digital signal processing circuits [1]. This integration of analog and digital circuits on one silicon substrate will cause substrate noise coupling problems: the performance of the analog circuits will degrade due to substrate noise generated by the digital circuits.

The substrate noise coupling problem consists of three parts: generation of substrate noise by the digital circuits, propagation of noise through the substrate and impact of substrate noise on analog circuits. Most research done in recent years has concentrated on modeling the propagation and the impact of substrate noise [2]. Those modeling and simulation techniques are only useful when working with small circuits because of the complexity of the extracted models. It is not possible to use those techniques to simulate substrate noise generation of large digital circuits. Other techniques have been proposed to model and simulate the noise generation. In [3] and [4] methodologies are proposed that use verilogHDL and analogHDL routines to count the switching transitions of a digital circuit and calculate the substrate noise using mathematical expressions. Because a mathematical expression is used for the generated substrate noise, rather than the real waveforms, these simulations can never result in an accurate prediction of generated substrate noise. A methodology that does make use of simulated noise waveforms is presented in [5], but a very simple model is used to extract the injected noise currents and the resulting substrate voltage is not calculated. All of these methodologies do not include noise coupling from the power supply, which can be a dominant source of substrate noise, and neglect noise generation from switching inputs that do not necessarily cause output switching events. Another simulation methodology that does take power supply noise coupling into account is presented in [6]. But only the root-mean-square of the power supply current is taken into account and not the transient behavior of this current.

In this paper, however, we present a methodology to simulate substrate noise generation from switching gates as well as the power supply. This allows to study the effect of different inductance values in the power supply connection and also the effect of extra on-chip decoupling capacitance. Our methodology also takes into account noise coupling from switching inputs, that do not necessarily cause an output change, and we use a detailed substrate model to extract the injected substrate noise currents. The high-level simulations result in the total generated substrate voltage noise. This substrate voltage can be used as input signal for a SPICE simulation of sensitive analog circuits, including a substrate model, to determine the performance degradation due to substrate noise coupling.

The paper is organized as follows. Section 2 will give a description of our high-level substrate noise simulation methodology. Section 3 and 4 will describe the different steps in this methodology in more detail. In section 5 the results of our high-level substrate noise simulations will be compared with SPICE simulations.

2 Substrate Noise Simulation Methodology

The high-level simulation methodology for substrate noise generation consists of two parts: a one-time characterization of all stan-

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dard cells to extract the substrate current generation for every possible switching combination and a VHDL gate level simulation (with an extended VHDL gate library) for each design to extract the switching events. From these switching events the total generated substrate noise is calculated. This methodology is schematically shown in figure 1. The characterization of a standard cell library,

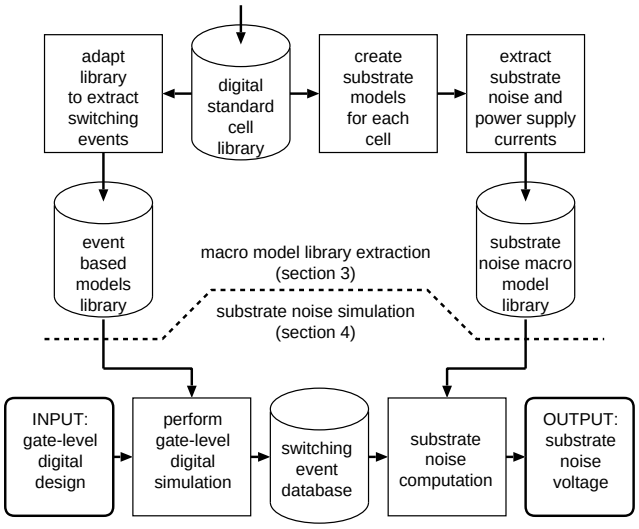

Figure 1: Substrate noise simulation methodology

shown in figure 1 above the dotted line, consists of creating detailed substrate models for each standard cell and extracting the generated switching noise and power current waveforms for all possible switching combinations. These currents, together with a reduced substrate model for the gate, are combined in a macro model. Finally all macro models are collected in a single library. The standard cell library also has to be extended to include switching event extraction routines.

Using the extended VHDL gate library a normal VHDL gate level simulation is performed for a given design. During the simulation all switching events are recorded and collected in a switching event file. Finally the macro models are combined together using the switching event data. The resulting equivalent substrate model for the entire digital circuit is used to simulate the total generated substrate voltage noise. The next two sections describe this methodology in more detail.

3 Macro Model Library Extraction

This section describes the steps that are necessary to extract substrate noise generation data from a given library of digital standard cells.

3.1 SPICE Substrate Modeling

Switching MOSFETs generate substrate currents via two mechanisms: capacitive coupling from source, drain and gate to substrate and impact ionization. Most substrate current is produced by capacitive coupling from drain and source junctions and, depending on the technology, impact ionization [7]. In our simulations we use the BSIM3v3 MOSFET model, which includes both capacitive coupling and impact ionization.

To simulate the amount of substrate noise generated by a digital gate, a model of the substrate must be included in the simulation. We have modeled the substrate in SPICE by adding substrate resistors and well capacitors to the original SPICE circuits of the digital gates. For the SPICE description of the digital gates, Layout Parasitics Extraction (LPE) data is used, to include interconnect coupling within the gates. Figure 2 shows this model for the example of a CMOS inverter. In this work only low-ohmic (typi-

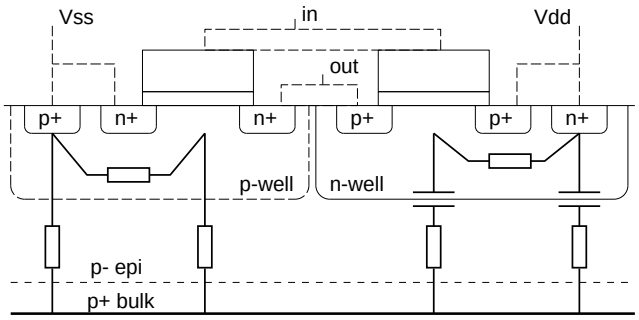

Figure 2: SPICE substrate model

cally 10 mΩcm) substrates are considered and therefore the entire substrate can be approximated by one electrical node. The resistor and capacitor values can be calculated using simple empirical expressions, taking into account geometry information of MOSFETs, wells and substrate taps. This model is used as a reference to calculate the accuracy of the high-level simulations. In [8], the validity of this model has been verified with measurements. More detailed substrate models can be created and are certainly required for high-ohmic substrates [9] and RF applications [10]. Other tools [11] [12] can be used to extract very accurate substrate models, but these models are too complex to be used to simulate the substrate noise generation of large digital circuits.

3.2 Substrate Macro Model

To simulate the substrate noise generation of large digital circuits, macro models for all digital gates have been created. These macro models include the two noise sources (i.e., coupling from the MOSFETs and coupling from the power supply) and a simplified version of the substrate model. The macro models are created in such a way that they can easily be combined in parallel to form the total substrate noise simulation model.

The basis for the macro model is the assumption that switching gates will inject a noise current into the substrate. This current flows back to AC ground via the substrate impedance, generating the substrate voltage. The substrate impedance (i.e., the impedance between substrate and AC ground) can be approximated by the parallel combination of a resistor and capacitor. Figure 3 shows that this approximation is valid up to several GHz. This figure shows the substrate impedance of a CMOS inverter gate for an accurate substrate model extracted with the tool LAYIN [12], for the simple substrate model shown in figure 2 and for the macro model.

The macro model is shown in figure 4. R_{sub} is determined by the resistance between Vss and substrate, C_{well} is the junction capacitance between Vdd and substrate and C_{cir} is the circuit capacitance between Vdd and Vss. Current source I_{noise} models the substrate current injection from switching nodes and current source I_{power} models the power supply current consumption.

Note that the substrate noise current I_{noise} does not directly correspond to the sum of the substrate currents of the MOSFETs in the digital gate. This current is derived in such a way that it will reproduce the correct substrate voltage that corresponds to the substrate voltage generated by the full SPICE substrate model.

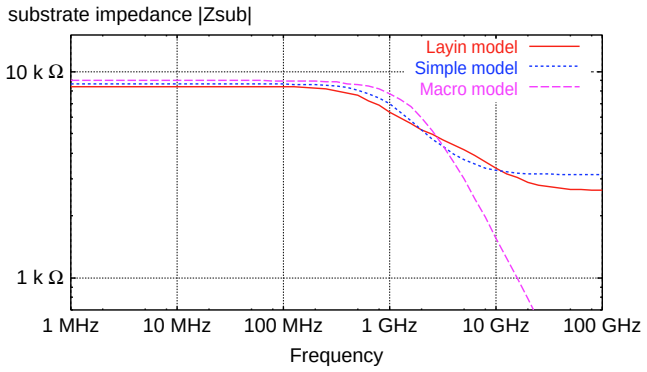

Figure 3: Substrate impedance of a CMOS inverter gate for the different substrate models

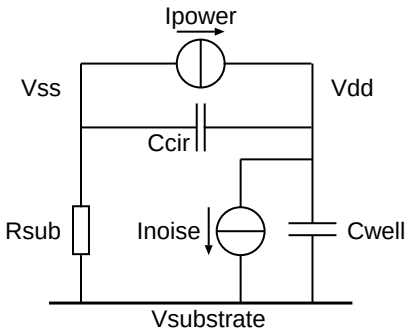

Figure 4: Macro model created for each digital gate

3.3 Noise Current Extraction

Noise coupling from switching MOSFETs is not only caused when the output of a digital gate switches, but also input transitions that do not cause output transitions will cause substrate noise. In figure 5 this is illustrated for a NAND gate ($Z = \overline{A\,B}$). The rising edge of

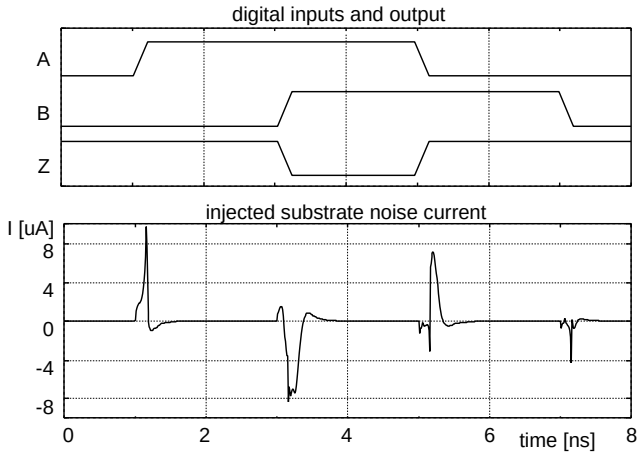

Figure 5: Injected substrate noise current for NAND gate

input A causes a substrate current that is as large as the current caused by a changing output. Also for flip-flops it is important to take noise coupling from switching inputs into account: negative clock edges (for a positive edge triggered flip-flop) and changes on the data input do not directly cause an output transition but will cause substrate noise and these input transitions occur constantly.

To extract the waveform for the current source I_{noise}, shown in figure 4, a SPICE simulation is performed for the digital cell with the detailed substrate model. A digital input pattern is applied to the gate that covers all switching combinations and the resulting substrate voltage is recorded. This voltage is then imposed on the substrate node of the macro model using a voltage controlled voltage source. By measuring the current flowing through this source the waveform for I_{noise} is obtained. This waveform is recorded for each switching action for a period of 2 ns and a time step of 10 ps.

3.4 Power Supply Current Extraction

Apart from substrate noise caused by switching MOSFETs there is another important noise source: noise coupling from the digital power supply [13]. This power supply will contain switching noise and can show oscillations (ringing or ground bounce). Since in each digital gate the ground is connected to the substrate via R_{sub}, the total resistance from ground to substrate can be very low (less than 1 Ω for large digital circuits). So all noise and ringing on the digital ground is directly coupled to the substrate and this noise source can easily dominate the total substrate noise generation. To include noise coupling from the power supply in our methodology, the current source I_{power} has been added in the macro model of figure 4. The waveform of this current source is extracted during the simulation of the noise currents by measuring the current flowing through the supply voltage source.

To accurately simulate noise coupling from the power supply, the ringing effects must also be included in the macro model. This requires that the circuit capacitance C_{cir} between power and ground is extracted for each cell and added to the macro model. This extraction is performed by a small signal simulation of the digital gate without the substrate model.

3.5 VHDL Library Extension

Finally, the VHDL standard cell library has to be extended to enable the detection of all input switching events. This library is created by adding switching event detection processes to the original VHDL library. When the cells from this library are invoked during a gate-level simulation all input transitions are recorded together with the time of occurrence, the cell type, instance name and state of the other inputs. For flip-flops also the output state is recorded.

Figure 6 shows the encapsulation of the VHDL standard cell with the switching activity sensors. This encapsulation does not change any input or output port declaration of the standard cell. A VITAL VHDL library is used for the standard cells to enable the use of back-annotation delays extracted from the layout or wire-load models. This delay information is crucial for an accurate extraction of the switching activities during the simulation. Also included in the encapsulation library is an input glitch removal process. Glitch removal is necessary because the VHDL simulation will record every glitch as a complete up-down (or vice versa) transition while in reality (or in the SPICE simulation) there is only a minor spike in the signal. When these glitches would not be removed from the VHDL simulation, two noise current waveforms, which do not necessarily cancel each other out, would be added to the total noise current, while in reality the noise associated with this glitch is negligible. However, the substrate noise generated by the gate that causes the glitch signal is taken into account.

3.6 Library Characterization Results

As a test case the library characterization has been performed for a commercial 0.5 μm CMOS technology for a design consisting

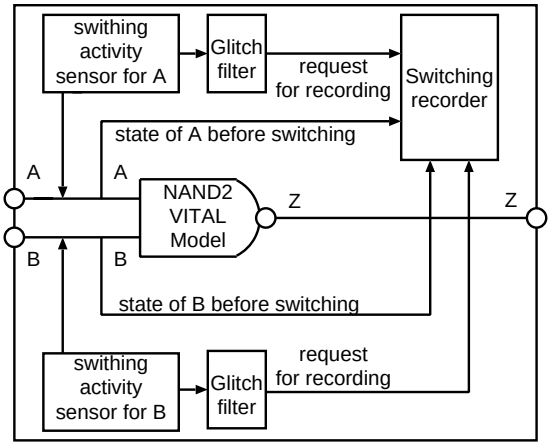

Figure 6: Switching recording in VHDL

of 96 different gates. The extraction figures are mentioned in the next table. The entire characterization is performed automatically by a C++ program. The macro model library size could be greatly reduced by storing the data in binary format instead of the current ASCII format.

number of different cells	96
number of switching combinations	4780
total extraction time	39 hours
macro model library size	21 Mbyte

4 Substrate Noise Simulation

To simulate the total generated substrate noise for a given circuit, first a normal gate-level VHDL simulation is performed using the special VHDL switching event detection library. During this simulation an output file is created that contains a list of all switching events. A part of such an output file is shown below.

```
55 NS     1H00------ FD2Q buf_reg_3
55 NS     1H01------ FD2  buf_reg_0
55.924 NS 11H1------ FD2  buf_reg_0
57.063 NS L1-------- EO   U31
57.063 NS L1-------- ND2  U29
57.08 NS  0H-------- EN   U30
57.08 NS  H--------- IV   U26
```

The elements recorded in this file are the time instance of the switching event, the state of the inputs (and in case of flip-flops, also the output state), the cell type and instance name.

Next, the macro models for all individual gates in the design have to be combined together. For high-ohmic substrates the macro models can be combined together in small groups taking the floorplanning information into account. These groups of macro models can be combined together by connecting the substrate nodes to a substrate resistor mesh. Also power routing parasitics can be added between the groups of macro models. For low-ohmic substrates, used in these experiments, this resistor mesh can be approximated by one electrical node and all macro models can be connected in parallel. This results in one equivalent substrate noise simulation model, shown in figure 7.

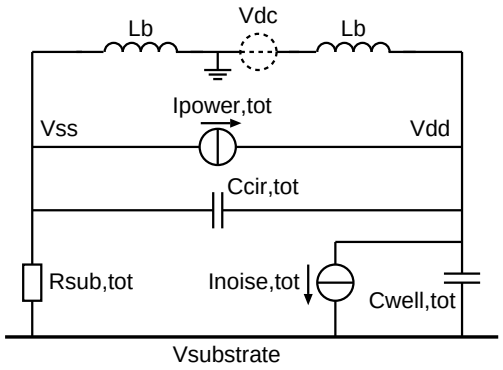

Figure 7: Equivalent substrate noise simulation circuit

The element values of this model are calculated using the following expressions:

$$\frac{1}{R_{sub,tot}} = \sum_{\text{all gates}} \frac{1}{R_{sub,gate}}$$

$$C_{well,tot} = \sum_{\text{all gates}} C_{well,gate}$$

$$C_{cir,tot} = \sum_{\text{all gates}} C_{cir,gate}$$

The waveforms of the noise current and power supply current in the total substrate model are calculated by accumulating all individual waveforms belonging to the switching events:

$$I_{noise,tot}(t) = \sum_{\substack{\text{all switching} \\ \text{events}}} I_{noise,event}(t - t_{event})$$

$$I_{power,tot}(t) = \sum_{\substack{\text{all switching} \\ \text{events}}} I_{power,event}(t - t_{event})$$

Finally, parasitics (e.g., inductances from wirebonds) in the power supply connections are added. An “external” voltage source can be included to set the correct operating point (e.g., set Vdd to 3.3 Volt).

By solving the equivalent substrate circuit, the resulting substrate voltage is obtained. The substrate noise generation of the switching gates, without power supply noise, can be simulated by using an ideal on-chip power supply (i.e., set the inductance Lb to 0 nH). The effect of different power supply connection parasitics (e.g., the use of different packages or number of parallel power connections) and extra (on-chip) decoupling capacitance on substrate noise and power supply noise can also be simulated.

5 Experimental Results

In this section the comparison between high-level and SPICE simulations will be shown for two circuits: a 4 bit counter and a multiplier. The last part of this section summarizes the simulation times and circuit details.

5.1 Four Bit Counter

The first test circuit is a 4 bit counter, consisting of 4 flip-flops and a combinatorial feedback circuit. Using our simulation methodology we can simulate the generated substrate noise of this circuit for different inductance values. Figure 8 shows the comparison between the SPICE and the high-level simulations of the substrate voltage

produced by the counter, for one clock period (a rising and falling clock edge). At the rising clock edge (55 ns) the four flip-flops are clocked and 13 combinatorial switching events occur. The negative clock edge (60 ns) only causes a falling edge on the clock inputs of the flip-flops. Although no output changes occur at the falling clock edge still a significant amount of substrate noise is generated. Figure 8 clearly shows the good correspondence between the

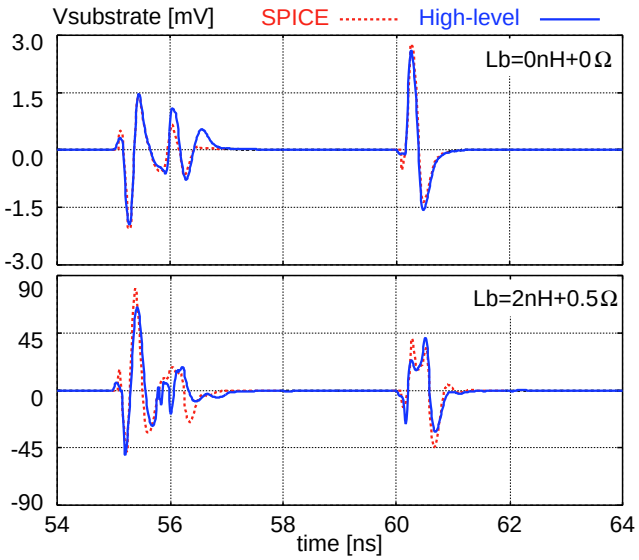

Figure 8: SPICE versus high-level simulation of generated substrate noise with (bottom) and without (top) power supply noise coupling for the counter circuit

SPICE and the high-level simulation. A quantitative comparison is given in the next table where the root mean square (RMS) values of the substrate noise are listed. This RMS value is an indication for the total substrate noise power.

	$V_{sub,rms}$[mV]	error
SPICE (with supply noise)	12.3	
High-level (no supply noise)	0.48	96.1%
High-level (with supply noise)	12.6	2.4%

For the high-level simulation with power supply noise coupling, an inductance value of 2 nH + 0.5 Ω has been used. The error value given in the table is the error of the high-level simulation result with respect to the SPICE simulation. These results show that a high-level substrate noise simulation without power supply noise coupling severely underestimates the amount of generated substrate noise.

5.2 Multiplier

The multiplier circuit consists of an 8-bit up counter and 8-bit down counter followed by a 16-bit Booth multiplier, which multiplies the two counter values. Figure 9 shows the comparison of a SPICE and high-level simulation for substrate voltage noise and power supply current. The simulation is performed without power supply noise coupling (Lb = 0 nH) and shows the result of approximately 170 switching activities, occuring after one rising clock edge. The next table gives the comparison of the RMS value of the substrate voltage for a SPICE simulation and high-level simulation with and without power supply noise coupling.

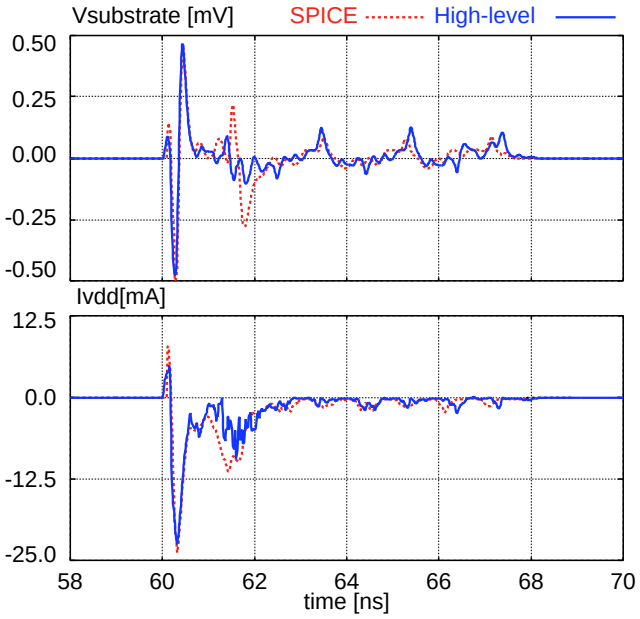

Figure 9: SPICE and high-level simulation of substrate noise voltage (top) and power supply current (bottom) for the multiplier circuit without power supply noise

	$V_{sub,rms}$[mV]	error
SPICE (with supply noise)	18.4	
High-level (no supply noise)	0.079	99.6%
High-level (with supply noise)	19.4	5.4%

Again it is clearly visible that the power supply noise coupling is a dominant source of substrate noise. To obtain a good correspondence with the SPICE simulations, the power supply noise coupling must be included in the high-level simulations.

It is also important that the high-level simulations are valid when studying the frequency spectrum of the generated substrate noise. Figure 10 shows the frequency spectrum of the substrate noise voltage (in dB relative to a 1 volt sine wave) for the multiplier circuit with power supply noise coupling included (Lb = 2 nH + 0.5 Ω). This spectrum is obtained by taking a Fast Fourier Transform of a 1200 ns period of the substrate voltage with a time step of 10 ps. The increase of the substrate noise around 400 MHz is caused by ringing of the on-chip power signal, which is coupled to the substrate. Most substrate noise is concentrated at multiples of the digital clock frequency of 42 MHz. The location and amplitude of the major noise peaks corresponds well for the SPICE and high-level simulation.

5.3 Simulation Figures

The next table summarizes the details of the circuits, the simulation times and model parameters. Also included in this table are figures for a large circuit, which can no longer be simulated with SPICE. This circuit is a multi-rate channel select filter and up/down converter for a cable modem front-end.

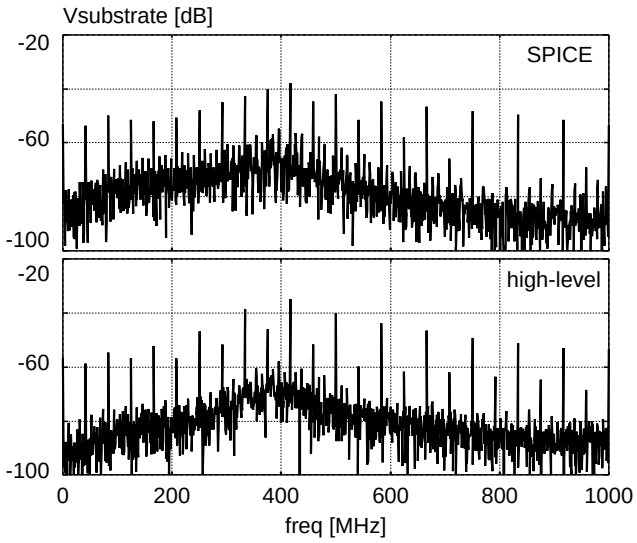

Figure 10: SPICE and high-level simulation of the frequency spectrum of the substrate noise voltage for a for the multiplier circuit with power supply noise included

circuit details	counter	multiplier	filter
area (equiv.gates)	34	994	81012
transistors	160	4178	371355
max.clk.freq.[MHz]	100	42	160
simulation data	counter	multiplier	filter
clock cycles	50	208	800
tot. switching events	856	63545	100981
SPICE sim. time (a)	435 sec.	37 hours	—
VHDL sim. time (b)	1.0 sec.	29 sec.	32 min.
Noise calculation (c)	5.2 sec.	4.9 min.	10 min.
Speedup = a/(b+c)	70x	412x	—
model parameters	counter	multiplier	filter
Rsub,tot [Ω]	327	10.8	0.14
Cwell,tot [F]	536f	15.24p	1.26n
Ccir,tot [F]	850f	26.40p	2.28n

6 Conclusions

For large designs it is not feasible to use a circuit simulator like SPICE to simulate the amount of generated substrate noise. Therefore a high-level substrate noise simulation methodology is required. In this paper a new methodology for the simulation of substrate noise generation for large digital circuits is presented. For each digital gate a macro model is extracted that models the substrate current injection and power supply current for all switching combinations. A VHDL switching event detection library is created to record all switching events during a standard VHDL gate-level simulation. By combining the switching event data with the substrate macro models, one equivalent substrate noise simulation model is derived for an entire digital circuit. This model is used to simulate the amount of generated substrate noise. We have verified our high-level methodology with SPICE simulations for two test circuits. It has been shown that a significant improvement in simulation speed is obtained while retaining good accuracy.

Acknowledgments

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