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To our loving families.

Contents

Preface

Computer-aided synthesis of digital circuits from behavioral level specifications offers an effective means to deal with the increasing complexity of digital hardware design. This book addresses both theoretical and practical aspects in the design of a high-level synthesis system that transforms a behavioral level description of hardware to a synchronous logic-level implementation consisting of logic gates and registers.

The present level of maturity of synthesis techniques for digital circuits has been proven by the large number of designs achieved by means of computer-aided tools. Synthesis from behavioral descriptions can leverage the expressive power of high-level models and shorten the design time of a circuit. High-level optimization algorithms can be extremely powerful in making decisions about the macroscopic structure of a circuit, with beneficial effects on the overall performance, area and testability.

Synthesis techniques provide a competitive edge in the design of *Application Specific Integrated Circuits* (ASICs), which represent a growing sector of the semiconductor market. In particular, high-level synthesis can be extremely useful to ASIC design, because of the paramount importance of short time to market.

This book addresses specific issues in applying high-level synthesis techniques to the design of ASICs. This complements previous results achieved in synthesis of general-purpose and signal processors, where *data-path* design is of utmost importance. In contrast, ASIC designs are often characterized by complex *control* schemes, to support communication and synchronization with the environment. The combined design of efficient data-path and control-unit is the major contribution of this book.

Three requirements are important in modeling ASIC designs: *concurrency*, *external synchronization*, and *detailed timing constraints*. The objective of the research work presented here is to develop a hardware model incorporating these requirements as well as synthesis algorithms that operate on this hardware model.

The contributions of this book address both theory and implementation of algorithms for hardware synthesis. The following novel synthesis algorithms have been developed: *relative scheduling*, a scheduling formulation that supports external synchronizations and detailed timing constraints; *constrained conflict resolution*, a method to resolve resource conflicts under timing constraints; *relative control synthesis*, a control generation approach for relative scheduling; *relative control optimization*, a novel optimization strategy that minimizes the size of the control implementation under timing constraints.

In addition, we developed a hardware description language called *HardwareC* with particular attention to ASIC design specification issues. The system implementation of the algorithms is provided by programs *Hercules* and *Hebe*, which serve as the front-end to Stanford's Olympus Synthesis system. They have been applied to the synthesis of benchmark examples and to some chip designs at Stanford University.

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G. De Micheli

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We would like to acknowledge the significant contributions of David Filo to the project. He co-developed the theory behind the control resynchronization optimization, described in Chapter 9 of this book. He implemented control optimization and register folding in program Hebe. Other supporting tools of the *Olympus* suite were developed by Frédéric Mailhot, who was responsible for the logic-level framework, which included technology mapping, logic simulation, and the SLIF interchange format and by Thomas Truong, who wrote a simulator for SIF and a graphic display package.

Rajesh Gupta spent a vast amount of time generating design and benchmark examples in HardwareC, working with Claudionor Coelho on the network co-processor and with Thomas Truong on the second version of the DAIO chip. Dave Kasle designed the MAMA decoder chip. Michiel Ligthart designed the first version of the DAIO chip. We are indebted to them for their tenacious work in using the prototype versions of the synthesis system. We also thank Polly Siegel, Jerry Yang and Maurizio Damiani for their suggestions and criticisms.

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