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# High mobility and high on/off ratio field-effect transistors based on chemical vapor deposited single-crystal MoS$_2$ grains

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We report the electrical characteristics of field-effect transistors (FETs) with single-crystal molybdenum disulfide (MoS$_2$) channels synthesized by chemical vapor deposition (CVD). For a bilayer MoS$_2$ FET, the field-effect mobility is $\sim$17 cm$^2$ V$^{-1}$ s$^{-1}$ and the on/off current ratio is $\sim$10$^8$, which are much higher than those of FETs based on CVD polycrystalline MoS$_2$ films. By avoiding the detrimental effects of the grain boundaries and the contamination introduced by the transfer process, the quality of the CVD MoS$_2$ atomic layers deposited directly on SiO$_2$ is comparable to or better than the exfoliated MoS$_2$ flakes. The result shows that CVD is a viable method to synthesize high quality MoS$_2$ atomic layers. © 2013 AIP Publishing LLC [http://dx.doi.org/10.1063/1.4801861]

The single-layer (SL) graphene has a linear Dirac-like band structure with no bandgap, which leads to the formation of massless Dirac fermions with remarkable electronic properties, e.g., an effective speed of light $v_F \approx 10^6$ ms$^{-1}$ and a room temperature mobility of 200 000 cm$^2$ V$^{-1}$ s$^{-1}$. However, the lack of a bandgap also limits the application of graphene. Recently, transition metal dichalcogenides (TMDs), in particular, molybdenum disulfide (MoS$_2$), have attracted a lot of attention. The bulk MoS$_2$ is a semiconductor with an indirect bandgap of $\sim$1.3 eV, and the SL MoS$_2$ has a direct bandgap of $\sim$1.8 eV.[1] Therefore, MoS$_2$ could complement graphene for many electronic and photonic applications. However, studies of mechanically exfoliated MoS$_2$ on SiO$_2$ found the room temperature mobility is $<$10 cm$^2$ V$^{-1}$ s$^{-1}$ for SL-MoS$_2$ and 10–15 cm$^2$ V$^{-1}$ s$^{-1}$ for bilayer MoS$_2$,[2,3] which are substantially lower than the measured $\sim$200 cm$^2$ V$^{-1}$ s$^{-1}$ of the bulk MoS$_2$ (Ref. 4) or the calculated $\sim$410 cm$^2$ V$^{-1}$ s$^{-1}$ of intrinsic n-type SL-MoS$_2$, which is limited only by optical phonon scattering.[5] The lower than expected mobility is partially due to the long ranged charge disorder or short ranged disorder caused by chemical bonding or roughness at the interfaces.[6] Furthermore, the mechanical exfoliation process cannot be scaled up for practical applications.

Only recently, large-area of SL and few-layer MoS$_2$ films have been synthesized by chemical vapor deposition (CVD),[7,8] sulfurization of MoO$_3$,[9] or thermolysis of (NH$_4$)MoS$_4$.[10] CVD has been demonstrated as the most practical method of synthesizing large-area and high quality graphene,[11] boron nitride,[12] and boron carbon nitride nanosheets.[13] However, devices fabricated from these polycrystalline MoS$_2$ films are still substantially inferior to their exfoliated counterparts.[2,14] One possible cause of the degradation of performance is the detrimental effects of the grain boundaries, which can be avoided in the case of graphene by going to a seeded growth single-crystal array approach by CVD to place graphene grains at predetermined locations where devices will be located.[15]

In this paper, we report the construction of field-effect transistors (FETs) based on single-crystal bilayer and few-layer MoS$_2$ grains. SL, bilayer, and few-layer grains with sizes up to 20 $\mu$m were synthesized directly on SiO$_2$ by CVD. Bilayer and few-layer FETs offer higher on-state current than the SL-MoS$_2$ FET while maintaining high on/off current ratios.[3] With a single-crystal bilayer MoS$_2$ conducting channel, we have achieved a superior mobility of 17.3 cm$^2$ V$^{-1}$ s$^{-1}$ and a current on/off ratio of $4 \times 10^8$ in a back-gated MoS$_2$ FET.

Our CVD-growth method of single-crystal MoS$_2$ grains is a modification of what is described in Ref. 7 for continuous MoS$_2$ films. However, we do not use seeds as nucleation centers to initiate the growth. Single-crystal MoS$_2$ grains were synthesized in a conventional horizontal quartz tube furnace with sulfur and MoO$_3$ powders as source materials. The MoO$_3$ (0.1 g, Alfa, 99.5%) was placed in an alumina boat and loaded into the center uniform-temperature zone of the furnace. However, we found the residues deposited on the wall of the quartz tube furnace also contribute to the subsequent MoS$_2$ growth, which is not the focus of this paper and will be discussed in detail in another paper.

A piece of Si wafer with 300 nm SiO$_2$ layer was put downstream in a separate boat as substrate. Another alumina boat with 0.4 g sulfur (Alfa, 99.5%) was placed upstream in a low-temperature zone. Before growth, the furnace was evacuated down to $\sim$70 mTorr and back-filled with Ar gas to ambient pressure. In the flow atmosphere of 100 sccm Ar, the furnace was heated to 700 °C at the center zone in 60 min subsequently up to 1100 °C in 130 min. The temperature of the sulfur and the substrate was increased concurrently to $\sim$100 °C and $\sim$700 °C, respectively. After 20 min, the furnace was cooled down naturally to room temperature.

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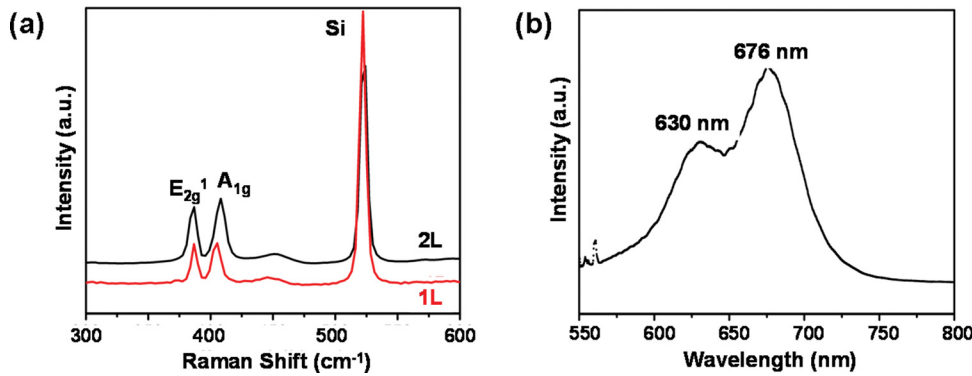
FIG. 1. (a) Raman spectra of typical single-layer and bilayer $MoS_2$ crystals. $E_{2g}^1$ at $385 cm^{-1}$ and $A_{1g}$ at $407 cm^{-1}$ for bilayer; $E_{2g}^1$ at $386 cm^{-1}$ and $A_{1g}$ at $404 cm^{-1}$ for single layer. (b) Photoluminescence spectrum of a typical bilayer $MoS_2$ crystal. The laser excitation wavelength is 532 nm.

Raman spectroscopy is used as a non-destructive method to characterize crystalline quality and thickness of $MoS_2$ grains. Representative Raman spectra of SL and bilayer $MoS_2$ grains are shown in Fig. 1(a). For $MoS_2$ crystals, two characteristic Raman active modes, $E_{2g}^1$ and $A_{1g}$, are found. They are associated with the in-plane and out-of-plane vibration of sulfides, respectively.[16] It has been reported that the peak frequency difference between $E_{2g}^1$ and $A_{1g}$ ($\Delta$) can be used to identify the number of $MoS_2$ layers.[8,9,17] Figures 2(a) and 2(b) show Raman intensity mappings of $E_{2g}^1$ at $385 cm^{-1}$ and $A_{1g}$ at $407 cm^{-1}$ of a triangular shape $MoS_2$ grain, which confirms the thickness and quality uniformity of the CVD grains. A $\Delta$ of $22 cm^{-1}$ suggests the grain is a bilayer $MoS_2$ crystal. For SL $MoS_2$, $\Delta = 18 cm^{-1}$ in our system. In Fig. 1(b), a typical photoluminescence (PL) spectrum of the bilayer grain presents two emission peaks at 676 nm and 630 nm, known as A1 and B1 direct excitonic transitions, respectively.[18] The PL result is also consistent with recent studies of large-area CVD $MoS_2$ films.[7,9]

The individual $MoS_2$ grains were first visually inspected and selected under an optical microscope, and their positions were recorded with respected to predefined marks. The numbers of $MoS_2$ layers of individual grains were determined by Raman spectroscopy. Subsequently, $MoS_2$ grains were fabricated into back-gated FETs with the standard microelectronics processes following steps similar to those described in Ref. 19. The patterned drain and source metal contact electrodes of 45 nm Pd (on top of a 5 nm adhesion layer of Cr) were fabricated on the selected $MoS_2$ grains by electron-beam lithography and a lift-off process.

Figure 3(a) shows an optical microscopy image of the FET under study. The channel of the FET is bilayer $MoS_2$ determined by Raman spectroscopy. The degenerately doped Si substrate, which is separated from the $MoS_2$ channel by a

300 nm $SiO_2$, is used as a back gate to tune the charge carrier density in the $MoS_2$ channel via the application of a back gate voltage $V_G$. Room temperature electrical measurements were performed under vacuum ($10^{-5}$–$10^{-6}$ Torr) in a Lakeshore TTP6 cryogenic probe station.

Figure 3(b) shows the drain current $I_{DS}$ at fixed drain–source voltage, $V_{DS} = +500 mV$, as a function of the applied back-gate voltage $V_G$, for the device shown in Fig. 3(a). The device is an n-channel normally on FET. The field-effect mobility is determined using the formula: $\mu = (L/WC_{ox})\Delta G/\Delta V_G$,[20] where $G = I_{DS}/V_{DS}$ is the conductance and $\Delta G/\Delta V_G = (1/V_{DS})(\Delta I_{DS}/\Delta V_G)$ is determined from the slope of a linear-fit of the data with the back-gate voltage ranges from $V_G = +80 V$ to $V_G = +100 V$. $L = 1 \mu m$ is the length and $W = 3.6 \mu m$ is the width of the $MoS_2$ channel determined from Fig. 3(a). $C_{ox} = \varepsilon_0\varepsilon_r/d$ is the capacitance per unit area, where $d = 300 nm$ is the thickness of the $SiO_2$ layer with $\varepsilon_0 = 8.854 \times 10^{-12} Fm^{-1}$ being the free-space permittivity and $\varepsilon_r = 3.9$ being the relative permittivity of $SiO_2$. The field-effect mobility of the CVD bilayer $MoS_2$ is determined to be $17.3 cm^2 V^{-1} s^{-1}$ comparing to the previously reported $0.02 cm^2 V^{-1} s^{-1}$ of CVD SL-$MoS_2$ (Ref. 7) and $0.04 cm^2 V^{-1} s^{-1}$ of the CVD few-layer $MoS_2$.[8] The much higher mobility of our device may be partially due to the elimination of grain boundary scattering as we reported previously for the CVD graphene.[15] Actually, the $17.3 cm^2 V^{-1} s^{-1}$ mobility of the CVD bilayer $MoS_2$ grain is comparable to the $0.1$-$10 cm^2 V^{-1} s^{-1}$ reported for exfoliated SL-$MoS_2$ (Ref. 2) and the $10$-$15 cm^2 V^{-1} s^{-1}$ for exfoliated bilayer $MoS_2$.[3] Another order of magnitude improvement is expected if a high-$\kappa$ dielectric is applied on the top of the $MoS_2$ channel to reduce the Coulomb effect.[2,3,21]

In Fig. 3(c), the drain current $I_{DS}$ is re-plotted on a logarithmic scale as a function of $V_G$. At $V_G = -100 V$, the
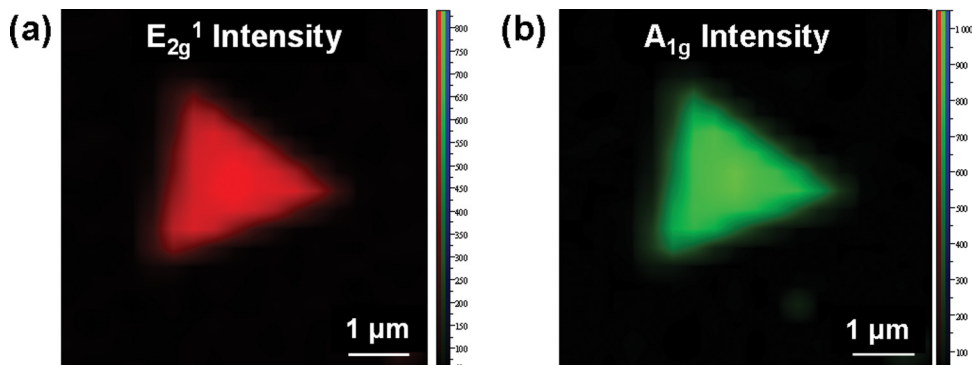


FIG. 2. Raman intensity mappings of (a) $E_{2g}^1$ and (b) $A_{1g}$ of a typical bilayer $MoS_2$ grain.
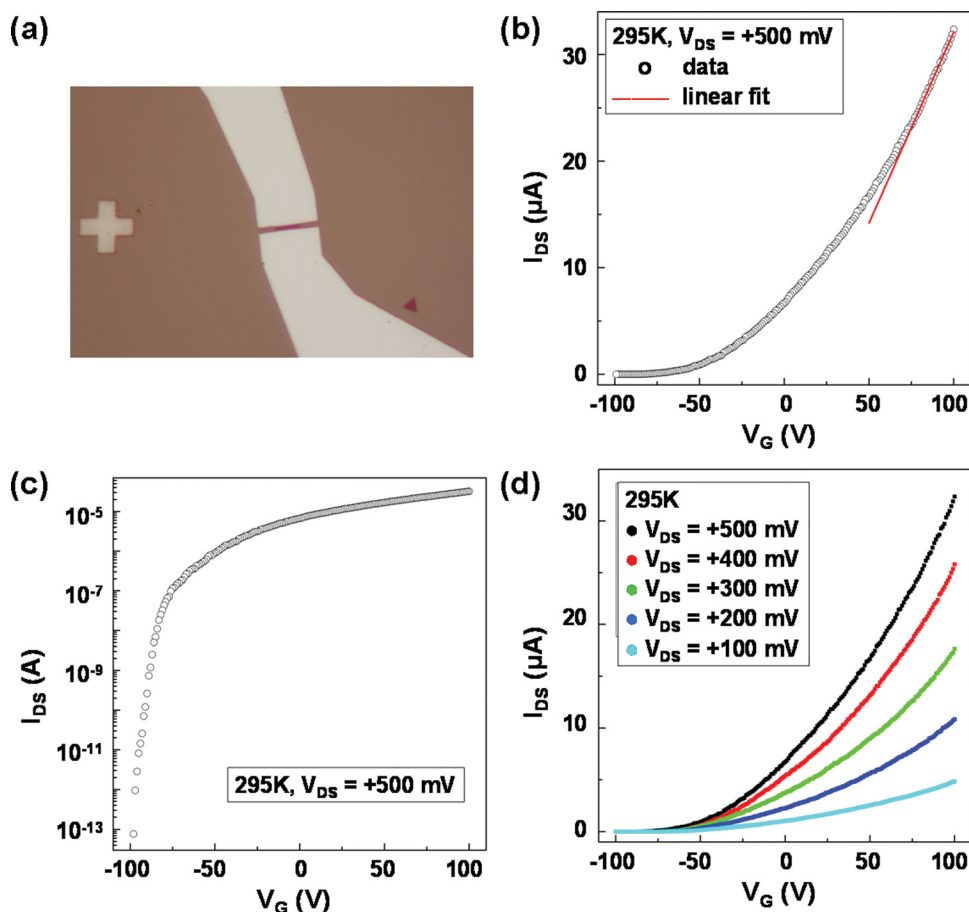
**(a)**

**(b)**



**(c)**

**(d)**

FIG. 3. (a) Optical image of the device. The gap between the two electrodes acrossing the $MoS_2$ grain is $1\,\mu m$, and the width of the channel is $3.6\,\mu m$. (b) Drain-source current $I_{DS}$ as a function of back-gate voltage $V_G$ at fixed drain-source bias voltage $V_{DS} = +500\,mV$ (open circles). (Red line) Linear-fit of the data within the back-gate voltage range from $V_G = +80\,V$ to $V_G = +100\,V$. From the linear fit data, the carrier mobility is calculated to be $\mu = 17.3\,cm^2\,V^{-1}\,s^{-1}$. (c) Drain-source current $I_{DS}$ plotted in logarithmic scale as a function of back-gate voltage $V_G$ at fixed drain-source bias voltage $V_{DS} = +500\,mV$. The optimized current pre-amplifier gain used in the measurement: $100\,pA/V$ for $V_G = -100\,V$ to $-90\,V$, $10\,nA/V$ for $V_G = -89\,V$ to $-80\,V$, $500\,nA/V$ for $V_G = -79\,V$ to $-40\,V$, and $10\,\mu A/V$ for $V_G = -40\,V$ to $+100\,V$. (d) Drain-source current $I_{DS}$ as a function of back-gate voltage $V_G$ at drain-source bias voltages $V_{DS} = +500\,mV$, $= +400\,mV$, $= +300\,mV$, $= +200\,mV$, and $= +100\,mV$.

$MoS_2$ channel of the FET is pinched off with an off-state $I_{DS} < 0.1\,pA$. The on-state $I_{DS}$ is $>30\,\mu A$ with $V_G = +100\,V$. The corresponding on/off current ratio is $4 \times 10^8$, which is higher than the $\sim 10^4$ on/off current ratio reported for CVD polycrystalline $MoS_2$ films[7] and comparable to the $\sim 10^8$ of the exfoliated SL-$MoS_2$ flakes.[2]

Figure 3(d) shows the room temperature transfer characteristics of the FET, i.e., the dependence of drain current on the back-gate voltage at various drain-source voltages. Due to the thick $SiO_2$ back-gate dielectric, no drain current saturation is observed. For comparison, another back-gated FET with a few-layer (<5 layers) $MoS_2$ channel was also fabricated, the mobility is also $\sim 17\,cm^2\,V^{-1}\,s^{-1}$, while the on/off current ratio might be slightly lower, but still $>10^4$. Most recently, ven der Zande *et al.* also reported the electrical characteristics of CVD single-crystal $MoS_2$ grains. The mobility measured within a grain was reported to be $3-4\,cm^2\,V^{-1}\,s^{-1}$, and the on/off current ratio was in the range of $10^5$–$10^7$.[22] Our results are consistent with their findings.

It is well known that the best reported mobility of graphene on $SiO_2$ is limited to $10\,000\,cm^2\,V^{-1}\,s^{-1}$ primarily due to the Coulomb effect.[23] For exfoliated multilayer $MoS_2$ on $SiO_2$, the room temperature mobility can be substantially enhanced by engineering the dielectric environment. For example, multilayer $MoS_2$ has exhibited a mobility $>100\,cm^2\,V^{-1}\,s^{-1}$ when sits on a 50-nm thick atomic layer deposited (ALD) $Al_2O_3$ (Ref. 14) and $470\,cm^2\,V^{-1}\,s^{-1}$ on 50-nm thick spin-coated PMMA.[6] Further enhancement of the $MoS_2$ mobility can be achieved by applying appropriate

gate dielectric on the top of $MoS_2$ channel. A mobility as high as $\sim 200\,cm^2\,V^{-1}\,s^{-1}$ was achieved with a HfO$_2$/SL-$MoS_2$/SiO$_2$ structure, which also exhibits a high on/off ratio ($\sim 10^8$) and low subthreshold swing ($\sim 70\,mV$ per decade).[2] Thus, in addition to fundamental scientific interests, $MoS_2$ FETs could be an attractive candidate for low power electronics, e.g., thin-film transistors (TFTs) in the next generation high-resolution liquid crystal (LCD) or organic light-emitting diode (OLED) displays.[24]

In conclusion, we report the electrical characteristics of back gated FETs fabricated on single-crystal $MoS_2$ grains synthesized by CVD on $SiO_2$. A FET with a bilayer $MoS_2$ channel has a mobility $\sim 17\,cm^2\,V^{-1}\,s^{-1}$ and an on/off current ratio $\sim 10^8$, while the FET with a few-layer $MoS_2$ channel exhibits comparable mobility but slightly lower on/off current ratio. Another order of magnitude improvement of mobility is expected by dielectric engineering to reduce the Coulomb effect. The results suggest that CVD is a viable method to synthesize high quality $MoS_2$ grains with performance comparable to the best mechanically exfoliated $MoS_2$ flakes, and $MoS_2$ FETs are promising candidates for low power electronics.

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