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High mobility holes in a strained Ge quantum well grown on a thin and relaxed $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) virtual substrate

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Epitaxial growth of a compressively strained Ge quantum well (QW) on an ultrathin, 345 nm thick, $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) virtual substrate (VS) has been demonstrated. The VS, grown with a low temperature $Si_{0.4}Ge_{0.6}$ seed layer on a Si(001) substrate, is found to be fully relaxed and the Ge QW is fully strained. The temperature dependence of Hall mobility and carrier density clearly indicates a two-dimensional hole gas in the Ge QW. At room temperature, which is more relevant for electronic devices applications, the samples show a very high Hall mobility of 1235 $cm^2\ V^{-1}\ s^{-1}$ at a carrier density of 2.36×10^{12} cm^{-2}. © *2009 American Institute of Physics*.
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In recent years significant progress has been made toward increasing the room-temperature carrier mobility in a two-dimensional hole gas (2DHG) by using modulation doped (MOD) heterostructures with a compressively strained Ge quantum well (QW) that acts as a channel for mobile carriers. By growing with an intermediate relaxed SiGe buffer on an underlying Si(001) substrate, the strain narrows the band gap of Ge and causes the appearance of a QW in the valence band. Holes confined in the strained Ge QW then have a lower effective mass that increases their mobility. Reduction in the carrier's scattering factor also leads to enhanced mobility in this material system. Indeed, very high 2DHG mobilities in the range 2400–3100 $cm^2\ V^{-1}\ s^{-1}$ with carrier densities of $5-41\times10^{11}$ cm^{-2} have become routinely achievable in 7.5–25 nm thick Ge QWs.[1–3]

Until now, very high mobility holes were only obtained in strained Ge QWs grown on relatively thick (1–8 μm), high Ge content, $Si_{1-x}Ge_x$ buffers.[2,3] However, the low thermal conductivity of undoped SiGe is a drawback for nanoscale metal oxide semiconductor field effect transistor (MOSFET) and modulation doped semiconductor field effect transistor (MODFET) device applications. At room temperature, the thermal conductivity of undoped $Si_{0.3}Ge_{0.7}$ is over 12 times lower than that of Si.[4] This could lead to overheating of the material and result in degradation of nanoscale device performance, as demonstrated in an *n*-channel strained Si MODFET on a $Si_{0.56}Ge_{0.44}$ buffer.[5] Therefore, a significant reduction in the SiGe buffer layer thickness is indeed required. Furthermore, thin SiGe buffers will have advantages for integration with other devices on a single chip. Moreover, none of the recently developed methods for fabricating thin SiGe/Si(001) virtual substrate (VS) has been able to demonstrate high mobility holes in a strained Ge QW.[6]

In this letter, we report the successful epitaxial growth of a compressively strained Ge QW on a recently developed ultrathin high Ge content relaxed SiGe/LT-SiGe/Si(001) VS.[7] This material system demonstrates excellent electronic and structural properties and has a high potential for future device applications.

The *p*-type Ge QW/$Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) MOD heterostructures were grown on Si(001) substrates by solid source molecular beam epitaxy (SS-MBE) in a commercial ultrahigh vacuum system. The samples were grown in a single process to the schematic design shown in Fig. 1 and consist of a 45 nm thick relaxed VS necessary to induce compressive strain in the Ge QW, on an underlying Si substrate. Prior to the growth *ex situ* substrate cleaning was performed in H_2SO_4:H_2O_2 and diluted buffered HF solutions followed by *in situ* thermal cleaning at 750 °C. The VS substrates were grown by a variable temperature approach: an initial very thin (5 nm) $Si_{0.4}Ge_{0.6}$ seeding layer was grown at a very low substrate temperature, followed by a 40 nm thick layer of the same Ge content grown at temperatures ramping up to 550 °C. After this the 300 nm thick $Si_{0.4}Ge_{0.6}$ buffer layer was grown, for an accurate evaluation of threading dislocations density (TDD).

The active region of the heterostructure was grown onto a 345 nm thick VS and consists of an 8 nm undoped compressively strained Ge QW layer to contain the 2DHG, a 10 nm $Si_{0.4}Ge_{0.6}$ undoped spacer layer, a 10 nm $Si_{0.4}Ge_{0.6}$

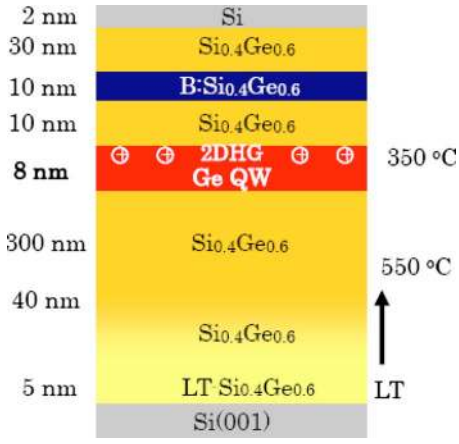

FIG. 1. (Color online) Schematic design of *p*-Ge QW/$Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) MOD heterostructure grown by SS-MBE.

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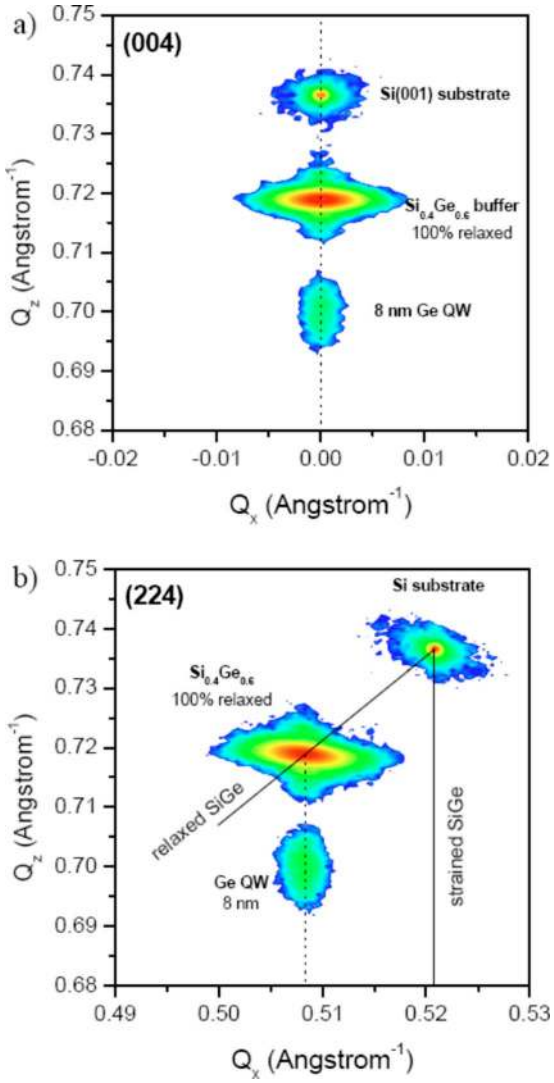

FIG. 2. (Color online) HR-XRD (a) symmetric (004) and (b) asymmetric (224) RSMs showing peaks from the QW, VS, and Si(001) substrate.

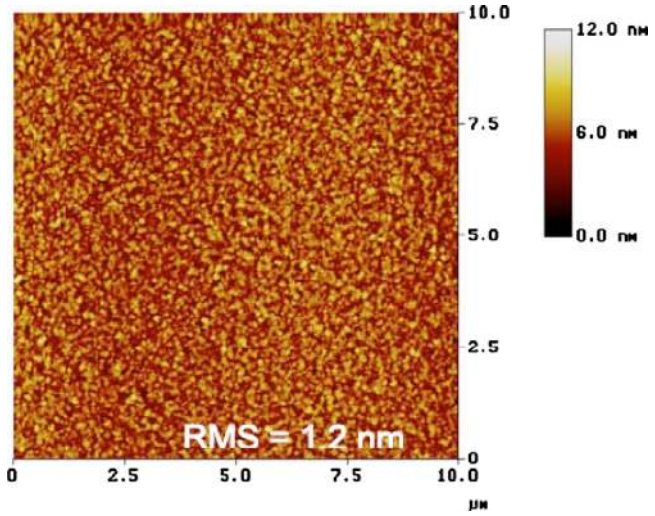

FIG. 3. (Color online) A typical 10×10 μm AFM image of the heterostructure surface with a rms surface roughness of 1.2 nm.

B-doped supply layer, a 30 nm $Si_{0.4}Ge_{0.6}$ undoped cap layer, and finally a 2 nm Si cap layer on the surface. The Ge QW layer is grown at 350 °C to retain the strain and to minimize Ge diffusion. The design of the MOD region was chosen to be similar to that of structures grown on thick buffers that previously demonstrated very high 2DHG mobility at both low and room temperatures,[2] in order to compare the quality of the thin $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) VS and its effect on the transport properties of the 2DHG in the Ge QW.

The Ge content and degree of relaxation of the grown epilayers were obtained by high resolution x-ray diffraction (HR-XRD) carried out at room temperature using a Philips XPert MRD system. In order to determine the lattice parameters of the SiGe and Ge layers, symmetric (004) and asymmetric (224) reciprocal space mapping (RSM) measurements were performed (Fig. 2). The (004) RSM consists of three peaks corresponding to the Si(001) substrate, $Si_{0.4}Ge_{0.6}$ buffer layers, and Ge QW layer. The Si diffraction peak is narrow and symmetrical, which indicates a defect-free crystal, but the peak associated with relaxed $Si_{0.4}Ge_{0.6}$ layer is broadened along Q_x axis, which is a sign of some imperfection of a crystal quality, such as mosaicity, due to the presence of defects. We assume this broadening is associated with the expected dislocations in the $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$ layers of the VS. Analysis of the (004) RSM did not reveal any tilt of the SiGe epilayers relative to the Si(001) substrate, which is a common feature of thick graded SiGe buffers. Thus, corrections to the (224) RSM were unnecessary and the data can be analyzed as they are. The (224) RSM in Fig. 2(b) also consists of three peaks originating from the same layers. The solid lines labeled "fully strained" and "fully relaxed" show the theoretical peak positions for a fully strained $Si_{1-x}Ge_x$ layer grown on Si(001) substrate and a fully relaxed one, respectively, for the full range x of Ge compositions. It is clearly seen that the $Si_{0.4}Ge_{0.6}$ layer is *fully relaxed* and analysis of the HR-XRD data confirms $x=0.60$ in this layer. The 8 nm Ge QW layer was similarly shown to be under *full compressive strain*. Measurements across the wafer showed no variation in Ge composition and relaxation within the experimental error.

The surface morphology of the samples was examined by atomic force microscopy (AFM) at room temperature with a Digital Instruments Multimode SPM Nanoscope IIIa in tapping mode. A typical 10×10 μm AFM image is shown in Fig. 3. Analysis of the AFM images obtained from various places on the wafer indicates a relatively low rms surface roughness of 1.2 nm. It is interesting to point out that the typical cross-hatch surface pattern, associated with thick graded SiGe buffers grown on Si, is *not* visible in these samples. The crosshatch is associated with variation in strain across the surface, due to strain fields arising from the inhomogeneous distribution of misfit dislocations, and its absence is a good characteristic feature of these thin VSs grown by the variable temperature technique.

Wet chemical etching, using diluted Schimmel and iodine etchants,[8] was used to reveal etch pits, which are typically associated with the surface termination of threading dislocations. The etch pit density, and hence TDD, was counted with the help of optical microscopy. An average TDD of 3.4×10^5 cm^{-2} was found, which is extremely low for thin, fully relaxed, high Ge content VSs on Si(001).

The 2DHG Hall mobility and sheet carrier density in the MOD heterostructure were obtained by a combination of resistivity and Hall effect measurements in the dark on a mesa-etched Hall-bar in the temperature range 3–300 K. At

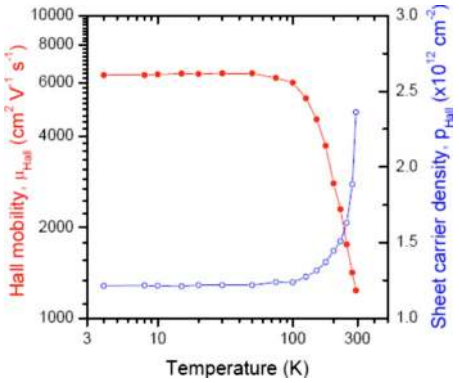

FIG. 4. (Color online) Temperature dependence of the Hall mobility and sheet carrier density of the *p*-Ge QW/$Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) MOD heterostructure.

3 K the 2DHG Hall mobility and carrier density are 6360 $cm^2 V^{-1} s^{-1}$ and 1.21×10^{12} cm^{-2}, respectively. Figure 4 shows that the Hall mobility and carrier density saturate below 50 K, which clearly indicates the presence of a 2DHG in the strained Ge QW and the absence of parallel conductions in the B-doped and $Si_{0.4}Ge_{0.6}$ layers. On increasing the temperature to 293 K the sheet carrier density increases due to the activation of parallel conduction in these layers. By contrast, the Hall mobility decreases with increasing temperature due both to an increase in acoustic and optical-phonon scattering and the lower mobility of these additional carriers in the parallel conduction channels. At 293 K the Hall mobility and carrier density are measured as 1235 $cm^2 V^{-1} s^{-1}$ and 2.36×10^{12} cm^{-2}, respectively.

It is well established that the main sources of carrier scattering in SiGe heterostructures, responsible for the degradation of the mobility at low temperatures, are a high density of defects and high interface/surface roughness. Hence, we might have expected the low TDD and very low rms surface roughness measured in these samples to result in a higher low-temperature hole mobility than we measure, given that a 2DHG mobility of 15 770 $cm^2 V^{-1} s^{-1}$ was obtained in a similar 7.5 nm Ge QW sample grown on much thicker (1100 nm) SiGe/Si(001) VS that had a much higher TDD of $\sim 3 \times 10^7$ cm^{-2} and a much larger rms surface roughness of ~ 7 nm.[2,9] We can speculate that the reason for the lower than expected low-temperature 2DHG mobility could be the proximity of the Ge QW to the $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$ region of the VS, which could contain some amount of misfit dislocations and point defects that could be sources of remote scattering for the holes in the Ge QW. Some degradation of the mobility may also occur because the carriers are confined against the rougher top interface of the Ge QW, since the present structures are MOD only from above the QW rather than from bottom side.[2]

By contrast, at room temperature the mobility is mainly limited by phonon scattering and will not be significantly affected by the low TDD and high quality interfaces.[9,10] Indeed, the measured room-temperature Hall mobility exceeds the value of 1110 $cm^2 V^{-1} s^{-1}$ reported for the similar 7.5 nm Ge QW structure grown on the thicker VS mentioned previously.[2] However, conventional resistivity and Hall effect measurements only yield the averaged density and mobility of carriers that exist not only in the QW but also in the other parallel conducting layers, e.g., the doped supply layer, the buffer layer, the substrate, and their interfaces. The transport properties of the various carriers can be separated using the technique of mobility spectrum analysis.[11] Using this technique, a very high room-temperature drift mobility of 2540 $cm^2 V^{-1} s^{-1}$ was obtained for the 7.5 nm Ge QW structure of Ref. 2 and this will be used to extract the room-temperature transport properties of just the 2DHG in the 8 nm Ge QW of these samples in the future.

In conclusion, the results obtained demonstrate the suitability of the proposed 345 nm thin $Si_{0.4}Ge_{0.6}$/LT-$Si_{0.4}Ge_{0.6}$/Si(001) VS for use in high mobility strained Ge QW heterostructures. A very low TDD of 3.4×10^5 cm^{-2} and a very low rms surface roughness of 1.2 nm were measured for *p*-type Ge MOD heterostructures grown on these buffers. HR-XRD shows that the VS is fully relaxed and the 8 nm Ge QW layer is fully strained. Furthermore, the temperature dependence of the Hall mobility and carrier density clearly indicates the existence of a high mobility 2DHG in the Ge QW. At room temperature, which is more relevant for MOSFET and MODFET devices applications, the samples show a very high Hall mobility of 1235 $cm^2 V^{-1} s^{-1}$ at a carrier density of 2.36×10^{12} cm^{-2}. These results exhibit a huge potential for further applications of such a material system for *p*-MOSFET and *p*-MODFET devices on Si(001) or SOI(001) substrates.

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