High-mobility modulation-doped graded SiGe-channel p-MOSFET's

High-Mobility Modulation-Doped Graded SiGe-Channel p-MOSFET's

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Abstract—**We report the successful fabrication and operation of the first modulation-doped SiGe-channel p-MOSFET's. A novel device design consisting of a graded SiGe channel, an n^+ polysilicon gate, and p^+ modulation doping is used. The boron-doped layer is placed underneath the undoped SiGe channel to achieve the desired threshold voltage without degrading the mobility. The low-field hole mobility for a channel graded from 25% to 15% germanium is 220 $cm^2/V \cdot s$ at 300 K and increases to 980 $cm^2/V \cdot s$ at 82 K.**

I. Introduction

IMPROVEMENTS in the speed performance of p-channel MOSFET's have been accomplished by scaling the channel length and gate oxide thickness, and by building surface-channel devices. Despite these efforts, the transconductance of the p-MOSFET remains inferior to that of the n-MOSFET, primarily because the field-effect hole mobility is over a factor of 3 lower than the field-effect electron mobility. MOS structures with undoped SiGe channels are receiving increased attention [1]–[3] as the holes traveling in the SiGe channel are expected to have enhanced mobilities due to the presence of the germanium. Furthermore, when the holes are confined in the SiGe channel, negligible surface scattering should occur since the SiGe is separated from the gate oxide by a thin silicon cap layer. Pure Ge with its high mobility can also be used as channel material [4]. Technologically, however, it is impossible to build pseudomorphic Ge channels directly on a Si substrate.

The threshold voltage of the SiGe-channel p-MOSFET can be adjusted in several ways. When n^+ polysilicon is used as gate material, the threshold voltage of a SiGe MOSFET with an undoped channel region is too high and shallow p-type doping is needed. With a p^+ polysilicon gate, enhancement-mode devices require n-type doping in the channel region. The SiGe p-MOSFET's discussed in this letter utilize an n^+ polysilicon gate design to suppress the turn-on of the parasitic channel in the Si cap layer [5]. Modulation doping, instead of uniform channel doping, was chosen to set the threshold voltage in order to maximize hole mobility and prevent carrier freeze-out at liquid-nitrogen temperature.

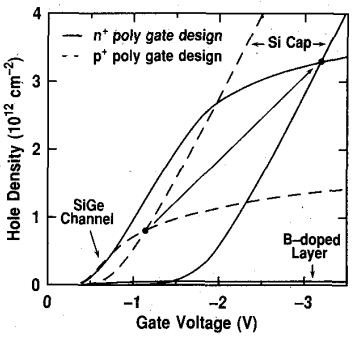

Fig. 1. Hole density versus gate voltage comparing an n^+ polysilicon gate design to a p^+ polysilicon gate design with identical threshold voltages (T = 300 K, t_{ox} = 7 nm, 30–15% graded Ge profile). The boron-doped layer in the MODMOS is separated from the channel by a 5-nm Si buffer.

II. Device Design and Fabrication

The type of gate material and channel doping used for the SiGe p-MOSFET has a strong effect on the parasitic conduction in the Si channels located at the SiO_2/Si interface and in the boron-doped layer. This is illustrated by the one-dimensional Poisson simulation results shown in Fig. 1 which compare a p^+-gate SiGe p-MOSFET with uniform channel doping to an n^+-gate modulation-doped SiGe p-MOSFET, or p-MODMOS. The hole densities in the SiGe channel and parasitic Si channels (Si cap and boron-doped layer) are shown as a function of gate voltage for devices with a 5-nm Si cap layer and a 15-nm-wide SiGe channel. The uniform n-type channel doping ($3 \times 10^{17}/cm^3$) of the p^+-gate SiGe p-MOSFET was chosen such that this device has the same threshold voltage as the p-MODMOS (integrated B dose of $1.5 \times 10^{12}/cm^2$).

For the p^+ polysilicon gate design, parallel conduction at the SiO_2/Si interface is significant shortly after threshold. The holes flowing in this surface channel screen the SiGe channel and hence limit the maximum concentration of high-mobility holes. The parasitic surface-channel charge exceeds the SiGe-channel charge for $|V_g| > 1.2$ V. Conversely, in the n^+-gate modulation-doped SiGe MOSFET, the extra holes

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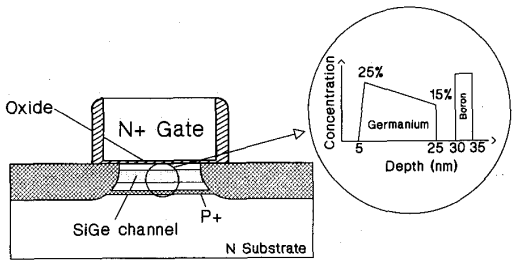

Fig. 2. Schematic cross section of the p-MODMOS.

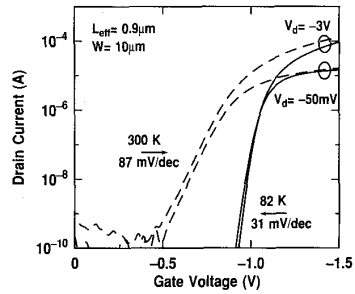

Fig. 3. Subthreshold characteristics of a 0.9-μm × 10-μm p-MODMOS at 300 and 82 K.

supplied by the p-type dopants increase the maximum number of holes in the SiGe channel. The parasitic Si charge at low gate voltage is caused by holes flowing in the boron-doped layer. The concentration of holes in this layer is, however, negligible compared to those in the SiGe channel as seen in Fig. 1. Furthermore, the parasitic charge in the Si cap becomes larger than the SiGe-channel charge only for $|V_g| > 3.1$ V. The n^+-gate SiGe MOSFET can hence be designed for operation at higher power supply voltages than the p^+-gate device.

The threshold voltage of the n^+-gate SiGe p-MOSFET is adjusted with modulation doping, thereby preventing mobility degradation due to ionized impurity scattering. The boron-doped layer can either be located *above* or *below* the SiGe channel. Locating the dopants above the channel leads to turn-on of the parasitic surface channel at low gate voltage. In addition, the transconductance is expected to be lower than for the undoped cap case since the minimum cap thickness is larger and more ionized impurity scattering will occur. This design is also expected to have a very process-sensitive threshold voltage as any thinning of the Si cap during fabrication will reduce the integrated boron dose. These disadvantages are avoided by placing the boron-doped layer below the SiGe channel with a thin undoped Si buffer in between (Fig. 2).

The fabrication of the p-MODMOS starts by the growth of a 5-nm boron-doped film, a 5-nm Si buffer, and the SiGe channel at 500°C using UHV/CVD [6] on a $5 \times 10^{16}/\text{cm}^3$ ⟨100⟩ n-type Si substrate. The total integrated Ge dose is the relevant figure of merit to ensure that the pseudomorphic SiGe films remain stable throughout device fabrication. To optimize the transconductance for a given integrated Ge dose, the Ge profile is graded with the highest concentration closest to the gate. This maximizes the gate-to-channel capacitance leading to a steep turn-on of the device. Grading the Ge profile also increases the number of high-mobility holes confined in the SiGe channel at high gate voltages. At the bottom of the channel, a valence-band discontinuity is required to ensure negligible conduction in the underlaying boron-doped layer. SIMS, RBS, and TEM indicate that the Ge was graded over 15 nm from 25% near the gate to 15% at the bottom of the channel. In addition, the Ge is ramped from 0% to 25% over 5 nm at the front of the channel to improve the quality of the Si/SiGe interface. The SiGe channel is separated from the 7-nm high-quality PECVD gate oxide by a 5-nm Si cap layer. *In-situ* arsenic-doped amorphous Si, activated with a 800°C 10-s RTA, is used as gate material. The source and drain are formed by antimony preamorphization and boron implantation, which is activated with a 30-min anneal at 600°C.

III. Experimental Results

The room-temperature threshold voltage of the p-MODMOS varies from −0.1 to −1.1 V corresponding to integrated boron doses in the range of $2.3 \times 10^{12}/\text{cm}^2$ to $1.4 \times 10^{12}/\text{cm}^2$. Fig. 3 shows typical subthreshold characteristics of a 0.9-μm p-MODMOS. The subthreshold slope is 87 mV/decade at 300 K and increases to 31 mV/decade at 82 K. Two significant advantages of the subsurface SiGe-channel p-MODMOS over an implanted buried-channel Si p-MOSFET are observed. First, the p-MODMOS exhibits higher punchthrough resistance since the boron-doped layer is very narrow and located very close to the gate (30 nm below the SiO_2/Si interface). Second, no abnormal subthreshold behavior of "kink" is observed at 82 K since the conducting holes are physically separated from the impurity atoms and hence no threshold voltage change will occur. The absence of freeze-out in the MODMOS was confirmed by subthreshold measurements at varying substrate bias.

Since the location of the inversion-layer charge, and hence the effective gate capacitance, is a function of gate voltage, the hole mobility cannot be extracted from the low-field transconductance alone. The split CV measurement technique was used to determine the inversion-layer charge versus gate voltage [7]. The total channel charge as a function of voltage is obtained from gate-to-source–drain CV measurements on large (100 μm × 100 μm) p-MODMOS devices. The hole mobility is then calculated from the ratio of the channel charge and the drain current ($V_d = -25$ mV), and it is shown in Fig. 4 as a function of gate voltage. At low gate voltage, the holes flow at the bottom of the SiGe channel and their mobility is degraded by impurity scattering with acceptor ions which diffused into the bottom of the SiGe channel during device fabrication. As the gate voltage increases, the holes move to the top of the SiGe channel, which is undoped, and their mobility is high and almost constant. At high gate voltage, a large fraction of the holes travels in the Si cap with a mobility degraded by scattering at the oxide/silicon interface. The peak hole mobility is 220 $\text{cm}^2/\text{V} \cdot \text{s}$ at 300 K and increases to 980 $\text{cm}^2/\text{V} \cdot \text{s}$ at 82 K. At low temperature, this is a factor of 2 higher than previously reported for submi-

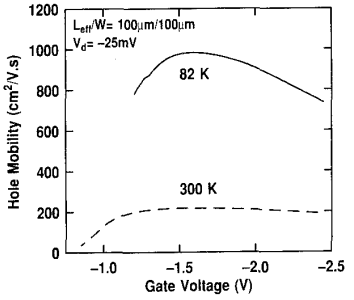

Fig. 4. Field-effect hole mobility as a function of gate voltage at 300 and 82 K, indicating a peak hole mobility of 220 and 980 $cm^2/V \cdot s$, respectively.

crometer Si p-MOSFET's [8]. Furthermore, these values are in good agreement with those obtained by Hall measurements on similar SiGe heterostructures grown by UHV/CVD [9].

IV. Conclusions

A novel subsurface SiGe-channel p-MOSFET was demonstrated in which modulation doping was used to control the threshold voltage without degrading the channel mobility. The boron-doped layer was located underneath the graded and undoped SiGe channel to minimize process sensitivity and maximize transconductance. Low-field hole mobilities of 220 $cm^2/V \cdot s$ at 300 K and 980 $cm^2/V \cdot s$ at 82 K were achieved in functional submicrometer p-MOSFET's. These results demonstrate the feasibility of modulation-doped SiGe-channel p-MOSFET's and their leverage over conventional Si p-MOSFET's.

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