High-Mobility Nanotube Transistor Memory

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Received April 9, 2002; Revised Manuscript Received May 16, 2002

ABSTRACT

A high-mobility (9000 cm^2/V·s) semiconducting single-walled nanotube transistor is used to construct a nonvolatile charge-storage memory element operating at room temperature. Charges are stored by application of a few volts across the silicon dioxide dielectric between nanotube and silicon substrate, and detected by threshold shift of the nanotube field-effect transistor. The high mobility of the nanotube transistor allows the observation of discrete configurations of charge corresponding to rearrangement of a single or few electrons. These states may be reversibly written, read, and erased at temperatures up to 100 K.

Decreasing the power required to write and erase memory devices requires either a reduction of the write voltage or a reduction in the number of electrons representing one bit. The former is fundamentally limited by the thermal energy at room temperature, and efforts have focused on the latter. The ultimate reduction, i.e., the storage of a single electronic charge, offers advantages over storing quasi-continuous quantities of charge:[1] the Coulomb energy associated with adding additional charges to the storage node can be used to guarantee a discrete charge state,[2] and the quantized nature of the charge stored makes the device characteristics less sensitive to the details of the device structure. However, the operation of a single-electron memory at useful temperatures presents two major challenges: the capacitance of the storage node must be small enough that its Coulomb charging energy is significantly larger than the thermal energy at the operating temperature, and the readout device must be sufficiently sensitive to detect a single nearby electronic charge. Efforts to date have focused on floating-gate charge storage nodes either patterned lithographically[3−5] or formed serendipitously in a polycrystalline channel.[1] Detection of single charges at elevated temperatures has been demonstrated with single-electron transistors[5] or very narrow silicon- or polysilicon-on-insulator field-effect transistors (FETs).[1,3,4] However, single-electron transistors that can operate at room temperature remain extremely difficult to fabricate, and the field-effect transistors demonstrated so far have modest mobilities.

Here we report on a charge-storage memory using a single semiconducting nanotube FET as the readout. Charge is reversibly injected and removed from the dielectric by applying a moderate voltage (<10 V) across the dielectric between nanotube and substrate. The nanotube FET is ideal as a charge detecting device; it has extremely high mobility (e.g. 9000 cm^2/V·s for the device described here), large geometrical capacitance, and its one-dimensional nature guarantees that local changes in charge density affect the global conductance. In the device reported here, discrete charge states corresponding to differences of a single or at most a few stored electrons are observed and can be written, read, and erased at temperatures up to 100 K, with changes in current of more than 50 nA. This rather crude device demonstrates the significant advantages of nanotube transistors for single-electron or few-electron memories; significant improvement is expected for shorter gate length devices and optimization of the charge storage node.

The carbon nanotube in this study was synthesized via chemical vapor deposition over iron nanoparticles at 900 °C, with methane as the feedstock gas,[6] on a conducting silicon substrate capped by 500 nm of thermally grown SiO$_2$. Source and drain electrical contacts to the nanotube are made via evaporated Cr/Au electrodes; the conducting substrate acts as a gate electrode. Room temperature and low temperature electrical measurements were carried out with the samples mounted on a cryostat in flowing helium gas. While all data presented here correspond to this device, qualitatively similar behavior was obtained with other semiconducting nanotube devices fabricated in a similar fashion.

We begin by discussing the room-temperature characteristics and charge-storage memory operation of our device. Figure 1A shows an atomic force microscope topograph of the device; the nanotube has a length $L = 4.8$ μm and a diameter $d = 2.7$ nm as determined from the height profile of this image. Figure 1B shows the drain current I as a function of gate voltage V_g with $V_{sd} = 500$ mV applied to the source electrode. The semiconducting nanotube acts as
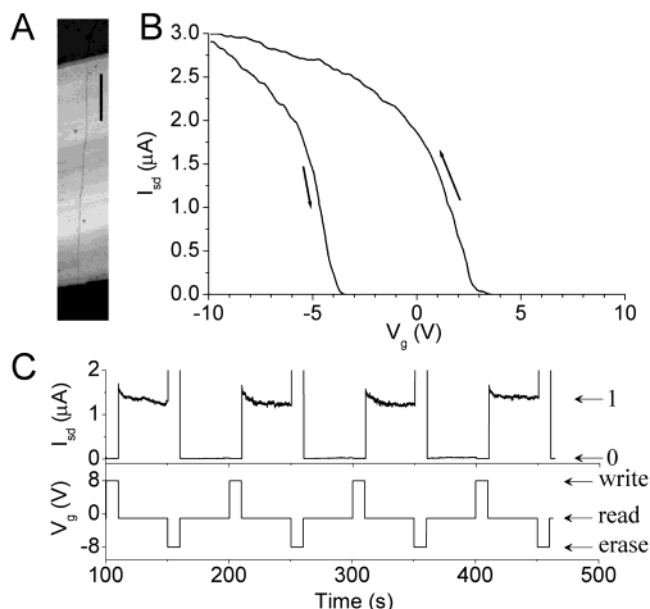
Figure 1. (A) Atomic force microscope (intermittent-contact mode) topograph of the nanotube device used in this study. The nanotube is the thin, nearly vertical gray line between the two electrodes (dark blocks at top and bottom). Scale bar: 1 micron. (B) Drain current as a function of gate voltage at room temperature and a source-drain bias of 500 mV. As the gate voltage is swept from positive to negative and back a pronounced hysteresis is observed, as indicated by the arrows denoting the sweep direction. (C) Four read/write cycles of the nanotube memory at room temperature. The upper panel shows the drain current at a source-drain bias of 500 mV, while the lower panel shows the gate voltage. The time axis is the same for both graphs. The memory state was read at -1 V, and written with pulses of ± 8 V.

a p-type FET, conducting at negative gate voltage and becoming insulating at positive gate voltage, as previously reported.[7,8] As the gate voltage is swept back and forth between $+10$ V and -10 V, a large hysteresis is evident in the $I-V_g$ curves; the threshold gate voltage V_{th} at which the nanotube begins to conduct is shifted by more than 6 V.

Figure 1C demonstrates that this hysteresis may be used as the basis of a stable memory at room temperature. Here the state of the device is read at $V_{sd} = 500$ mV, $V_g = -1$ V, and written and erased with pulses of the gate voltage to ± 8 V. A current of $> 1 \mu$A may be switched. After an initial slow decay (~ 50 s) the current remains constant; the hold time of the memory exceeds 5000 seconds.

We first determine the mobility of our nanotube FET in order to be able to relate changes in conductivity to changes in charge density. The Drude conductivity relation $\sigma = ne\mu$, where σ is the conductivity, n the linear carrier density, e the electronic charge, and μ the mobility, predicts that the conductivity of the nanotube will grow linearly with carrier density (and hence gate voltage) if the mobility is constant: $\sigma = C_g(V_{th} - V_g)\mu/L$, where C_g is the gate capacitance and L the channel length. From the linear portion of the $G(V_g)$ curve, a mobility of the tube μ may be inferred; $\mu = (L^2/C_g)dG/dV_g$. The gate capacitance may be determined directly from low-temperature Coulomb blockade measurements; $C_g = 54$ aF, or ~ 350 e/V for this device. From the slope[9] $dG/dV_g = \sim 2.2$ μS/V determined from the linear portion of the

$I-V_g$ curves in Figure 1B we calculate a hole mobility of ~ 9000 cm^2/V·s, greatly exceeding pure silicon (~ 450 cm^2/V·s). This mobility value also greatly exceeds the earlier values reported for laser-ablation-synthesized semiconducting nanotubes[8,10] but agrees with other recent results on CVD-synthesized semiconducting nanotubes.[11-13]

We now discuss the mechanism of charge storage in the nanotube memory device. The threshold shift indicates that a reconfiguration of charge near the nanotube occurs under the application of a gate voltage. This reconfiguration of charge could occur either via the movement of local charges already present in the system, e.g., electrons or ions in the dielectric, or by injection or removal of electrons from the dielectric through the electrodes or nanotube. The "sign" of the hysteresis loop, i.e., *positive* gate voltage *increases* the threshold voltage, indicates that charges are being injected into the dielectric from the nanotube, similar to a floating gate memory (the opposite sign hysteresis is observed for mobile ions or electrons, for example the "proton memory,"[14] which uses mobile hydrogen ions in SiO$_2$).

We propose the following mechanism to explain the memory effect in our nanotube devices. Due to the geometry of the device, the electric field is much higher at the nanotube than at the Si/SiO$_2$ interface; for this reason we concentrate on the nanotube as the source of charge injection. The nanotube diameter is small compared to the dielectric thickness, and the geometry may be approximated by a cylindrical capacitor with the nanotube as the center electrode. Because of the small size of the nanotube, the electric field at the nanotube surface is very high: $E = V_g/KR_t ln(R_g/R_t) \approx V_g/23R_t$ where $R_t = 1.35$ nm is the nanotube radius, $R_g = 500$ nm is the dielectric thickness, and $K = 3.9$ is the dielectric constant of SiO$_2$. Thus the electric field at the nanotube/SiO$_2$ interface for $V_g = 10$ V is greater than 0.3 V/nm, comparable to the breakdown field for SiO$_2$ (~ 0.25 V/nm), so it is reasonable to expect movement of charge in the dielectric. (Note that "breakdown field" is typically expressed as the potential difference across the dielectric divided by the dielectric thickness, i.e., does not include K, so the typically quoted value of ~ 1.0 V/nm for SiO$_2$ translates to an internal electric field of ~ 0.25 V/nm). We propose that at these high fields, electrons are easily injected into the dielectric from the nanotube and remain trapped in metastable states until the polarity is reversed. It is notable that a nonvolatile memory based on charge storage in a thick SiO$_2$ gate dielectric was recently reported in organic thin-film transistors; in this parallel-plate geometry $V_g = 100$ V ($E \approx 0.03$ V/nm) was sufficient to polarize the SiO$_2$ dielectric.[15] The same sign hysteresis was observed as in our case, indicating injection of charge into the dielectric.

Other possible mechanisms for charge rearrangement were considered. At such high electric fields the gas around the nanotube may experience corona discharge, and ionized gas could transport charge to the dielectric surface. However, this mechanism would be expected to exhibit a large dependence on the pressure and species of the gas around the nanotube; we found similar operation of the nanotube memory in humid air, dry helium, and dynamic vacuum
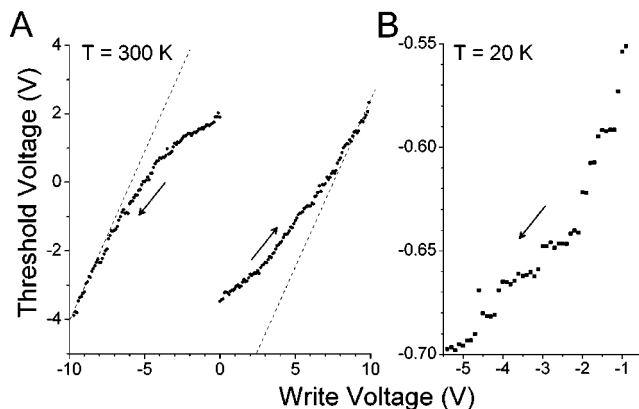
Figure 2. (A) Evolution of the threshold voltage (defined in text) after application of write voltage pulses of successively higher magnitudes at room temperature. The dielectric was first polarized at −10 V, and the threshold voltage was measured after successive application of one-second write pulses, increasing the pulse by 0.1 V each time (lower right curve). The dielectric was then polarized at +10 V, and the threshold voltage was again measured after application of one-second write pulses, now decreasing the pulse by 0.1 V each time (upper left curve). The dashed lines indicate a slope of unity. (B) Threshold voltage at 20 K after polarizing at +8 V and applying write voltage pulses successively decreased by 0.1 V. Several discrete plateaus in the threshold voltage are evident.

(10^{-3} Torr). It is also possible that the high electric field causes a rearrangement of adsorbates on the nanotube which act as dopants,[16] e.g., oxygen; however, it is difficult to explain the observed shift of the threshold voltage from positive to negative simply through rearrangement of electron acceptors.

Figure 2A illustrates the shift in threshold voltage with the magnitude of the applied pulse in gate voltage at room temperature. Threshold voltage is defined here as the gate voltage at which the conductance was 0.6 μS (approximately one-tenth the maximum conductance). This underestimates the onset of conductance; however, for this purpose we are interested in relative shifts of the threshold voltage, not the absolute magnitude. The lower curve represents a starting condition with the dielectric polarized at −10 V. The threshold voltage was measured after successive write voltage pulses of 1 s; after the write pulse the gate voltage was reduced until the conductance was 0.6 μS, defining V_{th}. V_{th} shifts toward higher values continuously, with no obvious sharp onset of polarization. A similar curve is obtained by starting with the dielectric polarized at +10 V and applying successive negative write voltage pulses (upper curve), followed by increasing the gate voltage until the conductance was 0.6 μS to obtain V_{th}. The smooth behavior of the threshold voltage shift indicates a continuous distribution of energies for the charge trap sites. Interestingly, the slope of the threshold voltage vs write voltage curve approaches unity (dashed lines) at high write voltages. This implies that only a finite range of charge density in the nanotube is accessible through electrostatic doping; at high gate bias the screening of the gate due to injected charge is nearly perfect. This fact should have significant consequences for the understanding of carbon nanotube transistors.

Figure 2B shows a similar measurement of the threshold voltage shift as a function of write voltage pulses, but now at a temperature of 20 K. At lower temperature the threshold voltage shift is smaller, and noticeable discrete steps are evident in the V_{th} curve. The gate capacitance of the device is approximately 54 aF, or 350 e/V. If we assume that the capacitance of the charges trapped in the dielectric is dominated by capacitance to the nanotube, then the V_{th} shift of ∼0.15 V in Figure 2B then corresponds to a charge of ∼50 e added to the nanotube. This number is somewhat larger but of the same order of magnitude as the approximately 10−15 discrete current levels observed in Figure 2B; the difference in conductance between plateaus arises from a change in the oxide charge of one, or at most a few, electrons.

Figure 3A shows the $I-V_g$ characteristics of the device at 20 K. Here V_g is swept back and forth over a particular region (between −1.3 V and −3 V); eight cycles are shown. Two branches of the $I-V_g$ curve are clearly visible, with switching between the branches occurring in specific ranges of V_g. Switching between the two curves occurs in discrete jumps, and no intermediate curves are seen. The gate voltage at which the switch occurs varies from sweep to sweep, indicating a stochastic process. This range of gate voltage was chosen in order to highlight this large hysteresis loop; other hysteresis loops could be observed with much smaller widths by scanning different ranges of gate voltage. This behavior is typical of our nanotube devices, most often only one or two large hysteresis loops may be observed, with switching occurring near the threshold gate voltage.

Figure 3B demonstrates memory operation of the device at 20 K. The drain current is measured at a gate voltage of −2.25 V and a source-drain bias of 500 mV. The drain current is switched between high and low states by application of a gate voltage pulse of ±0.75 V (relative to the −2.25 V baseline). The difference in current between high and low states is approximately 60 nA. The memory is stable for at least 100 seconds.

At higher temperatures ($T = 100$ K) and at high bias ($V_{sd} = 500$ mV), a hysteresis loop with two branches was still seen, but reversible switching between the two branches was observed at all gate voltages, appearing as random telegraph noise in the current at fixed gate voltage with a characteristic switching time of order 1 s at $V_g = -1.8$ V. This random telegraph noise was greatly reduced when V_{sd} was lowered to 50 mV, with one switching event occurring every few hundred seconds. However, applying a pulse to V_g alone with $V_{sd} = 50$ mV was found to be insufficient to ensure a write/ erase switch event. An additional pulse of V_{sd} to 500 mV applied only during the write/erase gate pulses was found to guarantee switching to the desired state. This resulted in the reliable writing and erasing of the memory at 100 K (Figure 3C), with gate voltage excursions of only ±0.4 V from the readout voltage of −1.8 V.

The discrete jumps in threshold voltage in Figure 2B and the discrete $I-V_g$ curves in Figure 3A strongly suggest that single-electron changes in the dielectric charge are responsible for the observed changes in the device characteristics;
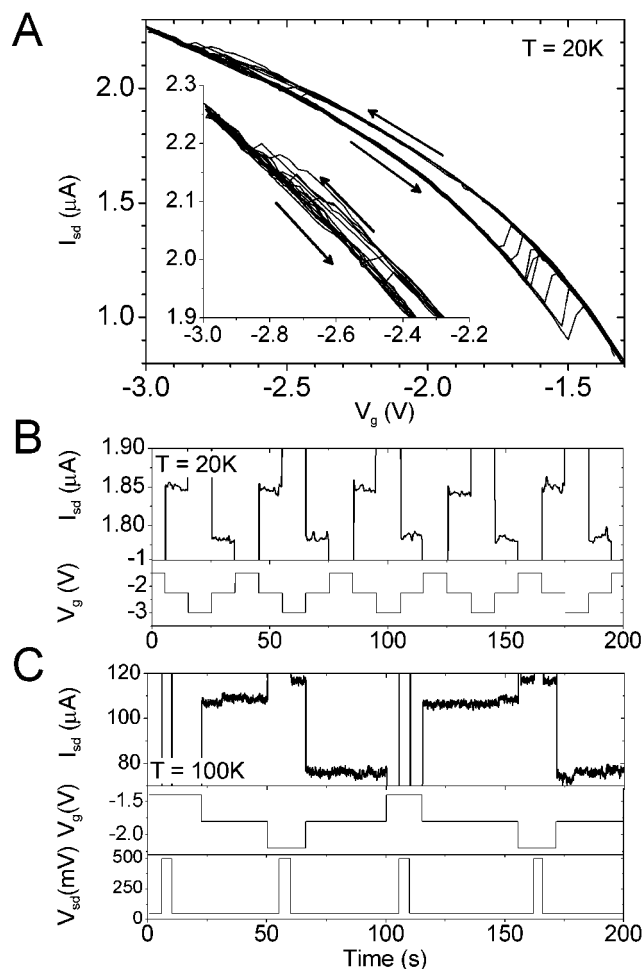
Figure 3. Operation of the memory with discrete charge states. (A) The drain current as a function of gate voltage at a source-drain bias of 500 mV and a temperature of 20 K. The gate voltage is swept between −1.3 and −3 V (toward positive eight times, and back negative seven times). Two discrete branches of the curve are evident, with discrete switching events between the branches occurring at different gate voltages for increasing/decreasing sweeps. The inset shows more clearly the right side of the main figure. (B) Five read/write cycles of the memory at 20 K. The horizontal (time) axis applies to both curves. The memory state was read at a gate voltage of −2.25 V, and written (erased) with pulses of −1.5 V (−3.0 V) to the gate. (C) Two read/write cycles of the memory at 100 K. Here the memory was read at a source-drain bias of 50 mV and gate voltage of −1.8 V, and written (erased) with pulses of −1.4 V (−2.2 V) to the gate and 500 mV to the source.

i.e., that the difference in conductance states in the memory (Figures 3B and 3C) is due to the movement of a single electronic charge. However, the discrete changes in conductance observed in Figure 2B and Figure 3A are somewhat larger than expected from a simple estimation of the threshold shift due to the addition of one electron to the entire nanotube. In Figure 2B, the plateaus are spaced 3−5 times farther apart than would be expected. In Figure 3A, the spacing in gate voltage between the two curves varies from 0.06 to 0.15 V, approximately 20−50 times larger than would be expected. We argue that this is reasonable and expected given the localized nature of the stored charge. The effects of trapped charge and gate charge are different: trapped charges are localized, while the gate charge affects the

nanotube globally. A localized charge may significantly affect the conductance of a small region (within an electrostatic screening length) of the nanotube, but because this region is necessarily in series with the rest of the nanotube, the global resistance is affected. The screening length of the nanotube may be estimated from scanned-gate microscopy (SGM) measurements;[17] SGM is able to resolve features with spacing of 50 nm in a lightly doped nanotube (zero global gate voltage), suggesting that the screening length is comparable to or less than 50 nm. A single electron would shift the potential of a 50-nm section of the nanotube by 300 mV, greater than the largest shift observed in Figure 3A, 150 mV.

The effect of localized charge may be exaggerated by the device being operated at high bias (near pinchoff), which would lead to greater sensitivity to charges near the source electrode, or due to local potential modulations in the nanotube, which cause greater charge sensitivity at specific locations.[18,19] The fact that the spacing in gate voltage between the two curves in Figure 3A varies significantly, becoming larger nearer the threshold (more positive gate voltage), argues that pinchoff is important; indeed, at the upper end of the gate voltage range the source-drain bias (500 mV) is comparable to the difference between the gate voltage (−1.5 to −3.0 V) and the threshold voltage ($\sim$ −1.1 V), and pinchoff should be significant.

These unoptimized nanotube memory devices already show the promise of using carbon nanotube FETs for single- or few-electron charge-storage memories at useful temperatures. Narrow, high-mobility nanotube FETs should significantly outperform other semiconductor FETs in charge detection. Significant improvement should be obtainable with shorter gate lengths and suitable charge traps, such as a floating metal gate or $SiO_2/Si_3N_4/SiO_2$ trilayer.

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