High-order continuous-time incremental $\Sigma\Delta$ ADC for multi-channel applications

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***Abstract*—A novel high-order single-loop incremental sigma-delta ADC for multi-channel applications is proposed. High-order continuous-time architectures are explored using a 3rd order single-bit modulator as a test-case. The performance of the proposed architecture, taking into account critical non-idealities, is analyzed and its advantages and issues are discussed. Behavioral simulations show a key advantage regarding the integrators' gain-bandwidth requirement of the proposed ADC compared to discrete-time counterparts. This advantage leads to possible low power solutions for multi-channel applications.**

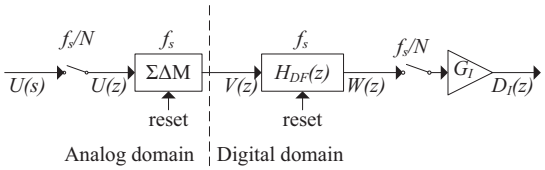

Fig. 1. IΣΔ ADC block diagram

I. Introduction

During the last years, there has been an increasing interest in multi-channel analogue-to-digital converters (ADCs) for low-power biomedical applications, such as portable lab equipments [1] and wearable and implantable systems [2]. The resolution requirements for this type of applications varies depending on the specific target application. While successive-approximation register (SAR) ADCs successfully cover low to medium resolution applications, incremental sigma-delta (IΣΔ) ADCs and extended range (ER) IΣΔ ADCs have been proposed for high resolution ($\geq$ 11-12 bits) applications. High-order single loop [2] [3] and cascaded [4] IΣΔ ADCs have been proposed using discrete-time (DT) implementation in order to limit the number of cycles per conversion, reducing the gain-bandwidth product (GBW) requirement for the integrators. This work explores the CT implementation features by proposing and analyzing a high-order single loop continuous-time (CT) IΣΔ ADC for electroencephalogram (EEG) applications.

II. Proposed IΣΔ ADC

IΣΔ ADCs have minor but critical differences compared to conventional ΣΔ ADCs [5] which makes them suitable for multi-channel applications. The most important one is that they operate continuously in transient mode. After N cycles, when the input sample with the required resolution is acquired, the ADC is reset and ready to accept the next sample. This feature provides an one to one mapping between input and output after every conversion cycle and makes it suitable for multi-channel operation. Moreover, depending on the type of digital filter employed, the ADC quantization error can be available at the output of the last integrator. This feature has been exploited to further reduce the quantization error.

Although both high-order and CT filters have been already used for implementing IΣΔ ADCs, they have not been yet applied simultaneously. To the authors knowledge, no high-order single-loop (SL) CT IΣΔ ADC has been proposed. With the aim of reducing the power dissipation by relaxing the integrators' GBW requirement, this work proposes a 3rd order SL CT IΣΔ ADC. The theoretical operation of high-order SL CT IΣΔ ADCs is presented and the main differences compared to DT implementations are pointed out. Moreover, the performace of the proposed architecture is analyzed and the impact of critical non-idealities, such as excess-loop delay (ELD), jitter, coefficients variation and finite amplifier's GBW, is investigated. Special attention is paid to the finite integrators' GBW as it affects the power consumption of the ADC. The proposed ADC targets an 8-channel digital recording system of clinical EEG with 12 bits resolution at 500 Hz sampling rate per channel to comply with the International Federation of Clinical Neurophysiology (IFCN) standard [6].

A. CT IΣΔ ADC Operation

The proposed IΣΔ ADC, shown in Fig. 1, consists of a channel sample-and-hold, sampled at f_s/N, which is followed by the CT ΣΔ modulator clocked at f_s. In the digital domain, the filter $H_{DF}(z)$ works at f_s, however, it does not produce a valid result until N cycles have passed. After N cycles, the valid result of $W(z)$ is sampled and the ΣΔ modulator as well as the digital filter are reset and ready to accept the next sample. The block diagram includes also the gain G_I relating the analog input $U(z)$ with the digital output $W(z)$ of the ADC. Although not covered in this paper, the selected digital filter for the proposed test case allows quantization error refinement.

Without loss of generality, a normalized sampling rate of 1 ($T_S = 1$) is assumed throughout this work and impulse invariant transformation (IIT) is used in order to perform

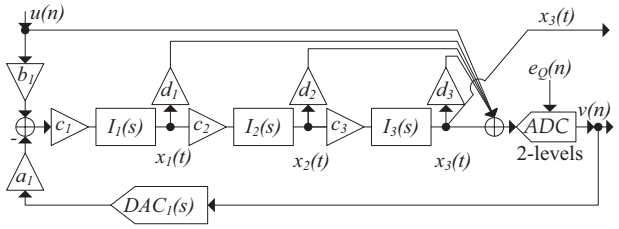

Fig. 2. Block diagram of the modulator used in IΣΔ ADC.

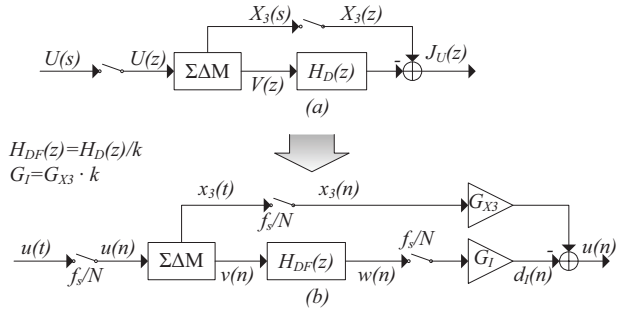

Fig. 3. Block diagram explaining the methodology to obtain $H_{DF}(z)$ and G_I.

continuous to discrete time (CTDT) transformations wherever needed. The CT $\Sigma\Delta$ modulator used in the IΣΔ ADC is a single-bit cascade of integrators in feed-forward configuration (CIFF) together with signal feed-forward, as shown in Fig. 2. The output of the modulator is given by:

$$\begin{aligned} V(z) &= U(z)\,STF(z) + E_Q(z)\,NTF(z) \\ &= V_U(z) + V_E(z) \end{aligned} \tag{1}$$

where $NTF(z)$ is the CTDT noise transfer function (NTF) when only the quantization noise $E_Q(z)$ is considered. $V(z)$ can also be expressed as a sum of two terms, $V_U(z)$ and $V_E(z)$, depending on $U(z)$ and $E_Q(z)$, respectively. $NTF(z)$ is designed to assure the stability of the modulator by obtaining the CT loop filter coefficients from a DT NTF, $NTF_{DT}(z)$, with a NTF infinity norm $H_{\inf} = 1.5$. In this case, switched-capacitor-resistor (SCR) coding scheme [7] is used in the feed-back digital-to-analogue converter (DAC) to reduce the sensitivity to ELD and jitter [8]. Similarly, $STF(z)$ is the CTDT signal transfer function (STF) when only the input signal $U(z)$, which is sampled by the channel sample-and-hold, is considered.

As the ADC quantization noise should be obtainable from the output of the last integrator, its CTDT output, $X_3(z)$, should be taken into account in the design of the digital filter $H_{DF}(z)$. Block diagrams illustrating the methodology to obtain $H_{DF}(z)$ and the gain G_I are shown in Fig. 3. The output of the 3rd integrator, at sampling times, is given by:

$$\begin{aligned} X_3(z) &= U(z)\,FF_{X_3}(z) - V(z)\,FB_{X_3}(z) \\ &= X_{3U}(z) + X_{3E}(z) \end{aligned} \tag{2}$$

where $FF_{X_3}(z)$ is the CTDT transfer function from the input sample-and-hold to the 3rd integrator output, and $FB_{X_3}(z)$ is the CTDT transfer function from the feed-back DAC to the 3rd integrator output. Similarly to $V(z)$, $X_3(z)$ can be expressed as the sum of $X_{3U}(z)$ and $X_{3E}(z)$ which depend on $U(z)$ and $E_Q(z)$, respectively. It can be observed that both of them contain terms dependent on $E_Q(z)$ and $U(z)$. This is unlike DT implementations where $X_3(z)$ depends only on $E_Q(z)$, assuming same topologies. Taking these dependencies into account it is possible to obtain the relationship between $V(z)$ and $D_I(z)$ so as to satisfy the requirement of the ADC quantization noise availability through $X_3(z)$. The direct acquisition of the ADC quantization noise through $X_3(z)$ can be obtained, as shown on Fig. 3(a), by solving the following set of equations:

$$X_{3E}(z) = V_E(z)\,H_D(z) \tag{3}$$

$$X_{3U}(z) = V_U(z)\,H_D(z) + J_U(z) \tag{4}$$

where $H_D(z)$ is the transfer function from where $H_{DF}(z)$ can be derived and $J_U(z)$ is the noiseless ADC output, from where the input signal and G_I can be derived. After solving the set of equations (3) and (4), $H_D(z)$ is found equal to:

$$H_D(z) = \left(\frac{\alpha}{(z-1)} + \frac{\beta}{(z-1)^2} - \frac{\gamma}{(z-1)^3}\right) k \tag{5}$$

where

$$\alpha = \frac{1}{8}\left(8\,\tau^2\left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) - 4\,\tau + 1\right)\tau \tag{6}$$

$$\beta = \frac{1}{2}\left(2\,\tau\left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right) - 2 + \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right)\tau \tag{7}$$

$$\gamma = \left(1 - \frac{1}{\mathrm{e}^{\frac{1}{2\,\tau}}}\right)\tau \tag{8}$$

$$k = c_3\,c_2\,c_1\,a_1 \tag{9}$$

where τ is the mean lifetime of the exponentially decaying DAC pulse. Similarly, $J_U(z)$ is found equal to:

$$\begin{aligned} J_U(z) &= U(z)\,c_3\,c_2\,c_1\,b_1 \\ &\cdot \left(\frac{1}{(z-1)^3} + \frac{1}{(z-1)^2} + \frac{1}{6}\frac{1}{(z-1)}\right) \end{aligned} \tag{10}$$

As the input signal is held through each conversion cycle, it remains constant, and, after N cycles, the time domain signal $j_U(n)$ will be equal to:

$$\begin{aligned} j_U(N) &= U \cdot \left(\frac{1}{6}N + \frac{N\,(N-1)}{2!}\right. \\ &\quad \left. + \frac{N\,(N-1)\,(N-2)}{3!}\right) c_3\,c_2\,c_1\,b_1 \\ &= U\,\frac{N^3}{6}\,c_3\,c_2\,c_1\,b_1 \end{aligned} \tag{11}$$

Where U is the constant input over a conversion cycle which can easily be derived from (11).

Similarly to the DT case, the integrators coefficients are acting as a scaling factor of the filter $H_D(z)$. Therefore, their deviation from the nominal value, as long as the modulator

remains stable, will only affect the gain of the ADC. Based on the previous values for $H_D(z)$ and $j_U(N)$ it is possible to derive the final values for $H_{DF}(z)$ and G_I, as shown on Fig. 3(b). The digital filter is implemented as a coefficient independent function given by:

$$H_{DF}(z) = \frac{H_D(z)}{k} \tag{12}$$

where k is given by (9). The output of the digital filter, $W(z)$, is then given by:

$$W(z) = V(z)\, H_{DF}(z) \tag{13}$$

Switching to time-domain, the gain relating the time-domain signal $w(n)$ at $n = N$, $w(N)$, with U is equal to:

$$G_I = \frac{U}{j_U(N)}\, k = \frac{6\, a_1}{N^3\, b_1} \tag{14}$$

The time-domain ADC output, scaled to the full-scale input values $\pm U_{\mathrm{FS}}$, at $n = N$, $d_I(N)$, is then given by:

$$d_I(N) = w(N)\, G_I = U + e_{Q-I}(N) \tag{15}$$

where $e_{Q-I}(N)$ is the ADC quantization noise, also scaled to $\pm U_{\mathrm{FS}}$. The relationship between $e_{Q-I}(N)$ and $x_3(N)$ is given by:

$$G_{X_3} = \frac{e_{Q-I}(N)}{x_3(N)} = \frac{6}{b_1\, c_1\, c_2\, c_3\, N^3} \tag{16}$$

This relationship is then used to determine the maximum ADC quantization noise and its maximum equivalent number of bits (ENOB). Assuming a maximum range for the output of the 3rd integrator equal to $\pm U_{\mathrm{FS}}$, the LSB quantization error will be given by:

$$V_{LSB} = 2\, U_{\mathrm{FS}}\, G_{X_3} = \frac{12\, U_{\mathrm{FS}}}{b_1\, c_1\, c_2\, c_3\, N^3} \tag{17}$$

The ENOB for an input differential signal with amplitude $\pm U_{\max}$ will then be given by:

$$\mathrm{ENOB} = \log_2\left(\frac{2\, U_{\max}}{V_{LSB}}\right) \tag{18}$$

This shows that the ENOB depends not only on the number of cycles N, but also on the maximum input signal $U_{\max}$ and the selected coefficients. Due to stability issues, it is always a tradeoff between the maximum input signal applied and the maximum value for the coefficients. Generally, the lower the maximum input signal, the higher the coefficients can be. It is worth to notice that the relationship between ENOB and N is slightly different than for DT implementations [5].

Based on (18), the number of cycles for the proposed IΣΔ ADC was chosen equal to 80 ($N = 80$) in order to obtain an ENOB of 12. The ADC sampling frequency f_s/N was set equal to $4\,\mathrm{kHz}$ ($f_s = 320\,\mathrm{kHz}$) in order to process 8 channels at a sampling rate of $500\,\mathrm{Hz}$ each.

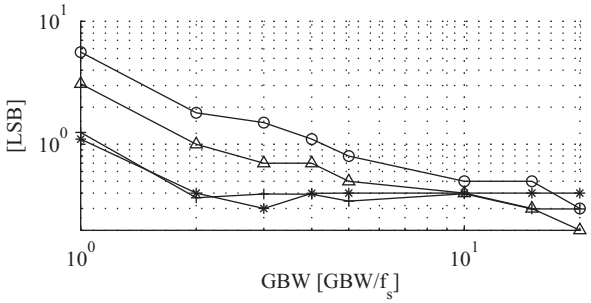

Fig. 4. ADC static performance vs. Integrators GBW [References: + $\mathrm{INL_{max}}$, ⋆ $\mathrm{DNL_{max}}$, ○ Gain error, △ Offset error].

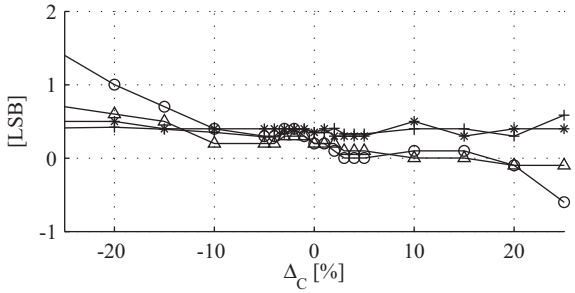

Fig. 5. ADC static performance vs. integrators coefficients deviation [References: + $\mathrm{INL_{max}}$, ⋆ $\mathrm{DNL_{max}}$, ○ Gain error, △ Offset error].

B. Non-Ideal Behavior

In order to validate the proposed IΣΔ ADC, critical non-idealities specific to CT implementation were considered and analyzed. MATLAB transient simulations were run while computing the ADC's static performance under different scenarios. This was performed by applying a ramp, between $\pm U_{\max}$, to the ADC which is sampled $2^{12} \cdot 8$ times to obtain an accuracy of at least 0.125 LSBs.

Single pole models were used to simulate the amplifier's finite GBW [9]. As shown in Fig. 4, a GBW approximately equal to f_s is required to keep INL and DNL under the 0.5 LSB limit and meet the desired ENOB. This is in-line with traditional CT ΣΔ ADCs' requirements and represents a key advantage in terms of power performance compared to DT implementations [1].

Coefficients variation was simulated to determine the impact of the integrators' process variation on the ADC performance. As expected from (11), simulation results shown in Fig. 5 confirm that the most significant impact of coefficient variation is on the gain error, while INL and DNL are considerably less affected. A coefficient variation of approximately $\pm 10\%$ assures an INL and DNL boundary of ± 0.5 LSB, imposing relaxed requirements on the calibration circuitry.

The impact of jitter and ELD was the most detrimental in the ADC performance when using a NRZ or return-to-zero coding scheme. Their effect was counteracted by using SCR coding scheme with an appropriate mean lifetime value $\tau = 0.02\, T_s$ determined through extensive simulations. As shown in Fig. 6 and Fig. 7, in order not to exceed 0.5 LSB in INL and DNL,

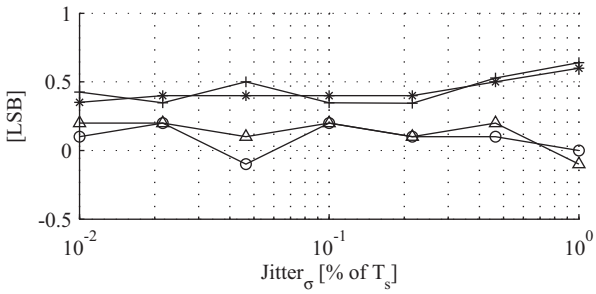

Fig. 6. ADC static performance vs. jitter standard deviation [References: + INL_{max}, ⋆ DNL_{max}, ○ Gain error, △ Offset error].

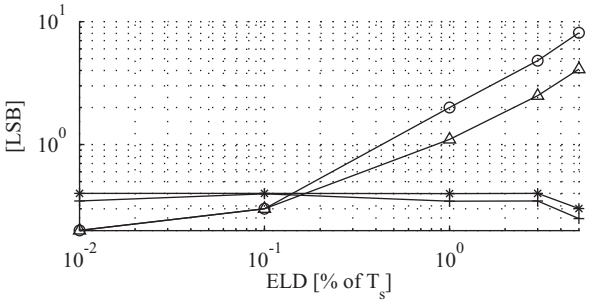

Fig. 7. ADC static performance vs. DAC ELD [References: + INL_{max}, ⋆ DNL_{max}, ○ Gain error, △ Offset error].

a value of less than 0.04% of T_s (1.25 ns) is required for the jitter standard deviation while up to 5% of T_s (156 ns) was shown sufficient for the ELD, values which are achievable in current CMOS technologies. It is worth to mention that, as the SCR scheme is active from the 2nd half of the period, as long as the quantizer is faster than 0.5 T_s, the ELD will be generated only by the DAC delay.

A final test, using practical values for all previous non-idealities, was performed. A GBW equal to 3 f_s was considered for the integrators while the DAC was assumed to have an ELD equal to 3% of T_s (93.7 ns). Moreover, a clock jitter standard deviation of 0.02% T_s (625 ps) and a coefficient deviation of -10% was included in the model. The simulation results show a gain and offset error of 3.4 LSB and 6.3 LSB respectively. The simulated INL and DNL results presented in Fig. 8 show a DNL performance in the 0.5 LSB limit while the INL is more relaxed. This allows 12 bits resolution while relaxing the integrators' GBW requirement.

III. Conclusion

A novel CT IΣΔ ADC has been proposed and analyzed. The operation of high order single loop CT IΣΔ ADCs has been presented using a 3rd order modulator as an example. The proposed architecture takes advantage of high-order filtering to reduce the number of required cycles to achieve certain resolution and CT implementation to relax the amplifiers' GBW requirement. These features have been validated through behavioral simulations where critical non-idealities have been considered and their impact has been investigated. Simulation

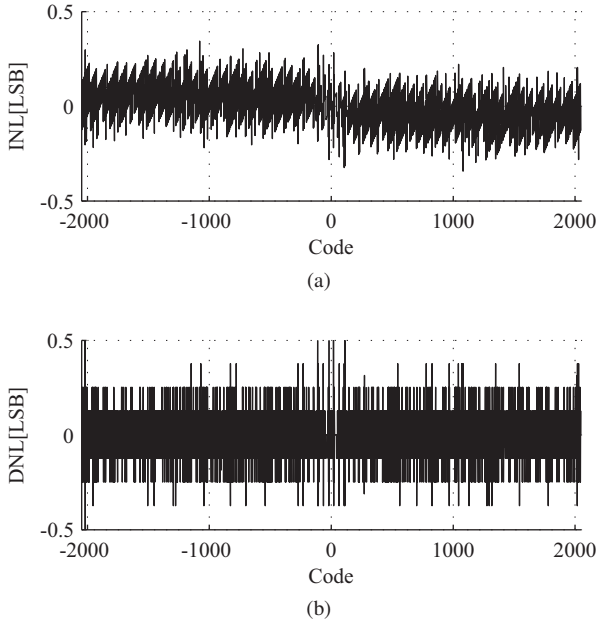

Fig. 8. INL (a) and DNL (b) performance of IΣΔ ADC.

results show that high-order single-loop CT IΣΔ ADC allows relaxing the requirement of the integrators' GBW which may provide a low power alternative to multi-channel applications.

Acknowledgment

This work has been supported by Swedish Research Council (VR) under DERFAW project.

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