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High Performance β-Ga_2O_3 Nano-Membrane Field Effect Transistors on a High Thermal Conductivity Diamond Substrate

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ABSTRACT To suppress severe self-heating under high power density, we herein demonstrate top-gate nano-membrane β-gallium oxide (β-Ga_2O_3) field effect transistors on a high thermal conductivity diamond substrate. The devices exhibit enhanced performance, with a record high maximum drain current of 980 mA/mm for top-gate β-Ga_2O_3 field effect transistors and 60% less temperature increase from reduced self-heating, compared to the device on a sapphire substrate operating under identical power density. With improved heat dissipation, β-Ga_2O_3 field effect transistors on a diamond substrate are validated using an ultrafast high-resolution thermoreflectance imaging technique, Raman thermography, and thermal simulations.

INDEX TERMS β-Ga_2O_3FET, diamond, nano-membrane, thermal conductivity, self-heating effect.

I. INTRODUCTION

β-Ga_2O_3 is an emerging wide bandgap semiconductor for the next generation power devices to replace GaN and SiC. It has an ultra-wide bandgap of 4.8 eV and a corresponding high breakdown field (E_{br}) of 8 MV/cm [1]–[5]. And low-cost large-size β-Ga_2O_3 native bulk substrates can be potentially realized by melt-grown methods [6]–[7]. However, the β-Ga_2O_3 bulk substrate has a low thermal conductivity (κ) of 10-25 W/m·K and thus severe self-heating effects (SHE) can be observed [8]. In high-power electronic devices, the output power density (P) and maximum drain current (I_D) can be significantly limited by elevated channel temperature caused by SHE [9], [10] and it has become a key challenges in β-Ga_2O_3 research because elevated temperature degrades electron mobility in β-Ga_2O_3 [8], [11]–[13]. In addition, high channel temperature can also severely degrade the gate dielectric, device variability, and long-term reliability [8], [14]. Recently, various studies regarding the thermal management of β-Ga_2O_3 devices have been reported [15]–[17]. In particular, it is important to mitigate SHE to sustain original device performance of β-Ga_2O_3 devices in practical applications. One solution is an integration of a low κ β-Ga_2O_3 channel on a high κ substrate, rather than taking advantages of the β-Ga_2O_3 native substrate.

In our previous works, we have demonstrated β-Ga_2O_3 field effect transistors (FETs) on a sapphire substrate (κ = 40 W/m·K) to replace a SiO_2/Si substrate (κ = 1.5 W/m·K for 270 nm SiO_2) [18]–[20]. The resulting device has shown a 70% higher maximum I_D, half the device surface temperature increase (ΔT), and half the thermal resistance (R_T), significantly reducing SHE in comparison to a SiO_2/Si substrate. Diamond has a much higher thermal conductivity (κ = 1, 000-2, 200 W/m·K) than sapphire; thus, it is of

great interest to investigate the heat dissipation effect of β-Ga_2O_3 devices on a diamond substrate. Diamond is also a current blocking substrate for transferred β-Ga_2O_3 nano-membranes due to its wide bandgap of 5.47eV [21]. In this work, we not only demonstrate the record performance of top-gate β-Ga_2O_3 FETs on a diamond substrate [22], [23], but also fully study the thermal properties of β-Ga_2O_3 on a diamond substrate using high-resolution thermoreflectance (TR) imaging [24], [25], Raman thermography, and thermal simulations.

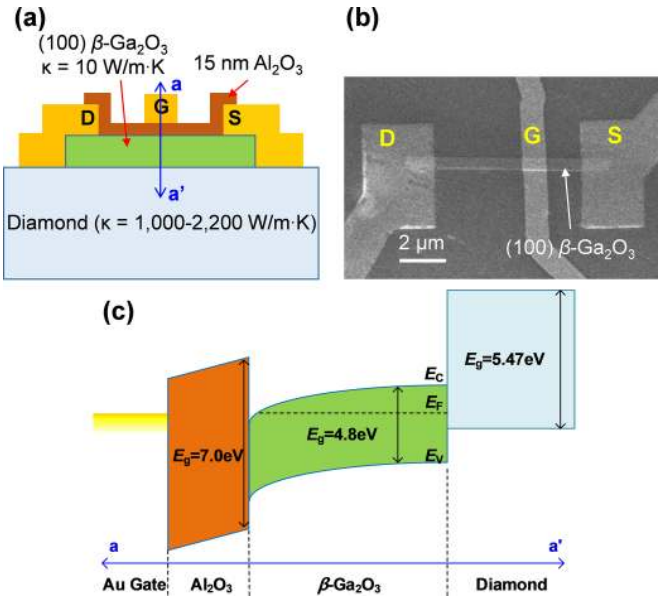

FIGURE 1. **(a) Schematic view of a top-gate β-Ga_2O_3 FET on a diamond substrate. (b) SEM top view of a β-Ga_2O_3 FET with $L_G = 1$ μm. (c) Thermal equilibrium energy band diagram of a β-Ga_2O_3 FET from the gate to the diamond substrate.**

II. DEVICE FABRICATION AND I–V CHARACTERISTICS

Fig. 1(a) and (b) are the schematic view and the top-view scanning electron microscopy (SEM) image of a top-gate β-Ga_2O_3 transistor on a diamond substrate. β-Ga_2O_3 nano-membranes with thicknesses from 50-150 nm (100), Sn-doped at 2.7×10^{18} cm^{-3} were transferred to a 500 μm-thick polished (100) diamond bulk single crystal substrate. A Ti/Al/Au (15/60/50 nm) metal stack was deposited and lifted-off in source and drain regions for the source and drain contact formation. The top-gate stack consists of 15 nm amorphous aluminum oxide (Al_2O_3) gate dielectric deposited by atomic layer deposition (ALD) at 175 °C and Ni/Au (50/50 nm) as the gate electrode. All the source, drain, and gate regions were patterned by electron-beam lithography. Fig. 1(c) shows the energy band line-up from the gate all the way to the diamond substrate of a fabricated top-gate β-Ga_2O_3 transistor on a diamond substrate.

The output and transfer characteristics of a representative top-gate depletion-mode β-Ga_2O_3 FET with channel thickness of ~80 nm, source to drain distance (L_{SD}) of 7.5 μm, gate length (L_G) of 1 μm, gate to drain distance (L_{GD}) of 4 μm, and gate to source distance (L_{GS}) of 2.5 μm is shown in Fig. 2(a)–(c). The physical gate width of β-Ga_2O_3 is 0.55 μm, and was determined via SEM. The gate bias (V_{GS}) is swept from 8 to −28 V in −2 V steps to turn off the device, while the drain bias (V_{DS}) is swept from 0 to 30 V. The threshold voltage at V_{DS} = 5V is −22.6 V from linear extrapolation of I_D-V_{GS}. The maximum transconductance (g_m) was found to be 53 mS/mm at V_{DS} = 30 V. Two peaks in the transconductance profile are mainly from Schottky-like source and drain contacts. Source and drain contacts with high Schottky barrier limit the drain current. However, at high V_{DS} and V_{GS} biases, this degradation can be mitigated partially because the tunneling current in the source contact increases due to the reduction of Schottky barrier width in the source contact at high bias conditions. Also, high V_{DS} can lower the drain barrier. That is why there is the second peak around V_{GS} of −4V in Fig. 2(b) when high V_{DS} of 30V is biased.

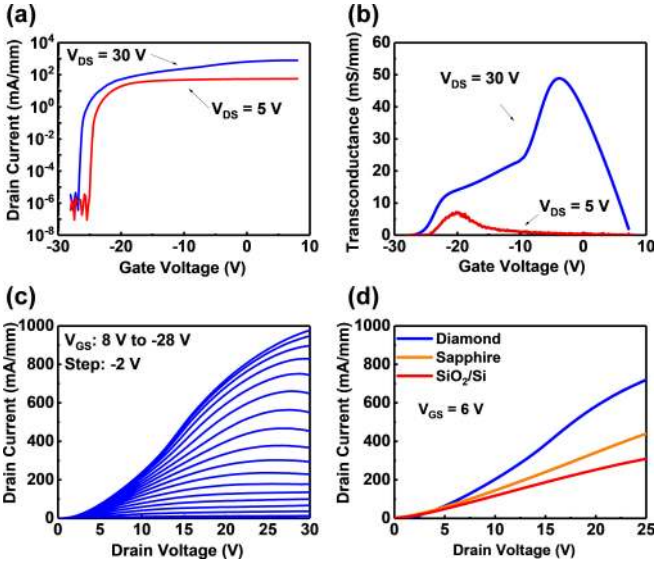

FIGURE 2. **(a) I_D-V_{GS}, (b) g_m-V_{GS} and (c) I_D-V_{DS} characteristics of a fabricated β-Ga_2O_3 FET with the record high maximum drain current among all top-gate β-Ga_2O_3 FETs. Two humps in the transconductance profile are from Schottky-like contacts. Certain hysteresis in the range of 1.5 ~ 2 V are exhibited during bi-directional sweeps of the transfer curves. (d) Comparison of I_D-V_{DS} of β-Ga_2O_3 FETs with the similar dimensions (L_g = 1 μm, L_{SD} ~ 6 μm, thickness ~80nm) on a diamond, sapphire, and SiO_2/Si substrate at V_{GS} of 6V. The diamond device shown in (d) is different from that in (a)–(c) for the fair comparison [20].**

The record high maximum drain current (I_{Dmax}) of 980 mA/mm among all demonstrated top-gate β-Ga_2O_3 FETs is obtained at the drain bias of 30 V and the gate bias of 8 V [18], [26]–[29]. Fig. 2(d) illustrates that the on-resistance of FETs on three different substrates with similar dimensions are similar.

The calculated values of the source and drain contact resistance (R_C) of all the three devices are about 80 kΩ. R_C was extracted when the gate voltage is large enough to minimize the channel resistance from output characteristics of three devices in the linear region [30], [31]. When the

power density is increased by increased drain voltage, the drain current level becomes significantly different depending on substrates.

The obtained high drain current can be ascribed mainly to the improved transport properties at lower channel temperatures from significantly reduced SHE. The heat generated in the channel under high bias dissipates much faster on a diamond substrate, compared to SiO_2/Si and sapphire substrates. The electron mobility of β-Ga_2O_3 decreases when the temperature increases above room temperature so that this improved transport properties by less self-heating effect on a diamond substrate could be the main reason for the increase of the maximum drain current [12].

III. TEMPERATURE MEASUREMENTS AND DISCUSSION

In order to study thermal characteristics, steady-state TR imaging experiments and Raman thermography were carried out on β-Ga_2O_3 FETs at various bias conditions as shown in Fig. 3 along with the thermal simulations shown in Fig. 4.

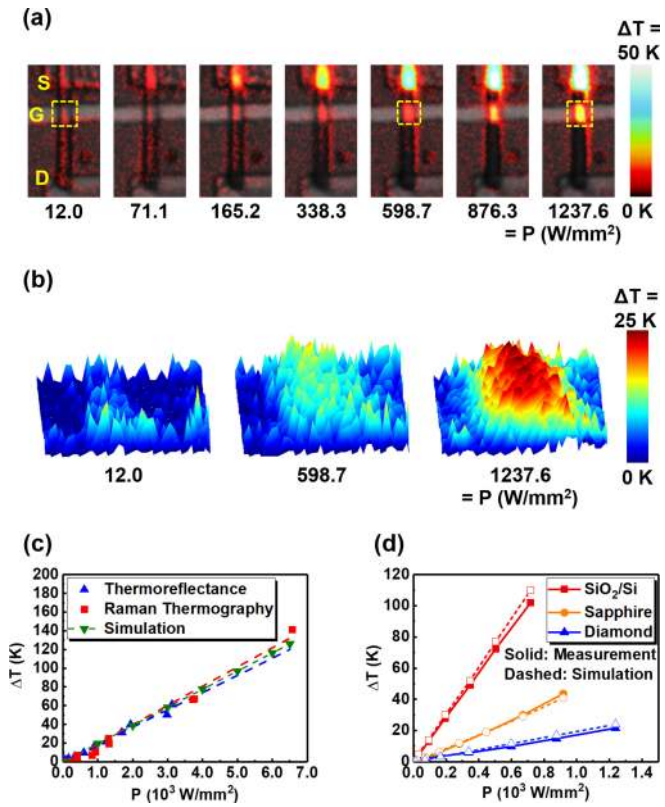

FIGURE 3. **Temperature maps of (a) top view and (b) gate region magnification of steady-state temperature increases at different P of a top-gate β-Ga_2O_3 FET on diamond substrate measured by a TR imaging set-up. (c) Comparison of measured and simulated ΔT vs. P (W/mm^2) characteristics of top-gate β-Ga_2O_3 FETs on a diamond substrate using TR imaging, Raman thermography, and the thermal simulations. (d) Measured by the TR method and simulated ΔT vs. P (W/mm^2) characteristics of top-gate β-Ga_2O_3 FETs on different substrates [18].**

For the TR measurement, the gate Ni/Au pads were illuminated through a green LED ($\lambda = 530$ nm). The change in reflectance of the gate pad was calibrated with Au TR

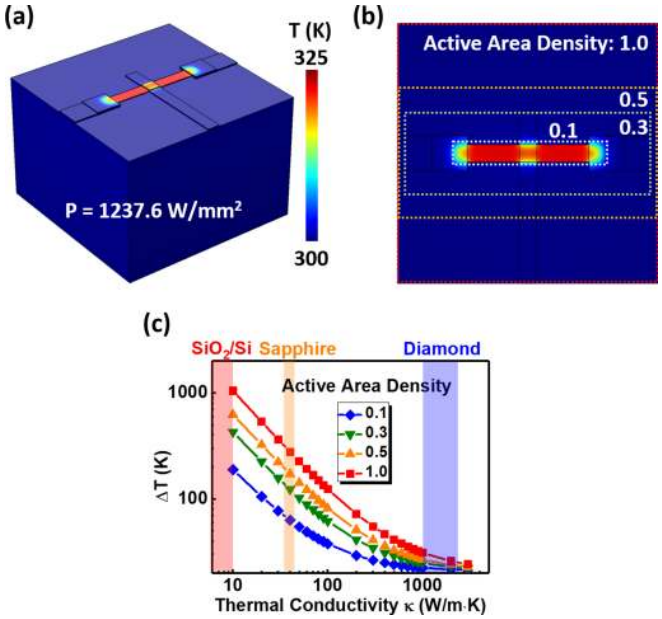

FIGURE 4. **(a) Simulated temperature distribution of a fabricated β-Ga_2O_3 FET on a diamond substrate. (b) Top view of the simulation boundary with various active area density. (c) Simulated ΔT vs. κ characteristics depending on active area density with fixed 1000 W/mm^2 power density.**

coefficient ($C_{TH} = -2.5 \times 10^{-4}$ K^{-1}) to extract temperature increase above room temperature [25]. The gate Au electrode region above the channel was measured as a representative of the channel temperature since β-Ga_2O_3 is transparent at the illumination wavelength of 530nm.

Micro-Raman measurements were performed using the peak-shift method and a confocal geometry [26]. A single-mode 488nm laser was made confocal with the detection axis using the beam-splitter part of a Volume-Bragg-Grating filter set from Optigrate. These filters allow Stokes and anti-Stokes Raman measurements closer than 10 cm^{-1} to the laser. A 50x microscope objective (NA = 0.65) was used to both focus the excitation light into a small spot ($\sim$ 0.4 μm) and collect Raman scattered photons. The Raman photons were dispersed in a half-meter Acton SP-2500 single-spectrometer and then detected using a Princeton Instruments CCD array (Spec-10:400BR back-thinned, deep-depleted). Temperature calibration of the device at zero bias was performed using a Lorentzian fit of the 169 cm^{-1} β-Ga_2O_3 Raman line in the 23-100 °C range, where linear behavior was observed [33].

Once the device is turned on at $V_{GS} = 0$V with positive V_{DS}, the channel is heated up within a few hundred ns in transient response [18] and steady-state ΔT can be determined easily under a greater time scale. Various V_{DS} were also applied to measure temperatures in different output power density. The V_{DS} modulation signal of a pulse width of 1 ms and 10% duty cycle and the 100 μs optical pulse width was applied during the TR measurement, which is long enough to measure steady state temperature. The measured β-Ga_2O_3 nano-membrane area (A) is 3.9×10^{-6} mm^2 and the output power density ($V_{DS} \times I_D$/A) is normalized

by area (W × L_{SD}) to avoid different heat dissipation areas from different sizes of β-Ga_2O_3 nano-membranes for accurate comparison. The bias conditions of each temperature measurement point in Fig. 3(a) are summarized in Table 1.

TABLE 1. Bias conditions of each temperature measurement point in Fig. 3(a).

	#1	#2	#3	#4	#5	#6	#7
V_{DS} (V)	1.81	3.57	5.3	6.49	8.08	9.17	10.9
I_D (uA)	26	78.1	122.2	204.3	290.5	374.6	446.7
A (mm^2)	3.9×10^{-6}						
P (W/mm^2)	12.0	71.1	165.2	338.3	598.7	876.3	1237.6
ΔT (K)	1.8	2.2	3.6	5.7	9.8	14.9	21.6

Fig. 3(c) shows the measured and simulated ΔT vs. P (W/mm^2) for the β-Ga_2O_3 FETs on a diamond substrate, performed both by TR imaging and Raman thermography. The thermal simulations were carried out using the COMSOL commercial finite-element analysis software package [34]. Agreement among these three methods was observed, with the highest temperature measured by Raman thermography to be 164 °C (ΔT = 141 K) at DC output power of 6,565 W/mm^2 (64.7 W/mm or V_{DS} = 35 V for this particular exfoliated FET geometry). Fig. 3(d) shows agreement of the TR measured and the simulated ΔT vs. P (W/mm^2) on different substrates. Except substrates, all process and materials including the doping concentration of β-Ga_2O_3 are exactly the same. The devices with similar dimensions (L_g = 1 μm, L_{SD} ~ 6 μm, thickness ~ 80 nm) for each substrate are selected for thermal measurement. The output power density of devices on three different substrates are normalized by the area of the device to make a fair comparison.

Thermal simulations were carried out using COMSOL with the finite-element method [34]. The simulated structure with temperature distribution of the β-Ga_2O_3 FET on a diamond substrate is shown in Fig. 4(a). In the simulation, the whole 80 nm thick β-Ga_2O_3 flake was defined as a heat source with the uniformly biased power density and bottom of the diamond substrate was defined as a heat sink at room temperature. The thermal boundary conductance of 17 $MW/m^2 \cdot K$ for the interface between β-Ga_2O_3 and a diamond substrate was used according to the recently reported value [35]. The results in Fig. 3(d) show that β-Ga_2O_3 FETs on a diamond substrate have more than 60% lower ΔT at the same P condition, compared to that of sapphire, and greatly improved when compared to that of SiO_2. The thermal resistance (R_T = ΔT/P) of the device on a diamond substrate is 1.71×10^{-2} $mm^2 \cdot K/W$ while those of sapphire and SiO_2/Si substrates are 4.62×10^{-2} and 1.47×10^{-1} $mm^2 \cdot K/W$, respectively. This shows that heat dissipates more effectively in a higher κ substrate, and as a result, the decreased peak channel temperature can sustain the good transport properties of β-Ga_2O_3 and achieve a greater I_{Dmax}.

In order to verify that the κ of a diamond substrate is high enough to minimize SHE under practical applications, such as high power density device applications, the simulations with constant power density at 1000 W/mm^2, various κ values, and various active area densities were carried out as well. The active area density was defined as the percentage of the active region area in the whole substrate surface area and was implemented by changing the width and length of the active area in the same simulation boundary as shown in Fig. 4(b). The graph of ΔT vs. κ in Fig. 4(c) shows that a diamond substrate with κ = 1, 000-2, 200 W/m·K can effectively absorb heat generated in the β-Ga_2O_3 FET. Moreover, when the active area density on a SiO_2/Si or sapphire substrate increases, the temperature change drastically increases in accordance. However, when the substrate is diamond, the temperature increase of the device is well suppressed relatively even in the high active area density. In conclusion, the effect of the improved heat dissipation by implementing diamond substrates can be even more significant since the practical power devices have larger active area than the single membrane device demonstrated in this work.

IV. CONCLUSION

In this work, we demonstrate top-gate nano-membrane β-Ga_2O_3 FETs on a high thermal conductivity diamond substrate. The devices exhibit enhanced performance with a record high maximum I_D of 980 mA/mm among all top-gate β-Ga_2O_3 FETs and 60% less channel temperature increase, compared to the devices on a sapphire substrate under the same DC biases. Thermal characteristics were investigated using TR imaging and matched well with thermal simulations. The calculated R_T of a diamond substrate was found to be 1.71×10^{-2} $mm^2 \cdot K/W$, which is much lower than those of sapphire and SiO_2/Si, 4.62×10^{-2} and 1.47×10^{-1} $mm^2 \cdot K/W$. This suggests that the close integration of β-Ga_2O_3 into a diamond substrate provides a potential solution to the self-heating of β-Ga_2O_3 in high-power device applications.

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REFERENCES

[1] M. Higashiwaki *et al.*, "Recent progress in Ga_2O_3 power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, Jan. 2016, Art. no. 34001. doi: 10.1088/0268-1242/31/3/034001.

[2] S. I. Stepanov, V. I. Nikolaev, V. E. Bougrov, and A. E. Romanov, "Gallium oxide: Properties and applications—A review," *Rev. Adv. Mater. Sci.*, vol. 44, no. 63, pp. 63–86, Apr. 2016. [Online]. Available: http://www.ipme.ru/e-journals/RAMS/no_14416/06_14416_stepanov.pdf

[3] M. Kim, J.-H. Seo, U. Singisetti, and Z. Ma, "Recent advances in free-standing single crystalline wide band-gap semiconductors and their applications: GaN, SiC, ZnO, β-Ga_2O_3, and diamond," *J. Mater. Chem. C*, vol. 5, no. 33, pp. 8338–8354, Jun. 2017. doi: 10.1039/C7TC02221B.

[4] S. J. Pearton *et al.*, "A review of Ga_2O_3 materials, processing, and devices," *Appl. Phys. Rev.*, vol. 5, no. 1, Jan. 2018, Art. no. 11301. doi: 10.1063/1.5006941.

[5] M. Higashiwaki and G. H. Jessen, "Guest editorial: The dawn of gallium oxide microelectronics," *Appl. Phys. Lett.*, vol. 112, no. 6, Feb. 2018, Art. no. 060401. doi: 10.1063/1.5017845.

[6] H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, "Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method," *Jpn. J. Appl. Phys.*, vol. 47, no. 11, pp. 8506–8509, Nov. 2008. doi: 10.1143/JJAP.47.8506.

[7] Z. Galazka *et al.*, "On the bulk β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Cryst. Growth*, vol. 404, pp. 184–191, Oct. 2014. doi: 10.1016/j.jcrysgro.2014.07.021.

[8] M. H. Wong, Y. Morikawa, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Characterization of channel temperature in Ga_2O_3 metal-oxide-semiconductor field-effect transistors by electrical measurements and thermal modeling," *Appl. Phys. Lett.*, vol. 109, no. 19, Nov. 2016, Art. no. 193503. doi: 10.1063/1.4966999.

[9] R. Gaska, A. Osinsky, J. W. Yang, and M. S. Shur, "Self-heating in high-power AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 19, no. 3, pp. 89–91, Mar. 1998. doi: 10.1109/55.661174.

[10] Y. Zhou *et al.*, "Thermal characterization of polycrystalline diamond thin film heat spreaders grown on GaN HEMTs," *Appl. Phys. Lett.*, vol. 111, no. 4, Jul. 2017, Art. no 041901. doi: 10.1063/1.4995407.

[11] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, "Electrical properties of β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Appl. Phys.*, vol. 110, no. 6, Sep. 2011, Art. no. 063720. doi: 10.1063/1.3642962.

[12] T. Oishi, Y. Koga, K. Harada, and M. Kasu, "High-mobility β-Ga_2O_3(-201) single crystals grown by edge-defined film-fed growth method and their Schottky barrier diodes with Ni contact," *Appl. Phys. Exp.*, vol. 8, no. 3, Feb. 2015, Art. no. 031101. doi: 10.7567/APEX.8.031101.

[13] A. Parisini and R. Fornari, "Analysis of the scattering mechanisms controlling electron mobility in β-Ga_2O_3," *Semicond. Sci. Technol.*, vol. 31, no. 3, Feb. 2016, Art. no. 035023. doi: 10.1088/0268-1242/31/3/035023.

[14] R. J. Trew, D. S. Green, and J. B. Shealy, "AlGaN/GaN HFET reliability," *IEEE Microw. Mag.*, vol. 10, no. 4, pp. 116–127, Jun. 2009. doi: 10.1109/MMM.2009.932286.

[15] B. Chatterjee, K. Zeng, C. D. Nordquist, U. Singisetti, and S. Choi, "Device-level thermal management of gallium oxide field-effect transistors," *IEEE Trans. Compon. Packag. Manuf. Technol.*, to be published. doi: 10.1109/TCPMT.2019.2923356.

[16] J. W. Pomeroy *et al.*, "Raman thermography of peak channel temperature in β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 189–192, Feb. 2019. doi: 10.1109/LED.2018.2887278.

[17] M. J. Tadjer, "Cheap ultra-wide bandgap power electronics? Gallium oxide May hold the answer," *Electrochem. Soc. Interface*, vol. 27, no. 4, pp. 49–52, 2018. doi: 10.1149/2.F05184if.

[18] H. Zhou, K. Maize, J. Noh, A. Shakouri, and P. D. Ye, "Thermodynamic studies of β-Ga_2O_3 nanomembrane field-effect transistors on a sapphire substrate," *ACS Omega*, vol. 2, no. 11, pp. 7723–7729, Nov. 2017. doi: 10.1021/acsomega.7b01313.

[19] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. D. Ye, "High-performance depletion/enhancement-mode β-Ga_2O_3 on insulator (GOOI) field-effect transistors with record drain currents of 600/450 mA/mm," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 103–106, Jan. 2017. doi: 10.1109/LED.2016.2635579.

[20] H. Zhou, K. Maize, G. Qiu, A. Shakouri, and P. D. Ye, "β-Ga_2O_3 on insulator field-effect transistors with drain currents exceeding 1.5 A/mm and their self-heating effect," *Appl. Phys. Lett.*, vol. 111, no. 9, Aug. 2017, Art. no. 92102. doi: 10.1063/1.5000735.

[21] S. V. Kidalov and F. M. Shakhov, "Thermal conductivity of diamond composites," *Mater. (Basel)*, vol. 2, no. 4, pp. 2467–2495, Dec. 2009. doi: 10.3390/ma2042467.

[22] J. Noh *et al.*, "β-Ga_2O_3 nano-membrane FETs on a diamond substrate," in *Proc. Compound Semicond. Week (CSW)*, May 2018, pp. 451–452.

[23] J. Noh, M. Si, H. Zhou, M. J. Tadjer, and P. D. Ye, "The impact of substrates on the performance of to-gate β-Ga_2O_3 field-effect transistors: Record high drain current of 980 mA/mm on diamond," in *Proc. Device Res. Conf. (DRC)*, Jun. 2018. doi: 10.1109/DRC.2018.8442276.

[24] M. Farzaneh *et al.*, "CCD-based thermoreflectance microscopy: Principles and applications," *J. Phys. D Appl. Phys.*, vol. 42, no. 14, Jun. 2009, Art. no. 143001. doi: 10.1088/0022-3727/42/14/143001.

[25] K. Maize, A. Ziabari, W. D. French, P. Lindorfer, B. Oconnell, and A. Shakouri, "Thermoreflectance CCD imaging of self-heating in power MOSFET arrays," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3047–3053, Sep. 2014. doi: 10.1109/TED.2014.2332466.

[26] B. Chatterjee, A. Jayawardena, E. Heller, D. W. Snyder, S. Dhar, and S. Choi, "Thermal characterization of gallium oxide Schottky barrier diodes," *Rev. Sci. Instrum.*, vol. 89, no. 11, Nov. 2018, Art. no. 114903. doi: 10.1063/1.5053621.

[27] A. J. Green *et al.*, "3.8-MV/cm breakdown strength of MOVPE-grown Sn-doped β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 902–905, Jul. 2016. doi: 10.1109/LED.2016.2568139.

[28] N. A. Moser *et al.*, "High pulsed current density β-Ga_2O_3 MOSFETs verified by an analytical model corrected for interface charge," *Appl. Phys. Lett.*, vol. 110, no. 14, Apr. 2017, Art, no. 143505. doi: 10.1063/1.4979789.

[29] K. D. Chabak *et al.*, "Recessed-gate enhancement-mode β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 67–70, Jan. 2018. doi: 10.1109/LED.2017.2779867.

[30] Z. Xia *et al.*, "Delta doped β-Ga_2O_3field effect transistors with regrown Ohmic contacts," *IEEE Electron Device Lett.*, vol. 39, no. 4, pp. 568–571, Apr. 2018. doi: 10.1109/LED.2018.2805785.

[31] J. P. Campbell, K. P. Cheung, J. S. Suehle, and A. Oates, "A simple series resistance extraction methodology for advanced CMOS devices," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1047–1049, Aug. 2011. doi: 10.1109/LED.2011.2158183.

[32] H. Bae *et al.*, "Extraction of separated source and drain resistances in amorphous indium–gallium–zinc oxide TFTs through C–V characterization," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 761–763, Jun. 2011. doi: 10.1109/LED.2011.2127438.

[33] D. Dohy, G. Lucazeau, and A. Revcolevschi, "Raman spectra and valence force field of single-crystalline β-Ga_2O_3," *J. Solid State Chem.*, vol. 45, no. 2, pp. 180–192, Nov. 1982. doi: 10.1016/0022-4596(82)90274-2.

[34] *COMSOL Multiphysics*. Accessed: May 24, 2018. [Online]. Available: http://www.comsol.com

[35] Z. Cheng, L. Yates, J. Shi, M. J. Tadjer, K. D. Hobart, and S. Graham, "Thermal conductance across β-Ga_2O_3-diamond van der Waals heterogeneous interfaces," *APL Mater.*, vol. 7, no. 3, Mar. 2019, Art. no. 031118. doi: 10.1063/1.5089559.