HIGH-PERFORMANCE BICMOS OUTPUT BUFFER DESIGN STRATEGIES

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ABSTRACT

This paper discusses design issues for high-performance BiCMOS output buffers, as required in T&Hs and data converters for advanced applications. We compare different topologies and analyze the main limitations. The best solution features a linearity better than -105 dB (HD_3) at an input frequency of 100 MHz. The simulation results referred to a conventional 0.8 μm BiCMOS process cover a huge range of performance parameters in terms of linearity, bandwidth and dynamic range. More in general, this paper helps the designer to identify the best strategy for given high speed and high resolution specifications.

1. INTRODUCTION

The output buffer is a popular block used in a large number of circuits as a final stage capable of driving a certain load without degrading signal characteristics. A typical application is as a last stage in high-speed (f_{ck} > 100 MHz) high-resolution (> 12 bit) track-and-hold, used as a front-end for high-performance A/D converters. Key specifications that we aim to achieve are:

- high linearity with an estimated load of 10 pF
- low input current to guarantee a reduced droop-rate on the previous sampling stage
- high-speed (i.e. minimum settling time)

This paper presents the various architectures using CMOS or BiCMOS technology. The solution proposed mainly aims at ensuring high linearity whilst maintaining the other two specifications at a good level.

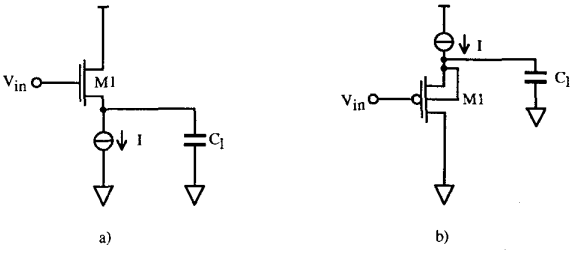

Figure 1. Schematic diagram of a level-shifter: a) NMOS; b) PMOS

2. SIMPLE CMOS BUFFER

The simplest way to implement an output buffer is to use a level-shifter [1]. A CMOS implementation (Fig. 1) ensures a minimum input current. We know that, aside from a fixed voltage shift, the output follows the input and the output impedance is quite low.

The first design issue concerns the choice of the input transistor type. It depends on the technology used: we know that the modulation of the threshold voltage, V_{th}, (Body Effect) causes a distortion in the signal. Hence, with an n-well process using a PMOS device allows us to overcome the body effect by connecting the well with source, thus reducing distortion. The two circuits shown in Fig. 1 have been simulated with a 1 MHz and 100 MHz, 0.5 V_{pp} input sinewave (I_{bias} = 10 mA). The results are shown in Table 1 and 2. As expected, the distortion of the NMOS level-shifter is worse at low frequency than that of the PMOS. However, we observe that at high frequency, the distortion of the p-channel approaches that of the n-channel.

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	1 MHz	100 MHz
HD_2	-53 dB	-58 dB
HD_3	-87 dB	-86 dB
HD_4	-118 dB	-115 dB

Table 1. Source follower: harmonic distortion with n-channel input transistors

	1 MHz	100 MHz
HD_2	-77 dB	-54 dB
HD_3	-112 dB	-85 dB
HD_4	-144 dB	-110 dB

Table 2. Source follower: harmonic distortion with p-channel input transistors

The use of differential solutions leads to a significant reduction of the even harmonics. Therefore, the most important harmonic component is the third one. For better design indications we analyzed the distortion effect in the 1-100 MHz range in more detail. Fig. 2 shows the results. We observe that at low frequencies it is advisable to use p-channel input but for high frequency applications the speed limits of the p-channel devices make a solution with n-channel input elements more convenient. The results correspond to an optimized design for the current used and transistor sizing. Therefore, because of the given level of harmonic distortion, we conclude that the simple CMOS buffer not viable for high linearity.

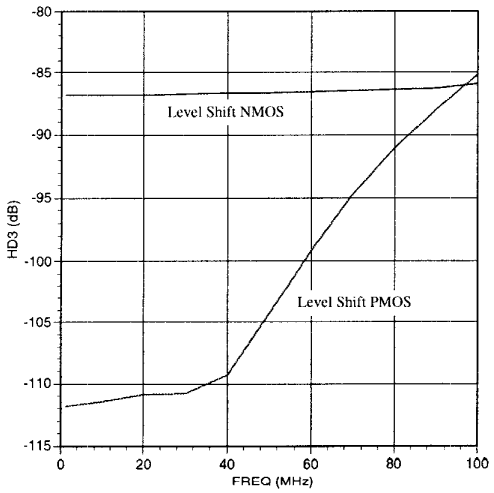

Figure 2. Third harmonic amplitude as a function of the input signal frequency for NMOS and PMOS level-shifters

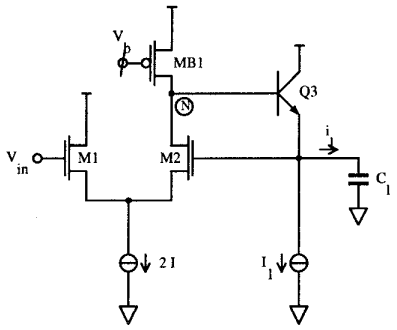

Figure 3. Schematic of the buffer with local-loop [2]

3. BiCMOS SOLUTION

A possible improvement to the simple level-shifter is shown in Fig. 3 [2]. The output of the buffer is achieved with a bipolar follower, Q3 and the current source I1. The output impedance is low because of the high transconductance of the bipolar transistor and the local feedback. High input impedance results from the use of an input MOS device. The BiCMOS technology used provides fast NPN transistors (the PNP are significantly slower). We therefore used n-channel MOS devices. The structure provides the following advantages:

- thanks to the feedback loop, the distortion at emitter Q3 is divided by the gain of the feedback
- the use of a bipolar device (Q3) allows us to increase the speed of the level-shifter
- the threshold voltage modulation (Body Effect) of M1 is not important as it is compensated by the equivalent modulation of M2.

Unfortunately, the above advantages do not produce significant improvements in harmonic distortion. In fact, circuit simulations lead to the results shown in Table 3. The performance is better, especially at low frequencies, than for a simple NMOS level-shifter, but it is similar or worse than the performance of a PMOS level-shifter. Since this result shows that the third harmonic component is not significantly better than in a simple source follower we can argue that, at the required level of harmonic distortion, performance is dominated by higher order effects. A careful analysis leads to a given number of possible limits.

	1 MHz	100 MHz
HD_2	-71 dB	-61 dB
HD_3	-113 dB	-87 dB
HD_4	-122 dB	-110 dB

Table 3. Circuit in Fig. 3: harmonic distortions

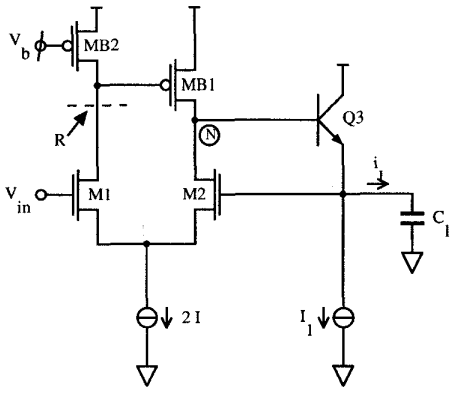

Figure 4. Schematic of the improved local-loop buffer

They are:

- the swing on node N modulates the small-signal output resistance of transistor MB1, r_{ds}, leading to a distortion contribution [3]
- the signal current i_l/β flows into the input stage, M1 and M2. This generates a difference, ΔV_{gs}, between their gate-to-source voltages, which produces distortion
- the gain β of Q3 is not constant but is a function of V_{ce}; thus worsening the above source of distortion

These three drawbacks are attenuated by introducing an internal loop to the input stage (Fig. 4) [4]. The feedback loop reduces the output resistance of MB1 and, consequently, its distortion. Moreover, the base current of the bipolar transistor i_l/β mainly comes from MB1. Therefore the currents in the pair M1 and M2 do not change significantly. This attenuates the second problem. Finally, the third limit is reduced because the second limit is attenuated. The simulation of the circuit leads to the results shown in Table 4. They confirm an improvement to linearity especially at low frequencies. At high frequencies behavior is better than in the previously discussed structures. However, the limited speed of the control feedback loop, leads to a limited -96 dB third harmonic distortion.

An alternative solution that reduces the signal current flowing through the input stage includes a Darlington structure [1]. As known, this allows the current required to be diminished by β. This circuit is shown in Fig. 5.

	1 MHz	100 MHz
HD_2	-78 dB	-66 dB
HD_3	-116 dB	-96 dB
HD_4	-140 dB	-116 dB

Table 4. Circuit in Fig. 4: harmonic distortions

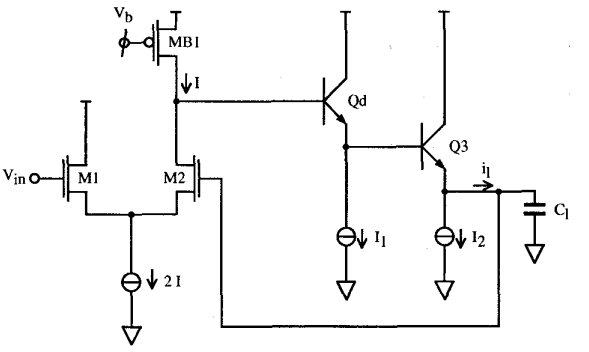

Figure 5. Schematic of local-loop buffer with a Darlington output stage

Simulation results show that the structure exhibits excellent linearity. Nonetheless, the first limit listed above persists. Moreover, the Darlington transistor reduces the voltage V_{ds} of MB1 by a diode. Thus, the Darlington solution shows an high-linearity but with a limited dynamic range at the input.

4. GLOBAL FEEDBACK SOLUTION

The previous sections discussed circuit solutions where the feedback is only used locally. Our objective is to improve linearity while maintaining high speeds. A global feedback solution is normally not suitable because high complexity leads to significant bandwidth limits. Nevertheless, modern BiCMOS technologies provide features that allow the global feedback solution to be reconsidered. One such scheme including some of the tricks discussed above is shown in Fig. 6. It is a two stage op-amp in unity gain configuration. The input stage is a PMOS pair with a BJT current mirror as active load; the output stage is a Darlington structure. Therefore, as for the topology in Fig. 5, the input base current, the main factor responsible for the input stage distortion, is divided by a factor of β.

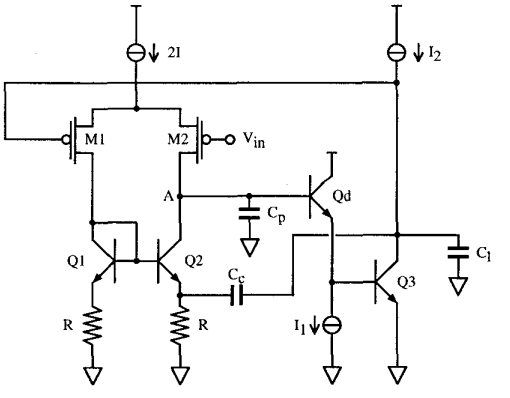

Figure 6. Schematic of the proposed PMOS-input buffer

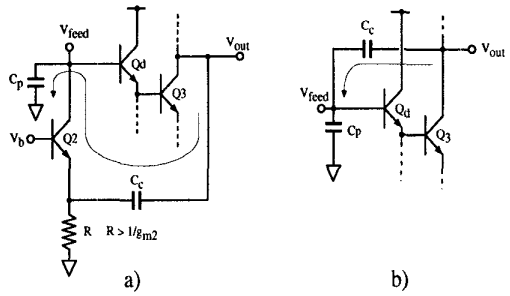

Figure 7. Compensation principle: a) Miller approach; b) proposed approach

Further advantages of the scheme are the following:

- the bipolar devices in the current mirror do not suffer from significant r_{ce} modulation even in the presence of a reduced V_{ce}
- thanks to the second gain stage, the signal at node A is very small, thus the distortion of the first stage is minimized
- because of the relatively high gain the input differential voltage is quite low; so that the nonlinear responses of M1 and M2 are almost compensated
- the use of a p-channel input permits well balanced dc biasing: the drop voltage across the current sources is well above the saturation limit, with benefits to the r_{ds}.

Since we use a two stage amplifier frequency compensation must be taken into account. To keep the bandwidth high even under significant capacitive loads, we used the technique proposed in [5]. The capacitive compensation current is injected into the output node of the first stage through the "virtual ground" established by the emitter of Q2. This current, integrated over the parasitic capacitance C_p determines a feedback voltage equal to $V_{out}C_c/C_p$ (Fig. 7a). This contrasts with the classical Miller approach, because to the parasitic C_p, the feedback voltage is only a fraction of the output signal (Fig. 7b). Although unity gain frequency is the same for the two compensation schemes, the circuit in Fig. 6 can drive high capacitive loads.

The use of a p-channel input transistor allows us to connect the well to the source (for n-well technologies). The circuit in Fig. 6 does not use this option because of speed limitations. We know that the threshold modulation of M1 and M2 compensate each other thanks to the differential topology. In addition, the distortion contribution of the non-linear capacitance C_{bd} is cancelled as well. Table 5 shows the simulated results. The values achieved for HD_3 are excellent and reflect the many tricks used in the circuit schematic and in the optimization design. Fig. 8 show the response to a step input with 0.5 V amplitude. The result given leads to an estimation of the settling time within an accuracy of $1/2^{16}$ as low as 3 ns. Therefore, demanding requests for high speed T&H to be used in data communication handling can be fulfilled.

	1 MHz	100 MHz
HD_2	-86 dB	-68 dB
HD_3	-115 dB	-105 dB
HD_4	-135 dB	-116 dB

Table 5. Circuit in Fig. 6: harmonic distortions

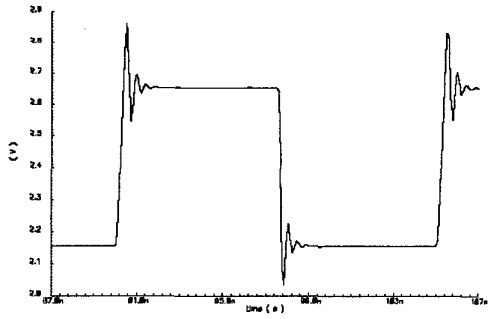

Figure 8. Step response of the proposed output buffer

5. CONCLUSION

Guidelines for the design of high speed output buffers with improved linearity were discussed. Various solutions of increasing complexity were presented, thus offering the designer the proper strategy for achieving given harmonic distortions. The most complex solution is a buffer with global feedback. A number of design tricks allowed third order linearity better than -105 dB with a 100 MHz, 0.5 V_{pp} input signal, to be achieved using a conventional 0.8 µm BiCMOS process. The settling time required to achieve a 0.01% accuracy was below 3 ns.

6. REFERENCES

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