# High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes

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**Single-walled carbon nanotubes (SWNTs) have many exceptional electronic properties. Realizing the full potential of SWNTs in realistic electronic systems requires a scalable approach to device and circuit integration. We report the use of dense, perfectly aligned arrays of long, perfectly linear SWNTs as an effective thin-film semiconductor suitable for integration into transistors and other classes of electronic devices. The large number of SWNTs enable excellent device-level performance characteristics and good device-to-device uniformity, even with SWNTs that are electronically heterogeneous. Measurements on p- and n-channel transistors that involve as many as ~2,100 SWNTs reveal device-level mobilities and scaled transconductances approaching ~1,000 $cm^2 V^{-1} s^{-1}$ and ~3,000 $S m^{-1}$, respectively, and with current outputs of up to ~1 A in devices that use interdigitated electrodes. PMOS and CMOS logic gates and mechanically flexible transistors on plastic provide examples of devices that can be formed with this approach. Collectively, these results may represent a route to large-scale integrated nanotube electronics.**

Fundamental studies of charge transport through individual SWNTs reveal remarkable room-temperature properties, including mobilities more than ten times larger than silicon, current-carrying capacities as high as $10^9$ A $cm^{-2}$ and ideal subthreshold characteristics in single-tube transistors[1–4]. The implications of these behaviours could be significant for many applications in electronics, optoelectronics, sensing and other areas[5–9]. Devices that use single SWNTs as functional elements might not, however, form a realistic basis for these technologies, due in part to their low current outputs and small active areas. More importantly, integration of single tube devices into scalable integrated circuits requires a solution to the very difficult problem of synthesizing and accurately positioning large numbers of individual, electrically homogeneous tubes with linear geometries. The use of densely packed, perfectly aligned horizontal arrays of non-overlapping linear SWNTs as an effective thin-film electronic material has the potential to avoid these problems while retaining the attractive properties of the individual tubes. The multiple, parallel transport pathways in these arrays provide large current outputs and active areas, together with statistical averaging effects that lead to small device-to-device variations in properties, even with tubes that individually have widely different transport characteristics. Although theoretical work has examined some of the anticipated electrical properties of such arrays[10,11], experimental results are lacking[12–14], owing to difficulties associated with generating dense, large-scale, aligned SWNTs at the extremely high degrees of alignment and linearity needed to avoid percolating transport pathways, tube/tube overlap junctions, electrostatic screening effects and non-ideal electrical properties[15–17]. This paper presents high-performance p- and n-channel transistors and unipolar and complementary logic gates that use perfectly aligned arrays of long, pristine, individual SWNTs with perfectly linear geometries. The excellent properties of the devices derive directly from a complete absence, to within experimental uncertainties, of any defects in the arrays, as defined by tubes or segments of tubes that are misaligned or have nonlinear shapes. This level of perfection represents several orders of magnitude improvement over previous results[12,18–20]. Analysis of measurements on these devices using rigorous models of the capacitance coupling of the arrays to the gate electrodes reveals device-level properties that approach those of pristine individual tubes. These features, together with the ability of these devices to provide both p- and n-type operation and CMOS circuit designs, and their compatibility with a range of substrates, suggest that these approaches have some promise for realistic SWNT-based electronic and optoelectronic technologies.

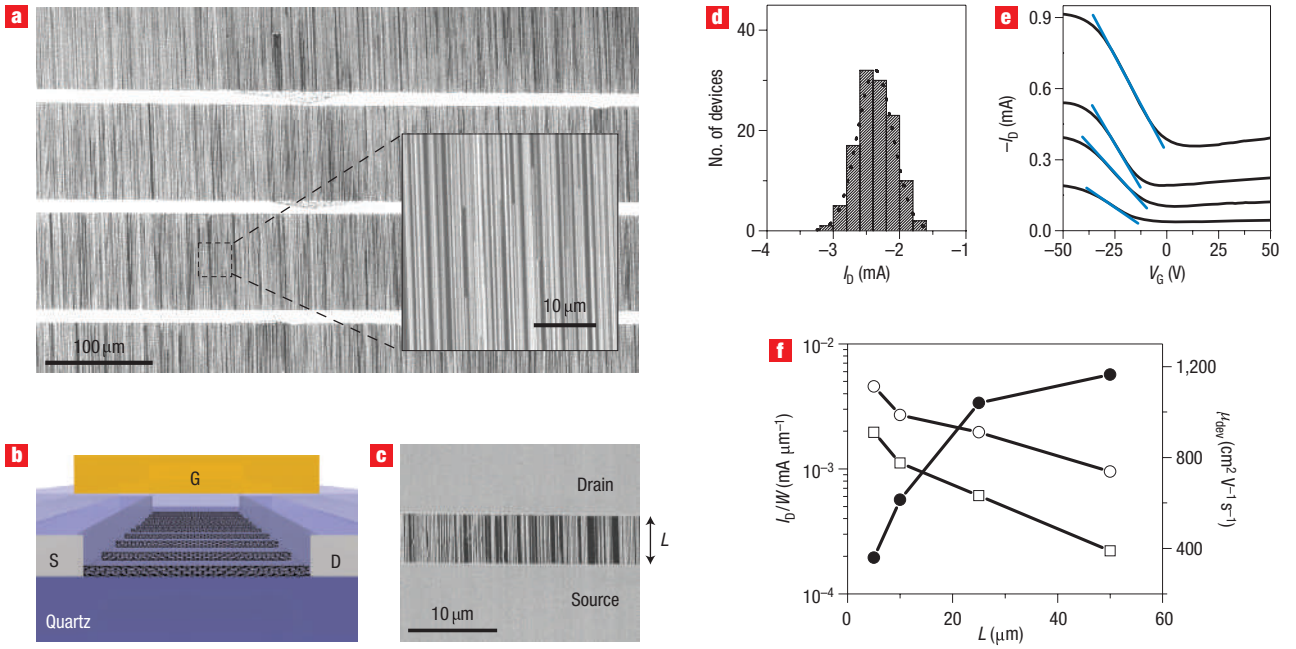


**Figure 1 Perfectly aligned arrays of long, linear SWNTs and their implementation in thin-film-type transistors. a**, SEM image of a pattern of perfectly aligned, perfectly linear SWNTs formed by CVD growth on a quartz substrate. The bright horizontal stripes correspond to the regions of iron catalyst. The inset provides a magnified view. These arrays contain ~5 SWNTs μm$^{-1}$. **b**, Schematic illustration of the layout of a type of transistor that incorporates these aligned SWNTs as the semiconductor. The device uses source (S), drain (D) and gate (G) electrodes, and a dielectric layer formed sequentially on top of the SWNTs on quartz. **c**, SEM image of the channel region of such a device. The distance between the source and drain electrodes defines the channel length ($L$). **d**, Output currents ($I_D$) measured on more than 100 two-terminal test structures using electrodes with widths, $W$, of 200 μm and separated by distances (that is, channel lengths, $L$) of 7 μm, evaluated with an applied potential, $V_D$, of 10 V. **e**, Transfer curves ($I_D$ as a function of gate voltage, $V_G$) measured from transistors with $L = 5$, 10, 25 and 50 μm, from top to bottom, and $W = 200$ μm at $V_D = -0.5$ V. The blue lines indicate the linear regions of the transfer curves. These devices used polymer gate dielectrics, with thickness of ~1.5 μm. **f**, Width-normalized on and off currents (open circles and squares, respectively, left axis) and linear-regime device mobilities (solid circles, $\mu_{dev}$, right axis) as a function of $L$.

## FABRICATION OF NANOTUBE ARRAYS AND DEVICES

Figure 1 shows scanning electron microscope (SEM) images of representative arrays of SWNTs, SEM images and schematics of their integration into transistors, and some electrical properties. Chemical vapour deposition (CVD) on ST (stable temperature) cut quartz wafers using patterned stripes of iron catalyst and methane feed gas forms arrays of individual SWNTs with average diameters of ~1 nm, lengths of up to 300 μm, and densities ($D$) approaching ~10 SWNTs μm$^{-1}$. More than 99.9% of the SWNTs lie along the [2$\bar{1}\bar{1}$0] direction of the quartz, to within $<0.01^\circ$, with perfectly linear configurations, within the measurement resolution of an atomic force microscope[12]. (Fig. 1a; see also Supplementary Information, Fig. S1). This nearly ideal layout, in particular as obtained at high $D$, is critically important to the device results presented here, and represents a significant improvement over previously reported results[18–20]. The simplest method to integrate these arrays into transistors begins with photolithography to define source and drain electrodes (Ti, 1 nm/Pd, 20 nm) on the SWNT/quartz substrates in regions between the catalyst stripes. Etching SWNTs outside the channel region, spin casting a uniform epoxy gate dielectric (1.5 μm) and photolithographically defining top gate electrodes (Ti, 1 nm/Au, 20 nm) aligned to the channel regions yields arrays of electrically isolated transistors. Figure 1b,c shows a schematic illustration and image. We formed devices in this manner with channel lengths ($L$) between 5 and 50 μm, all with widths ($W$) of 200 μm. For these geometries, each device incorporates ~1,000 perfectly linear parallel SWNTs in the channel, most of which (for example, >80%, even for $L = 50$ μm) span the source/drain electrodes. This large number of active tubes per device provides high current outputs and good statistics for uniform reproducible properties. Figure 1d presents measurements that show a ~10% standard deviation in source/drain currents, $I_D$, measured in more than 100 two-terminal test structures (source/drain voltage, $V_D = 10$ V; $L = 5$ μm; $W = 200$ μm). We observe high yields both for growing the arrays and for building devices that incorporate them (see Supplementary Information, Figs. S1 and S2).

Figure 1e shows typical transfer characteristics measured from a set of devices. The responses indicate p-channel behaviour, consistent with observations in single-tube devices that use similar materials and designs (see Supplementary Information, Fig. S3). The large current outputs are consistent with the high channel conductance provided by the multiple tubes. These currents vary approximately linearly with the channel length, indicating diffusive transport, with ratios of the on and off currents in a range (between ~2.3 and ~5) consistent with the relative populations of metallic and semiconducting SWNTs (see Supplementary Information, Figs. S1 and S4). Resistances of the semiconducting tubes in their 'on' state (that is, biased to gate voltages, $V_G$, of −50 V), are $36 \pm 10$ kΩ μm$^{-1}$ for $L = 50$ μm, where the effects of contacts are least significant. Single-tube device results, computed using reported diameter-dependent resistances[1] and diameter distributions measured from these arrays (see Supplementary Information, Fig. S1), yield a resistance of ~21 kΩ μm$^{-1}$. Similar calculations for the metallic tubes in these

devices yield higher and lower resistances in the low- and high-bias regimes, respectively, than the best single-tube device measurements[14,21–23] (see Supplementary Information, Figs. S4–S6).

## CAPACITANCE COUPLING AND MOBILITY CALCULATIONS

The low on-state resistances of the semiconducting tubes yield excellent device-level transistor properties. Figure 1f presents linear-regime device mobilities as a function of channel length, computed from the transfer curves, the physical widths of the source/drain electrodes ($W = 200\,\mu m$), and a parallel plate model for the capacitance, $C$, according to $\mu_{dev} = (L/WC)(1/V_D)\partial I_D/\partial V_G$. These mobilities are as high as $\sim$1,100 $cm^2\,V^{-1}\,s^{-1}$ for $L > 25\,\mu m$, decreasing with $L$, likely owing to effects of contacts[1,24,25] that are not considered explicitly in these calculations. The validity of this simple parallel plate model for the capacitance can be explored through measurements and calculations for devices having different values of $D$. Figure 2a,b presents SEM images of SWNT arrays with $D$ between $\sim$0.2 SWNTs $\mu m^{-1}$ and $\sim$5 SWNTs $\mu m^{-1}$, obtained by controlling the growth conditions. The responses of devices built with these arrays and with single tubes are similar to those in Fig. 1 (see Supplementary Information, Figs. S3 and S7). The influence of fringing fields and partial electrostatic screening by the tubes on the capacitance, $C$, are important in this range of tube spacing and gate dielectric thickness[10,11]. Figure 2c,d presents results of calculations that include these effects, the quantum nature of the tubes and their intrinsic capacitance for $D = 5$ SWNTs $\mu m^{-1}$, where screening is dominant, and for $D = 0.2$ SWNTs $\mu m^{-1}$, where it is small. In the former regime, the calculated $C$ differs, only by $\sim$10%, from that determined by a simple parallel plate model. In the latter case, the capacitance coupling to each individual tube is nearly the same as that for isolated tubes (see Supplementary Information, Figs. S8 and S9).

Such models enable calculations of the average per tube mobilities, which we denote as $\langle\mu_t\rangle$, according to $\langle\mu_t\rangle = (L/WC_tD_s)(1/V_D)\partial I_D/\partial V_G$ where $C_t$ is the capacitance per unit length for a semiconducting tube in the array (computed using $D$), and $D_s$ is the density of semiconducting tubes that span the channel. For $L = 50\,\mu m$ and $D = 5$ SWNTs $\mu m^{-1}$, $\langle\mu_t\rangle \approx 2{,}200 \pm 130\,cm^2\,V^{-1}\,s^{-1}$, if we assume that approximately two out of three of the SWNTs in the channel are semiconducting and that $\sim$80% of them span the source and drain electrodes. As with the device mobility, the per tube mobility (as computed in a manner that does not account for the contacts) decreases with channel length (for example, $\sim$570 $cm^2\,V^{-1}\,s^{-1}$, $L = 5\,\mu m$), which is qualitatively consistent with expectations based on reports on single-tube devices[1,24–26]. Averaging the diameter-dependent mobilities inferred from single-tube devices[1], weighted by the measured distribution of tube diameters in the arrays (see Supplementary Information, Fig. S1d), yields $\sim$3,000 $cm^2\,V^{-1}\,s^{-1}$ if we assume that most of the 3–4 nm tubes are small bundles ($\sim$4,300 $cm^2\,V^{-1}\,s^{-1}$ without this assumption). This value is only somewhat higher than the results determined from measurements on the array devices. An analysis of per tube mobilities in devices with various tube densities at $L = 10\,\mu m$, where the effects of contacts are significant, yields $\langle\mu_t\rangle \approx 800 \pm 100\,cm^2\,V^{-1}\,s^{-1}$, with a negligible systematic dependence on $D$. Similar mobility values are observed in single-tube devices (see Supplementary Information, Fig. S3).

## HIGH-PERFORMANCE NANOTUBE ARRAY DEVICES

Although the devices of Figs. 1 and 2 have high mobilities, their on/off ratios are modest, owing to the presence of metallic tubes,

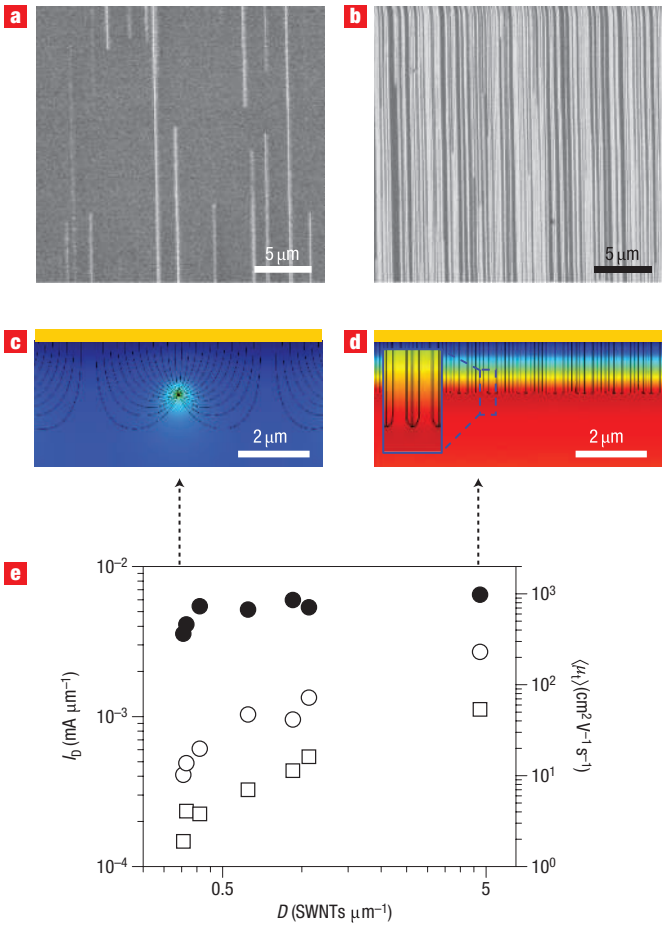


**Figure 2 Capacitance effects and density scaling studies of transistors that use aligned arrays of SWNTs. a**,**b**, SEM images of an array of aligned SWNTs with $\sim$0.2 SWNTs $\mu m^{-1}$ (**a**) and $\sim$5 SWNTs $\mu m^{-1}$ (**b**). **c**,**d**, Colour contour plots and electric field lines for the computed electrostatic coupling of a gate electrode (top yellow plate) through a dielectric layer to an array of SWNTs with low density (that is, average spacing between the SWNTs is larger than the gate dielectric) (**c**), and with high density (average spacing between the SWNTs is smaller than the gate dielectric) (**d**). The results in **c** and **d** show field distributions that are similar to those associated with an isolated tube and a parallel plate, respectively. **e**, Width-normalized on and off currents (open circles and squares, respectively, left axis) measured in transistors built with arrays of SWNTs with different densities, $D$. The thickness of the gate dielectric was $\sim$1.5 μm. The plot also shows the average per tube mobilities (filled circles, $\langle\mu_t\rangle$, right axis) computed from transfer curves measured from these devices.

and their transconductances are low, owing to the use of low-capacitance gate dielectrics. The on/off ratios can be improved by destroying the metallic tubes in a breakdown procedure that involves slowly increasing $V_D$, while holding $V_G$ at a large positive value (Fig. 3a; see also Supplementary Information, Fig. S10) in a manner similar to previous demonstrations on random-network and multiwalled nanotube devices[15,27]. To implement this procedure, the SWNT arrays were first transferred, with high yields (see Supplementary Information, Figs. S10–S12), onto a substrate of epoxy (150 nm)/$SiO_2$ (100 nm)/Si, using an adaptation of previously reported techniques[28–30]. The epoxy/$SiO_2$ bilayer and Si provided the gate dielectric and gate, respectively, in a back-gate geometry that leaves the SWNTs exposed to air to facilitate the breakdown

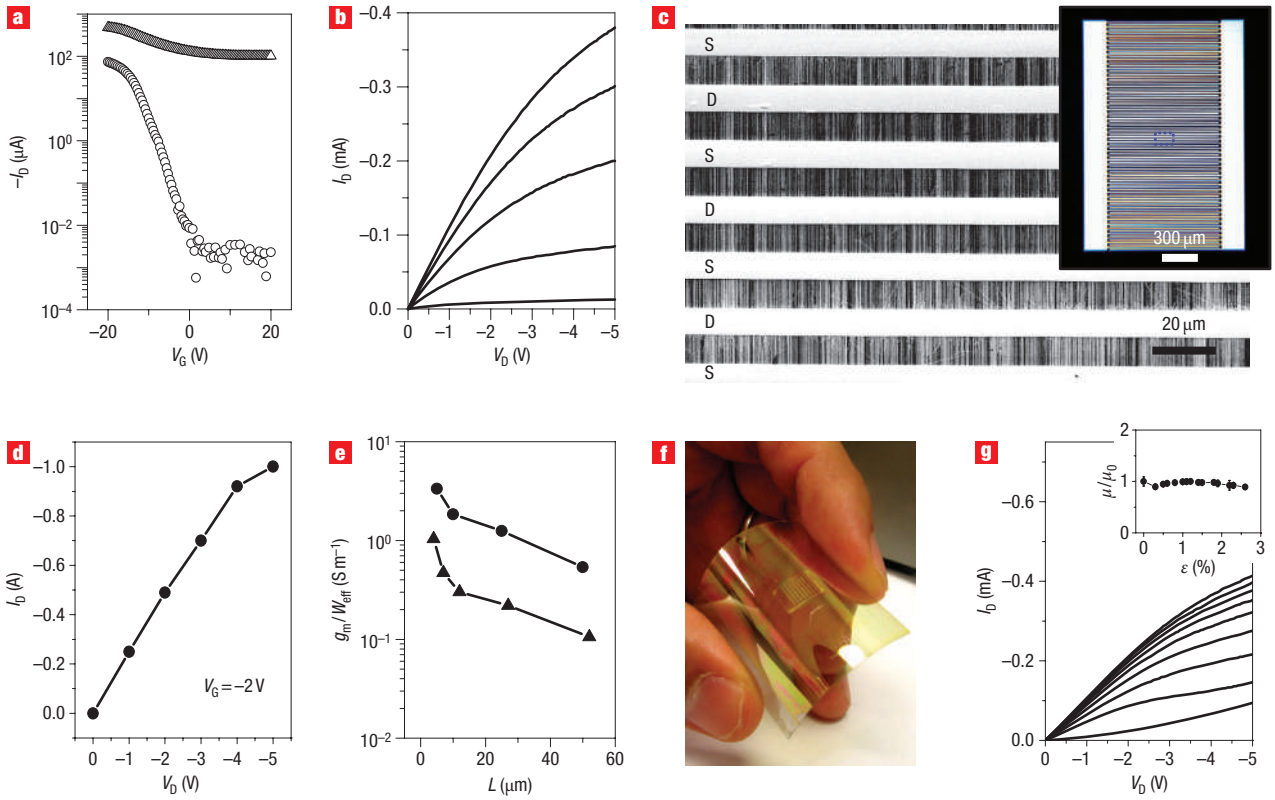


**Figure 3 High on/off ratios, current outputs and transconductances in transistors that use aligned arrays of SWNTs as the semiconductor, on rigid and flexible substrates. a**, Transfer curves from a transistor ($L = 12$ μm, $W = 200$ μm) that uses aligned arrays of SWNTs ($D = 4$ SWNTs μm$^{-1}$) transferred from the quartz growth substrate to a doped silicon substrate with a bilayer dielectric of epoxy (150 nm)/$SiO_2$ (100 nm). The data correspond to measurements on the device before (open triangles) and after (open circles) an electrical breakdown process that eliminates metallic transport pathways from source to drain. This process improves the on/off ratio by a factor of more than 10,000. **b**, Full current/voltage characteristics of the same device, measured after breakdown, illustrating a well-behaved response. The gate voltage varies from −5 V to 5 V (top to bottom). **c**, Optical (inset) and SEM images of a transistor that uses interdigitated source and drain electrodes, in a bottom gate configuration with a gate dielectric of $HfO_2$ (10 nm) on a substrate and gate of Si. The width and length of the channel are 93 mm and 10 μm, respectively. The box indicated by the dashed blue lines in the optical image inset delineates the region shown in the SEM image. **d**, Output current ($I_D$) as a function of $V_D$ at $V_G = -2$ V, for the device shown in **c**. High on currents (up to ~1 A) can be obtained. **e**, Transconductance per unit effective width ($g_m/W_{eff}$) as a function of channel length ($L$), for devices ($D = 2$ SWNTs μm$^{-1}$) that use a polymer electrolyte gate (solid circles, $V_D = -0.5$ V) and a 10-nm $HfO_2$ (solid triangles, $V_D = -0.5$ V) gate dielectric, respectively. **f**, Optical image of an array of SWNT transistors with $D = 3$ SWNTs μm$^{-1}$ on a flexible plastic substrate (PET), and $L = 27$ μm and $W = 200$ μm. **g**, Current/voltage characteristics of a typical device. The gate voltage varies from −20 V to 20 V (top to bottom). The linear-regime field-effect mobility was ~480 cm$^2$ V$^{-1}$ s$^{-1}$, representing the highest p-channel mobility reported for a device on plastic. The inset shows the variation of the normalized mobility as a function of bending-induced strain, down to a radius of curvature of 0.4 cm. Beyond this degree of bending, failure occurs due to fracture of the gate electrode.

process. Transfer curves in Fig. 3a, collected before and after this process for a typical case of $D = 4$ SWNTs μm$^{-1}$ ($L = 12$ μm, $W = 200$ μm, $V_D = -0.5$ V), demonstrate that the on/off ratios can be increased by four orders of magnitude, or more, in this manner. Figure 3b shows full current/voltage characteristics recorded after breakdown. The response is consistent with a well-behaved device (that is, saturated and linear current outputs for $V_D \gg V_G$ and $V_D \ll V_G$, respectively), offering large current output even with low operating voltages (selected to avoid hysteresis) and the low-capacitance dielectrics used here. The differences in threshold voltages observed in Fig. 3a,b result from hysteresis that occurs at the high voltages associated with measurements in Fig. 3a.

Increasing the capacitance of the gate dielectric improves the transconductance and eliminates the hysteresis. These aspects, as implemented in devices described in the following, also increase the voltage gain by more than one order of magnitude. In addition, extremely high current outputs can be obtained in this manner, especially in devices that use interdigitated source and drain electrodes to increase $W$. Figure 3c,d shows images and electrical responses of such a device that uses an array of SWNTs ($D = 7$ SWNTs μm$^{-1}$) transferred onto a substrate of $HfO_2$ (10 nm)/Si, where the $HfO_2$ serves as the gate dielectric and the Si provides the gate. In such a device, each SWNT in the array is active at multiple separate segments along its length, similar to related demonstrations in single-tube systems[31]. For this device, the output current reaches ~1 A at $V_G = -2$ V and $V_D = -5$ V, as illustrated in Fig. 3d. The transconductance ($g_m$), computed using an effective width ($W_{eff}$) defined by the summed widths of the SWNTs that are active in the device, in a manner analogous to similar analyses of single-tube devices[31], can also be high in such devices. Figure 3e shows results from devices that use slightly lower tube densities ($D = 2$ SWNTs μm$^{-1}$), non-interdigitated electrodes and various channel lengths. The peak values of

transconductances scaled in this manner are $\sim$800 S m$^{-1}$ (at $V_D = -0.5$ V, $L = 7$ μm) with $HfO_2$ (10 nm) dielectrics, and up to $\sim$ 3,000 S m$^{-1}$ (at $V_D = -0.5$ V, $L = 5$ μm) with polymer electrolyte gating[32].

The transfer process used for these devices also enables integration onto unusual substrates, including flexible plastics. As an example, Fig. 3f,g shows an image and electrical characteristics of devices ($D = 3$ SWNTs μm$^{-1}$) on a sheet of poly(ethylene terephthalate) (180 μm), where polyimide (1.6 μm) and indium tin oxide (150 nm) provide the gate dielectric and gate, respectively, with $L = 27$ μm and $W = 200$ μm. The linear-regime mobility, computed using a parallel plate approximation for the capacitance, is $\sim$ 480 cm$^2$ V$^{-1}$ s$^{-1}$. The inset of Fig. 3g shows the normalized mobility as a function of bending induced strain ($\varepsilon$) for bending down to radii of curvature of 0.4 cm. At higher values of strain, the devices fail owing to fracture of the gate electrode.

Many of the exceptional electrical properties can be obtained, at once, in suitably designed devices. Figure 4 provides optical micrographs and electrical measurements of such devices, formed on quartz growth substrates in top gate geometries similar to the devices of Figs. 1 and 2, but with high-capacitance dielectrics and with split gate electrodes aligned to the transistor channel to avoid parasitic overlap capacitances for high-speed operation. The dielectric consists of a bilayer of $HfO_2$ ($\sim$10 nm) deposited by atomic layer deposition, on top of a layer of benzocyclobutene (BCB, $\sim$20 nm) spin-cast on the SWNTs. Figure 4a–c shows several devices that use arrays with $D = 7$ SWNTs μm$^{-1}$. The design enables high-speed (radio frequency, RF) operation, and provides electrode pad layouts in the ground–signal–ground configuration to facilitate RF probing. The mobilities can be computed using the parallel plate model for the capacitance or using rigorous calculations similar to those for $\langle\mu_t\rangle$, but which also include capacitance contributions from the metallic tubes. Figure 4d shows the results, along with the average per tube mobility, from measurements on 15 devices. The high mobilities and scaling behaviours are quantitatively similar to those of the devices in Fig. 1. The on resistances of the semiconducting tubes are also similar, at $\sim$ 40 kΩ μm$^{-1}$. The current outputs are high; they scale linearly with $W$, and in an expected manner with $L$. Figure 4e,f presents these results. The high-capacitance gate dielectrics lead to transconductances scaled by $W_{eff}$ as high as $\sim$2,900 S m$^{-1}$, as shown in Fig. 4g. Behaviours in the upper end of the range for all of these properties are achieved in devices with $L = 4$ μm and $W = 600$ μm, where, for example, the mobility, scaled transconductance and current output are 400 $\pm$ 50 cm$^2$ V$^{-1}$ s$^{-1}$ (using the parallel plate capacitance, $\sim$160 nF cm$^{-2}$), $\sim$3,000 S m$^{-1}$ and 8 mA, respectively. The mobility is 800 $\pm$ 100 cm$^2$ V$^{-1}$ s$^{-1}$ when evaluated using the rigorous models for the capacitance ( $\sim$ 70 nF cm$^{-2}$). These devices also have a strong potential for high-speed operation. Measurements using a network analyser indicate small signal gain up to frequencies ($f_T$) approaching 0.5 GHz, evaluated without any de-embedding (see Supplementary Information, Fig. S14).

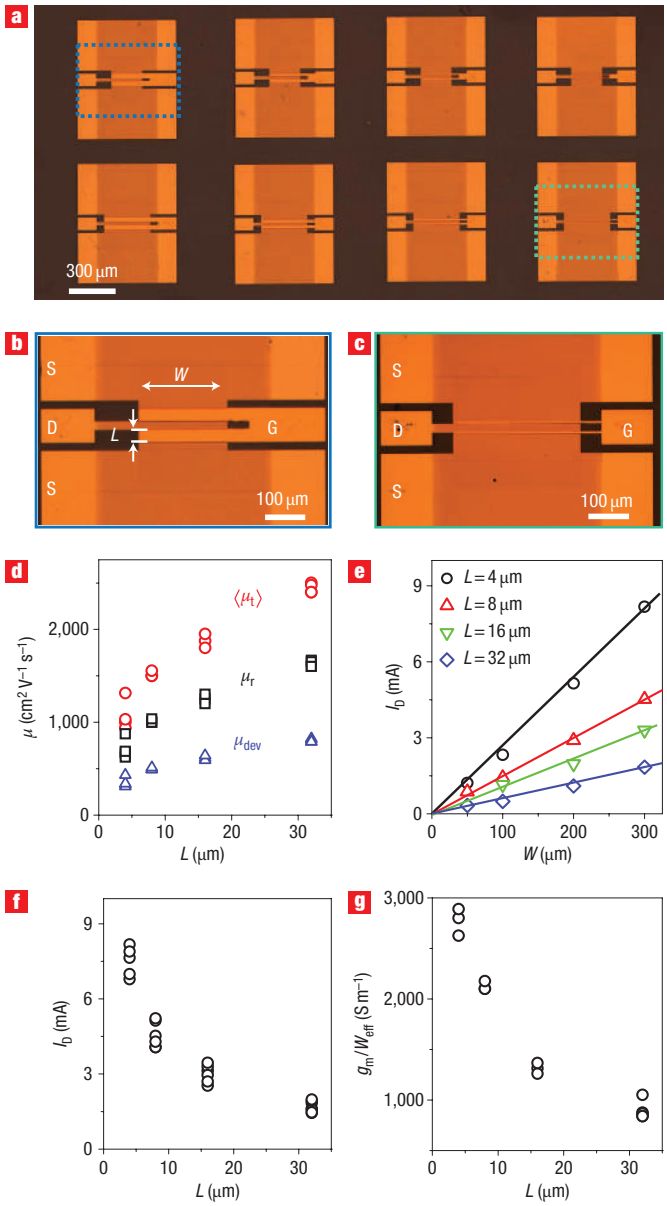


**Figure 4 High-performance top gate transistors that use aligned arrays of SWNTs for the semiconductor. a**, Optical micrograph showing an array of eight transistors that use SWNT arrays for the semiconductor, the quartz growth wafer as the substrate, high-capacitance bilayer gate dielectrics of BCB (20 nm)/$HfO_2$ (10 nm) and split gate electrodes aligned to the channels of the devices. **b**, Optical micrograph of a device with $L = 32$ μm and $W = 200$ μm, corresponding to the box indicated by the dashed blue line in the left portion of part **a. c**, Optical micrograph of a device with $L = 4$ μm and $W = 300$ μm, corresponding to the box indicated by the dashed green line in the right portion of part **a. d**, Mobilities computed using parallel plate ($\mu_{dev}$, blue triangles) and rigorous ($\mu_r$, black squares) models for the capacitance coupling between the gate electrode and the SWNT arrays. The plot also shows the average per tube mobilities ($\langle\mu_t\rangle$, red circles). **e**, Output currents, $I_D$ ($V_D = -1$ and $V_G = -1$ V), for devices with $L = 4$, 8, 16 and 32 μm at $W =$ 50, 100, 200 and 300 μm. **f**, Output currents, $I_D$ ($V_D = -1$ and $V_G = -1$ V), for 18 devices with $L$ between 4 and 32 μm. **g**, Scaled transconductances ($g_m/W_{eff}$) for 15 devices with $L$ between 4 and 32 μm.

## COMPLEMENTARY DEVICES AND LOGIC GATES

As illustrated in Fig. 5a–c, coating the devices with polyethyleneimine (PEI)[15,33] enables n-channel operation, similar to observations in single-tube devices[33]. These results provide straightforward means to form complementary and unipolar logic gates (inverters), and other circuit elements. Figure 5d shows a PMOS inverter that uses an SWNT-array-based p-channel transistor (response shown in Fig. 5b) as the drive and an array of SWNTs, partially processed by electrical breakdown, as the load. Combining n- and p-channel devices yields CMOS inverters, as illustrated in Fig. 5e. The gains observed in the PMOS and CMOS inverters were 2.75 and 1.8, respectively, as

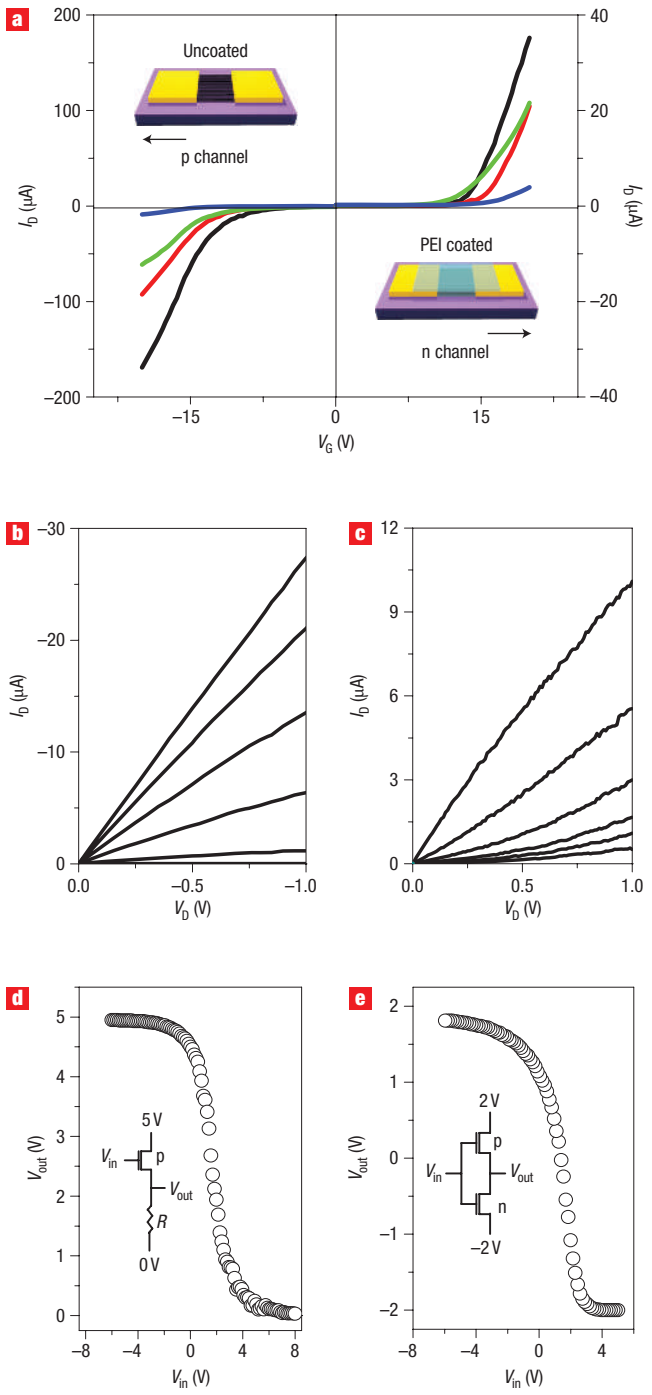


**Figure 5 n- and p-type SWNT array transistors, with implementation in CMOS and PMOS logic gates. a**, Transfer curves of p- and n-channel transistors that use aligned arrays of as-fabricated and PEI-coated arrays of SWNTs, respectively. All devices were processed using electrical breakdown to achieve high on/off ratios. In the case of the n-channel devices, this process was performed before PEI coating. $L = 4$ μm, black; $L = 7$ μm, red; $L = 12$ μm, green; $L = 27$ μm, blue; $V_D = -0.5$ V. **b**. Current/voltage response of a typical p-channel device in a regime of small $V_D$ ($V_G = \sim 5$ V to $-5$ V). **c**, Similar results from an n-channel device. ($V_G = \sim 0$ V to 5 V). **d**, Transfer curve from a PMOS inverter that uses an SWNT-array transistor for the drive, and a two-terminal device with SWNT arrays for the resistive load. The gain of the PMOS inverter is 2.75. The inset provides a circuit schematic. **e**, Similar information for a CMOS inverter that combines p- and n-channel SWNT-array transistors. The gain of the CMOS inverter is 1.8.

measured at $V_{DD} = 5$ V for the PMOS device and $V_{DD} = \pm 2$ V for the CMOS device. Taken together, these and the other results presented in this paper indicate a scalable path to SWNT-based thin-film electronics, with high-performance capabilities. Initial applications might be envisioned in areas that require unusual substrates (for example plastics), such as flexible displays or conformal structural health monitors, or optical transparency, such as in heads-up displays and certain security devices. The high-performance attributes, combined with the possibility of direct integration with silicon, also create interest in the possible use of nanotube array devices with Si CMOS for enhanced operation (for example, power-handling capabilities, linear-response or high-speed operation). The array geometry should also be useful for a range of other applications, which currently exist only in the form of single-tube demonstrations. Examples include light-emitting diodes, photodetectors, chemical sensors, nanoelectromechanical oscillators, and electrically or thermally conductive elements. These and other related systems appear promising for future study.

## METHODS

### GROWTH OF PERFECTLY ALIGNED ARRAYS OF LONG, LINEAR SWNTs

CVD procedures were used to grow SWNTs on ST cut quartz wafers (Hoffman), which were annealed at 900 °C in air for 8 h. The first step of the growth process involved photolithography to open lines ($W = 10$ μm and $L = 1$ cm) in a layer of photoresist (AZ 5214) on the quartz, followed by electron beam evaporation ($3 \times 10^{-6}$ torr; Temescal CV-8) of Fe (Kurt J. Lesker; 99.95%) to a nominal thickness of $<0.5$ nm. Lifting off the photoresist with acetone left a pattern of Fe lines. Annealing the Fe at 550 °C in air formed isolated iron oxide nanoparticles with diameters near ~1 nm. The particles served as the catalytic seeds for CVD growth of the SWNTs. Purging with hydrogen at 900 °C for 5 min and then introducing a flow of methane (1,900 s.c.c.m.) and hydrogen (300 s.c.c.m.) at 900 °C for 1 h led to the growth of SWNTs (see Supplementary Information, Fig. S2, for the reproducibility of this growth technique).

### FABRICATION OF TOP AND BOTTOM GATE TRANSISTORS

To make top gate transistors on the quartz growth substrates, Ti (1 nm)/Pd (20 nm) (electron beam evaporated at $3 \times 10^{-6}$ torr; Temescal CV-8) source/drain electrodes were formed by photolithography and lift-off. For device isolation, these electrodes and the channel region were covered with photoresist, the exposed tubes were removed by reactive ion etching (50 mtorr, 20 s.c.c.m. $O_2$, 30 W, 30 s), and then the resist was washed away with acetone. A spin-cast layer of a photodefinable epoxy (SU8-2, Microchem) formed the gate dielectric. On top of this layer, we defined the gate (Ti (1 nm)/Au (20 nm)) using photolithography and lift-off. Reactive ion etching through the epoxy, using a layer of photoresist as a mask, created openings to enable probing of the source and drain electrodes (see Supplementary Information, Figs S3–S6, for various measured properties of devices with different tube densities and layouts). For the high-performance devices of Fig. 4, spin-casting and atomic layer deposition techniques defined the high-capacitance bilayer dielectrics of BCB and $HfO_2$. In addition, gate electrodes with widths comparable to the channel length provided low overlap capacitances for high-speed operation. The electrodes' layouts match probing configurations for high-speed measurements with a network analyser.

For bottom gate devices, the SWNT arrays were transferred from quartz onto other substrates. To pick up the aligned tubes, a 100-nm layer of Au was first deposited on the nanotubes/quartz by electron beam evaporation ($3 \times 10^{-6}$ torr, 0.1 nm $s^{-1}$; Temescal CV-8). On top of this Au layer, a film of polyimide (polyamic acid, Aldrich) was spin-coated at 3,000 r.p.m. for 30 s and cured at 110 °C for 2 mins. Physically peeling away the polyimide/Au/SWNT film lifted the tubes off the quartz with nearly 100% transfer efficiency. Placing this film on the receiving substrate ($SiO_2$/Si) coated with an adhesive layer of SU8-2 (150 nm) and then etching away the polyimide by reactive ion etching (150 mtorr, 20 s.c.c.m. $O_2$, 150 W, 35 min) left the Au/SWNTs film on the substrate. Photolithography and etching of the Au (Au-TFA, Transene) defined the Au source and drain electrodes. In the final step of the fabrication, SWNTs outside the channel regions were removed by reactive ion etching to isolate the devices (see Supplementary Information, Figs. S11 and S12, for SEM images that indicate the nearly 100% efficiency of this process).

### FABRICATION OF TRANSISTORS WITH POLYMER ELECTROLYTE AND $HfO_2$ GATE DIELECTRICS

To achieve high transconductances, we used high-capacitance gate dielectrics consisting of either 10-nm $HfO_2$ or a polymer electrolyte. The electrolytes were made by directly dissolving $LiClO_4 * 3H_2O$ in poly(ethylene oxide) (PEO, $M_n = 550$) or in polyethylenimine (PEI, $M_n = 800$) in air at room temperature with 2.4:1 and 1:1 polymer to salt weight ratios, respectively. The electrolytes were injected into a polydimethylsiloxane (PDMS) fluidic channel laminated over aligned arrays of SWNTs on quartz substrates with source/drain electrodes defined according to the previously described procedures. In these devices, gate voltages were applied through a silver wire dipped in the electrolyte. The $HfO_2$ was prepared on a doped silicon substrate by atomic layer deposition (Savannah 100, Cambridge NanoTech) using $H_2O$ and $Hf(NMe_2)_4$ (99.99+%, Aldrich) and a substrate temperature of 150 °C. SWNT arrays were transferred onto the $HfO_2$ using the procedures described above, but without the adhesive layer. Photolithography and etching defined the Au electrodes for source and drain.

### FABRICATION OF *n*-TYPE TRANSISTORS, CMOS AND PMOS LOGIC GATES

Spin-coating layers of PEI ($M_n = 800$, Aldrich) on the top of the nanotubes switches the operation of the transistors from unipolar p-channel to unipolar n-channel. To form these coatings, PEI was first dissolved in methanol with a volume concentration of 1:5. Spin-casting the PEI directly onto the SWNTs at 2,000 r.p.m. for 30 s created the coatings. Heating at 50 °C for 10 h gave n-channel transistors. Suitable interconnection of such devices can yield logic gates of various types. For PMOS inverters, one transistor served as a resistor load, and the other served as the drive. CMOS inverters were formed with uncoated p-channel devices and PEI-coated n-channel devices.

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## Author contributions

S.J.K, C.K. and J.A.R. designed the experiments, S.J.K., C.K. and T.O. performed the experiments, S.J.K., C.K., T.O., M.S., N.P., M.A.A., S.V.R. and J.A.R. analysed the data, S.J.K, C.K. and J.A.R. wrote the paper.

## Competing financial interests

The authors declare that they have no competing financial interests.