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High-performance flexible BiCMOS electronics based on single-crystal Si nanomembrane

Jung-Hun Seo[1,3], Kan Zhang[1], Munho Kim[1], Weidong Zhou[2] and Zhenqiang Ma[1]

In this work, we have demonstrated for the first time integrated flexible bipolar-complementary metal-oxide-semiconductor (BiCMOS) thin-film transistors (TFTs) based on a transferable single crystalline Si nanomembrane (Si NM) on a single piece of bendable plastic substrate. The n-channel, p-channel metal-oxide semiconductor field-effect transistors (N-MOSFETs & P-MOSFETs), and NPN bipolar junction transistors (BJTs) were realized together on a 340-nm thick Si NM layer with minimized processing complexity at low cost for advanced flexible electronic applications. The fabrication process was simplified by thoughtfully arranging the sequence of necessary ion implantation steps with carefully selected energies, doses and anneal conditions, and by wisely combining some costly processing steps that are otherwise separately needed for all three types of transistors. All types of TFTs demonstrated excellent DC and radio-frequency (RF) characteristics and exhibited stable transconductance and current gain under bending conditions. Overall, Si NM-based flexible BiCMOS TFTs offer great promises for high-performance and multi-functional future flexible electronics applications and is expected to provide a much larger and more versatile platform to address a broader range of applications. Moreover, the flexible BiCMOS process proposed and demonstrated here is compatible with commercial microfabrication technology, making its adaptation to future commercial use straightforward.

npj Flexible Electronics (2017)1:1 ; doi:10.1038/s41528-017-0001-1

INTRODUCTION

In traditional microelectronics, complementary metal-oxide semiconductor (CMOS) transistors have clear advantages over their counterpart, bipolar transistors, such as lower power dissipation and higher packing density. On the other hand, bipolar transistors also have their own unique advantages over CMOS, namely, higher current driving capability and higher gain.[1, 2] Therefore, CMOS has been traditionally used to address logic applications (note: advanced CMOS can also address some radio-frequency (RF) applications) and bipolar junction transistors (BJTs) have been mainly used to address analog, including microwave, applications. BiCMOS technology, which is a combination of bipolar technology and CMOS technology, was developed to achieve complementary advantages from both technologies and thus offer lower power dissipation, and better gain and current driving capability on the same Si chip.[3, 4] As a result, BiCMOS technology has been widely used in logic circuits and particularly mixed-signal systems[5–8] in electronics industry for the last two decades or so.

An emerging category in electronics that has been intensively researched in the past decade is inorganic semiconductor-based flexible electronics. Flexible electronics have mainly focused on their form factors such as bendability, lightweight, and large area with low-cost processability.[9–13] Up to date, all the Si-based thin-film transistors (TFTs) have been realized with CMOS technology because of their simple structure and process.[12–14] However, as more functions are required in future flexible electronic applications (i.e., advanced bioelectronic systems or flexible wireless power applications),[15–17] an integration of functional devices in one flexible substrate is needed to handle complex signals and/or various power levels. In light of the development in and wide applications of the rigid-chip-based semiconductor transistors, a mechanically flexible BiCMOS platform will also be able to open a new pathway in fulfilling the needs of advanced flexible electronics. However, it has been a challenge to realize flexible metal–oxide–semiconductor field-effect transistors (MOSFETs) and BJTs in the same batch of process, due to the very different requirements that are needed for processing BJT and CMOS. The single-crystalline semiconductor nanomembranes (NMs) that were investigated over the last decade not only exhibit good flexibility for doping to fabricate n-type MOSFET (NMOS) and p-type MOSFET (PMOS) TFTs, but also offer excellent mechanical durability and electronic properties.[18–20] Thus, it enables us to demonstrate high performance flexible CMOS TFTs such as flexible RF TFTs, high sensitivity light sensors, bio-medical devices, and environment-friendly devices.[12–16, 21–24] Although these demonstrations were very successful on their own, all of them have been fabricated using CMOS technology that is inadequate to handle high power signals or to satisfy more functionally advanced flexible electronics.

In this paper, we demonstrate flexible Si NM-based BiCMOS TFTs, including NMOS, PMOS, and NPN BJTs with a single batch of microfabrication process. In order to realize BiCMOS TFTs on a 340-nm thick single crystalline Si NM layer, various fabrication processes and techniques were carefully designed and employed, such as multiple ion implantations with different ion species, combined diffusion processes for n^+ and p^+ wells, and transfer printing at the final fabrication stage. All types of TFTs were successfully integrated into the Si NM on a single piece of plastic

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Received: 1 November 2016 Revised: 12 January 2017 Accepted: 24 January 2017
Published online: 26 September 2017

npj nature partner journals

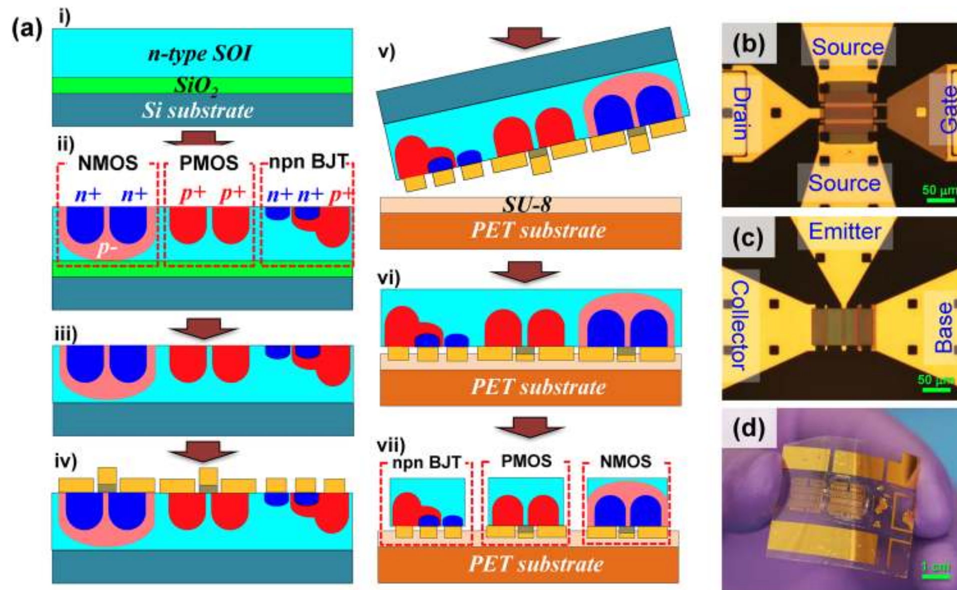

Fig. 1 BiCMOS TFT fabrication process and images **a** Process flow for TFT fabrication. (i) Preparation of n^- SOI wafer. (ii) Ion implantations to form p-well, p^+ and n^+ regions in the device layer (see Fig. 2 for the detailed sequence of ion implantations). (iii) Released doped Si NM sitting on handling substrate. (iv) Metallization for source/drain/gate and emitter/base/collector electrodes and dielectric deposition for SiO gate oxide layer. (v) NM flip-transferred to a PET substrate. (vi–vii) Dry etching of a transferred Si NM to isolate TFTs and to expose electrodes. A microscopic image of Si NM **b** NMOS TFT, and **c** NPN BJT. **d** An optical image of an array of bent BiCMOS TFTs

substrate and demonstrated excellent DC and RF characteristics with stable transconductance and current gain under bending conditions. It should be noted that our Si NM BiCMOS process can be easily adapted to wafer level state-of-the-art CMOS processes by scaling up the transfer-printing method to large-area printing techniques such as roll-to-roll or fully automated transfer printing[25–27] and by applying advanced lithography technology such as nanoimprinting lithography to realize sub 100 nm features.[14]

RESULTS

The fabrication process for flexible Si NM-based BiCMOS TFTs is shown in Fig. 1a and consists of three major steps: a multiple ion implantation step (Fig. 1a ii), a transfer-printing step (Fig. 1a v), and a microfabrication step (Fig. 1a vii). Among these steps, the precise ion implantation and the subsequent high-temperature annealing are the key processes that enable us to realize flexible Si NM-based BiCMOS TFTs as it is critical to form multiple selectively doped regions on a thin Si NM (340 nm). The detailed processing conditions can be found in the Methods Section and elsewhere.[19, 28] Briefly, a lightly doped n-type silicon-on insulator (SOI) wafer with a 340-nm thick Si template layer was implanted with phosphorus and boron, followed by a diffusion step to define the n^+, p^+ and p^- wells. Thereafter, the top Si device layer (i.e., the Si NM) was released and the source/drain electrodes, emitter/base/collector electrodes, and SiO dielectric layer were deposited using an e-beam evaporator. The device layer was subsequently flip-transferred onto an adhesive-coated polyethylene terephthalate (PET) substrate. Note that, after the transfer-printing step, all metal electrodes and Si NMs were flipped together and therefore, the metal electrodes were covered by the Si NMs. The final fabrication steps involved additional dry etching to define the channel regions and isolate the devices. As a result, the metal electrodes, which were buried under the Si NM layer, were partially exposed. The current-voltage (I–V) characteristics and the RF characteristics of the finished devices were measured using an Agilent 4155B semiconductor parameter analyzer and an Agilent E8364A performance network analyzer, respectively. The “open” and “short” features were used for a de-embedding procedure to obtain the intrinsic RF characteristics of the devices.

Rigid-chip based BiCMOS is generally made on a p^- Si substrate, where CMOS devices are fabricated using eithera single-well (an n-well for PMOS) or a double-well process. Both CMOS and BJTs are built on an epitaxially grown buried layer. To realize the vertical structure of BJTs on a rigid chip, complicated processing steps are needed. To maintain the mechanical flexibility of the finished BiCMOS TFTs using the thin (340 nm) Si NM and also to reduce the fabrication cost, we adopted a lateral BJT structure (Fig. 1a) without growing extra materials for the collector, the base, or the emitter layers of the BJT. To minimize the number of needed ion implantations (as detailed below) in the fabrication process that are required for the three types of transistors we chose n^- SOI substrate instead of p^- SOI substrate.

It is critical to form various types of implanted regions with high precision in both depth and in lateral dimensions in a 340-nm thick Si layer of SOI wafer to realize the NMOS, PMOS, and BJT in the same batch while maintaining their high performance.

In particular, the width of the base region (Fig. 1a ii) is the most critical in order to achieve high performance BJTs. Therefore, the ion implantation process needs to be carefully designed, taking into consideration the implantation condition (energy and dose) and diffusion time to minimize the number of implantation and out-diffusion among implanted regions/wells, while maintaining the correct doping type and concentration. In order to achieve accurate doping profiles, a Silvaco Athena 2-dimensional (2D) implantation simulator was employed to simulate the ion implantation and diffusion conditions. It should be noted that the sequence of implantation and their dose/energy were designed based on the diffusivity of each ion and also based on the target depth after the thermal diffusion steps. The implantaion designs were aimed to share the the same p^+ implantation procedure for the source/drain regions in PMOS and the base region in BJT. The designs were also to share the same n^+ implantation procedure for the source/drain regions in NMOS and the emitter/collector regions in BJT. By sharing the same ion implantation steps, processing complexity and the related costs are reduced. In order to realize the different implantation depths

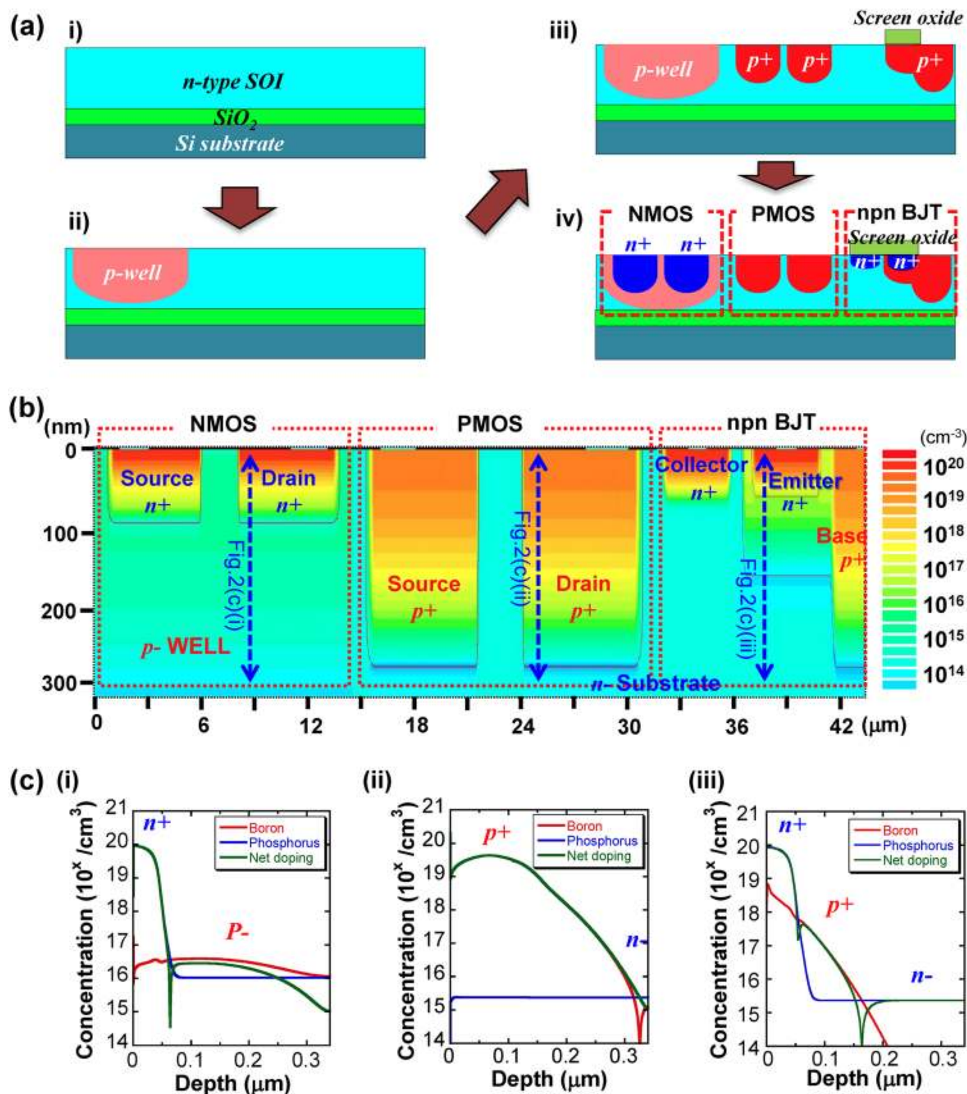

Fig. 2 Illustration of ion implantation processes and their simulations **a** Process flow for ion implantations. i, Preparation of SOI wafer. ii, Formation of a lightly doped *p*-well for NMOS. iii, Formation of a heavily doped p^+ regions for the source/drain contacts in PMOS and for the base region in BJT. iv, Formation of a heavily doped n^+ regions for source/drain contacts in NMOS and emitter/collector regions in BJT. Note that a patterned screen oxide was covering "the emitter region" (step iii) or "the emitter and the collector regions" (step iv) of BJT in order to reduce the implantation depth. **b** Simulated doping profiles for each type of device formed on the same layer. The simulated ion implantation values (dose and energy) were used to fabricate the actual doped Si NM. **c** Plots of doping profiles in each of the corresponding regions. (i) NMOS (*n*+ source/drain regions, p-well and the net doping), (ii) PMOS (*p*+ source/drain regions and substrate), (iii) NPN BJT (*n*+ emitter, *p*+ base, *n*-collector and the net doping)

needed for different TFTs under the same ion implantation conditions, a patterned screen oxide was used to make the adjustment of depth. The screen oxide consumes part of the kinetic energy of the implanted ions and thus helps reduce the implanted ion depth. For example, a layer of screen oxide was used to cover "the emitter region" or "the emitter and the collector regions" of the BJTs when performing the p^+ or n^+ ion implantation, respectively (see details in the Methods Section). The selection of oxide thickness was based on simulations results. The different diffusivity values of the ion species were also taken into consideration during the design of the process flow. For example, a boron implantation was performed first, because the diffusivity of boron is five times smaller than the diffusivity of phosphorus in Si.[2] As a result, the borons in the *p* well was not severely out-diffused during the second phosphorus diffusion. We then used high dose/energy boron implantation to form the p^+ source/drain regions in PMOS and the p^+ base region in BJT. Similarly, high dose/energy phosphorus implantation was carried out to form the n^+ source/drain regions in NMOS and the n^+ collector/emitter regions in BJT by the same implantation step. Therefore, all the needed doped regions for the BiCMOS TFTs could be formed by three rounds of ion implantation (Fig. 2b). As shown in Fig. 2a, the ion implantation process starts with light boron doping into the n-type SOI wafer (Phosphorus, 1×10^{15} cm^{-3}) to form a *p*-well of 5×10^{16} cm^{-3} for the NMOS (Fig. 2a ii), followed by a high temperature annealing process in a furnace to diffuse and recrystallize the Si NM. Prior to the second ion implantation step, a 90-nm thick SiO_2 screen oxide layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned it to block the emitter region (Fig. 2a iii). Then, boron implantation was conducted to create p^+ doping of 8×10^{19} cm^{-3} for the source/drain regions in PMOS and for the base region in NPN BJT. Without any annealing process, another 90-nm thick SiO_2 screen oxide layer was deposited and patterned it to block the emitter and collector regions (Fig. 2a iv), followed by phosphorus implantation to form n^+ doping of 1×10^{20} cm^{-3}

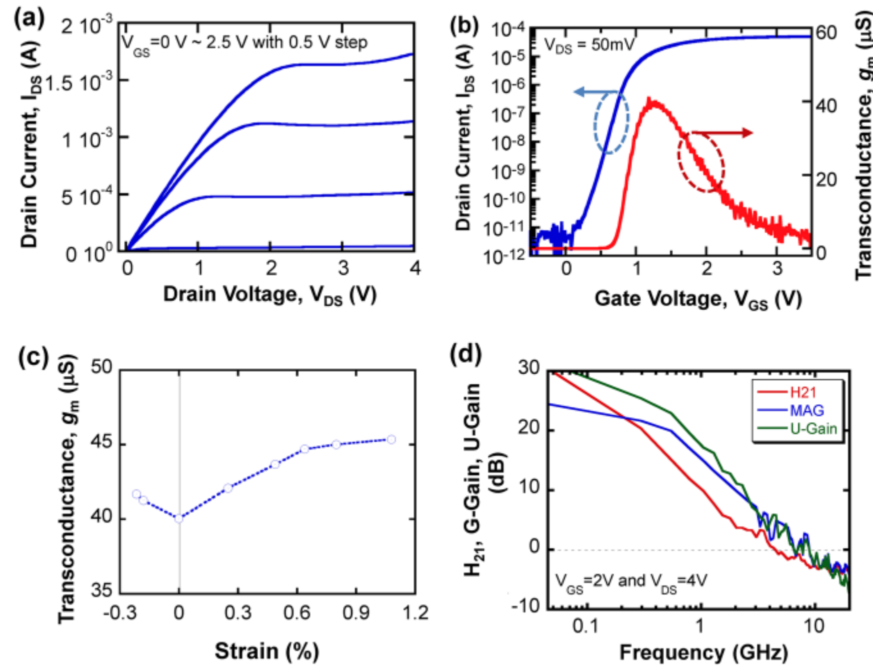

Fig. 3 Device characteristics of NMOS TFT **a** Drain current (I_{DS})–voltage (V_{DS}) characteristics with different V_{GS} values ranging from 0 V to 2.5 V with 0.5 V increments. **b** Drain current (I_{DS}) and transconductance (g_m) curves with a drain bias of 50 mV and a V_{GS} ranging from –0.5 V to 3.5 V. **c** Transconductance (g_m) with respect to applied strain at a fixed voltage bias point of $V_{GS\,=}$ 1 V and $V_{DS\,=}$ 3 V. **d** Current gain (h_{21}) and unilateral power gain (*U*-gain) as a function of frequency from 45 MHz to 20 GHz

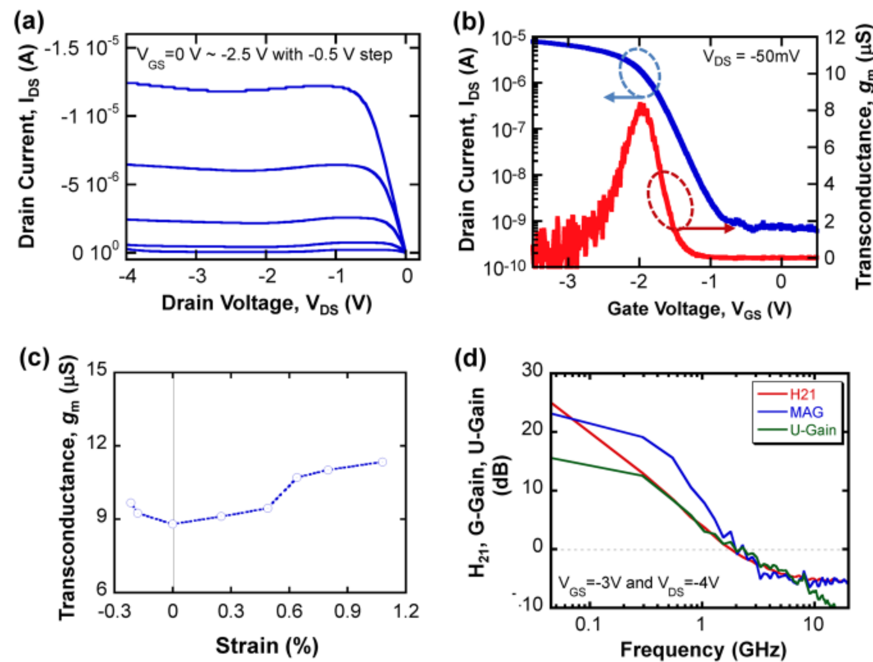

Fig. 4 Device characteristics of PMOS TFT **a** Drain current (I_{DS})–voltage (V_{DS}) characteristics with different V_{GS} values ranging from 0 V to −2.5 V with 0.5 V increments. **b** Drain current (I_{DS}) and transconductance (g_m) curves with a drain bias of 50 mV and a V_{GS} ranging from 0.5 V to −3.5 V. **c** Transconductance (g_m) with respect to applied strain at a fixed voltage bias point of $V_{GS\,=}$ −1 V and V_{DS} = −3 V. **d** Current gain (h_{21}) and unilateral power gain (*U*-gain) as a function of frequency from 45 MHz to 20 GHz

for the source/drain regions in NMOS and the emitter/collector regions in NPN BJT. Finally, the sample was annealed to diffuse and recrystallize the Si NM. In total, only three ion implantations and two thermal annealing steps were used for the entire fabrication of all three types of transistors. The finished PMOS/NMOS and BJT are shown in Fig. 1b, c. Figure 1d shows the bent image of the flexible BiCMOS chip. Figure 2b shows the simulated doping concentration and their profiles based on the actual parameters used for the ion implantation process. Figure 2c show the detailed plots of the doping profiles from NMOS, PMOS and NPN BJT, respectively.

Electrical characterizations of the NMOS and PMOS TFTs are shown in Figs. 3 and 4, respectively. The physical gate length, gate width (W_g), and effective gate (channel) length (L_g) of NMOS and

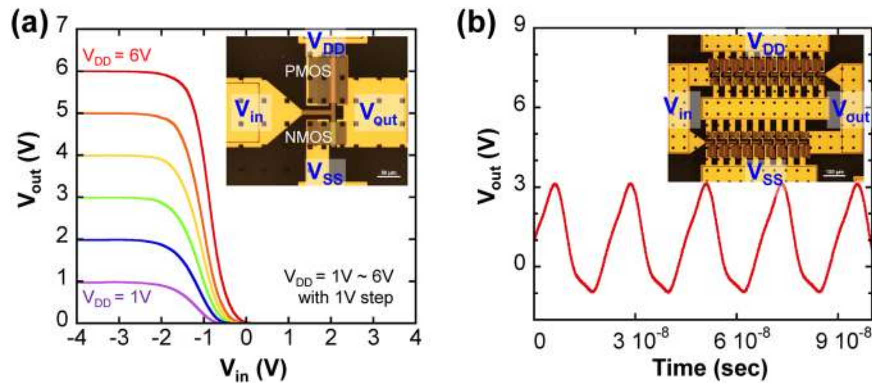

Fig. 5 Electrical characteristics of CMOS inverter and 10-stage ring oscillator. **a** Output voltage characteristics of a CMOS inverter with $V_{DD} = 6$ V. **b** Measured time domain responses of a 10-stage CMOS ring oscillator. Optical microscope images of the inverter and ring oscillator appear in insets

PMOS TFTs are 2, 25, and 1.5 μm, respectively. The output characteristics of the NMOS and PMOS TFTs under various gate biases from 0 V to 2.4 V with 0.6 V steps are shown in Figs 3a and 4a, respectively. Figures 3b and 4b show the typical transfer characteristics of the NMOS and PMOS TFTs, respectively, biased at a V_{DS} of 50 mV. The highest transconductance (g_m) of NMOS TFTs was 40.9 μS at a V_{GS} of 1.18 V, while the highest g_m of PMOS TFTs was 8.6 μS at a V_{GS} of −2.0 V. Field-effect mobility of 160 cm^2/V s from NMOS and 34 cm^2/V s from PMOS were measured based on the following equation,[2] $\mu = (L_g \cdot g_m)/(W_g \cdot C_{ox} \cdot V_{DS})$, where C_{ox} is the oxide capacitance. The inferior PMOS performance compared to NMOS is partially caused by the slower hole mobility value than that of the electron mobility value, but is mainly attributed to the inadequate boron doping concentration because the implantation and annealing conditions were designed to accommodate BJT fabrication. The performance of PMOS can be further improved by using two separated implantation steps for the source/drain regions of PMOS and for the base of the BJT (but at additional cost). A threshold voltage (V_{th}) and a subthreshold swing of 0.95 V and 480 mV/decade, respectively, from NMOS and −1.9 V and 770 mV/decade, respectively, from PMOS were also extracted from transfer curves. Supplementary Fig. S2 shows that the transfer characteristics measured more than ten PMOS devices. The calculated threshold voltage (V_{th}) was distributed between 0.68s ~ 0.72 V with an average V_{th} of 0.71 V. Considering that the devices were not passivated and built on flexible substrate, V_{th} values within ± 5% variation indicate good uniformity of the electrical performance of BiCMOS devices. The high threshold voltages and subthreshold swings can be further improved by employing ion implantation to form well-defined n^+ regions. Although the PMOS performance was sacrificed somewhat, we believe that it is still a cost-effective decision to implement boron doping for both PMOS and BJT TFTs using the single implantation step. The peak transconductance of NMOS and PMOS TFTs under different bending situations from 0.21% tensile strain to 1.08 % compressive strain are shown in Figs. 3c and 4c, respectively. Both types of TFTs performed subtle increments in their transconductance as the strain increases. During bending, electron and hole mobilities of Si nanomembrane are enhanced by the strain-induced band splitting which was theoretically and experimentally reported before.[12, 13, 29, 30] The improvement in mobility directly leads to an increase in the transconductance of TFTs during the bending by the following equation: $g_m = \mu \cdot C_{ox} \cdot V_{DS} \cdot (W/L)$, where C_{ox} is the oxide capacitance, μ is the mobility, V_{ds} is the drain bias, W/L is the ratio of width and length of the channel, respectively. It is worth to note that although a comparison of electrical characteristics between pre-transferred and post-transferred devices was not performed, David Troadec et al. reported no performance degradation after the devices were transferred onto the flexible substrate.[31]

Figures 3d and 4d show the measured current gain (h_{21}) and the Masons unilateral gain (U-gain) of NMOS TFT and PMOS TFT with a DC bias of $V_{GS} = 2$ V and $V_{DS} = 4$ V, and $V_{GS} = -3$ V and $V_{DS} = -4$ V, respectively. Details on the RF results, including the measured S-parameters of NMOS and PMOS from 45 MHz to 20 GHz can be found in Supplementary Figs. S1a, b of Supplementary Information. The measured f_T and f_{max}, after de-embedding, were 4.5 and 8.8 GHz for NMOS and 1.7 and 2.2 GHz for PMOS, respectively. The lower f_T and f_{max} values in PMOS are attributed to the poor hole mobility and transconductance.

Measurements of a typical CMOS inverter appear in Fig. 5a with various drain voltages (V_{DD}) from 1 V to 6 V. The output voltage of the inverter shows poor gain characteristics which are attributed to the unoptimized current matching between PMOS and NMOS. Figure 5b shows the output voltage (V_{OUT}) as a function of time of a ten-stage CMOS ring oscillator with 10 V of V_{DD}. The distorted waveform is attributed to the current mismatch associated with the unexpected parasitic capacitances between stages. Such issues can be further improved by fine-tuning the doping profiles in n^+ and p+ regions, as well as the p-well concentration in NMOS.

The electrical characterizations of an NPN BJT TFT with common emitter configuration are shown in Fig. 6. The emitter dimension is 5 × 20 μm^2. Figure 6a shows the forward on-state characteristics of the NPN BJT. Output curves of I_C vs. V_{CE} were measured with different base currents from 40 nA to 140 nA with increments of 20 nA. Despite the unoptimized BJT structure, NPN BJT showed a high early voltage (V_A) of −76 V which is compatible with the values from other BiCMOS BJTs built on rigid Si substrates.[32] A specific on-resistance of 6.0 ohm cm (based on the active area) was measured. Figure 6b shows a Gummel plot measured at a V_{CE} of 1 V. The highest current gain (β) was calculated to be 143. The ideality factor (n) of the base current was close to 1.12, with very low leakage currents at the low base–emitter voltages (V_{BE}), indicating that two PN junctions were clearly formed. Figure 6c shows the measured current gains at room temperature as a function of the collector current density. A current density of 2.1 A/cm^2 with a maximum current gain of 143 indicates that our BJTs have good current handling capability, sufficing many current hungry applications. Under an extreme bending condition (that is, at a bending radius of 15.5 mm), the maximum β value increased slightly to 152, which is probably attributed to the reduction of series resistance between emitter to base and base-to-collector junction diodes, as well as the increased mobility.[13, 33] Figure 6d shows the highest β of an NPN BJT under different bending situations from 0.21 % tensile strain to 1.08 % compressive strain. Interestingly, the bending result indicates that the β of BJT tends to change more than the transconductance of TFT (18 % of BJT vs. ~10 % of NMOS). Such a large degree change of the β in BJT can be attributed to the structural characteristics of BJT, i.e., a series

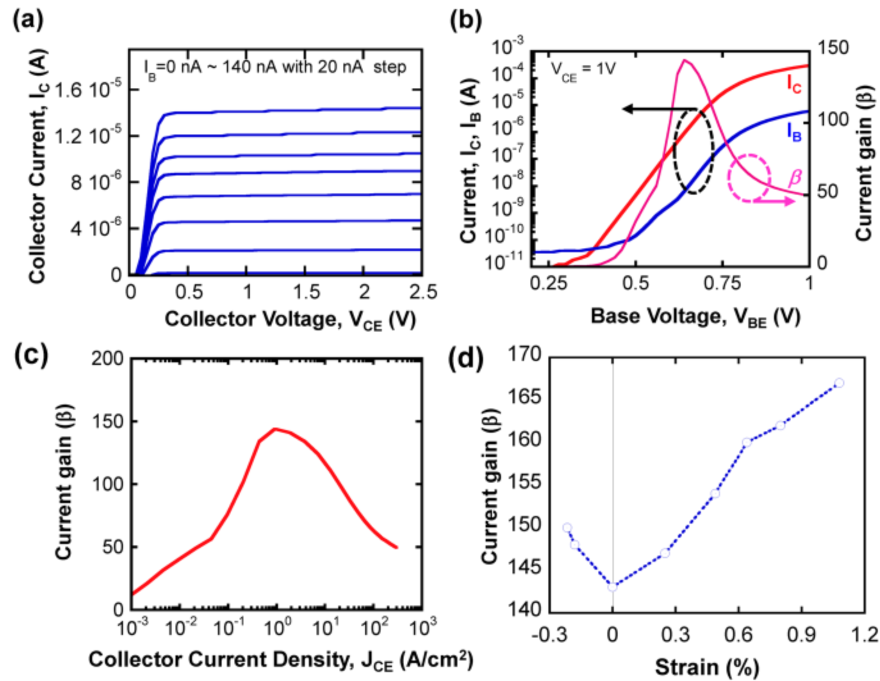

Fig. 6 Device characteristics of NPN BJT **a** Collector current (I_{CE})–voltage (V_{CE}) of the NPN BJTs with different base current (I_B) from 40 to 140 nA with 20 nA increments. **b** Gummel plot and current gain (β) plot showing a maximum DC gain of 143 at V_{CE} of 1 V. **c** Current gain (β) as a function of the collector current density. **d** Changes in current gain (β) under bending conditions up to 1.08 % of strain

connection of N–P and P–N diodes with a thicker intrinsic layer that is more sensitive to the mechanical bending than the MOS structure. Due to the limitation of lithography, i.e., the large emitter width, RF characteristics of the NPN BJTs were not characterized.

DISCUSSION

In conclusion, integrated high-performance flexible BiCMOS TFTs, including n-channel, p-channel MOSFETs, and NPN BJTs, based on transferable single crystalline Si NM were successfully demonstrated on a single piece of bendable plastic substrate using a simple yet robust fabrication process. All these TFTs exhibit excellent DC and/or RF characteristics that are comparable to their rigid counterparts of equivalent feature sizes along with robustness against mechanical bending. Considering the versatility and more functionalities provided by BiCMOS, we expect that the demonstrations made in this work will enable a broader range of flexible electronics applications than present only NMOS- or only CMOS-based flexible electronics, including a microwave module and signal processing sector (these parts can be consisted of RF NMOS and PMOS in this work), a power converter (BJT in this work), and signal amplification and modulation (with a combination of NMOS, PMOS and BJT). Moreover, the flexible TFT-form BiCMOS process demonstrated here is completely compatible with commercial microfabrication technology, making its adaptation to industrial usage straightforward.

METHODS

Device fabrication

The process flow starts with a 340-nm thick lightly phosphorus doped n-type SOI (Fig. 1a), which has a background doping concentration of about 5×10^{15} cm^{-3} (Fig. 2a i). The background doping concentration is suitable as the collector region of NPN BJT. As depicted in Fig. 2a ii, the *p*-type well region was first formed for NMOS TFTs by using ion-implantation of boron at a low dose (dose: 1×10^{12} cm^{-2}, energy: 30 keV) and annealing at 950 °C for 2 h in a nitrogen (N_2) ambient. Another boron implantation was then performed at a dose of 5×10^{14} cm^{-2} and energy of 17 keV to create p^+ regions for both the source and drain regions of PMOS and for the base region of BJT. Prior to the second boron implantation step, a 90-nm thick screen oxide was deposited by PECVD and patterned to block the emitter region (Fig. 2a iii) to only achieve a moderate boron doped region, while maintain heavy doping in other regions (i.e., p^+ regions for source/drain of PMOS and base of NPN BJT). Similarly, another 90-nm thick SiO_2 screen oxide layer was deposited and patterned it to block the emitter and collector regions (Fig. 2a iv). The source and drain regions of NMOS and the emitter region of BJT were then doped by phosphorous implantation with a dose of 4×10^{14} cm^{-2} and an energy of 6 keV. It should be noted that the sample was annealed after finishing both heavy boron and heavy phosphorus implantations to reduce the number of processing steps. Namely, furnace annealing was performed to activate both types of dopants together at 850 °C in an N_2 ambient for 40 min. The lower anneal temperature was chosen to suppress boron diffusion and achieve the designed doping profile for the BJT. After the completion of the implantation and the diffusion processes, an array of holes on the Si NM was patterned by photolithography and reactive-ion etching to expose the buried oxide (BOX) layer. The sample was then soaked in concentrated hydrofluoric acid (HF, 49%) to release the top Si NM from the handling Si substrate (Fig. 1a iii). After rinsing and drying the sample, the Si NM was weakly bonded to the handling Si substrate via Van der Waals forces. As shown in Fig. 1a iv, the gate stack (SiO/Ti/Au 100/20/130 nm) and electrodes (Ti/Au 20/250 nm) for NMOS, PMOS, and BJT were deposited by e-beam evaporation, simultaneously. After the completion of the metallization step, all device layers (including metal electrodes and Si NM) were flip-transferred together to a PET substrate coated with an adhesive layer (SU-8 2002, Microchem). The sample was cured to glue the transferred layer onto the PET substrate (Fig. 1a v and vi). After the transfer step, the Si NM layer is positioned face-up and the electrodes were buried underneath the Si NM. Finally, the active device regions was defined and the electrodes were exposed by using the photoresist patterning and dry etching steps (Fig. 1a vii).

Implantation simulations in Si NM

The simulation is carried out by Silvaco® Athena. The same dimension, background doping concentration, and material parameters as the actual values were used to model the device. In order to achieve the accurate implantation profile, we employed the Monte–Carlo method with 1 million

of the projected ions. For the diffusion step, the actual ramping up and down values of 20 and 10 °C/min were used in the simulation.

Strain calculation

The strain was calculated using the following equation: $\varepsilon(\%) = 1/[2 \cdot R(\text{mm})/t(\mu\text{m})] + 1$, where R is the radius of the fixture and t is the thickness of the bent object (μm). The t includes the thicknesses of the PET film (175 μm), the adhesive layer (1 μm), and the Si NM (0.34 μm). The bending test was performed using the metal fixture with various curvatures. The flexible BiCMOS device was mounted on concave and convex shape fixtures with radii ranging from 15 to 77.5 mm for the convex fixtures to create uniaxial tensile strain and with radii ranging from 110 to 85 mm for the concave fixtures to create uniaxial compressive strain. The associated bending tensile strains for the device were calculated to be 0.215 and 0.18 % for the compressive strain and 0.25, 0.49, 0.64, 0.8 and 0.108 % for the tensile strain.

ACKNOWLEDGEMENTS

The work was supported by the Air Force Office of Scientific Research (AFOSR): Presidential Early Career Award in Science & Engineering (PECASE) grant # FA9550-09-1-0482. The program manager is Dr. Gernot Pomrenke.

AUTHOR CONTRIBUTIONS

J.-H.S., Z.K., M.K., W.Z. and Z.M. conducted the research; Z.M. designed the research; J.-H.S., Z.K. and Z.M. interpreted the data and wrote the manuscript. W.Z. contributed to the manuscript writing. J.-H.S. and Z.K. contributed equally to this work.

ADDITIONAL INFORMATION

Supplementary Information accompanies the paper on the *npj Flexible Electronics* website (doi:10.1038/s41528-017-0001-1).

Competing interests: The authors declare that they have no competing financial interests.

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