High-Performance Germanium-Seeded Laterally Crystallized TFT's for Vertical Device Integration

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***Abstract*—Increasing chip complexity and area has resulted in interconnect delay becoming a significant fraction of overall chip delay. Continued scaling of design rules will further aggravate this problem. Vertical integration of devices will enable a substantial reduction in chip size and thus in interconnect delay. We present a novel technique to achieve vertical integration of CMOS devices. Germanium is used as a seeding agent at the source and/or drain of thin film transistors (TFT's) to laterally crystallize amorphous silicon films, resulting in high-performance devices. This is achieved through the formation of large grain polysilicon with a precise control over the location of the grain. TFT's have been demonstrated offering substantial performance improvement over conventional unseeded polycrystalline TFT's, with demonstrated mobilities as high as 300 cm^2/V-s. The process is fully CMOS compatible and has a low thermal budget. It is highly scalable to deep-submicron technologies and, with suitable optimization, should enable the production of high-performance, high density, vertically integrated ULSI.**

***Index Terms*— Lateral crystallization, SOI technology, solid phase crystallization, thin film transistors, vertical integration.**

I. Introduction

INCREASING chip area and decreasing feature size has resulted in interconnect delay becoming a significant fraction of the overall chip delay. Numerous techniques are under consideration to decrease interconnect delay, including the use of low resistivity interconnect materials [1], low-k dielectrics [2], and increased packing density using various techniques to increase the level of achievable integration for a given device generation. Of these, the increase of packing density using vertical integration of devices is particularly interesting, as it offers the additional benefits of decreasing block-level routing complexity (through the ability to layer blocks) and dramatically decreasing the consumed silicon real-estate. Various simple vertically integrated cells have been demonstrated in the past, such as vertically integrated SRAM cells [3].

Vertical integration of devices using thin film transistors (TFT's) is a promising means of achieving three-dimensional (3-D) integration. Unfortunately, TFT performance is typically substantially worse than that of bulk devices, limiting the use of such cells to only noncritical paths. Additionally, for deep submicron VLSI applications, statistical variation in device performance is introduced by the random distribution of grains in the device [4], since the grain size is on the order of the device size. This variation in performance results in an unacceptable degradation in uniformity. Uniformity can be improved by reducing the grain size; however, this degrades device performance substantially.

A method to achieve large grain TFT's with a control over the location of the grain is therefore highly desirable. Lateral solid-phase crystallization using a seeding agent to precisely nucleate the grains is an extremely promising means of achieving this. Metal induced crystallization has been studied in the past, using metals such as nickel [5]. Unfortunately, the integration of such a process into a CMOS technology is problematic due to the deleterious effect of nickel on device performance [6]. A metal-contamination-free technique to achieve lateral crystallization could be integrated into a standard CMOS process with significantly less difficulty.

In this paper, we present a novel technique to achieve lateral crystallization through the use of germanium seeding [7]. This technique is free of metallic seeding agents and is therefore easily integrated into a CMOS technology. Additionally, the technique performs extremely well for small devices, making it very promising for next generation VLSI applications. The actual process is remarkably simple and is a batch process, and can therefore be used with a relatively small increase in cost. The process has been used to fabricate high-performance TFT's suitable for 3-D integration applications. We describe the fabrication process and device performance and discuss the potential for using this technique as a means to achieve vertical integration of devices for next generation VLSI applications.

II. Background Information

A. Solid-Phase Crystallization

The solid-phase crystallization (SPC) of amorphous silicon to polysilicon occurs through the processes of nucleation and grain growth [8]. Clusters of a critical size nucleate within the amorphous matrix and subsequently enlarge. Both nucleation and grain growth are characterized by specific activation energies. For the SPC of amorphous silicon by homogenous nucleation, the activation energy of grain growth is less than that of nucleation [9]. Therefore, the amount of nucleation relative to grain growth decreases with decreasing temperature. To maximize grain size, it is desirable to minimize the nucleation/grain growth ratio. Therefore, SPC is typically done at a low temperature. The disadvantage of this technique is that the crystallization may take a long time (several hours

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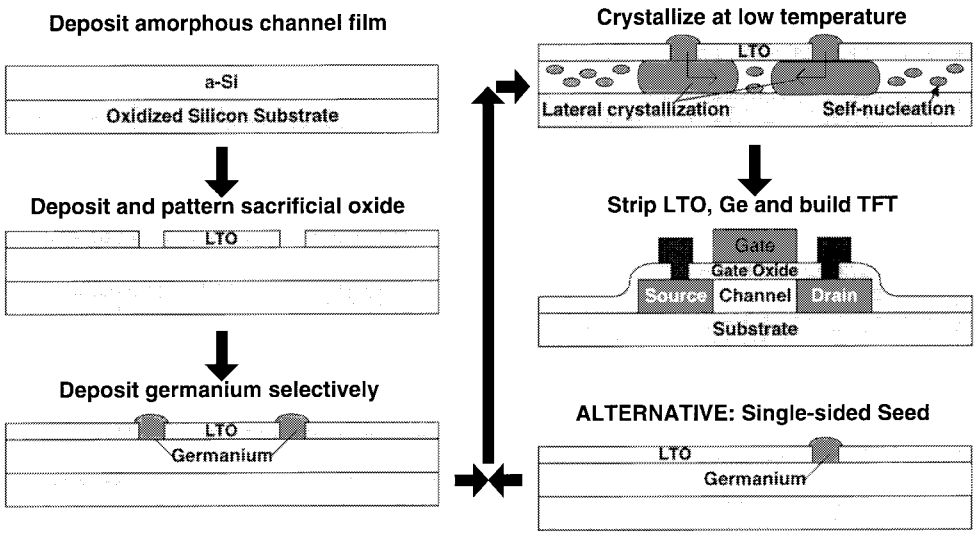


Fig. 1. Process flow for Ge-seeded laterally crystallized TFT fabrication.

at 600 °C). A large fraction of this time consists of the time before any nucleation has occurred, called the incubation time. Efforts have been made to reduce the incubation time without sacrificing conditions favorable to the maximization of grain size [10].

While the long incubation time associated with the amorphous to (poly)crystalline transition is a generally a disadvantage associated with low temperature SPC, it can be exploited to achieve lateral crystallization. In this process, nucleation is artificially induced in selected regions of the amorphous films using seeding agents. Typically, metals are used [5]; however, the use of selective heating as a noncontact seed has also been demonstrated [11]. The nuclei formed at these seed sites enlarge while the rest of the film is still in the incubation stage. Therefore, it is possible to form abnormally large grains with controlled location of the grain. The laterally crystallized grains cannot grow infinitely; after the passage of the incubation time, homogenous nucleation is induced in the rest of the film.

B. Silicon–Germanium Alloys

Silicon–germanium (SiGe) alloys exhibit a variation in thermodynamic properties from those of silicon to those of germanium. In fact, the thermal properties exhibit a dependence that is often almost linearly related to the ratio of the melting points of silicon and germanium, scaled to the germanium fraction of the film. This phenomenon applies to crystallization as well; SiGe alloys crystallize faster than pure silicon at a given temperature [12]. This fact has been used to reduce the incubation time of amorphous silicon films for thin film transistors by replacing the amorphous silicon with a bi-layer of SiGe and Si [13]. This same fact can also be used to enable the use of germanium as a seeding agent for the lateral crystallization of amorphous silicon; the germanium reacts with the Si to form a SiGe layer at the Ge-Si interface, which nucleates the lateral crystallization.

Volumetrically, the germanium needed to induce nucleation in silicon is quite small. Given the exponential dependencies involved, the formation of a small amount of high Ge-fraction alloy at the interface is sufficient to cause nucleation. Additionally, Ge is not an excessively fast diffuser in Si, unlike typical metallic seeding agents. Therefore, any effect of Ge is essentially confined to the Ge-Si interfacial region and its surroundings.

These phenomena detailed above can be utilized to enable the germanium-seeded lateral crystallization of amorphous silicon to fabricate high-performance TFT's.

III. Experimental Details

To simulate the intended application of the devices, all devices in this study were fabricated on oxidized silicon wafers. The overall process flow is shown in Fig. 1. Amorphous silicon (100 nm) was deposited by LPCVD at 500 °C/1000 mtorr from SiH_4. These deposition conditions were chosen as they were previously identified as resulting in films having a long nucleation incubation time. On these silicon films, 50-nm LPCVD (LTO) SiO_2 was deposited for use as a sacrificial layer. Square seeding windows of 1 μm side were opened in this layer. The windows were positioned either over the drain of the TFT structure, or over both the source and drain of the same. Then, Ge was deposited by LPCVD at 500 °C/100 mtorr from GeH_4. Under these conditions, the Ge was deposited as a polycrystalline material. The deposition of Ge from GeH_4 is inherently selective on Si versus SiO_2. Therefore, the Ge deposited only within the previously opened seeding windows. These last three steps represent the only significant modifications to a conventional high-temperature TFT process flow. They involve two extra depositions (of the sacrificial oxide and the germanium) and a lithography step (to pattern the seed holes). Immediately after Ge deposition, the wafers were annealed in argon at 500–550 °C to fully crystallize the channel films. This immediate crystallization also removes the need to perform a wafer cleaning step after Ge deposition, which would be complicated by the fact that Ge etches in most common cleaning solutions. The immediate crystallization was thus used to eliminate this step

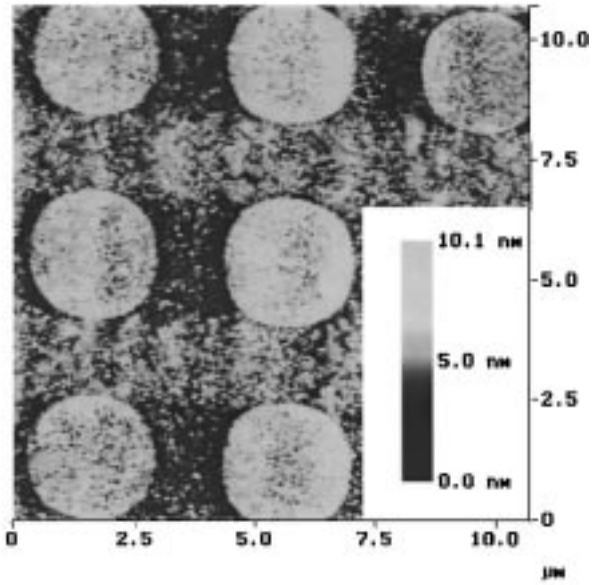


Fig. 2. Atomic force micrograph showing elevated polycrystalline seed points after defect etch.

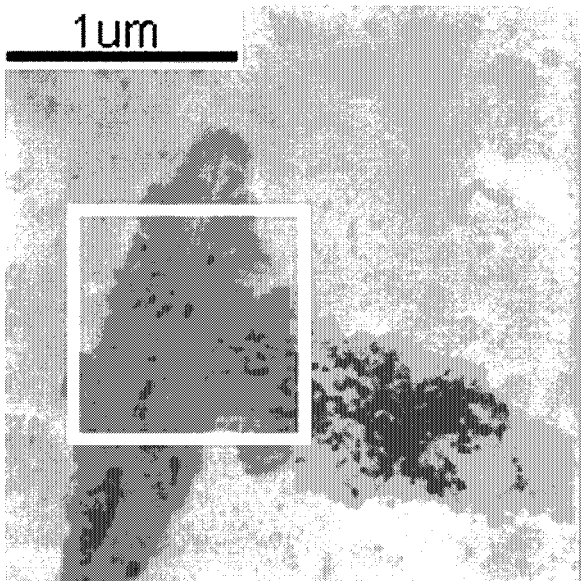


Fig. 3. Plan-view TEM showing growth of seeded grains with seed structure boundary overlaid in white.

entirely. For comparison, wafers without any Ge seeding were crystallized simultaneously. After crystallization, the remaining Ge was removed in H_2SO_4:H_2O_2, and the sacrificial oxide was removed in HF. Both processes offer excellent selectivity to Si and therefore do not cause any significant damage to the channel film. Standard planar top-gate self-aligned TFT's were then fabricated. Thermal SiO_2 (30 nm) was used as the gate dielectric, and 250 nm *in situ* doped polysilicon was used as the gate electrode. Junctions were formed using implantation of boron and phosphorus. No LDD or spacer technology was used. The peak process temperature was 900 °C. After device fabrication, electrical performance of the TFT's was evaluated. Plan-view TEM's of the channel films were also made to determine the seeding efficiency.

IV. Results

To determine the extent of crystallization into the channel films, AFM images were taken of defect-etched seeded films after partial crystallization. The seed points used for these test structures were 2-μm diameter circular holes. Enough crystallization was performed to form the SiGe alloy without causing too much lateral crystallization, enabling estimation of seeding efficiency. As is evident from the AFM image, shown in Fig. 2, polycrystalline silicon is formed at the seed point and is not etched as rapidly as the surrounding amorphous film, resulting in a height differential. Focused EDAX of the same film indicates the presence of less than 1% Ge within the seeded regions and its total absence in the remaining Si.

A plan-view TEM of a further-annealed seeded region is shown in Fig. 3. It is evident from this figure that grains are formed in the seeded region, and extend into the still-amorphous matrix. The size of the seed holes used in this work (1 μm and larger) have been scaled to smaller dimensions and materials tests performed, indicating that the seed hole size does not represent a limiting factor on scaling of the technology. Note that numerous grains may grow out of each seed point, depending on the size of the point. These grains have numerous defects within them. Some of these defects are annealed out during the subsequent high temperature processing.

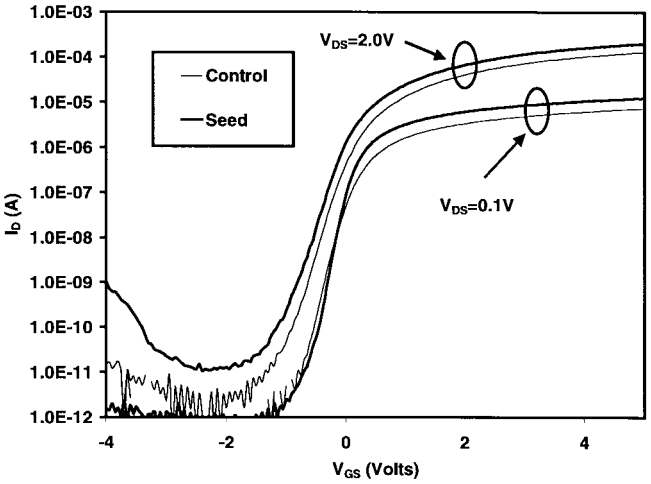
Electrical characteristics of 0.9 μm/0.7 μm NMOS and PMOS devices are shown in Fig. 4. It is evident that there is substantial improvement in device performance. The seeded devices shown in these plots were seeded in both the source and drain regions. To compare the performance of the seeded devices with the unseeded devices, various device parameters were calculated, and are summarized in Table I. Clearly, the seeded devices are superior to the unseeded ones. In particular, on-state performance shows substantial improvement. However, off-state and subthreshold performance only show marginal improvement, suggesting the presence of leakage causing defects within the channel. NMOS and PMOS devices show asymmetric improvement; the NMOS devices show substantially more improvement in on-state performance than shown in PMOS devices. This is probably related to the distribution of trap states within the bandgap and the relative impact of the reduction of grain boundary populations on the same.

To determine the extent of lateral crystallization, the variation in mobility with device dimensions was analyzed. The variation in mobility versus channel length for both dual-seeded (seeded in both the source and the drain) and single-seeded (seeded in only the drain) versus control devices is shown in Fig. 5, where it is apparent that seeded devices perform better than unseeded devices in all cases. The extent of improvement increases dramatically for smaller devices. For larger devices, dual seeded structures are superior. However, a crossover occurs, and single-seeded devices are better at shorter channel lengths.

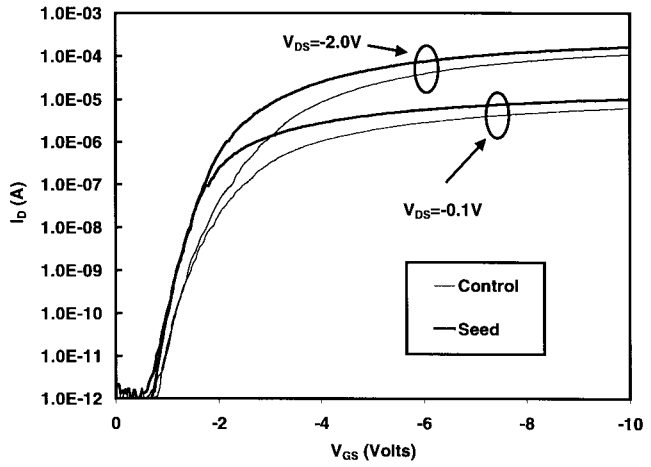
The effect of overall device geometry on seeding efficiency was also analyzed. The variation in mobility improvement is shown as a function of both channel length and width in Fig. 6.

TABLE I
SUMMARY OF DEVICE CHARACTERISTICS ($W/L = 0.9\ \mu m/0.7\ \mu m$).

Parameter	NMOS		PMOS	
	Unseeded	Dual-seeded	Unseeded	Dual-seeded
Field-effect mobility (cm^2/V-s)	100	254	70	101
Sub-threshold slope (V/dec.)	0.22	0.22	0.25	0.22
Leakage current (pA/μm)	5	7	1	1



(a)



(b)

Fig. 4. Electrical characteristics of (a) NMOS and (b) PMOS TFT's ($W/L = 0.9\ \mu m/0.7\ \mu m$).

Note that the smallest devices show the most improvement, as noted above. A crucial factor affecting the implementation of any lateral crystallization technology is that of uniformity. The mobility distribution achieved using the two seeding structures is contrasted to unseeded devices in Table II.

V. DISCUSSION

The efficiency of seeding is apparent from Fig. 2; every seed point exhibits the existence of polycrystalline material.

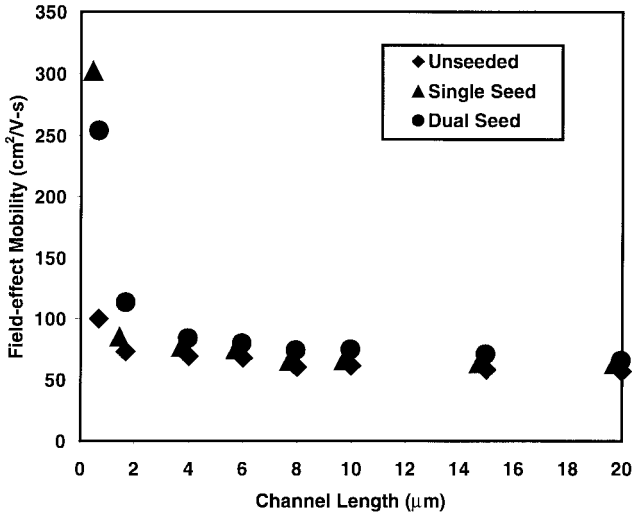


Fig. 5. Variation in field-effect mobility with channel length.

These nucleated regions result in the formation of laterally crystallized grains away from the seed point into the device channel. Different orientations have different growth rates, and therefore, high growth rate orientations tend to dominate. This leads to the prevalence of a majority of devices with essentially one laterally crystallized grain extending into the channel from each seed point, resulting in the relatively good uniformity detailed in Table II for dual-seeded devices.

The difference in performance and uniformity obtained from dual-seeded and single-seeded devices is explained upon consideration of the effect of device geometry upon performance. For large devices, the laterally crystallized region is a relatively small fraction of the overall channel; typical laterally crystallized grains have been found to be approximately 1 μm long. Therefore, the resulting improvement in performance is marginal. Since the dual seeded devices have two laterally crystallized regions, they exhibit better performance than the single-seeded devices, which have only one laterally crystallized region. As the channel length and width are reduced, the laterally crystallized region becomes a larger fraction of the overall device. This is shown schematically in Fig. 7. For extremely small devices, the channel becomes almost a single grain (for the single-seeded devices) or two grains (for the dual-seeded structures). This results in the crossover in performance noted in Fig. 5. Since a grain boundary is inherently located in the channel of the dual-seeded devices, this is a

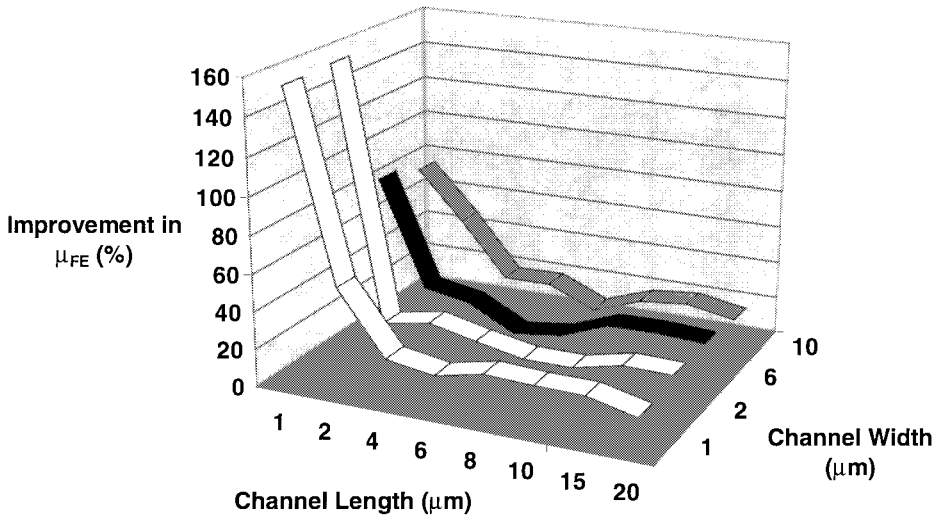


Fig. 6. Variation in mobility improvement with device size.

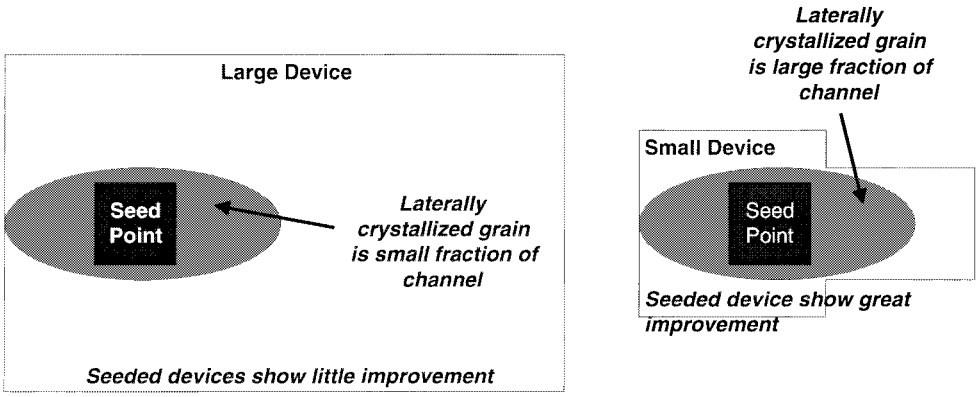


Fig. 7. Schematic view of lateral crystallization in the device channel.

TABLE II
SUMMARY OF INTRAWAFER MOBILITY UNIFORMITY ($W/L = 0.9\ \mu\text{m}/0.7\ \mu\text{m}$)

Process	Mobility (cm^2/V-s)	Variation	Notes
Unseeded	100	40%	Typical distribution
Dual-Seeded	254	20%	Slightly lopsided
Single-Seeded	303	40%	Extremely long tail

limiting factor the performance enhancement achievable using a dual-seeding scheme.

The uniformity of dual-seeded small devices is better than unseeded devices because the two seeded grains impinge to form a two-grain structure in the majority of devices. This is because the overall laterally crystallized region can extend as much as 2 μm, due to the summation of the two grains, and is therefore much larger than the channel dimensions. In single-seeded devices, on the other hand, the grain size is the same or less than the device size (upon inclusion of the separation of the seed point from the channel, approximately 0.7 μm). Therefore, though performance is improved in many devices, uniformity is poor due to the statistical variations in the extent of lateral crystallization. This also explains the one-sided population distribution noted in Table II.

Based on the results and analysis detailed above, it is apparent that excellent performance can be obtained using this technology, through the elimination of grain boundaries from within the channel of the devices. Even from the large devices detailed in this work, in which the complete removal of grain boundaries is prevented by the maximum achievable grain size, it is apparent that substantial performance improvement is achievable. Further scaling to smaller devices should enable complete lateral crystallization of the channel. However, as is apparent from Fig. 3, several intra-grain defects are still in existence. These degrade the device performance to below that of bulk devices, and result in the poor sub-threshold slope noted in Table I.

To develop this technology to its full potential, it will be necessary to reduce the number of intra-grain defects within the channel. One way of achieving this is through the replacement of silane with disilane, allowing for more optimized low-temperature, high-deposition rate (and therefore more amorphous) films. This will result in a lower density of defects through a reduction in the nucleation rate and also in an increased average grain size [14]. The increase in average grain

size will result in improved uniformity for smaller devices. Furthermore, the use of this technology in deep-submicron devices, as mandated by VLSI, should enable the fabrication of extremely high-performance devices offering good uniformity.

The overall thermal budget used in the crystallization process is low. The maximum temperature excursion is 550 °C, excluding the gate oxidation step. Replacement of this thermal oxide dielectric with a high-quality deposited dielectric will further reduce the thermal budget, making the process fully compatible with the bulk devices existing on lower levels. Obviously, interconnection of multiple layers of active devices is a significant challenge. Two levels of devices could be interconnected using modified conventional location interconnect and plug technologies. Advances in plug technologies should enable the interconnection of these devices, resulting in the development of a vertically integrated, high-performance CMOS technology for next-generation giga-scale integration applications. The device technology described in this work may also find application in the fabrication of high-performance pixel and integrated driver circuitry for flat-panel display applications.

VI. Conclusions

A novel technique to fabricate high-performance laterally-crystallized thin film transistors has been described. Germanium seeding is used to nucleate the lateral crystallization of amorphous silicon films using a low thermal budget, CMOS-compatible process. The resulting film is used as the channel film for the fabrication of high-performance TFT's. The seeding technique excels at short channel lengths, making it extremely promising as a means of fabricating devices offering near-single-crystal performance on insulating layers. Therefore, the technique can be used to enable the vertical integration of CMOS devices for 3-D VLSI applications.

Experimental results show that the technique can be used in the fabrication of essentially single-grain transistors. Extension of the technology using advanced deposition processes and deep-submicron devices should enable the development of a technology for the manufacture of high-performance TFT's for vertically integrated circuit applications, enabling higher chip speeds through reduced interconnect delays and substantially increased packing densities.

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Vivek Subramanian (S'94), for a photograph and biography, see p. 1695 of the August 1998 issue of this Transacations.

Krishna C. Saraswat (M'70–S'85–F'89), for a photograph and biography, see p. 1695 of the August 1998 of this Transacations.