

12-14-2012

High Performance Multilayer MoS₂ Transistors with Scandium Contacts

Saptarshi Das

Birck Nanotechnology Center, Purdue University, sdas@purdue.edu

Hong-Yan Chen

Birck Nanotechnology Center, Purdue University, chen200@purdue.edu

Ashish Verma Penumatcha

Birck Nanotechnology Center, Purdue University, apenumat@purdue.edu

Joerg Appenzeller

Birck Nanotechnology Center, Purdue University, appenzeller@purdue.edu

Follow this and additional works at: <http://docs.lib.purdue.edu/nanopub>



Part of the [Nanoscience and Nanotechnology Commons](#)

Das, Saptarshi; Chen, Hong-Yan; Penumatcha, Ashish Verma; and Appenzeller, Joerg, "High Performance Multilayer MoS₂ Transistors with Scandium Contacts" (2012). *Birck and NCN Publications*. Paper 1317.
<http://dx.doi.org/10.1021/nl303583v>

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

High Performance Multilayer MoS₂ Transistors with Scandium Contacts

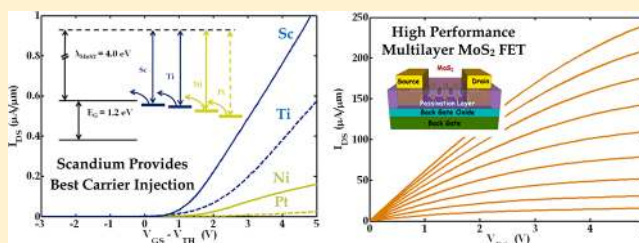
Saptarshi Das,* Hong-Yan Chen, Ashish Verma Penumatcha, and Joerg Appenzeller

Birk Nanotechnology Center & Department of ECE, Purdue University, West Lafayette, Indiana, United States

S Supporting Information

ABSTRACT: While there has been growing interest in two-dimensional (2-D) crystals other than graphene, evaluating their potential usefulness for electronic applications is still in its infancy due to the lack of a complete picture of their performance potential. The focus of this article is on contacts. We demonstrate that through a proper understanding and design of source/drain contacts and the right choice of number of MoS₂ layers the excellent intrinsic properties of this 2-D material can be harvested. Using scandium contacts on 10-nm-thick exfoliated MoS₂ flakes that are covered by a 15 nm Al₂O₃ film, high effective mobilities of 700 cm²/(V s) are achieved at room temperature. This breakthrough is largely attributed to the fact that we succeeded in eliminating contact resistance effects that limited the device performance in the past unrecognized. In fact, the apparent linear dependence of current on drain voltage had mislead researchers to believe that a truly Ohmic contact had already been achieved, a misconception that we also elucidate in the present article.

KEYWORDS: 2-d semiconductor, layered dichalcogenide, MoS₂, field-effect transistor (FET), contact, mobility



Low-dimensional materials in general and two-dimensional (2-D) layered materials in particular are interesting not only because they provide access to novel physical phenomena, but also because their unique electrical, optical, mechanical, and chemical properties make them attractive from a technological standpoint. Graphene, hexagonal boron nitride (h-BN), and more recently 2-D nanostructures of Bi₂Se₃ and Bi₂Te₃ (topological insulator materials)^{1–5} are considered as promising candidates for various future nanoelectronics applications. Another class of 2-D materials that is receiving an increasing amount of scientific attention, is the rich family of transition metal dichalcogenides comprised of MoS₂, WS₂, WSe₂, and many more.^{6–12} While graphene shows the highest reported mobility in excess of 100 000 cm²/(V s)¹³ within this family, the absence of an energy gap in the electronic band structure of graphene paves the way for the exploration of semiconducting 2D materials like MoS₂^{14,15} and others.

MoS₂ is a semiconductor with an indirect bandgap of 1.2 eV (single-layer MoS₂ shows a direct bandgap of 1.8 eV, and bilayer MoS₂ exhibits an indirect bandgap of 1.3 eV), an electron affinity of 4.0 eV^{16,17} and a maximum reported mobility of 517 cm²/(V s)¹⁷ Single and multilayer MoS₂ field-effect transistors (FETs) with on/off-current ratios as high as 10⁸ and steep subthreshold swing (74 mV/decade) have already been demonstrated in a top-gated transistor architecture.^{8,18–20} Moreover, initial studies also indicate that MoS₂ may be useful for sensing and energy-harvesting applications.^{21,22} However, one of the major performance-limiting factors for any low-dimensional material in general and 2-D materials in particular is the interface. While the focus has been

on evaluating and solving interface problems between the gate dielectric and the 2-D semiconducting channel material to obtain ultimate gate control,^{23,24} much less attention has been paid to the metal/semiconductor contact interface at the source and drain end.

In this Letter, we present a thorough experimental study of contacts to MoS₂ using in particular low work function metals like scandium ($\Phi_M = 3.5$ eV) and titanium ($\Phi_M = 4.3$ eV) to shine some light on the impact of Schottky barriers on the carrier transport in MoS₂ FETs. Our study is complemented by comparing the results obtained with large work function metals like nickel ($\Phi_M = 5.0$ eV) and platinum ($\Phi_M = 5.9$ eV). Recently a number of articles^{8,15,25,26} have utilized large work function metals and yet reported excellent n-type contact formation and electron injection without emphasizing the fact that this experimental observation is rather peculiar.²⁷ From a detailed temperature-dependent study that considers both thermionic emissions over the Schottky barrier as well as thermally assisted tunneling through the same, we have extracted the Schottky barrier height for the various metal electrodes and found ~230 meV for platinum, ~150 meV for nickel, ~50 meV for titanium, and ~30 meV for scandium. Our experiments provide unambiguous evidence that the MoS₂-to-metal interface is strongly impacted by Fermi level pinning close to the conduction band of the MoS₂ similar to the case of many III–V materials. While earlier reports had claimed that

Received: September 26, 2012

Revised: November 29, 2012

Published: December 14, 2012

gold ($\Phi_M = 5.4$ eV)-to-MoS₂ contacts are Ohmic,^{8,15,25} our results clearly indicate the existence of Schottky barriers for large work function metals like Ni and Pt.

We have also evaluated the field effect mobility of multilayer MoS₂ flakes for different metal contacts and different flake thicknesses using a back-gated transistor geometry. As expected, the extracted mobility values were strongly dependent on the metal-to-MoS₂ contact interface; that is, the intrinsic mobility is *masked* easily by the presence of the aforementioned Schottky barrier at the source and drain contacts. We have also observed a nonmonotonic trend in the intrinsic field effect mobility of MoS₂ as a function of the MoS₂ layer thickness. To describe our experimental findings we have employed a model including Thomas–Fermi charge screening and interlayer coupling. The highest mobility values were obtained for a finite layer thickness of around 10 nm. In this case the extracted mobility values are 21, 90, 125, and 184 cm²/(V s) for Pt, Ni, Ti, and Sc contacts, respectively, clearly indicating that improving the contact quality is essential to harvest the intrinsic material properties.

A significant enhancement in the field effect mobility up to 700 cm²/(V s) is achieved by covering the top of the back-gated MoS₂ transistor with a thin layer of 15-nm-thick Al₂O₃. While the mobility we find is substantially higher than previously reported, the effect itself had been also observed by other groups.^{8,10,12}

Extraction of Schottky Barrier Height. Single-layer MoS₂ consists of a stack of three hexagonally packed atomic layers of sulfur–molybdenum–sulfur with strong intralayer covalent bonding.^{16,17} In contrast, bulk MoS₂ is a stack of single layers, held together by weak van der Waals interlayer interaction and, therefore, allows for micromechanical exfoliation of mono or few layers—similar to the fabrication of graphene from graphite. Figure 1a,b shows atomic force microscopy (AFM) and optical images of a 3 nm (4 monolayer) thick MoS₂ flake, exfoliated using standard scotch tape technique on 100 nm silicon dioxide (SiO₂) substrate with underlying highly doped silicon. Figure 1c,d shows a 3-D sketch and an scanning electron microscopy (SEM) image of a prototype back-gated MoS₂ transistor used for our contact study. Standard

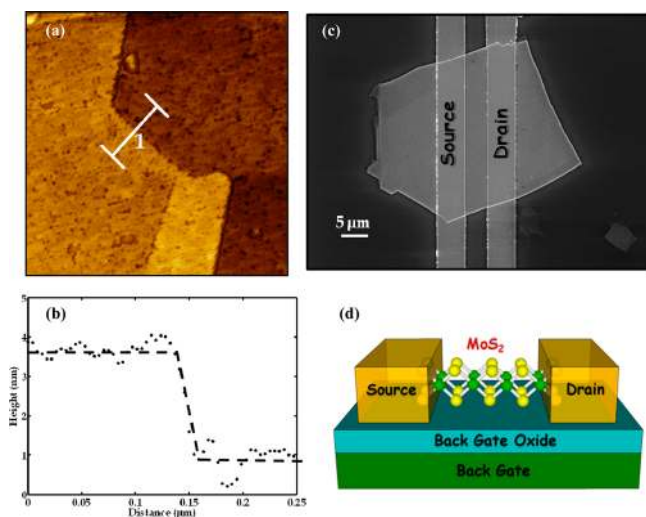


Figure 1. (a) AFM image and (b) AFM height profile of a 3 nm thin MoS₂ flake. (c) SEM image and (d) 3-D cartoon of a prototype back-gated MoS₂ transistor used for the study.

lithographic techniques were employed to pattern the source/drain contacts, and electron beam evaporation was used to deposit the desired metal contacts (Sc, Ti, Ni, and Pt). The channel length for all of the devices is 5 μ m, and the flake thicknesses range between 2 and 12 nm (3–18 mono layers). The deposited source/drain contact film thickness is 50 nm for Ti, Ni, and Pt while to avoid damaging of the contacts in case of scandium required a 30 nm Sc/20 nm Ni stack.

Figure 2a shows the expected line-up of the metal Fermi level with the electronic bands of MoS₂ if only the difference of the

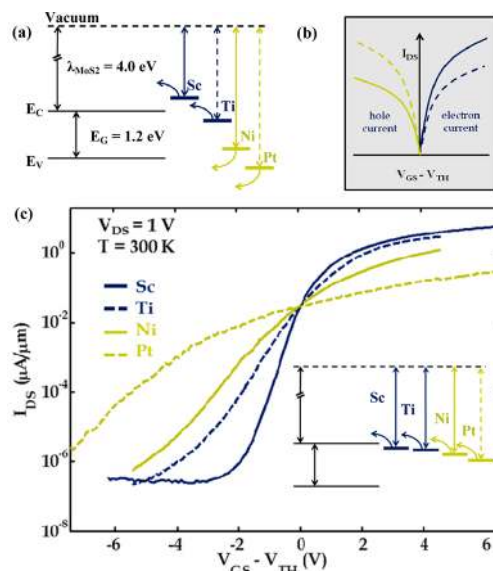


Figure 2. (a) Expected (not correct) line-up of metal Fermi level with the electronic bands of MoS₂ flake if only the difference of the electron affinity of MoS₂ and the work function of the corresponding metal is considered. (b) The cartoon of expected transfer characteristics based on part a. (c) Transfer characteristics of back-gated 6-nm-thick MoS₂ transistor with Sc, Ti, Ni, and Pt metal contacts. The inset shows the actual line-up based on the experimental data.

electron affinity of MoS₂ and the work function of the corresponding metal is considered. Electron injection should occur for Sc and Ti, while Ni and Pt are expected to provide access to the valence band and should thus enable hole injection. Figure 2b illustrates the expected device characteristics qualitatively under this assumption. On the other hand Figure 2c shows the experimental transfer characteristics of back gated MoS₂ transistors with Sc, Ti, Ni, and Pt metal contacts after adjusting for the threshold voltage shift. The threshold voltages for Sc, Ti, Ni, and Pt contact devices were found to be on average (sampled over 4–5 devices) –6.0, –1.0, 1.5, and 4.0 V, respectively. Threshold voltages are defined by the deviation of the I_{DS} versus V_{GS} characteristics from their exponential behavior in the subthreshold regime. Note that the trend in the values of the threshold voltages is consistent with the observed trend in on-currents.²⁸ Interestingly, all of the metal contacts exhibit n-type FET characteristics, which indicate that the Fermi levels for all of these metals line-up close to the conduction band edge of MoS₂ as shown in the inset of Figure 2c. Also, there is a clear trend of decreasing on-state performance, that is, decreasing on-current for positive $V_{GS} - V_{TH}$ from Sc to Pt, suggesting a change in the charge injection properties of the various contact metals. As will be discussed below these findings are consistent with Schottky

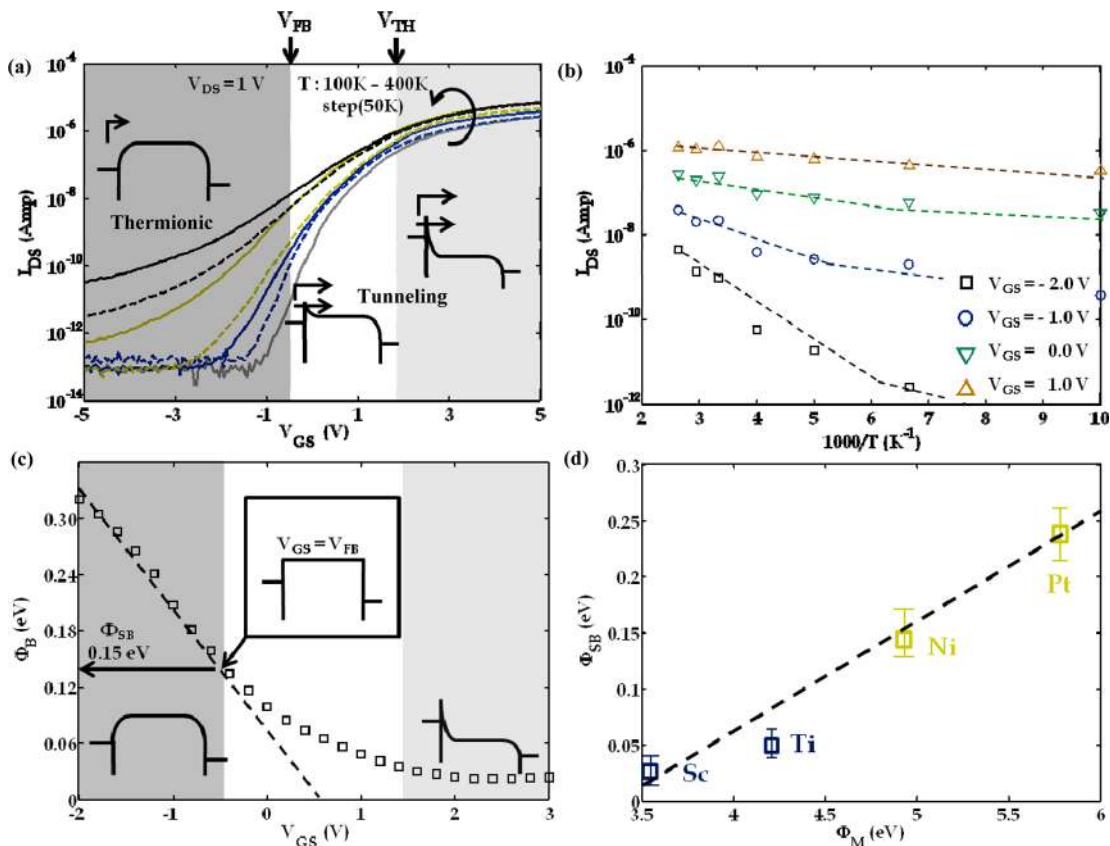


Figure 3. (a) Experimental transfer characteristics of a back-gated MoS₂ transistor with Ni contacts at different operating temperatures. The insets represent the energy band diagrams corresponding to the applied gate biases in three distinct regions: below flat band, below threshold, and above threshold. (b) Arrhenius-type plot constructed using part a at different gate voltages and (c) extracted effective barrier height (Φ_B) as a function of applied gate voltages for Ni contact devices. (d) Extracted true Schottky barrier height Φ_{SB} for different work function metals like Sc, Ti, Ni, and Pt. The dotted line is a guide to the eyes.

barriers of varying heights formed at the metal-to-channel interface, and a detailed temperature-dependent study has been used to quantitatively analyze those barriers.

As described in greater detail in ref 29, tunneling through Schottky barrier at the source-to-channel interface is not only limiting the charge injection in the device on-state but also plays a critical role when evaluating the device off-state in the subthreshold region of the transistor. In fact it is the thermally assisted tunneling that impacts the inverse subthreshold slope in Schottky barrier devices in general.³⁰ The band bending diagrams in Figure 3a illustrate the contributions of thermionic emission current component ($I_{\text{thermionic}}$) and the thermally assisted tunneling current component ($I_{\text{tunneling}}$) under different gate voltage conditions. Figure 3a shows the change in current through the device with the gate voltage for different temperatures that are used to create the Arrhenius plot in Figure 3b. When evaluating the current flow through the device as a function of temperature, both contributions— $I_{\text{thermionic}}$ and $I_{\text{tunneling}}$ —need to be considered. The band diagrams also illustrate that the tunneling current can only be ignored when the gate voltage is below the flat band voltage V_{FB} . If one can identify V_{FB} , the Arrhenius plot for this gate voltage will reveal the true Schottky barrier height Φ_{SB} .³¹ To do so, the slope of the curves in Figure 3b in the high-temperature region is analyzed assuming conventional thermionic emission theory. Using the equation $I_{DS} = AT^2 \exp((q\phi_B)/(k_B T)) [1 - \exp(-(qV_{DS})/(k_B T))]$, the effective Schottky barrier height is extracted. In this equation I_{DS} is the current through the

device, A is the Richardson's constant, k_B is the Boltzmann constant, q is the electronic charge, T is the temperature, and V_{DS} is the source to drain bias. V_{FB} can now be readily determined from Φ_B (at the source-to-channel interface) as a function of gate voltage. Figure 3c shows our findings for Ni electrodes. For sufficiently negative gate voltages the effective barrier height extracted from Figure 3b linearly responds to the gate voltage V_{GS} (also see the Supporting Information). This is a result of the fact that only $I_{\text{thermionic}}$ determines the current flow through the device. It is when Φ_B deviates from this linear trend when $I_{\text{tunneling}}$ becomes relevant and V_{FB} is reached. Note that the threshold voltage V_{TH} that defines the device on-state is larger than V_{FB} . From Figure 3c, a true Schottky barrier height of 150 meV is extracted. Figure 3c also illustrates how the wrong choice of gate voltage—one that is larger than V_{FB} —can easily result in the extraction of a barrier height that is too small since thermally assisted tunneling adds another current component that is not included in the standard thermal emission theory. It is this additional tunneling current that is responsible for a perceived “Ohmic contact” at the interface even for substantial Schottky barrier heights. The key is that an ultrathin channel like MoS₂ will always give rise to a short tunneling distance and thus substantial tunneling currents as has been discussed in greater detail previously.^{32,33}

Figure 3d shows the extracted Schottky barrier heights for the different metals used for our contact study as a function of their corresponding work functions. We find Schottky barrier heights of 230, 150, 50, and 30 meV for Pt, Ni, Ti, and Sc,

respectively. In total more than 4–5 devices were characterized per metal contact type under investigation. The extracted slope $d\Phi_{SB}/d\Phi_M$ of around 0.1 (note that this number is approximately 0.27 in the case of silicon³⁴) indicates that different from previous assumptions strong pinning at the metal/MoS₂ interface determines the line-up between the metal Fermi level and the conduction band of MoS₂. It also explains why only n-type characteristics are obtained in all reported cases²⁷ even if large work function metals had been used. Note that if the chemical reactivity, deposition-induced mechanical deformation, or wettability of the metals was to influence the Schottky barrier height analysis significantly, the linear trend in Figure 3d would be obscured.

Impact of Metal Contact. Next we turn our attention to the impact of the Schottky barrier heights on the device characteristics. The inset of Figure 4 shows the output

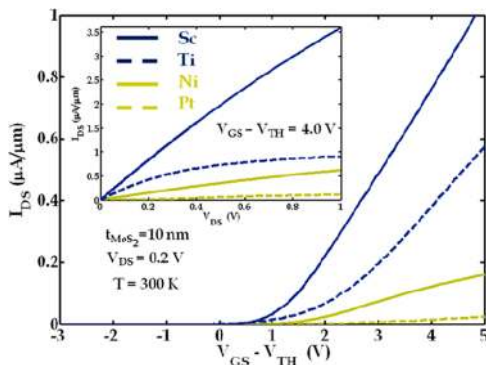


Figure 4. Transfer characteristics of 10 nm thin MoS₂ back-gated transistors with Sc, Ti, Ni, and Pt metal contacts at 300 K for $V_{DS} = 0.2$ V. The inset shows the output characteristics of the corresponding devices for a gate voltage overdrive of 4.0–5.0 V.

characteristics of a back-gated ~ 10 -nm-thick MoS₂ transistors at 300 K for different metal contacts for the same gate voltage overdrive ($V_{GS} - V_{TH} = 4$ V) which corresponds to a carrier concentration of $\sim 1.4 \times 10^{12}/\text{cm}^2$. The current through the Pt contact device shows an exponential dependence on the source

to drain bias (V_{DS}) for low V_{DS} values which is consistent with the fact that Pt exhibits the largest Schottky barrier height of 230 meV. The current through Ni contacted devices, however, shows a linear dependence on V_{DS} despite the presence of a sizable Schottky barrier of 150 meV at the Ni–MoS₂ interface. As discussed above, thermally assisted tunneling is responsible for this finite temperature effect, and consequently a linear relationship between current and drain voltage does not necessarily indicate an Ohmic contact.³³ The increasing magnitude of the current from 0.1 to 0.7 to 1.0 to 4.8 $\mu\text{A}/\mu\text{m}$ at a V_{DS} of 1 V for Pt, Ni, Ti, and Sc contacted devices, respectively, is consistent with the fact that smaller Schottky barrier heights at the metal-to-MoS₂ interface result in better carrier injection and hence smaller contact resistance values.

Figure 4 also shows the transfer characteristics of 10-nm-thick MoS₂ transistors with Sc, Ti, Ni, and Pt metal contacts for $V_{DS} = 0.2$ V at room temperature. The transconductance g_m (defined as $g_m = dI_{DS}/dV_{GS}$) normalized by the width (g_m/W) shows a monotonic increase from 0.03, 0.14, 0.20 to 0.28 $\mu\text{S}/\mu\text{m}$ from Pt, Ni, Ti to Sc contacted devices. Field effect mobility values of the ~ 10 nm MoS₂ flakes were extracted using the conventional equation of $g_m = \mu_n C_{OX}(W/L)V_{DS}$ at low $V_{DS} = 0.2$ V (where μ_n is the field effect mobility and W and L are the channel width and the channel length, respectively, $C_{OX} = \epsilon_{OX}/d_{OX}$, where ϵ_{OX} is the dielectric constant and d_{OX} is the thickness of the gate oxide, $d_{OX} = 100$ nm and for SiO₂, $\epsilon_{OX} = 3 \times 10^{-11}$, which gives $C_{OX} \sim 3 \times 10^{-4}$ F/m², and finally $L \sim 5$ μm). The extracted effective field-effect mobility values were found to be 21, 36, 125, and 184 $\text{cm}^2/(\text{V s})$ for Pt, Ni, Ti, and Sc contacted devices respectively, clearly highlighting how even small Schottky barriers can impact the mobility extraction significantly. Note that the maximum values of g_m were used to extract the mobility values. The above findings clearly indicate the importance of proper contact formation to harvest the intrinsic properties of novel nano materials and explain the extremely high mobility values reported below by the use of Sc contacts. Also note that the mobility values extracted by Radisavljevic et al.,⁸ for monolayer MoS₂ and Wang et al.,¹² for bilayer MoS₂ using a back-gated device geometry are similar to ours prior to the deposition of a high- k dielectric layer and are

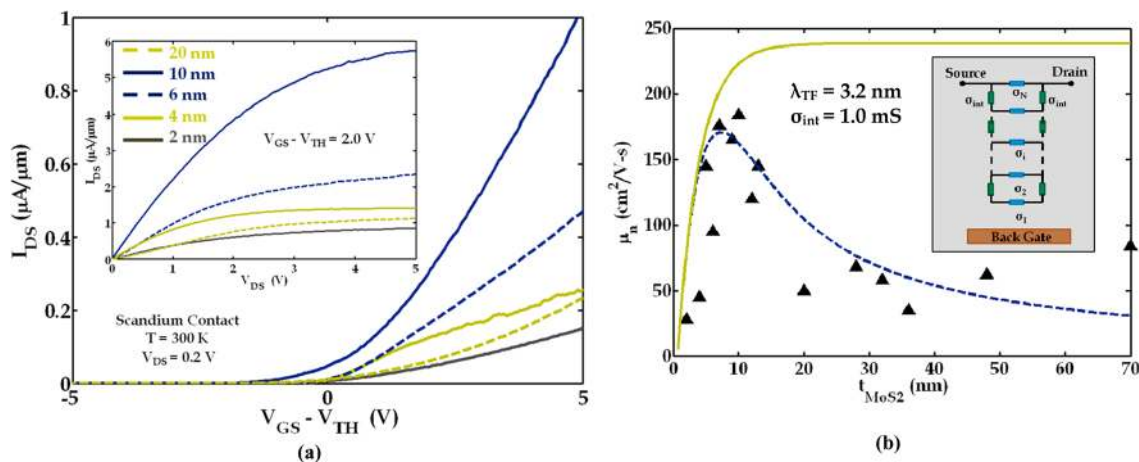


Figure 5. (a) Transfer characteristics of 20, 10, 6, 4, and 2 nm thick MoS₂ field effect transistor with Sc as the source/drain contacts at room temperature for $V_{DS} = 0.2$ V. The inset shows the output characteristics for the same flakes for a gate overdrive voltage of 2 V. (b) The extracted effective field effect mobility as a function of the MoS₂ layer thickness. The dotted line is a fit to the experimental data using a model (inset) that includes Thomas–Fermi screening with $\lambda = 3.0$ nm and interlayer conductivity with $\sigma_{int} = 1$ mS. The solid line is the simulated field effect mobility without any interlayer resistance.

10 and 15 $\text{cm}^2/(\text{V s})$, respectively, using Au and Ti/Au contacts. This is consistent with our findings since Au is a high work function metal ($\Phi_{\text{M}} = 5.6 \text{ eV}$) and mono and bilayer flakes have larger bandgaps that translate into even higher Schottky barrier heights as reported here. To emphasize our main finding again: the extracted mobility values for fully gated metal contacted MoS_2 FETs do not reflect the intrinsic mobility of MoS_2 unless highly transmissive contacts as scandium are used.³⁵

Ideal Layer Thickness. Back-gated MoS_2 FETs with Sc as the source and the drain contacts were fabricated using flake thicknesses ranging from 2 to 70 nm. Figure 5a shows the transfer and output characteristics (inset) of 2, 4, 6, 10, and 20 nm thick MoS_2 FETs. The extracted room temperature field-effect mobility values were found to depend strongly on the flake thickness in a nonmonotonic fashion as shown in Figure 5b. This nonmonotonic trend suggests that, to harvest the maximum potential of MoS_2 for high performance device applications, a layer thickness in the range of 6–12 nm would be ideal. The nonmonotonic trend can be readily explained within the extension of a resistor network model (see inset of Figure 5b) that we successfully employed before to describe transport in multilayer graphene devices.³⁶ The key is that metal source/drain contacts are connected only directly to the top MoS_2 layer, while access to lower layers involves additional interlayer resistors (σ_{int} is the interlayer conductivity). Gating on the other hand impacts the lowest layers most, and charge screening results in a decreasing number of charges for top MoS_2 layers. For small layer thicknesses the absence of sufficient screening of the substrate impact results in a lower mobility value than observed in bulk MoS_2 .³⁷ For large layer thicknesses it is the finite interlayer conductivity σ_{int} that results in an effectively (not intrinsically) lower total mobility of the system (as the Schottky barrier in case of Pt resulted in a lower effective mobility). The combination of these two components gives rise to a maximum mobility value for a finite layer thickness. Our two-parameter model can be used to fit the experimental data well if we assume a Thomas–Fermi screening length of $\lambda_{\text{TF}} \sim 3 \text{ nm}$ and an interlayer conductivity of 1 mS (see dotted curve in Figure 5b). Note that the screening length is about 5 times larger than in the case of multilayer graphene while the interlayer conductivity is about 8 times smaller. Mobility plots similar to the one shown above are observed for all metal contacts providing further evidence of the applicability of the proposed resistor network. In general, the use of a finite number of MoS_2 layers is beneficial since the impact of the substrate on the device performance can be eliminated.

High- k for High Performance. Finally, to prove that the above-reported mobility values are on par or even exceed previously reported experimental data, we followed an approach reported before that has shown to result in a substantial improvement in mobility after atomic layer deposition (ALD) of high- k materials onto MoS_2 .^{8,11,12,18} We have combined this treatment with our findings about the ideal contact and layer thickness from above by depositing 15 nm of Al_2O_3 on top of our back-gated transistors. Figure 6 shows the measured output and transfer characteristics of a 10 nm MoS_2 FET with scandium contacts and ALD layer. The effective field-effect mobility of the MoS_2 flake extracted assuming a parallel plate capacitor arrangement (ignoring any possible impact of fringing fields and the top dielectric) is increased by a factor of 3.8, from 184 to 700 $\text{cm}^2/(\text{V s})$. As mentioned above, this high value is a

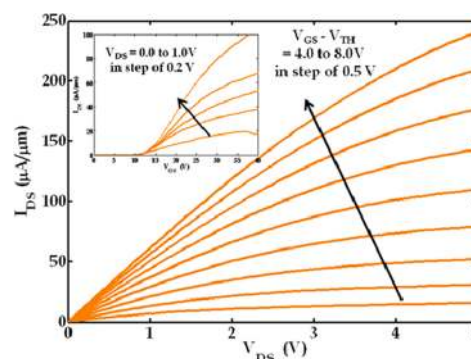


Figure 6. Output characteristics of a high-performance MoS_2 transistor exhibiting extremely high mobility, saturation current density, and transconductance for different gate overdrive voltages with 15 nm of high- k dielectric (Al_2O_3). The inset shows transfer characteristics of the same device for different drain bias values.

consequence of the use of low Schottky barrier scandium contacts and the suppression of substrate effects through the use of a sufficiently thick MoS_2 flake. A saturation current density of 240 $\mu\text{A}/\mu\text{m}$ for a carrier density of $\sim 2.8 \times 10^{12}/\text{cm}^2$ and a transconductance of 4.7 $\mu\text{S}/\mu\text{m}$ at $V_{\text{DS}} = 1.0 \text{ V}$ are obtained for a channel length of 5 μm . Both values are higher than previously reported data when considering the scaling aspects of FETs.^{12,39}

Conclusion. In conclusion, we have performed a thorough experimental study to determine the ideal metal contact for the evaluation of intrinsic transport properties of MoS_2 thin flake field effect transistors. Our findings indicate that the metal-to- MoS_2 interface is strongly impacted by Fermi level pinning close to the conduction band of MoS_2 . Lower work function metals like Sc have been employed to form improved contacts with thin MoS_2 flakes, resulting in high carrier injection and lower contact resistances. We have observed a nonmonotonic trend in the effective field effect mobility of MoS_2 flakes as a function of the layer thickness which can be modeled using a resistor network and considering proper screening between individual layers. The intrinsic field-effect mobility of a 10-nm-thick multilayer MoS_2 flake was found to be as high as 184 $\text{cm}^2/(\text{V s})$ and can be significantly boosted up to 700 $\text{cm}^2/(\text{V s})$ using a high- k dielectric environment. Record high saturation current densities of 240 $\mu\text{A}/\mu\text{m}$ for relatively low carrier concentrations of $\sim 2.8 \times 10^{12}/\text{cm}^2$ and record high transconductance values of 4.7 $\mu\text{S}/\mu\text{m}$ were measured providing encouraging news about the usefulness of MoS_2 for high-performance electronics applications.

■ ASSOCIATED CONTENT

§ Supporting Information

Extraction of Schottky barrier height: Sc, Ti, Ni, and Pt contact. This material is available free of charge via the Internet at <http://pubs.acs.org>.

■ AUTHOR INFORMATION

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

We would like to acknowledge Dave Lubelski for helping with the Sc deposition and Ali Razavieh for ALD deposition. This work was supported by the Nanotechnology Research Initiative

(NRI) through a supplement to the Network for Computational Nanotechnology (NCN), which is supported by National Science Foundation (NSF) under grant no. EEC-0634750.

REFERENCES

- (1) Novoselov, K. S.; Jiang, D.; Schedin, F.; Booth, T. J.; Khotkevich, V. V.; Morozov, S. V.; Geim, A. K. Two-dimensional atomic crystals. *Proc. Natl. Acad. Sci. U.S.A.* **2005**, *102*, 10451–53.
- (2) Kim, S.; Nah, J.; Jo, I.; Shahjerdi, D.; Colombo, L.; Yao, Z.; Tutuc, E.; Banerjee, S. K. Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. *Appl. Phys. Lett.* **2009**, *94*, 062107.
- (3) Lipp, A.; Schwetz, K. A.; Hunold, K. Hexagonal Boron Nitride: Fabrication, Properties and Applications. *J. Eur. Ceram. Soc.* **1989**, *5*, 3–9.
- (4) Avouris, P. Graphene: Electronic and Photonic Properties and Devices. *Nano Lett.* **2010**, *10*, 4285–94.
- (5) Zhang, H.; Liu, C.; Qi, X.; Dai, X.; Fang, Z.; Zhang, S. Topological insulators in Bi_2Se_3 , Bi_2Te_3 , and Sb_2Te_3 and with a single dirac cone on the surface. *Nat. Phys.* **2009**, *5*, 438–442.
- (6) Joensen, P.; Frindt, R. F.; Morrison, S. R. Single-layer MoS_2 . *Mater. Res. Bull.* **1986**, *21*, 457–461.
- (7) Wilson, J. A.; et al. The transition metal di-chalcogenides discussion and interpretation of the observed optical, electrical and structural properties. *Adv. Phys.* **1969**, *18*, 193–335.
- (8) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
- (9) Hwang, W. S.; Remskar, M.; Yan, R.; Protasenko, V.; Tahy, K.; Chae, S. D.; Zhao, P.; Konar, A.; Xing, H. G.; Seabaugh, A.; Jena, D. Transistors with chemically synthesized layered semiconductor WS_2 exhibiting 10^5 room temperature modulation and am-bipolar behavior. *Appl. Phys. Lett.* **2012**, *101*, 013107.
- (10) Fang, H.; Chuang, S.; Chang, T. C.; Takei, K.; Takahashi, T.; Javey, A. High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts. *Nano Lett.* **2012**, *12*, 3788–92.
- (11) Radisavljevic, B.; Whitwick, M. B.; Kis, A. Integrated Circuits and Logic Operations Based on Single-Layer MoS_2 . *ACS Nano* **2011**, *5*, 9934–38.
- (12) Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated Circuits Based on Bilayer MoS_2 Transistors. *Nano Lett.* **2012**, *12*, 4674–80.
- (13) Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh electron mobility in suspended graphene. *Solid State Commun.* **2008**, *146*, 351–55.
- (14) Yoon, Y.; Ganapathi, K.; Salahuddin, S. How Good Can Monolayer MoS_2 Transistors Be? *Nano Lett.* **2011**, *11*, 3768–73.
- (15) Chang, C.; Zhang, W.; Lee, Y.-H.; Lin, Y.-C.; Chang, M.-T.; Su, C.-Y.; Chang, C.-S.; Li, H.; Shi, Y.; Zhang, H.; Lai, C.-S.; Li, L.-J. Growth of Large-Area and Highly Crystalline MoS_2 Thin Layers on Insulating Substrates. *Nano Lett.* **2012**, *12*, 1538–44.
- (16) Han, S. W.; Kwon, H.; Kim, S. K.; Ryu, S.; Yun, W. S.; Kim, D. H.; Hwang, J. H.; Kang, J.-S.; Baik, J.; Shin, H. J.; Hong, S. C. Band-gap transition induced by interlayer van der Waals interaction in MoS_2 . *Phys. Rev. B* **2011**, *84*, 045409.
- (17) Salmani, J. M.; Tan, Y.; Klimeck, G. Single Layer MoS_2 Band Structure and Transport. *Int. Semiconductor Device Res. Symp.* **2011**, pp 1–2; DOI: 10.1109/ISDRS.2011.6135408.
- (18) Liu, H.; Ye, P. D. MoS_2 Dual-Gate MOSFET with Atomic-Layer-Deposited Al_2O_3 as Top-Gate Dielectric. *IEEE Trans. Electron Devices* **2012**, *33*, 546–48.
- (19) Qiu, H.; Pan, L.; Yao, Z.; Li, J.; Shi, Y.; Wang, X. Electrical characterization of back-gated bi-layer MoS_2 field-effect transistors and the effect of ambient on their performances. *Appl. Phys. Lett.* **2012**, *100*, 123104.
- (20) Lee, K.; Kim, H.-Y.; Lotya, M.; Coleman, J. N.; Kim, G.-T.; Duesberg, G. S. Electrical Characteristics of Molybdenum Disulfide Flakes Produced by Liquid Exfoliation. *Adv. Mater.* **2011**, *23*, 4178–82.
- (21) Eda, G.; Yamaguchi, H.; Voiry, D.; Fujita, T.; Chen, M.; Chhowalla, M. Photoluminescence from Chemically Exfoliated MoS_2 . *Nano Lett.* **2011**, *11*, 5111–16.
- (22) Li, H.; et al. Fabrication of Single- and Multilayer MoS_2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature. *Small* **2012**, *8*, 63–67.
- (23) Xie, R.; Phung, T. H.; Yu, M.; Zhu, C. Effective Surface Passivation by Novel SiH_4 - NH_3 Treatment and BTI Characteristics on Interface-Engineered High-Mobility HfO_2 -Gated Ge pMOSFETs. *IEEE Trans. Electron Devices* **2010**, *57*, 1399–1407.
- (24) Martens, K.; Chui, C. O.; Brammertz, G.; de Jaeger, B.; Kuzum, D.; Meuris, M.; Heyns, M.; Krishnamohan, T.; Saraswat, K.; Maes, H. E.; Groeseneken, G. On the Correct Extraction of Interface Trap Density of MOS Devices with High-Mobility Semiconductor Substrates. *IEEE Trans. Electron Devices* **2008**, *55*, 547–56.
- (25) Neal, A. T.; Liu, H.; Gu, J. J.; Ye, P. D. Metal Contact to MoS_2 . *Proc. DRC* **2012**, 65–66.
- (26) Popov, I.; Seifert, G.; Tománek, D. Designing electrical contacts to MoS_2 monolayers: A computational study. *Phys. Rev. Lett.* **2012**, *108*, 156802.
- (27) We note at this point that an article by Fontana et al.³⁸ found p-type conduction with Pd contacts. This data set is the only one we are aware of that does not follow the trends published by other authors using large work function metal contacts and observed by us as described here.
- (28) For scaled gate oxides, the threshold voltage of a metal contacted field-effect transistor is in general expected to be independent of the contact metal used. However, the relatively thick back gate oxide used in our study results in the contact Schottky barrier height impacting the actual threshold voltage value due to a transmission probability substantially smaller than unity.
- (29) Appenzeller, J.; Radisavljević, M.; Knoch, J.; Avouris, Ph. Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors. *Phys. Rev. Lett.* **2004**, *92*, 048301.
- (30) Appenzeller, J.; Knoch, J.; Derycke, V.; Martel, R.; Wind, S.; Avouris, Ph. Field-Modulated Carrier Transport in Carbon Nanotube Transistors. *Phys. Rev. Lett.* **2002**, *89*, 126801.
- (31) Note that our Schottky barrier analysis does not take into account any temperature dependent scattering in the MoS_2 channel. However, because of the fact that typical scattering rates exhibit a power law dependence on temperature and not an exponential dependence as the Schottky barrier transmission probability, the slope of the Arrhenius type plot is believed to be a fairly accurate measure of the Schottky barrier heights.
- (32) Appenzeller, J.; Knoch, J.; Bjork, M. T.; Riel, H.; Schmid, H.; Riess, W. Towards nanowire electronics. *IEEE Trans. Electron Devices* **2008**, *54*, 2827–45.
- (33) Heinze, S.; Tersoff, J.; Martel, R.; Derycke, V.; Appenzeller, J.; Avouris, Ph. Carbon Nanotubes as Schottky barrier transistors. *Phys. Rev. Lett.* **2002**, *89*, 106801.
- (34) Sze, S. M. *Semiconductor Devices*, 2nd ed.; John Wiley & Sons: New York.
- (35) Note that even in the case of small Schottky barriers the term “Ohmic contacts” is ONLY justified if gating does not include the metal electrode-to-channel interface.
- (36) Sui, Y.; Appenzeller, J. Screening and Interlayer Coupling in multilayer graphene field effect transistors. *Nano Lett.* **2009**, *9*, 2973–77.
- (37) Any insulating substrate (gate oxides) has potential variations due to fixed charges that reside in them. Thicker the layer thickness higher is the potential variation.
- (38) Fontana, M.; Deppe, T.; Boyd, A. K.; Rinzan, M.; Liu, A. Y.; Paranjape, M.; Barbara, P. Photovoltaic effect in gated MoS_2 Schottky junctions. *arXiv:1206.6125*.
- (39) Lembke, D.; Kis, A. Breakdown of High Performance Monolayer MoS_2 Transistors. *ACS Nano* **2012**, *6*, 10070–75.