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INVITED REVIEW

High-performance N-polar GaN enhancement-mode device technology

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Online at stacks.iop.org/SST/28/074006**Abstract**

In this paper, we report the recent progress in the high-frequency performance of enhancement-mode devices in the novel N-polar GaN technology and provide a pathway for further scaling. The intrinsic advantages of electron confinement, polarization doping of the back-barrier and the absence of a source barrier in N-polar GaN technology were leveraged with polarization engineering with a top barrier for enhancement mode operation and advanced self-aligned source/drain technology for low parasitic access resistances. The scalability of the device structures are explored in terms of short-channel effects and high-frequency performance. Low-field electron mobility in vertically scaled channel was also investigated providing insights on the scattering mechanism.

(Some figures may appear in colour only in the online journal)

1. Introduction and background

Since the first report of GaN-based light-emitting diode and high-electron mobility transistors (HEMTs) [1, 2], there has been incredible progress in GaN electronics and optoelectronics technology with a broad range of applications. The unique properties of high-electron mobility in a polarization doped two-dimensional electron gas (2-DEG) in AlGa_xN/GaN hetero-structure and high breakdown enabled by the large bandgap of GaN has been an attractive feature of GaN electronic devices [3]. This distinct combination leads to high-frequency and high-voltage operation in GaN devices unlike the traditional III-V and Si electronics, with orders of magnitude higher power handling capabilities in microwave and mm-wave frequencies [4–7]. Aggressive gate length scaling of GaN devices can push the device operation well into near THz operation. Due to the high-voltage operation capability of these devices, they have the potential to operate in space that is not accessible to other technologies [8].

There has been remarkable progress in high-frequency GaN field-effect transistors (FETs) in recent years enabled by aggressive gate length scaling to 20 nm and also by drastic

reduction in parasitic source resistance by incorporating source/drain regrowth with peak reported current gain cutoff frequency of 370 GHz [9–14]. In order to maintain the electrostatic integrity of the ultra-scaled devices with tight gate control of the channel, new technologies with back-barrier for electron confinement are being pursued [14–16]. The novel N-polar GaN technology where the material is grown on (000–1) axis offers a natural back-barrier, which is an attractive option for ultra-scaled devices [17, 18]. In addition to providing electron confinement, it offers several other advantages for GaN transistors for high-frequency operation. N-polar GaN FETs with a top gate dielectric and a bottom charge inducing wide bandgap AlGa_xN back-barrier provide a structure similar to ultrathin body silicon-on-insulator (UTB-SOI) devices and hence have the potential advantage in scaling to sub-50 nm gate lengths. Moreover, the absence of a polarization inducing wide-bandgap AlGa_xN material on top of the channel removes the barrier to electron flow from the source contact to the 2-DEG, thus reducing the source parasitic resistance [17, 19].

Depletion-mode N-polar GaN HEMTs on molecular beam epitaxy (MBE) grown material was first reported

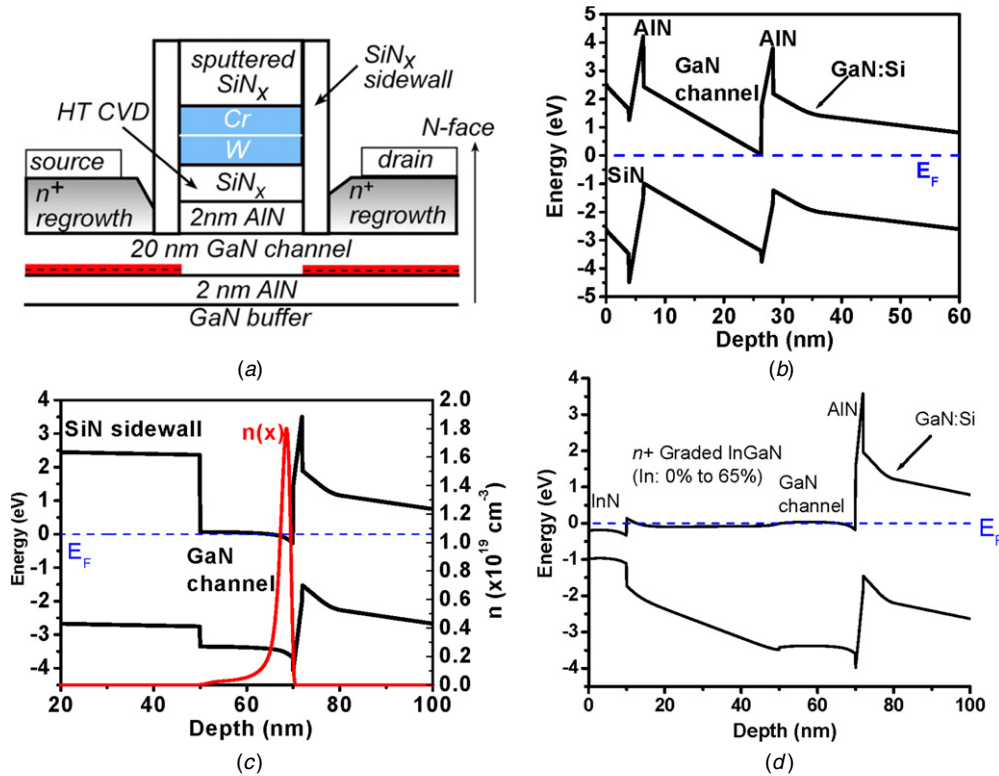


Figure 1. (a) Cross-section schematic of a self-aligned E-mode N-polar device. (b) Simulated band diagram and electron density of the device (a) under the gate showing normally off mode, (b) under the sidewall regions with a 2-DEG density of $5 \times 10^{12} \text{ cm}^{-2}$, and (d) under the source contact after MBE regrowth. (a), (b) and (c) © [2011] IEEE, reprinted, with permission from [27].

in 2007 [17]. Within a short period of time, significant progress has been made on N-polar device technology with comparable results to the more mature Ga-polar GaN HEMT technology [19–23]. Low source contact resistance and source access resistances in GaN HEMTs were first demonstrated in N-polar GaN devices by incorporating self-aligned source/drain regrowth technology [24]. In conjunction with a strain-free lattice matched InAlN back-barrier layers record high transconductance and power gain cutoff frequency has been reported [21, 25]. Thus, N-polar GaN technology has evolved as a viable candidate for ultra-scaled GaN HEMT technology. In this paper, we review the recent progress on the enhancement-mode (E-mode) N-polar GaN technology for high-frequency applications. E-mode devices are attractive due to the single voltage which simplifies the circuit topologies.

The basic device structure of an N-polar GaN HEMT consists of a GaN channel on top of a wide-bandgap $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer similar to inverted AlGaAs/GaAs HEMT. The inherent polarization from the back-barrier in N-polar devices leads to a 2-DEG in the GaN channel and a normally on depletion mode operation. If a wide-bandgap AlGa_xN layer is grown on top of the channel, the negative polarization charge at the top interface will deplete the 2-DEG. If sufficient negative polarization charge is induced either by increasing Al composition or thickness of the wide bandgap $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer, the 2-DEG can be completely depleted and an enhancement-mode device can be obtained. Besides the negative polarization charge for enhancement-mode operation, other considerations such as strain relaxation, gate capacitance, ease of etching and

etch selectivity will be crucial in designing the top barrier layer. Using AlN top-layer for enhancement-mode operation has the advantages of low thickness that increases the gate capacitance which also at the same time has the potential to offer highest selectivity in etch rates between AlN and GaN.

Removing the top 2-DEG depleting AlN layer in the access regions recovers the 2-DEG which will reduce the access resistance. In addition, highly doped source/drain regions can be grown to further reduce the access resistance [26]. In the next section, we report on the details of devices design and fabrication of self-aligned N-polar GaN enhancement-mode devices.

2. First generation of E-mode devices

The first generation of E-mode devices reported was on a 20 nm thick GaN channel with self-aligned source/drain regrowth [27, 28]. A schematic cross-section of the self-aligned device structure is shown in figure 1(a). The device utilized a gate-first refractory metal process with self-aligned source drain regions by MBE regrowth. Figure 1 also shows the simulated band-diagrams of the various regions of the device. Under the gate, the band-diagram shows that the 2-DEG is completely depleted by the top AlN layer and the device will be normally off. In the sidewall access regions, where the top AlN layer is removed and plasma-enhanced chemical vapor deposition (PECVD) SiN_x is deposited the 2-DEG is recovered in the GaN channel. In the source/drain regions a graded InGa_x/InN regrowth is carried out after gate formation, the simulated band-diagram

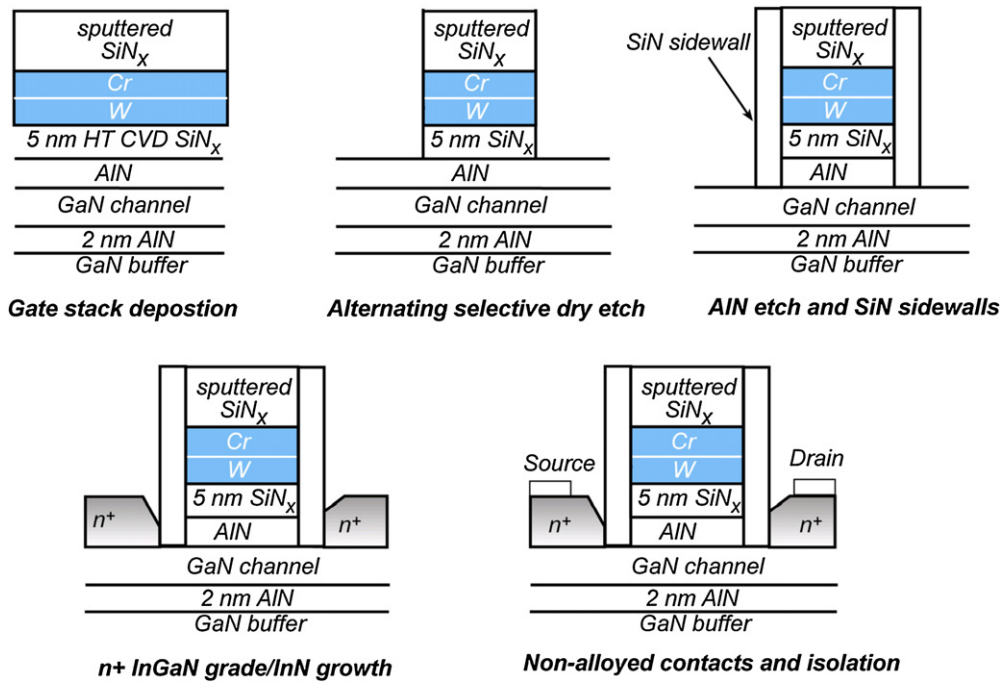


Figure 2. Self-aligned N-polar GaN device fabrication process. The gate etch process was adapted from III-V MOSFET process in [29].

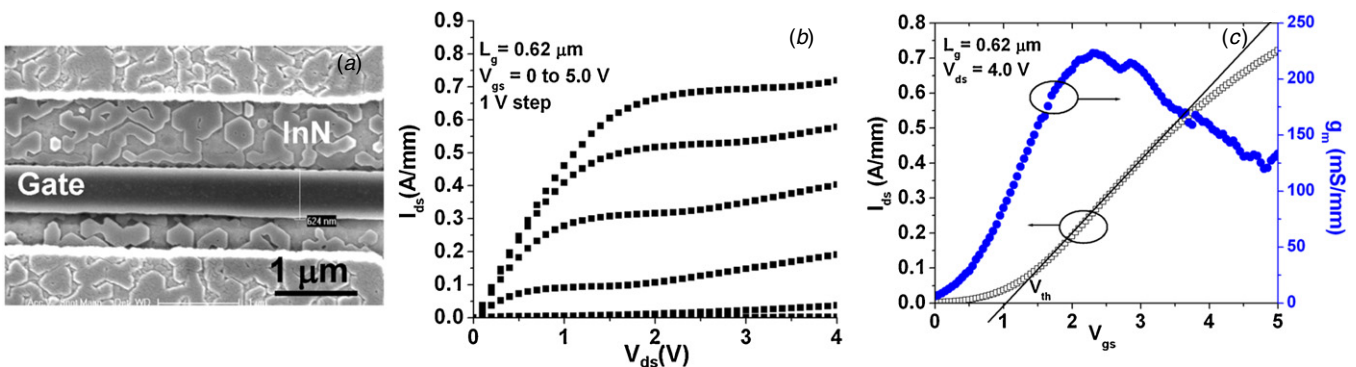


Figure 3. (a) SEM image of the device showing InN growth next to gate. (b) dc output, and (c) dc input characteristics of a $0.62 \mu\text{m}$ gate length device. © [2011] IEEE, reprinted, with permission from [27].

shows that there is no barrier to electrons from the source contact to the channel [24, 26].

All the device structures reported here were grown by plasma-assisted MBE. The 20 nm GaN channel device structure was grown on C-face SiC substrates to obtain N-polarity. An AlN nucleation layer followed by a two-step GaN buffer was adopted for growing a high-quality, semi-insulating buffer. After the device was grown, 5 nm of SiN_x was deposited on top by high-temperature chemical vapor deposition (HT-CVD) for the gate barrier. Next a composite W/Cr/ SiN_x gate stack was deposited; W and SiN_x were deposited by Ar-sputtering and the Cr was deposited by electron beam evaporation. The gate stack process was adapted from III-V MOSFET process reported in [29], with the top SiO_2 layer replaced by Ar-sputtered SiN_x layer for etch selectivity with the HF-based wet etch process for the top-AlN layer. The composite W/Cr/ SiN_x gates were defined by electron beam lithography and selective dry etches with gate lengths varying from 10 to $0.18 \mu\text{m}$.

The device fabrication process is shown in figure 2. After the gate definition, the AlN layer in the access regions was selectively wet etched by UV-Ozone oxidation followed by buffered HF etch [28]. This etch selectively removes the AlN layer stopping on the GaN channel layer. The high selectivity of the etch enables an over etch of AlN layer without the danger of etching the thin GaN channel layer. Before source/drain regrowth, SiN_x sidewalls were defined by a low-power reactive ion etch. The source/drain regions were grown by plasma-assisted MBE [26]. After the regrowth, non-alloyed Ti/Au source/drain contacts were formed and the devices were mesa isolated by reactive ion etching.

Figure 3(a) shows a scanning electron microscope (SEM) image of a device after regrowth, which shows the InN growth next to gate. The dc characteristics of the device are shown in figures 3(a) and (b). The device clearly shows an enhancement-mode operation with a linearly extrapolated threshold voltage (V_t) of 1.0 V, which was expected from the simulated band-diagrams of the device structure. The deposition of SiN_x gate

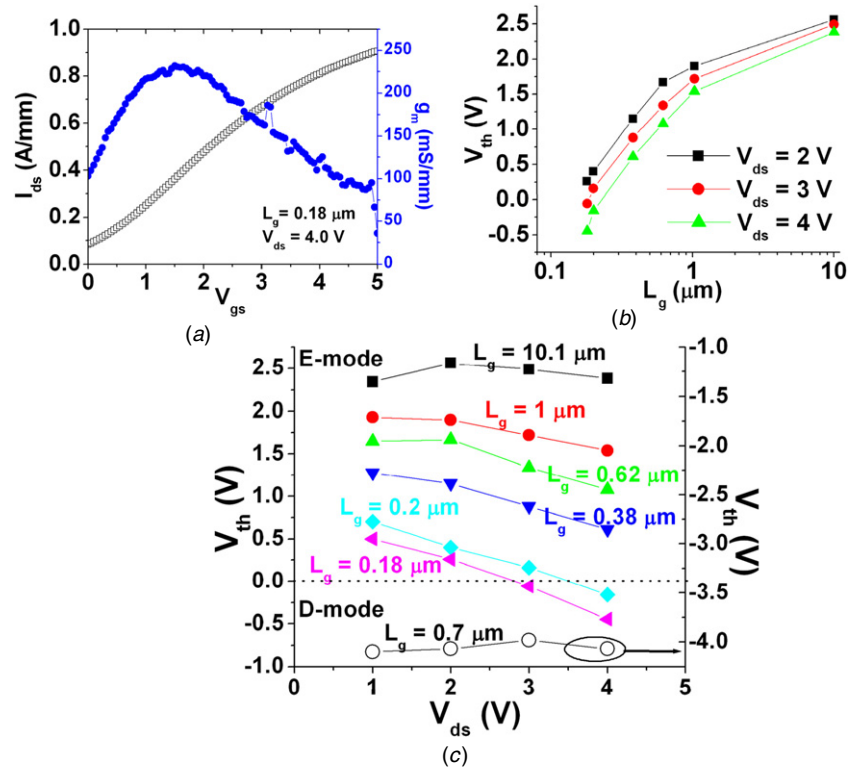


Figure 4. (a) Input characteristics at $V_{ds} = 4.0$ V for a $0.18 \mu\text{m}$ length devices. (b) Threshold voltage roll off with decreasing gate length and (c) increasing drain bias. The open circles (right y-axis) in (c) show the V_{th} for a non-self-aligned D-mode device. © [2011] IEEE, reprinted, with permission from [27].

dielectric does not lead to a depletion mode device which was observed in Ga-polar devices [30]. The maximum drain current (I_d) and maximum transconductance (g_m) of the device were 0.74 A mm^{-1} and 225 mS mm^{-1} , respectively.

The gate length scalability of the device structure was investigated with respect to dc device performance. As the gate length is reduced, the devices show threshold voltage roll-off with the $0.18 \mu\text{m}$ gate length device showing a depletion mode operation (figure 4(a)). The threshold voltage dependence on gate length and drain bias is shown in figure 4. As seen in figure 4, the threshold voltage decreases with increasing drain bias for a given gate length device. It also decreases with decreasing gate length at a given drain bias. Drain-induced barrier lowering (DIBL) is the reason for the observed V_t roll-off, which has been observed in Ga-polar E-mode devices [31]. However, the roll off observed in these devices is faster than that reported in Ga-polar HEMTs [32]. The V_t roll off is also faster than depletion-mode N-polar devices with non-self-aligned devices as shown in figure 4(c).

The aspect ratio of the device dictates the FET electrostatics and DIBL effect [33]. The aspect ratio (L_g/t_{bar}) of the $0.18 \mu\text{m}$ device is 6.7, a low value at which the short channel effects are expected [33]. In addition, N-polar GaN devices show poor dc saturation and DIBL effect arising from traps in the back barrier [34, 34]. The E-mode devices here show enhanced V_t roll off because of the self-aligned drain structure. The self-aligned drain leads to a more intrinsic drain voltage that enhances the DIBL effect. Such enhanced DIBL effect has been reported in Si metal-oxide semiconductor FETs (MOSFETs) [36].

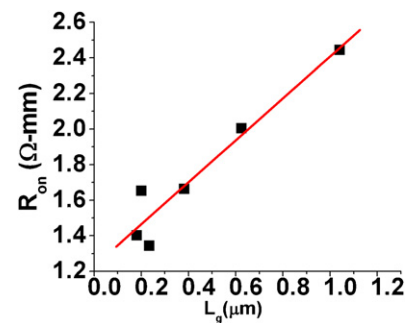


Figure 5. Device on-resistance versus gate length. A total source/drain parasitic access resistance of $1.2 \Omega\text{-mm}$ is extracted from the linear interpolation to zero gate length. © [2011] IEEE, reprinted, with permission from [27].

Figure 5 shows the variation of the device on-resistance with gate length. The extrapolated source access resistance is $0.6 \Omega\text{-mm}$. In order to evaluate the components of the source resistance, transfer length method (TLM) structures were measured on the regrown InN/InGaN layer, which give a sheet resistance and contact resistance of $540 \text{ Ohm}/\square$ and $0.04 \Omega\text{-mm}$, respectively. The contribution of the 50 nm SiN_x sidewall region is calculated from the measured sheet resistance of the SiN_x/GaN process monitor sample. The total source access resistance calculated from the test structures is $0.51 \Omega\text{-mm}$, while the extrapolated resistance is $0.6 \Omega\text{-mm}$. The difference of $0.09 \Omega\text{-mm}$ is the contribution from the regrowth interface resistance. The regrowth interface resistance can be further reduced to the fundamental limit as reported in [37].

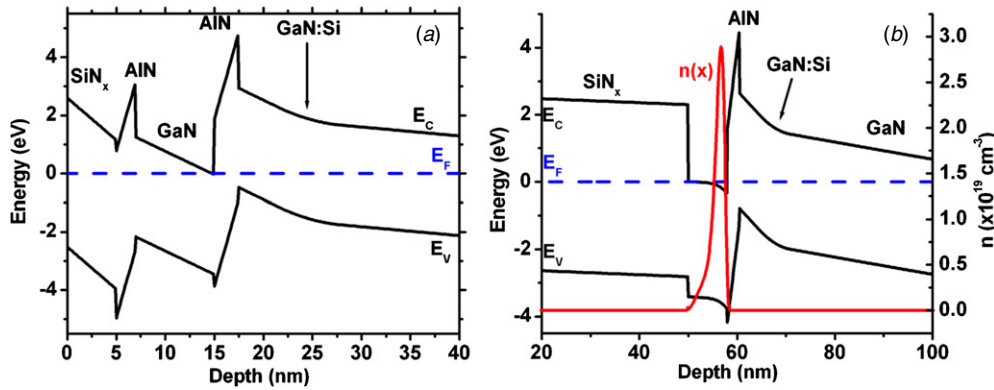


Figure 6. Band diagram for the 8 nm thick GaN channel device (a) under the gate showing E-mode operation. (b) Under the SiN_x sidewall access region. © [2011] The Japan Society of Applied Physics, reprinted, with permission from [38].

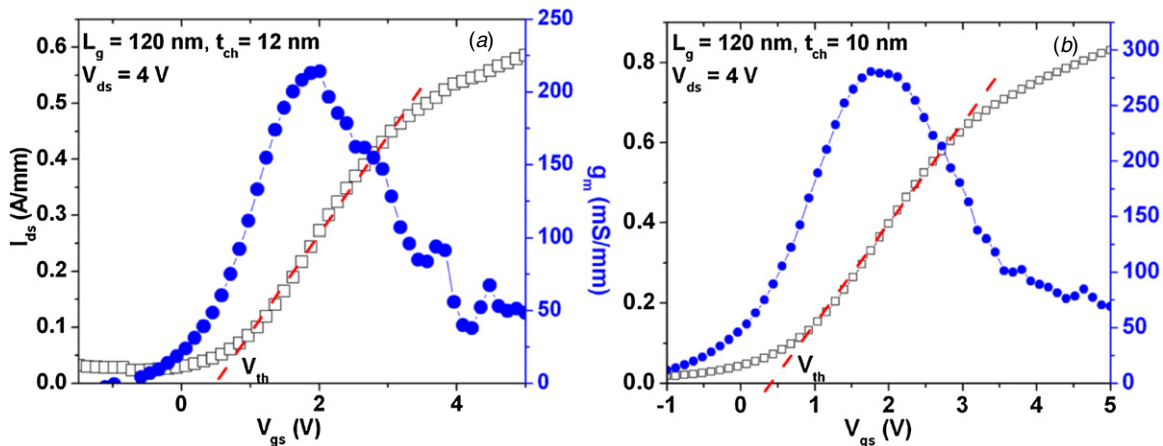


Figure 7. DC input characteristics of a 120 nm gate length device with (a) 12 nm thick GaN channel and (b) 10 nm thick GaN channel. Both devices show a linearly extrapolated positive threshold voltage.

The OFF state performance of the device shows severe limitations. The ON–OFF ratio of the $0.62 \mu\text{m}$ devices is 720, which degrades to 10 for the $0.18 \mu\text{m}$ devices. The three-terminal breakdown of the $0.62 \mu\text{m}$ device is 15 V, which is low compared to the non-self-aligned devices. The self-aligned structure with higher intrinsic drain voltage leads to lower breakdown than a non-self-aligned device. An offset drain voltage structure with lower drain doping will increase the breakdown voltage.

In summary, the first generation of E-mode devices with 20 nm thick GaN channel show good dc performance. However, due to the low aspect ratio the device gate lengths cannot be scaled beyond $0.18 \mu\text{m}$ while maintaining a positive V_t . In order to maintain E-mode operation in ultra-scaled device, the devices' vertical dimension has to be reduced to increase the aspect ratio.

3. Vertical scaling of the GaN channel

In order to reduce the gate transit time and obtain high frequency operation in N-polar GaN devices, the gate length has to be scaled along with the vertical dimensions of the device. In this section, we summarize the results of vertical scaling of the GaN channel in E-mode N-polar devices [38].

The device design goals for vertically scaled channel structures are E-mode operation under the gate and high charge density under the sidewall regions which have opposite requirements on the back-barrier doping density. A higher polarization doping would increase the conductivity of the sidewall access regions; however, the larger value will require a thicker AlN layer to deplete the 2-DEG which may crack due to strain. The proximity of the surface in scaled channels provides a challenge in device design because it has direct impact on the 2-DEG charge density and electron mobility. Keeping these constraints in mind, we designed three devices with GaN channel thickness of 12 nm, 10 nm and 8 nm, respectively. The simulated band diagrams for the 8 nm thick GaN channel device under the gate and under the sidewall are shown in figure 6. The simulated 2-DEG concentrations under the sidewall regions for the 12 nm, 10 nm and 8 nm thick GaN channel devices are 6.6×10^{12} , 7.6×10^{12} and $9.7 \times 10^{12} \text{ cm}^{-2}$, respectively.

Self-aligned FETs were fabricated on these samples with electron beam lithography (EBL)-defined gates following the process described in the previous section. The dc characteristics of $0.12 \mu\text{m}$ gate length devices with 12 nm and 10 nm GaN channel thickness are shown in figure 7. As seen in the figure, both devices have positive threshold voltage, while similar gate length devices with 20 nm thick

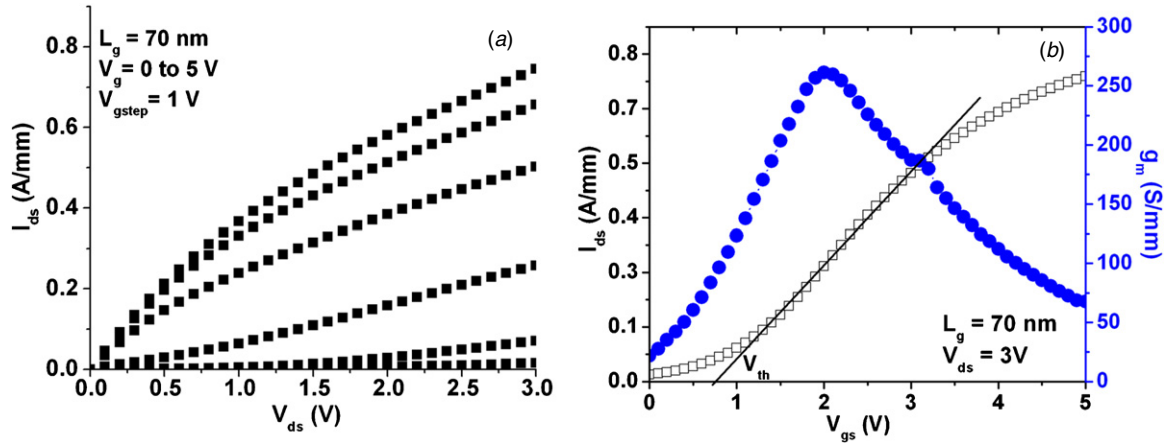


Figure 8. Common-source output and input characteristics of the 70 nm gate length device with 8 nm thick GaN channel. © [2011] The Japan Society of Applied Physics, reprinted, with permission from [38].

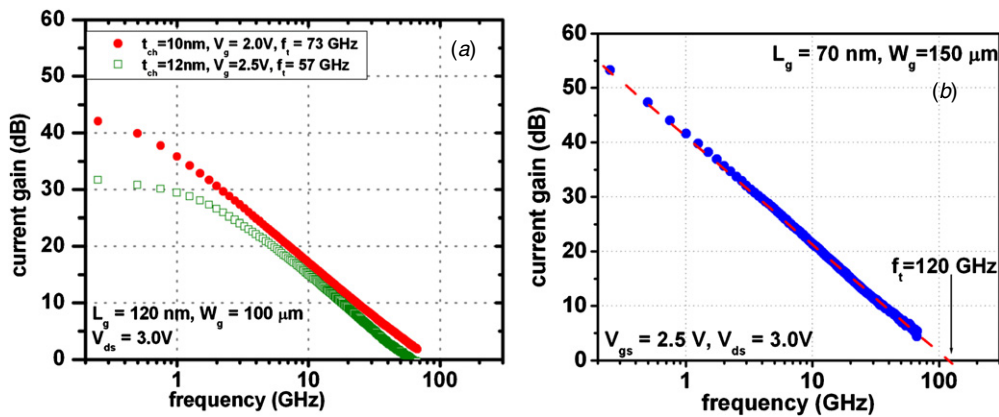


Figure 9. Measured short circuit current gain (h_{21}) versus frequency for (a) 12 nm and 10 nm thick GaN channel devices with gate length of 120 nm, and (b) 8 nm thick GaN channel device with a gate length of 70 nm. A current gain cut off frequency (f_t) of 120 GHz is extrapolated. (b) © [2011] The Japan Society of Applied Physics, reprinted, with permission from [38].

GaN channel were depletion mode with negative threshold voltages. The increased aspect ratio helps maintain the positive V_t till $0.12 \mu\text{m}$. However, these devices still show gate length dependent and drain voltage dependent threshold voltages. Both the 12 nm and 10 nm GaN channel devices become depletion-mode at a gate length of 70 nm (not shown).

On further scaling of the GaN channel thickness to 8 nm, E-mode operation with positive V_t is obtained for 70 nm gate length device. The dc output and input characteristics of the device is shown in figure 8. The peak current and peak transconductance of the device are 0.74 A mm^{-1} and 260 mS mm^{-1} , respectively, with a linearly extrapolated positive threshold voltage of 0.7 V at $V_{ds} = 3.0 \text{ V}$.

The high-frequency performance of these devices was characterized by measuring the s-parameters on Agilent E8316A PNA from 100 MHz to 67 GHz. The PNA was first calibrated using Cascade Microtech LRRM standard, which brings the measurement reference plane to the probe tips. In order to de-embed the device pad parasitics and determine the intrinsic device performance, on-wafer open-short pads were measured after calibration. The intrinsic device s-parameters were determined by de-embedding the pad reactance calculated from the on-wafer open-short test structures [39].

The small-signal current gain versus frequency for the 12 nm and 10 nm thick GaN channel E-mode devices is shown in figure 9(a). The peak current gain cut-off frequency (f_t) for the 12 nm and 10 nm thick GaN channel devices is 57 and 73 GHz, respectively. The higher f_t for the 10 nm thick channel device is due to the higher transconductance compared to the 12 nm thick channel that results from increased gate capacitance.

The small-signal performance of the 8 nm thick channel device is shown in figure 9(b). The peak f_t is 120 GHz. Scaling the channel thickness ensures positive V_t and also increases the f_t due to increased gate capacitance. The power-gain cut off frequency of all the three devices reported here was low due to the high gate resistance of the thin W gate metal layer.

Despite excellent high frequency operation in these devices, they show poor dc saturation. The principle cause for this is the device structure. The device structure has been found to have direct impact on the dc output conductance of an N-polar HEMT [35]. The abrupt junction device structure used in this study has the highest dc output conductance resulting from traps at the bottom interface [35]. The device structure in combination with the self-aligned structure results in the observed high dc output conductance. This trap-induced dc

Sample	t_{ch} (nm)	MDL / Si (cm^{-3})	USL	UAL (nm)	Etch*
A	20	4.5 nm GaN / 1×10^{19}	4 nm GaN	2	Y
B	8	4.5 nm GaN / 2×10^{19}	4.5 nm GaN	2	Y
C	5	6 nm GaN / 3×10^{19}	2nm AlN / 4 nm GaN	3	Y
D	8	4 nm GaN / 3×10^{19}	2nm AlN / 5 nm GaN	2	Y
E	8	30 nm graded $Al_xGa_{1-x}N$ (x: 0.05 to 0.25) / 4.5×10^{18}	5 nm $Al_{0.25}Ga_{0.75}N$	2	Y
F					N
G					Y
H					N
I					Y

Cap
GaN channel
UID AlN interlayer (UAL)
UID spacer layer (USL)
Modulation doping layer (MDL)
GaN buffer/SiC

* 2 X of 5 minute UV-Ozone-30sec-BHF

Figure 10. Details of the N-polar structures for transport study. All the samples except for H and I had 40 nm of PECVD SiN_x cap.

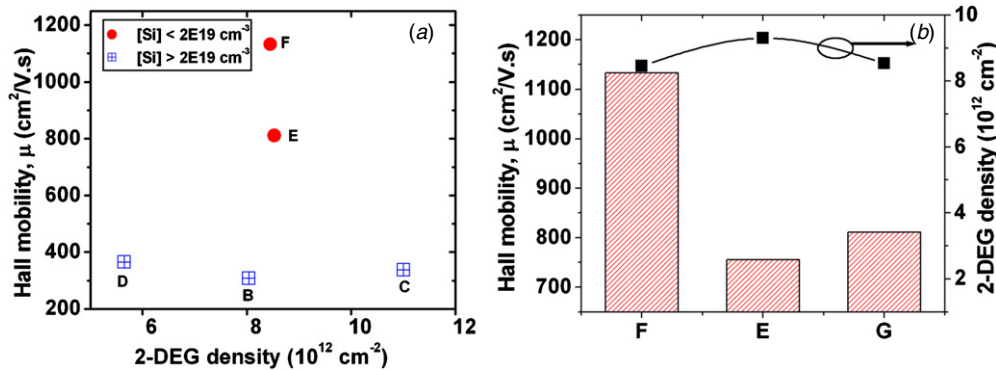


Figure 11. (a) Hall mobility and 2-DEG density of samples B to F. High 3-D Si doping leads to low mobility in B, C and D. (b) Hall mobility and 2-DEG density of 8-nm GaN channel samples with (E, G) and without (F) exposure to UV-Ozone-BHF treatment.

output conductance does not impact the RF output conductance values. Separation of trap induced and short channel dc output conductance in these devices will require extensive modeling. The future devices incorporated a graded back-barrier design in order to reduce the impact of this trap [35] and also improve mobility.

The on-resistance in these scaled channel devices reported in this section was high compared to the 20 nm thick GaN channel devices in the previous section. The contact resistance measured from TLMs for the 12 nm and 10 nm thick GaN channel device was 0.02 Ω -mm, while the TLM did not show a linear response due to inhomogeneous growth for the 8 nm GaN channel device resulting only in partial coverage of InN near the gate. The growth of InN is very sensitive to actual temperature with a narrow window of growth [40].

Besides the regrowth resistance, the sidewall access resistance in these samples was also high due to surface effects. The measured sidewall region mobility in thin 8 nm channel devices was 350 cm²/V.s, which was lower than the mobility of 1060 cm²/V.s in a 20 nm thick channel device. Systematic mobility studies were carried out to understand the scattering mechanisms.

4. Mobility in N-polar quantum well channels

The mobility in the vertically scaled GaN channels needs to be high in order to reduce the access resistance and also to ensure that the device achieves ballistic operation [41]. The sidewall access region conductivity in the self-aligned N-polar FETs is determined by the 2-DEG density and mobility. The access

region is exposed to various fabrication processes such as UV-Ozone-HF etch and PECVD deposition that can adversely impact the 2-DEG density and mobility. In addition, the device structure will also influence the scattering mechanisms and mobility. The GaN channel in N-polar GaN devices is a double hetero-structure quantum well, which will influence the electron scattering mechanism. In order to gain insight into mobility-limiting mechanisms, a systematic study was carried out.

Figure 10 gives the list of device structures studied to separate the contribution of the device structure and the fabrication process to electron scattering. The basic device structure consists of a modulation doping layer, a setback and an AlN interlayer. The modulation doping layer, in addition to proving electrons to the 2-DEG, moves the Fermi-level away from the valance band that removes the high-frequency dispersion and improves dc output resistance [17, 35].

Hall mobility was measured on these samples in the Van-der Pauw geometry with In contacts. In figure 11, the mobility of 5 nm and 8 nm thick GaN channels is seen to depend on the back-barrier modulation doping density. The devices with high three-dimensional (3D) Si doping ($> 2 \times 10^{19}$ cm⁻³) density have lower mobility than devices with lower 3-D density. Higher Si doping density could lead to higher roughness and hence lower mobility. As a result the graded AlGaN back-barrier layer leads to higher mobility, as this requires lower 3-D Si doping in order to keep the Fermi-level away from the valance band to reduce the high-frequency dispersion. The mobility also depends on the process history of the sample. The samples with UV-ozone-BHF etch show a degradation of

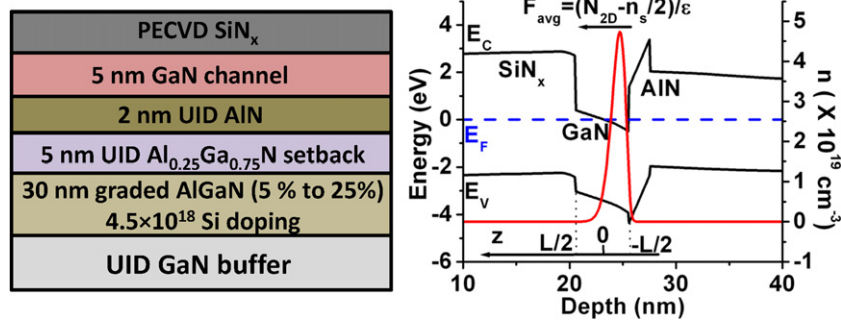


Figure 12. (a) The layer structure schematic and (b) simulated band diagram and electron density of the 5 nm GaN channel device. The UID in the AlN inter layer is $1 \times 10^{18} \text{ cm}^{-3}$, the doping in the AlGa_N graded layer is $4.5 \times 10^{18} \text{ cm}^{-3}$. Reprinted from [42]. © 2012, American Institute of Physics.

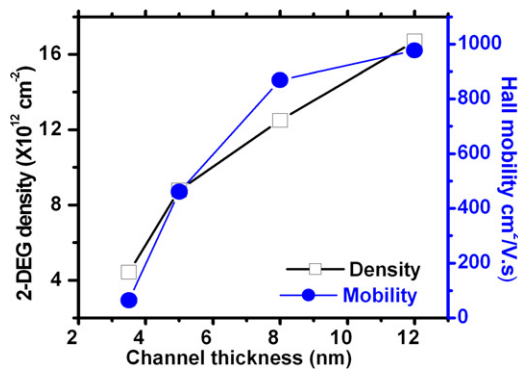


Figure 13. Measured room temperature Hall mobility and 2-DEG density as a function of GaN channel thickness. Reprinted from [42]. © 2012, American Institute of Physics.

mobility. This etch is selective to GaN; however, it can roughen the GaN surface to reduce the mobility.

In order to quantify the scattering mechanisms we carried out a theoretical and experimental investigation of graded-back barrier samples that were not exposed to UV-ozone etch [42]. The device structure (figure 12) consists of a top GaN channel, a 2 nm AlN back-barrier which reduces the alloy scattering rate of the 2-DEG, a 5 nm un-intentionally doped Al_{0.25}Ga_{0.75}N setback layer, a 30 nm graded AlGa_N modulation doping layer ((Si) = $4.5 \times 10^{18} \text{ cm}^{-3}$) and a GaN buffer. Four samples with channel thicknesses of 12 nm, 8 nm, 5 nm and 3.5 nm were grown within a short period of time to minimize any drift in the device material quality; all of them have the same layer structure shown in figure 12. The devices were grown by plasma-assisted molecular beam epitaxy (PA-MBE) on C-face SiC. For Hall measurement purpose, the devices were diced into 7 mm × 7 mm square pieces. Next, the native surface oxide was removed with 1 minute buffered hydro-fluoric acid (BHF) treatment before deposition of 50 nm of silicon nitride (SiN_x) by plasma-enhanced chemical vapor deposition (PECVD). Annealed indium contacts were formed at the corners of the square pieces for Hall measurement.

The variation of the 2-DEG density and Hall mobility at room temperature (RT) with thickness of the GaN channel is shown in figure 13. Both the 2-DEG density and the Hall mobility decrease with channel thickness resulting in a very low mobility of 65 cm²/V.s for the 3.5 nm channel device. The Fermi-level pinning at the SiN_x/GaN interface [43] leads

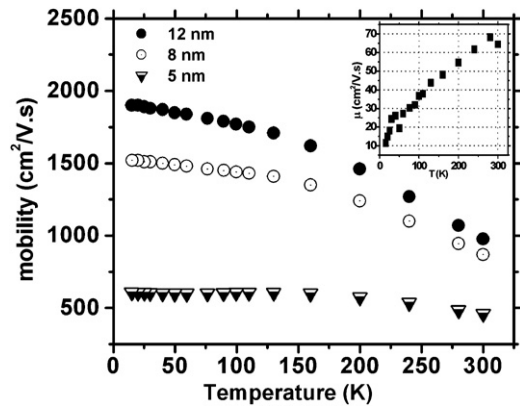


Figure 14. Measured Hall mobility as a function of temperature for the 12 nm, 8 nm and 5 nm channels. The inset shows the measured Hall mobility for the 3.5 nm channel device. Reprinted from [42]. © 2012 American Institute of Physics.

to increased depletion of the 2-DEG in thinner channels. In order to quantify the mobility-limiting mechanism in thin channels, temperature-dependent Hall mobility measurement was carried out for the samples. Figure 14 shows the measured Hall mobility for all the samples from 15 K to room temperature (300 K).

The mobility variation of the 12 nm, 8 nm and 5 nm samples shows similar behavior of increasing mobility with decreasing temperature and then saturation, while the 3.5 nm channel device shows a distinct trend of decreasing mobility with decreasing temperature. Reduced phonon population at low temperatures leads to a reduction in optical and acoustic phonon scattering rates that subsequently increase the mobility as observed for the 12 nm, 8 nm and 5 nm samples. However, the low temperature mobility saturated at a relatively lower value of <2000 cm²/V.s as compared to Ga-polar GaN HEMTs. This suggests a temperature-independent Coulombic scattering mechanism as the limiting scattering phenomenon in these devices. It is noted that the 2-DEG density remained unchanged from RT to 15 K in all the samples.

To quantify the mobility-limiting mechanisms, we calculated the 2-DEG mobility in the relaxation time approximation and in the electric quantum limit of ground state sub-band occupancy. The scattering mechanisms considered are interface roughness (IR), optical phonon (OP) scattering, acoustic phonon (AP) scattering, ionized

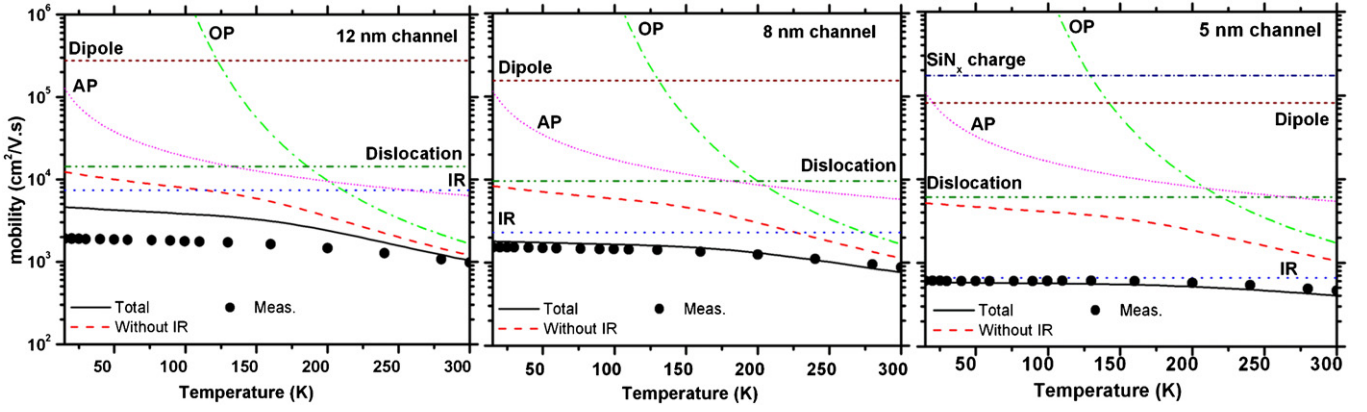


Figure 15. Calculated and measured mobilities for the 12 nm, 8 nm and 5 nm channel device. The dislocation density is assumed to be $1 \times 10^{10} \text{ cm}^{-2}$ with a filling factor $f = 0.5$, the trapped charge in the SiN_x is assumed to be $1 \times 10^{13} \text{ cm}^{-2}$, the optical phonon energy for GaN is 92 meV and the deformation potential for acoustic phonons is 9.1 eV. For IR scattering, $\Delta = 0.48 \text{ nm}$ and $\Lambda = 3.0 \text{ nm}$ is used for all the samples. The roughness parameters of the top and bottom interfaces are assumed to be same and uncorrelated. The F_{avg} for 12 nm, 8 nm, 5 nm and 3.5 nm samples are 1.25 MV cm^{-1} , 1.67 MV cm^{-1} , 2.0 MV cm^{-1} , and 2.34 MV cm^{-1} respectively. Reprinted from [42]. © 2012, American Institute of Physics.

impurity scattering (II), scattering due to charged dislocations, scattering due to un-intentional doping (UID) in the AlN interlayer, and scattering due to trapped charges in the PECVD SiN_x . The interface roughness scattering has not been previously considered in N-polar device structures.

Unlike the roughness scattering calculation GaAs quantum wells [44, 45] the quantum well devices studied here have a high transverse electric field ($\sim \text{MV cm}^{-1}$) in the channel arising from the polarization in the wurtzite III-N system. We use a variational wavefunction for an electron confined in a quantum well with an electric field (F) which is given by [46, 47]

$$\psi(z) = N(\beta) \cos\left(\frac{\pi z}{L}\right) \exp\left(-\beta\left(\frac{z}{L} + \frac{1}{2}\right)\right), \quad |z| < L/2, \quad (1)$$

where L is the channel thickness, z axis is in the direction growth, $N^2(\beta) = 4\beta(\beta^2 + \pi^2) \exp(2\beta) / L\pi^2 (\exp(2\beta) - 1)$ is the normalization constant, and β is the variational parameter that depends on the electric field in the channel. Using this wavefunction, we calculate the interface roughness scattering rate as [42]

$$\frac{1}{\tau_{\text{IR}}} = \frac{2\Delta^2 \Lambda^2 m^*}{\hbar^3} \left(\frac{eF}{2} + \frac{\hbar^2 \pi^2}{m^* L^3} \right)^2 \times \int_0^1 \frac{u^4 \exp(-u^2 \Lambda^2 k_F^2)}{\left(u + G(q) \frac{q_{\text{TF}}}{2k_F}\right)^2 \sqrt{1-u^2}} du \quad (2)$$

where Δ and Λ are the Gaussian roughness parameters, k_F is the Fermi wave vector, q is the difference in the initial and final electron momentum vectors, $u = q/k_F$, q_{TF} is the Thomas–Fermi screening vector, and $G(q)$ is the form factor for screening due to the finite width of the 2-DEG. We use Price's approximation [48] for $G(q)$ which is given by $G(q) \cong 1/(1 + bq)$ where $b = (\int_{-\infty}^{\infty} \psi^2(z) dz)^{-1}$.

A form factor $F(q)$, $F(q) = \int_{-\infty}^{\infty} \psi^2(z) \exp[q|z-d|] dz$ due to the finite width of 2-DEG wavefunction is used where d is the distance of the delta doping from the 2-DEG

for Coulombic scattering. The alloy scattering is negligible in these devices because the 2 nm thick AlN interlayer with a large conduction band offset with GaN quenches the wavefunction rapidly with an extremely low probability of the wavefunction in the AlGaIn alloy layer.

The scattering rates were calculated numerically and the total mobility was calculated using Matthiessen's rule. For the variational waveform calculation, the electric field in the channel was taken as the average electric field given by $F_{\text{avg}} = e(N_{2D} - n_s/2)/\epsilon_{\text{GaN}}$, where n_s is the measured 2-DEG density, and N_{2D} is the total integrated Si (2D) doping density.

Figure 15 shows the measured and calculated mobility for the 5 nm, 8 nm and 12 nm GaN channels as a function of the temperature. Roughness parameters of $\Delta = 0.48 \text{ nm}$ and $\Lambda = 3.0 \text{ nm}$ were used to fit the low temperature mobility of the 8 nm channel. The same values of Δ and Λ were used for 5 nm and 12 nm samples. The Δ value of 0.48 nm used to fit the data here is larger than the typical values in Ga-polar GaN HEMTs [49]. The inverted N-polar HEMT structure where the GaN channel is grown on an AlN layer with an underlying Si doping layer could be the reason for larger values similar to the higher roughness observed in inverted AlGaAs/GaAs HEMTs. The root mean square (rms) surface roughness measured by atomic force microscopy (AFM) of the wafers grown under similar conditions with a similar layer structure was 0.6–0.8 nm, which is again higher than typical Ga-polar GaN HEMTs.

The roughness scattering increases rapidly as the GaN channel thickness is reduced from 12 to 5 nm as shown in the calculated scattering rates in figure 15. The roughness scattering has two components as shown in equation 2: (i) the first component with F^2 dependence is similar to the roughness scattering in Si MOSFETs [50] and (ii) the second component with L^{-6} dependence is similar to the roughness scattering reported for GaAs quantum wells [44]. Both these components of the roughness scattering increase with decreasing channel thickness. When the channel thickness was reduced, the 2-DEG density in the channel decreases due to the depletion from the surface pinning at the SiN_x/GaN interface that

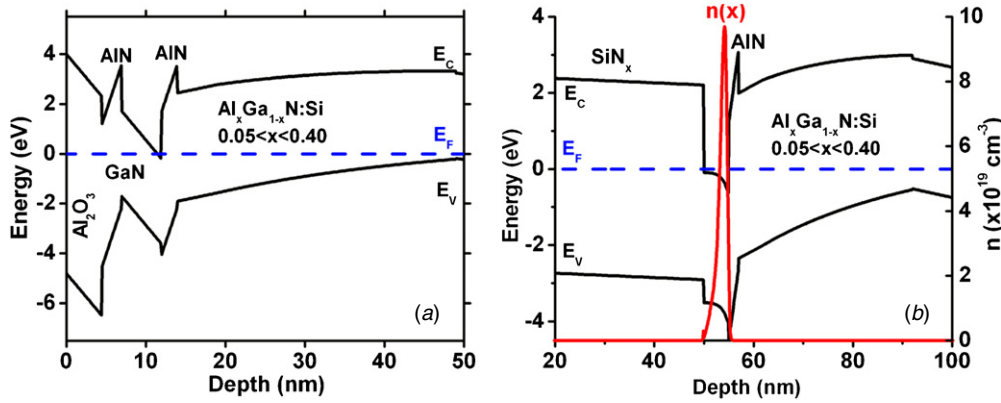


Figure 16. (a) The simulated band diagram under the gate. The thickness of the grade is 30 nm, and the Si modulation doping in the grade is $6 \times 10^{18} \text{ cm}^{-3}$. There is 5 nm of unintentionally doped (UID) $\text{Al}_{0.40}\text{Ga}_{0.60}\text{N}$ between the modulation doped layer and the AlN back-barrier. (b) The simulated band diagram under the SiN_x sidewall access region. © [2012] IEEE, reprinted, with permission from [51].

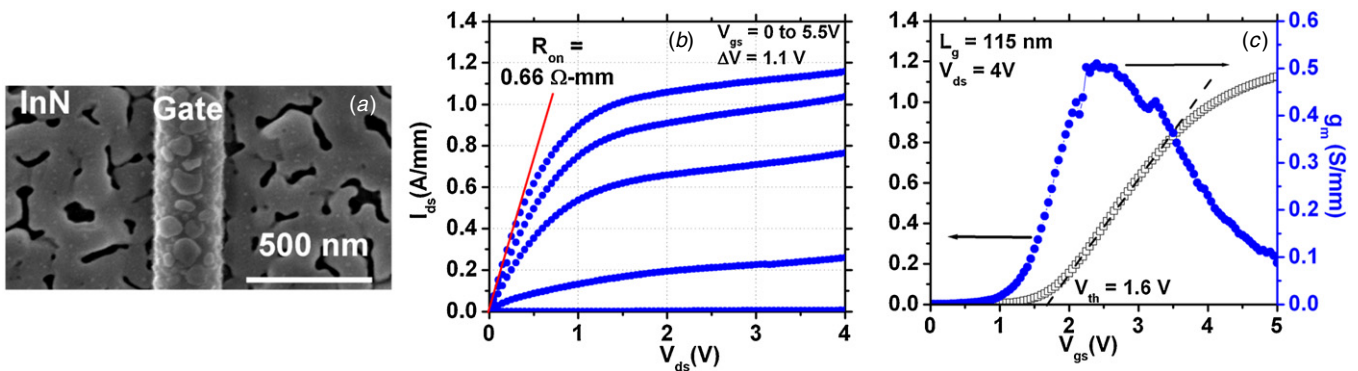


Figure 17. (a) SEM of InN regrowth coverage near the gate for the optimized InN regrowth condition for devices reported in this letter. (b) output and (c) input characteristics of the 115 nm gate length device. © [2012] IEEE, reprinted, with permission from [51].

results in an increase in the average field in the channel. This increased field subsequently leads to higher roughness scattering due to the F^2 dependence. The second component of roughness scattering also increases rapidly for channel thickness of 5 nm due to the $1/L^6$ dependence. The discrepancy between the calculated and measured low temperature mobility of the 12 nm sample could be due to the non-inclusion of the second sub-band occupation in the mobility calculations, which is highly likely due to the large 2-DEG density of $1.7 \times 10^{13} \text{ cm}^{-2}$.

The measured mobility variation for the 3.5 nm sample was different from the other samples, with decreasing mobility with decreasing temperature. While the model predicts (not shown in figure 15) a constant mobility of $100 \text{ cm}^2/\text{V}\cdot\text{s}$ with decreasing temperature. This trend of mobility with temperature can be explained by strong localization of electrons in the channel due to the high roughness. The localization leads to hopping-type conduction which is a thermally activated process and hence the mobility decreases with decreasing temperature. This further validates that the roughness is an issue in the structures studied here. This is an Anderson metal-insulator transition phenomenon [50]. From the expression for the roughness scattering it is clear that the mobility can be increased by decreasing the electric field in the channel and having smoother interfaces. The calculated RT mobility for the 3.5 nm GaN channel device with

$1 \times 10^{13} \text{ cm}^{-2}$ 2-DEG density (i.e. reduced depletion from the SiN_x/GaN interface states) and $\Delta = 0.1 \text{ nm}$ is $1250 \text{ cm}^2/\text{V}\cdot\text{s}$ which is reasonably high for the ultra-thin quantum well channel FETs.

In summary, we have studied the dependence of mobility in N-polar GaN quantum well channels with thickness and have shown that roughness is the principal reason for lower mobility in the thin channels. The roughness leads an Anderson metal-to-insulator transition in the 3.5 nm channel device.

5. Graded AlGaIn back-barrier devices with 5 nm GaN channel

Building upon the knowledge gained from the previous studies, we designed a 5 nm GaN channel device that will be scalable to sub-50 nm dimensions and maintain E-mode operation. The device structure is shown in figure 16 [51]. It incorporates a graded AlGaIn back-barrier to reduce the dc output conductance arising from the trap at the back-barrier, and also to improve the mobility. The gate barrier was Al_2O_3 high-k dielectric deposited by atomic layer deposition (ALD). Self-aligned devices with EBL-defined W/Cr/SiN gates were fabricated. The smallest gate length was 115 nm.

The dc characteristics of a 115 nm gate length FET shows (figure 17) a maximum I_d of 1.15 A mm^{-1} at $V_{gs} = 5.5 \text{ V}$ and

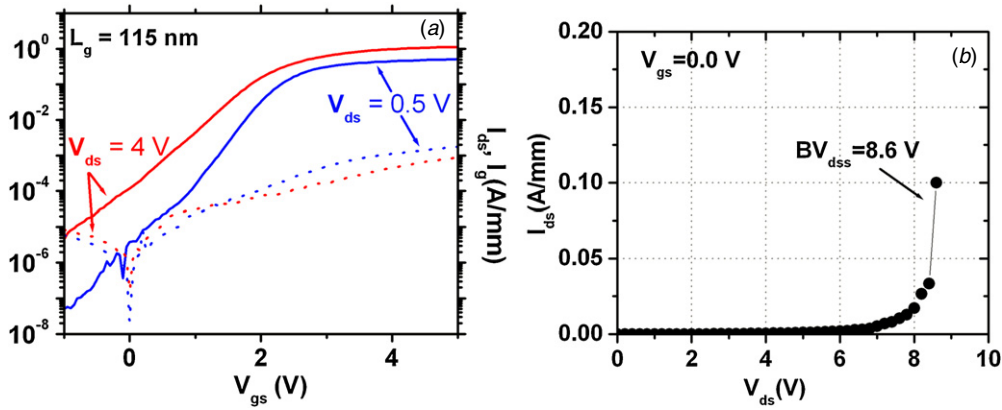


Figure 18. Plot of $\log I_{ds}$ versus V_{gs} and $\log I_g$ versus V_{gs} for a drain bias of 0.5 V and 4.0 V, respectively, (b) breakdown characteristics of the device at $V_{gs} = 0$ V. © [2012] IEEE, reprinted, with permission from [51].

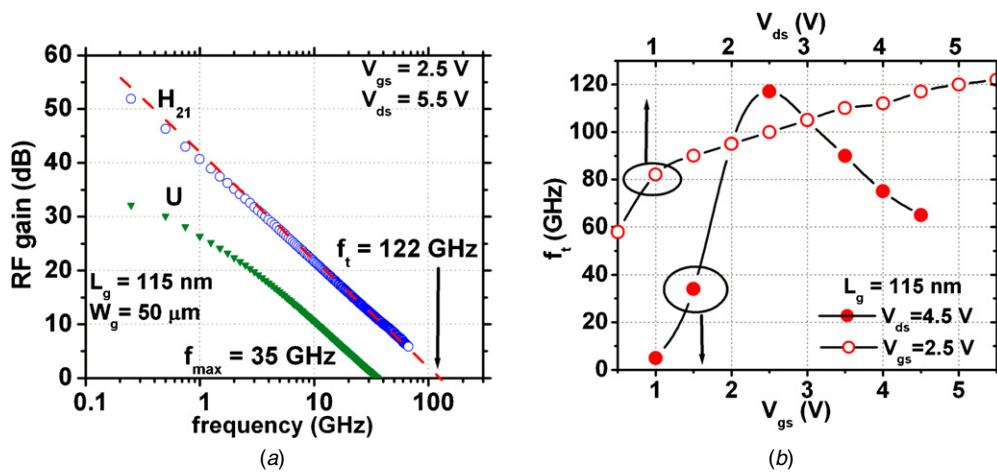


Figure 19. (a) RF gains of the device versus frequency of the device shown in figure 2. A f_t of 122 GHz and f_{max} of 35 GHz is extrapolated. (b) f_t versus gate voltage for $V_{ds} = 4.5$ V (bottom x-axis, filled circles), and f_t versus drain bias for $V_{gs} = 2.5$ V (top x-axis, open circles). © [2012] IEEE, reprinted, with permission from [51].

$V_{ds} = 4.0$ V, and a peak g_m of 510 mS mm^{-1} at $V_{gs} = 2.5$ V and $V_{ds} = 4.0$ V. A positive threshold voltage of 1.6 V is extracted from the linear extrapolation of the I_d - V_g plot, which is larger than the previous E-mode devices. This device structure is expected to maintain positive V_t at sub-50 nm devices.

The on resistance (R_{on}) of the device is $0.66 \Omega\text{-mm}$. The low R_{on} is achieved due to a number of improvements in the device structure and regrowth process. In order to reduce the access resistance, the Si doping in the InGaN regrowth was increased to $>1 \times 10^{20} \text{ cm}^{-3}$. In addition, the regrowth condition for InN was optimized to get complete coverage near the gate (figure 17(a)) compared to the previously reported E-mode devices (figure 3(a)). Complete coverage of InN is ensured with a lower 450°C regrowth temperature to reduce decomposition and increase the InN growth time. The surface Fermi-level pinning of the InN is within the conduction band and thus reduces the depletion of electrons in the device access regions [26]. Transmission line measurements (TLM) on the regrowth region gave a low sheet resistance of $100 \Omega/\square$ for the n^{++} InGaN/InN regrowth layer, and a lateral contact resistance of $5 \Omega\text{-}\mu\text{m}$ between Ti and InN. The sidewall access resistance was also reduced due to the increase in the

2-DEG conductivity of the channel under the sidewall, and also by decreasing the sidewall thickness to 30 nm. A sheet resistance of $490 \Omega/\square$ is measured for the sidewall regions on a process monitor sample with a 2-DEG density (n_s) of $1.7 \times 10^{13} \text{ cm}^{-2}$ and Hall mobility of $750 \text{ cm}^2/\text{Vs}$.

Due to the reduced effect of the trap in the graded back-barrier design, the pinch-off and the dc output resistance of the device are significantly better than the previously reported E-mode devices in sections 2 and 3. Figure 18 shows that at $V_{ds} = 4.0$ V, the $I_{on}(V_{gs} = 5.0 \text{ V})/I_{off}(V_{gs} = 0.0 \text{ V})$ is 1.16×10^4 , while the I_{on}/I_{off} is 74 for the devices reported in [7] under similar bias conditions. The three-terminal breakdown of the device is 8.6 V at $V_{gs} = 0$ V. At $V_{ds} = 4.0$, the maximum I_{on}/I_{off} is 2.2×10^5 , the off-state leakage limited by the gate leakage at $V_{gs} = -1$ V. Lower sub-threshold swing and leakage currents can be achieved by improving the dielectric-semiconductor interface.

Small-signal RF measurement of the device was performed on an Agilent E8361A PNA. After de-embedding the pad parasitics, the peak current gain cut-off frequency of the device is 122 GHz (figure 19) with an f_t - L_g product of $14 \text{ GHz}\text{-}\mu\text{m}$ at a gate bias of 2.5 V and a drain bias of

5.5 V. If the same $f_i L_g$ is maintained, a f_i of 280 GHz could be achieved at 50 nm gate length. The improvement in $f_i L_g$ product for this device is because of the low source access resistance and higher output resistance which are the results of the optimized regrowth condition and graded back-barrier design, respectively. Figure 19(b) shows the variation of f_i with gate bias and drain bias.

A small-signal model of the transistor was developed. The extracted gate-drain capacitance (C_{gd}) was 140 fF mm^{-1} which is larger than the value reported in a non-self-aligned device [52]. Removing the drain sidewall will reduce the feedback capacitance and increase the f_i [20]. A thick low-k dielectric drain sidewall can also be used to reduce this delay, which will also improve the breakdown voltage.

6. Conclusion

In conclusion, we have reported on the challenges and the recent progress in the N-polar E-mode technology. The scalability of the device structures was explored. The self-aligned devices show enhanced short-channel effects compared to non-self-aligned devices. In order to maintain E-mode operation at sub-50 nm gate lengths, the devices have to be vertically scaled to channel thickness of 5 nm. The device structure is also shown to impact the dc characteristics. The graded AlGaIn back-barrier designs show less dc output conductance arising from the trap at the bottom interface [35]. A 5 nm channel design with graded back-barrier and Al_2O_3 high-k gate dielectric shows improved dc performance in terms of ON-OFF ratio. This structure has the potential to scale sub-50 nm gate dimensions maintaining E-mode operation.

We have also investigated the impact of the device structure on electron mobility. The graded AlGaIn barrier designs with lower 3-D Si doping in the back-barrier show higher mobility than devices with higher 3-D doping in the abrupt junction devices. Roughness scattering is found to be the dominant scattering phenomenon in the vertically scaled channel devices.

Incorporation of the strain-free lattice matched InAlN back-barrier design in E-mode technology could provide more flexibility and improvement of E-mode designs. A systematic study on the correlation between the growth method and device structure on electron mobility will be necessary to further improve the conductivity of the sidewall access regions.

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