High-Performance nMOSFETs Using a Novel Strained Si/SiGe CMOS Architecture

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***Abstract*—Performance enhancements of up to 170% in drain current, maximum transconductance, and field-effect mobility are presented for nMOSFETs fabricated with strained-Si channels compared with identically processed bulk Si MOSFETs. A novel layer structure comprising Si/$Si_{0.7}Ge_{0.3}$ on an $Si_{0.85}Ge_{0.15}$ virtual substrate (VS) offers improved performance advantages and a strain-compensated structure. A high thermal budget process produces devices having excellent on/off-state drain-current characteristics, transconductance, and subthreshold characteristics. The virtual substrate does not require chemical-mechanical polishing and the same performance enhancement is achieved with and without a titanium salicide process.**

***Index Terms*—CMOS, drain-current enhancement, nMOSFETs, self-heating, SiGe, strained silicon, thermal budget, transconductance enhancement, virtual substrate.**

I. Introduction

THE LAST few years have seen the Si/SiGe material system widely integrated into bipolar technology [1], [2]. Sales of Si/SiGe bipolar/BiCMOS technologies doubled in 2001 compared with sales in 2000, despite the overall decrease of 30% in the silicon semiconductor market [3]. The tremendous success of Si/SiGe bipolar and BiCMOS technologies has resulted in the desire to expand the performance gains achievable by using SiGe and research is now focusing on obtaining enhanced CMOS devices by incorporating SiGe [4]. The 4.2% lattice mismatch between Si and Ge can be used to obtain strained layers, where electron (in Si under tension) and hole (in SiGe under compression) transport are improved [5]. The strained layers are generated by epitaxial growth on a substrate of differing alloy composition to the growing film. The larger atomic spacing of Ge compared with Si results in tensile strained Si when grown on a relaxed SiGe virtual substrate (VS). In order to achieve compressively strained SiGe, growth may either be on unstrained Si or a SiGe VS of lower alloy composition than the strained SiGe layer [6]. Modification to the electronic band structure and a reduced in-plane effective mass enhances hole mobility in compressively strained SiGe compared with unstrained Si. Enhanced electron mobility is achieved in tensile strained Si through reduced intervalley scattering and a reduction in the in-plane effective mass. By fabricating MOSFET devices on the strained Si/SiGe layers, faster CMOS devices and performance enhancements are predicted without the high costs associated with aggressive geometric scaling [4]. The enhanced mobility in strained Si/SiGe devices compensates the reduction in mobility of conventional Si transistor channels as the gate insulator thickness is reduced [7]. Furthermore, the similarity of strained Si/SiGe and conventional Si renders SiGe technology a relatively inexpensive choice for attaining high performance CMOS. Consequently, Si/SiGe MOS has been included as a key emerging research technology in the 2001 International Technology Roadmap for Semiconductors [8].

The development of Si/SiGe FET technologies was initially hindered by the poor quality of relaxed SiGe virtual substrates. However, growth techniques have since improved dramatically and SiGe material with defect densities of 10^5 cm^{-2} is now routinely available. Nevertheless, the demonstrated performance of strained Si/SiGe MOS devices remains below theoretical expectations. The relatively low electrical performance of the Si/SiGe MOS devices is mainly attributed to the Si/SiGe MOS process being modified to conserve the strained layers [9]. Strained layers may only be grown below a critical thickness h_c before the strain relaxes. As well as losing the benefits of enhanced carrier transport, strain relaxation causes an introduction of misfit dislocations, which degrade device performance. The critical thickness decreases with increasing lattice mismatch between the strained layer and the substrate. However, strain and hence enhanced transport properties increase for higher values of lattice mismatch between the strained layer and underlying substrate [10], particularly for the p-channel and n-channels up to VS alloy compositions of approximately $Si_{0.8}Ge_{0.2}$. Therefore there is a clear limitation to the performance enhancement achievable in strained Si/SiGe MOSFETs. Although it has been shown that a strained layer can be grown on a given alloy composition material to a thickness greater than h_c without relaxation [11], so-called "metastable" material cannot withstand the high thermal budget processing commonly used in MOS fabrication. Consequently, most researchers have attempted fabrication of strained Si/SiGe

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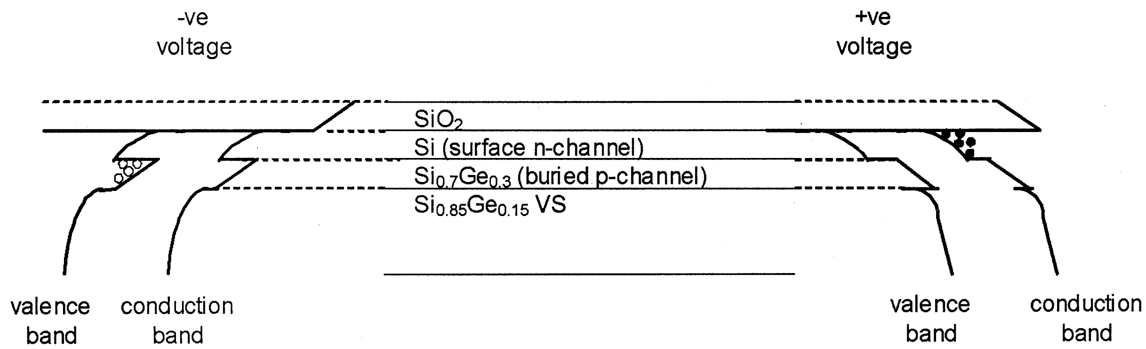

Fig. 1. Optimized CMOS architecture showing electrons in tensile strained Si and holes in compressively strained $Si_{0.7}Ge_{0.3}$ under inversion conditions.

MOSFETs using reduced thermal budgets and/or by lowering the alloy compositions, ultimately sacrificing the performance gains achievable [12]–[14].

In addition, all Si/SiGe devices reported to date have epitaxially grown Si/SiGe layers designed to maximize the performance of either n- or p-channel devices. Advanced CMOS, however, requires high performance from both n- and p-channel devices. In the present study, by using a layer structure which does not compromise the performance of either n- or p-channel devices, coupled with conventional MOS fabrication, high-performance strained silicon nMOSFETs are demonstrated, with maximum performance benefits predicted for p-channel devices using the same VS [15]. Consequently a new route is presented for obtaining high-performance CMOS. The layer structure is additionally designed such that strain-compensation occurs between the n- and p-channels, and with strained channel thicknesses sufficient to allow conventional surface cleans and oxidation necessary for high-performance CMOS. The performance of the strained Si nMOSFETs presented in this paper exceeds that of recently reported devices [16] and is significantly enhanced compared with unstrained Si control devices over a wide range of gate lengths; our increases in drain current (I_d) and transconductance (g_m) are the highest reported to date. Furthermore, the performance gains are achieved without VS polishing thus the present technology is more compatible with conventional Si technology. The novel design used in the current study has therefore overcome the usual trade-off encountered in Si/SiGe MOS technology between performance gains achievable (due to strain and consequently alloy composition) and thermal budget, while proving the most compatible n- and p-channel device architecture suitable for advanced mainstream CMOS applications to date.

II. Device Design and Fabrication

The epitaxial layer structure of the strained Si/SiGe devices is shown schematically in Fig. 1. The strained $Si/Si_{0.7}Ge_{0.3}$ channel layers are grown on a relaxed constant composition $Si_{0.85}Ge_{0.15}$ VS. By growing a $Si_{0.7}Ge_{0.3}$ layer on the VS, the higher Ge content alloy layer is compressively strained, making the layer ideal for a p-channel of high-mobility holes in a MOS device [15]. The smaller lattice constant of Si dictates that the subsequent Si layer (Fig. 1) is in tension, allowing electron mobility enhancement suitable for the n-channel of strained Si nMOSFETs. Furthermore, the band offsets between

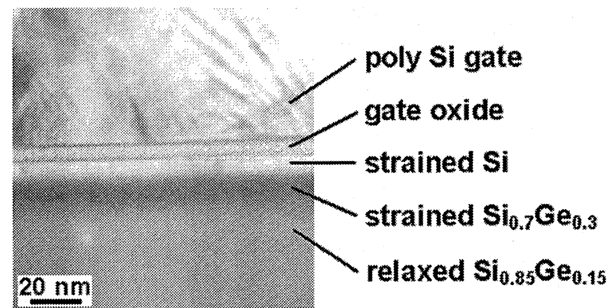

Fig. 2. High-resolution TEM image of the gate oxide and the strained $Si/Si_{0.3}Ge_{0.3}$ layers on the relaxed $Si_{0.85}Ge_{0.15}$ VS.

the strained Si and $Si_{0.7}Ge_{0.3}$ layers enable the confinement of holes in the buried $Si_{0.7}Ge_{0.3}$ layer under negative bias conditions and a layer of electrons at the surface of the strained Si when a positive bias is applied to the MOS gate (Fig. 1). Thus, the present design describes a high-performance CMOS architecture incorporating a surface n-channel and buried p-channel. Following selective etching to remove some of the strained Si material (i.e., the n-channel) above the buried p-channel in order to increase the pMOSFET device transconductance, maximum performance is predicted from both n- and p-channel devices on the single VS architecture [15]. The sequence of SiGe under compression and Si in tension creates a strain-compensated structure, minimizing cumulative strain in the devices. Transmission electron microscopy (TEM) analysis of the epitaxial layers following processing verified that the final tensile strained Si surface channel was approximately 7 nm (Fig. 2). The compressively strained $Si_{0.7}Ge_{0.3}$ layer was measured as 12 nm. The n-channel (strained Si) was intended to be slightly thicker than measured, and since the strained $Si_{0.7}Ge_{0.3}$ layer was slightly thicker than anticipated, it is likely that smearing of the heteroboundaries due to the high thermal budget process (below) may have caused the slight deviation from layer specification. Nevertheless, both the strained Si n-channel and strained $Si_{0.7}Ge_{0.3}$ p-channel were above the minimum thickness required to achieve maximum performance gains [17].

The Si/SiGe layers were grown by low-pressure chemical vapor deposition in an Applied Materials Centura tool using SiH_4 and GeH_4 in a H_2 carrier gas with B_2H_6 for p-type doping [18], [19]. The 1-μm constant composition $Si_{0.85}Ge_{0.15}$ VS and the preceding graded $Si_{1-x}Ge_x$ layer (x = 0 to 0.15) were

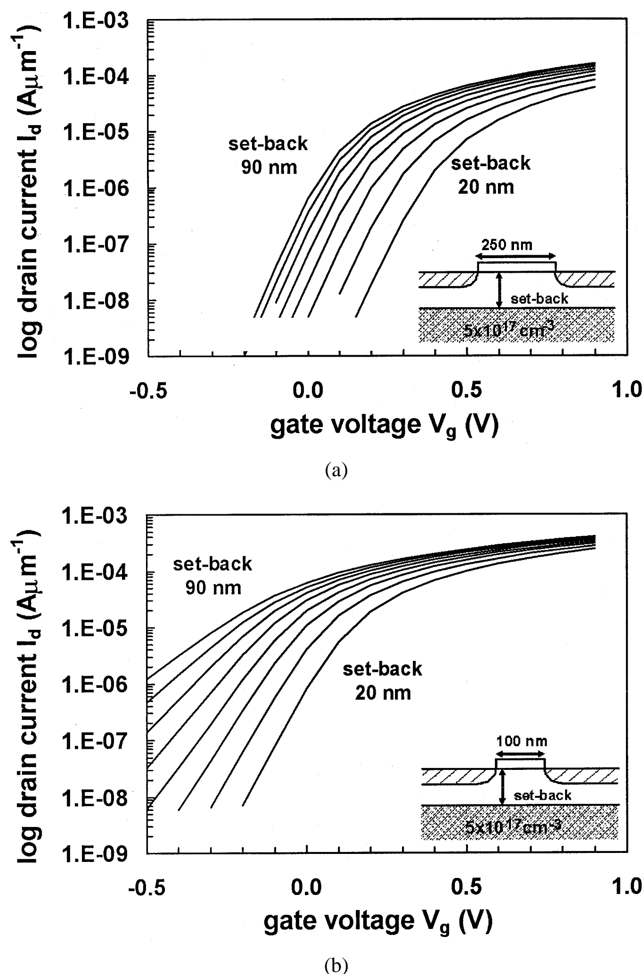

Fig. 3. Simulated dependence of subthreshold characteristics on background doping set-back layer thickness at $V_d = 1.0$ V for (a) 100-nm and (b) 250-nm gate length devices. The set-back layer thickness ranges from 20–90 nm in steps of 10 nm.

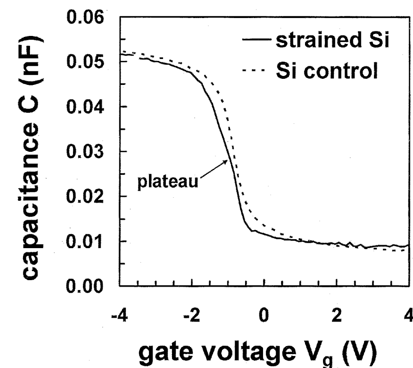

Fig. 4. *C–V* characteristics of 100 μm × 100 μm MOS capacitors on strained Si/SiGe and control device wafers. The similarity of the strained Si/SiGe accumulation capacitance and the Si control accumulation capacitance indicates equivalent gate oxide thickness of the devices.

grown above 800 °C in order to promote misfit dislocation nucleation and propagation [20]. The strained $Si/Si_{0.7}Ge_{0.3}$ layers were subsequently grown at reduced temperature for maximum control of layer thickness and Ge segregation. Secondary ion mass spectroscopy, x-ray diffraction, and Raman spectroscopy were used to confirm the as-grown layer thickness, alloy composition and strain of a strained Si layer grown directly on a $Si_{0.85}Ge_{0.15}$ VS at the same time as the device wafers.

Drift-diffusion technology computer aided design (TCAD) simulations were carried out in Medici [21] in order to determine a suitable as-grown B profile for the devices. Fig. 3 shows the simulated variation of subthreshold characteristics with substrate doping (N_a) set-back layer thickness (the separation between the substrate doping and the strained Si surface channel) for MOSFETs with a 6 nm gate oxide. The characteristics were investigated for set-back layer thicknesses ranging from 20–90 nm in 10-nm intervals. The data is simulated at a drain voltage (V_d) of 1.0 V and suggests that a final set-back layer thickness of approximately 50 nm between a 5×10^{17} cm^{-3} (B) diffusion edge and the strained Si surface channel would enable good subthreshold characteristics for 0.25-μm gate length devices [Fig. 3(a)], while a greater dependence of set-back layer thickness is observed for 100-nm gate length devices [Fig. 3(b)]. The channel doping was taken to be 1×10^{16} cm^{-3} in order to maintain high carrier mobility. An allowance of 25 nm was incorporated into the initial set-back layer thickness based on simulations of B diffusion during thermal processing [22]. Diffusion coefficients for B in SiGe were adapted from [23], [24] and all processing steps carried out at temperatures greater than 400 °C were included in the simulation.

The Si/SiGe wafers did not require chemical-mechanical polishing (CMP), since the as-grown rms roughness of the VS was low, at 1.3 nm, as measured by AFM and optical profilometry on 25 μm × 25 μm areas around the wafer. This is one of the lowest roughness values reported for as-grown $Si_{0.85}Ge_{0.15}$ VS material to date. Device fabrication mainly followed standard 0.25-μm CMOS processing. Active areas were defined in deposited oxide and dry thermal oxidation at 800 °C followed by a N_2 anneal produced a 6-nm gate oxide, measured by capacitance–voltage (*C–V*) profiling on MOS capacitors fabricated on the device wafers and by TEM (Fig. 2). Representative *C–V* characteristics of 100 μm × 100 μm MOS capacitors are shown in Fig. 4. The similarity of the two accumulation capacitances indicates that the oxide thickness of the strained Si/SiGe wafer is equivalent to that of the control wafer. The small plateau in capacitance observed on the strained Si/SiGe MOS capacitor at approximately -1 V is due to the confinement of holes in the $Si_{0.3}Ge_{0.7}$ layer [25]. Fig. 5 shows the interface trap density (D_{it}) as a function of bandgap energy measured using a quasistatic *C–V* technique [26]. D_{it} at mid-gap was found to be approximately 6×10^{10} $cm^{-2}eV^{-1}$ for both capacitors, confirming that the Si/SiO_2 interface quality of the strained Si/SiGe devices was similar to the control devices. The small discrepancy in the gate oxide thickness measured by TEM (6 nm) and the electrical oxide thickness measured by *C–V* (6.5 nm) is due to quantum mechanical and polysilicon depletion effects [27]. Electron beam lithography defined polysilicon gate lengths (L) down to 150 nm and As implants annealed at 1050 °C for 20 s created the source and drain. Duplicate Si/SiGe and control Si wafers additionally underwent a salicide process split using Si_3N_4 side-wall spacers and $TiSi_2$. A bright-field TEM image of a typical silicided strained Si/SiGe device structure is shown in Fig. 6. The silicide was found to reduce the sheet resistance of the Si/SiGe source and drain regions from 68 Ω/sq to below

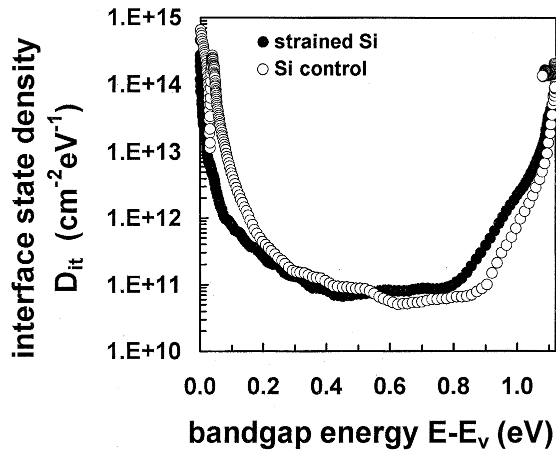

Fig. 5. Interface trap density (D_{it}) versus bandgap energy for a strained Si/SiGe and Si control MOS capacitors indicating equivalent mid-band D_{it} values.

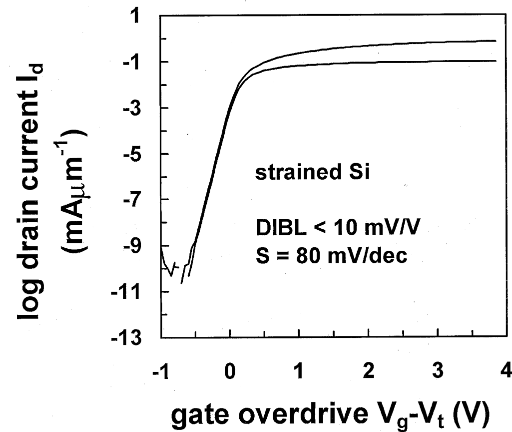

Fig. 7. Typical log I_d versus V_g–V_t characteristics for a 0.3 μm (L) × 5 μm (W) silicided strained Si device at $V_d = 0.1$ V and 1.0 V. I_{on}/I_{off} exceeds ten orders of magnitude.

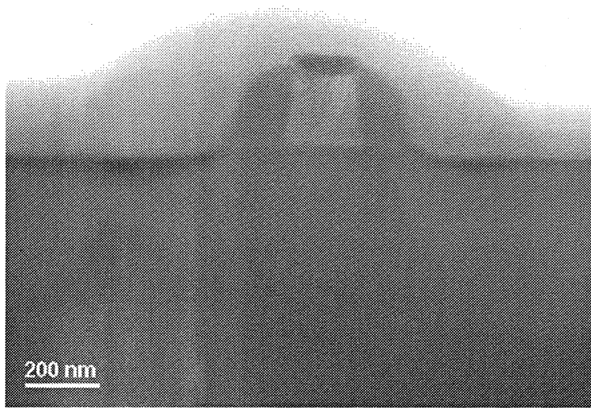

Fig. 6. Bright-field TEM image of a 150-nm drawn gate length strained Si/SiGe device structure.

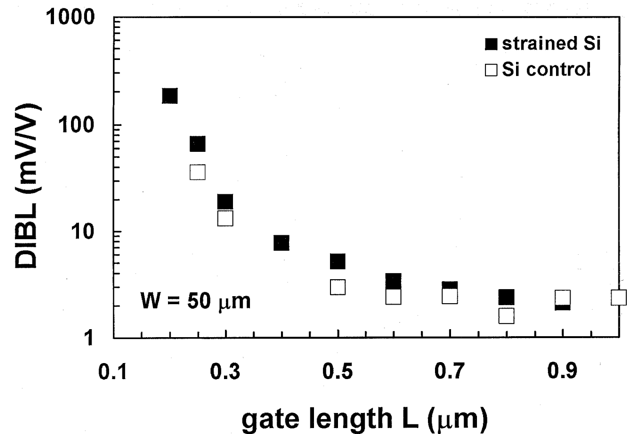

Fig. 8. DIBL as a function of gate length for silicided devices. Similar electrostatic integrity of strained Si and control devices is achieved at all gate lengths.

8 Ω/sq, as measured on standard Van der Pauw structures on the device wafers.

III. Device Results

The nMOSFETs exhibited excellent subthreshold characteristics. Fig. 7 shows the transfer characteristics of a 0.3-μm (L) silicided strained Si device at $V_d = 0.1$ V and 1.0 V. The nMOSFET gate width (W) is 5 μm. V_g is the applied gate voltage and V_t is the device threshold voltage. There is a ten order of magnitude difference between the on-state drain current (I_{on}) and the off-state drain current (I_{off}) and the subthreshold slope is 80 mV/dec. Drain-induced barrier lowering (DIBL) was found to be below 10 mV/V and equal to the control devices over a wide range of gate lengths (Fig. 8). V_t as a function of L for the devices is shown in Fig. 9 and the steepness of the roll-off characteristics for the strained Si/SiGe devices are also found to be similar to those of the Si control devices. Enhanced diffusion of As in SiGe compared with that in bulk Si may cause the slightly earlier roll-off observed for the strained Si/SiGe MOSFETs compared with the Si controls. *C–V* profiling of MOS capacitors on the Si/SiGe and Si control device wafers confirmed that N_a of the Si/SiGe wafer was equivalent to that of the Si control wafers. Therefore, the lower V_t values observed for the strained Si/SiGe device are mainly attributed to the differing electron affinities of the materials [16], [28].

The variation of transconductance g_m with gate overdrive, V_g–V_t, for 0.2 μm (L) × 5 μm (W) silicided strained Si and Si control devices is presented in Fig. 10. The maximum g_m (g_m^{max}) of the strained Si device is 334 $mSmm^{-1}$ and is enhanced by 50% compared with the Si control device at $V_d = 1.0$ V. Fig. 11 shows output characteristics of unsilicided 0.3 μm (L) × 5 μm (W) devices. Large increases in I_d of the strained Si device compared with the control device are observed despite d.c. self-heating at higher V_d, evident as the negative gradient in the curves. The self-heating of the strained Si/SiGe devices arises from the lower thermal conductivity of SiGe compared with Si [29] and results in a significantly elevated channel temperature [30]. Nevertheless, I_d of the strained Si nMOSFETs is substantially higher than recently reported strained Si devices with a similar geometry and subthreshold characteristics [16]. This is in spite of our devices having an increase in gate oxide thickness of 50% and characteristics measured without using an a.c. conductance technique to remove the effect of self-heating. At $V_d = 1.5$ V and V_g–$V_t = 1.5$ V, I_d of the

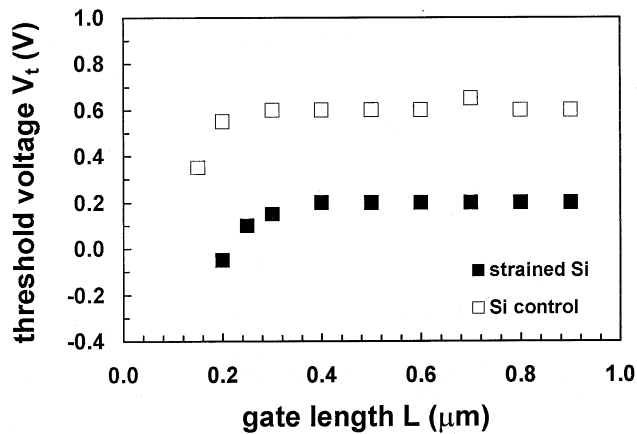

Fig. 9. V_t as a function of L for the strained Si and Si control devices.

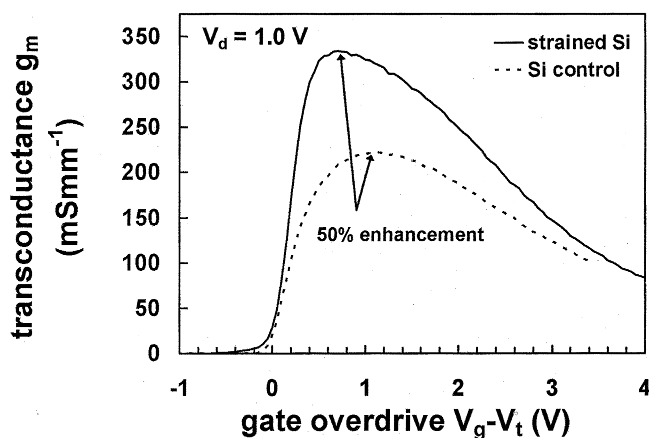

Fig. 10. g_m versus V_g–V_t curves for 0.2 μm (L) × 5 μm (W) silicided strained Si and Si control devices at $V_d = 1.0$ V. The strained Si device exhibits an increase in g_m^{max} of 50% compared with the control device.

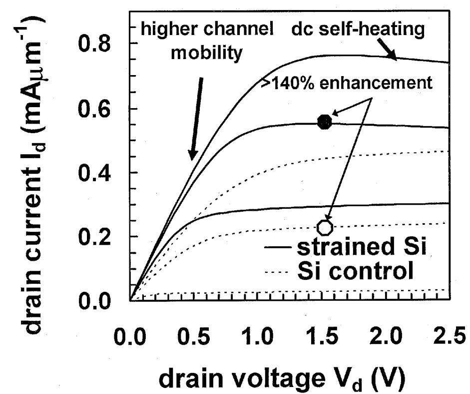

Fig. 11. I_d versus V_d characteristics of unsilicided 0.3 μm (L) × 5 μm (W) devices in V_g–V_t steps of 1.0 V from 0.5 V to 2.5 V. Current drive of the strained Si device is increased by over 140% compared with the Si control device at $V_d = 1.5$ V, V_g–$V_t = 1.5$ V despite evidence of self-heating.

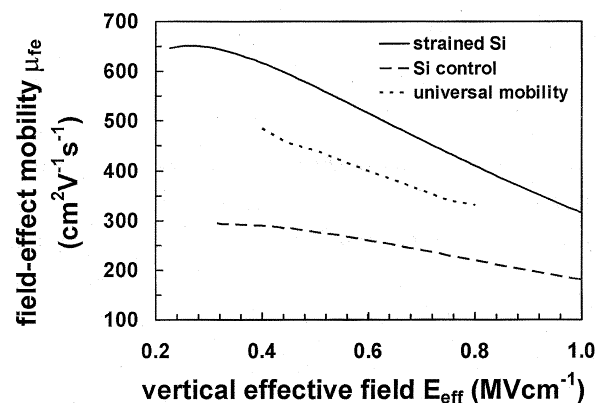

Fig. 12. Field-effect mobility μ_{fe} versus effective electric field E_{eff} measured at $V_d = 0.1$ V.

strained Si device is approximately 0.55 mAμm^{-1} and is increased by over 140% compared with the Si control device, exceeding recently published data [14], [16], [31], [32]. Moreover, unlike the strained Si devices reported in [16] and [31], the excellent performance of our devices is achieved without requiring any CMP stages. Therefore, our SiGe MOS technology provides an improved cost-effective solution to Moore's Law. The higher performance of our strained Si/SiGe nMOSFETs is attributed to full thermal budget processing and simultaneously achieving optimum channel thickness and strain conditions through use of a relatively low alloy composition VS. In addition, the strained Si/SiGe material exhibited a very low defect density. Schimmel etching was carried out and the threading dislocation density was found to be approximately 2 × 10^4 cm^{-2}. Consequently the probability of such defects degrading electrical performance is small. Simulations show that the high alloy content strain compensation layer will also allow maximum performance advantages from p-channel devices [15]. Thus, the novel design and fabrication process described have overcome the usual performance trade-off encountered in strained Si/SiGe MOS technology arising from the critical thickness, while demonstrating the most compatible architecture suitable for advanced CMOS performance to date.

The higher mobility of the strained Si MOSFET channel is indicated by the early saturation in Fig. 11. This was confirmed by examining the field-effect mobility μ_{fe} [33] on large (10 μm) gate length devices as a function of effective field E_{eff} at $V_d = 0.1$ V (Fig. 12). The peak μ_{fe} was found to be 650 cm^{2}V^{-1}s^{-1} for the strained Si devices, increased by over 120% compared with the Si control device and equivalent to the highest reported electron mobility enhancement in strained Si surface channel MOSFETS to date [16]. In addition, the peak μ_{fe} of the strained Si is greater than recently reported high-performance devices [32]. Moreover, our mobility data refers to field-effect mobility μ_{fe}, whereas commonly reported effective mobility (μ_{eff}) inflates mobility values by up to 25%, particularly at high vertical fields [33]. Nevertheless, Fig. 12 shows that strained Si mobility enhancements exceeding 100% compared with the control devices are achieved at vertical fields above 0.6 MVcm^{-1}, suitable for sub-100-nm devices. Significant mobility enhancements over the universal mobility curve are also achieved throughout the E_{eff} range investigated. The deviation observed between the Si control data and the universal mobility data is considered to primarily arise from the Si control devices being fabricated directly on bulk Czochralski-grown Si, which exhibits poor material quality compared with epitaxially grown Si. In addition, unlike field-effect mobility data, universal mobility data refers to

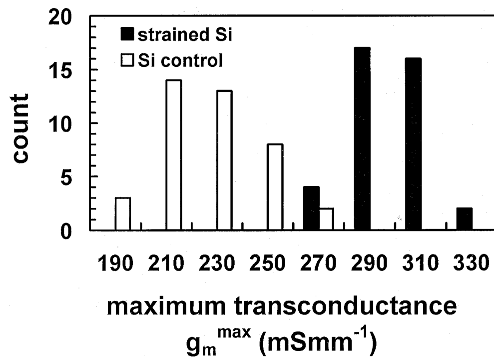

Fig. 13. Comparison of the variation in g_m^{max} of all 0.3 μm (L) $\times$ 5 μm (W) strained Si/SiGe and Si control devices. The nMOSFETs are unsilicided and the measurements were carried out at $V_d = 1.0$ V. The standard deviation of the mean value of g_m^{max} was equivalent for both sets of devices, highlighting the excellent Si/SiGe material uniformity.

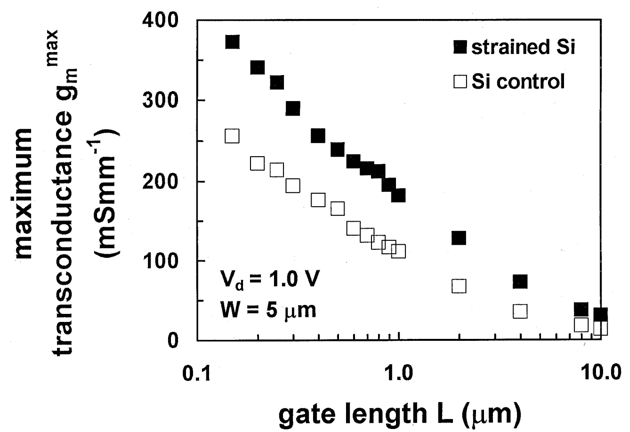

Fig. 14. g_m^{max} versus L for silicided devices at $V_d = 1.0$ V. Intrinsic values of g_m^{max} are shown. Large performance gains are achieved at all gate lengths.

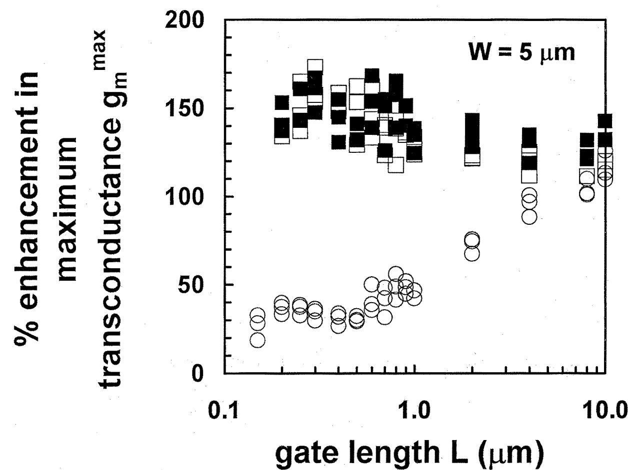

Fig. 15. Percentage enhancement in strained Si g_m^{max} (extrinsic) compared with Si control devices as a function of gate length. ■ $V_d = 0.1$ V (silicided); □ $V_d = 0.1$ V (unsilicided); ○ $V_d = 1.2$ V (unsilicided). Peak performance gains exceeding 170% are demonstrated. Similar enhancements for silicided and unsilicided strained Si devices over all gate lengths indicate successful Ti silicidation of Si/SiGe material. Self-heating causes reduced gains of strained Si/SiGe devices at higher drive currents (small L, high V_d).

effective mobility, which takes into account the degradation to mobility due to the vertical field [33].

Excellent uniformity of the strained Si nMOSFET performance was determined by device measurements on all die on the wafers. A histogram comparing the variation in g_m^{max} for 0.3 μm (L) $\times$ 5 μm (W) strained Si and control devices at $V_d = 1.0$ V is shown in Fig. 13. The standard deviation of the mean value of g_m^{max} for the strained Si devices was less than 5% and within experimental error of the deviation in g_m^{max} of the control devices. The high degree of electrical uniformity exhibited by the nMOSFETs is attributed to the uniform Si/SiGe material and demonstrates its suitability for commercial manufacture; equivalent conventional Si industrial processes currently run with similar deviations in device gain [34]. The superior g_m as well as μ_{fe} of the strained Si/SiGe devices verifies successful layer design and fabrication as well as material quality.

The higher performance of the strained Si/SiGe nMOSFETs at $V_d = 1.0$ V was consistently observed at all gate lengths investigated, as shown in Fig. 14. The relative performance of the strained Si devices and the Si controls is shown in Fig. 15. At $V_d = 0.1$ V the enhancement in g_m^{max} of the strained Si devices is greater at smaller gate lengths. Performance gains in g_m^{max} (extrinsic) exceeding 170% are clearly demonstrated. These are the highest room temperature enhancements in g_m^{max} of strained Si/SiGe surface channel nMOSFETs reported to date. The exceptional performance is shown for both silicided and unsilicided devices and indicates the success of the $TiSi_2$ process on strained Si/SiGe material. Furthermore, Fig. 8 shows that the improved performance does not compromise electrostatic integrity. As V_d is increased, transconductance enhancements of strained Si devices are reduced for all L, and in particular at shorter L; at $V_d = 1.2$ V the enhancement is reduced to below 50% for L < 0.6 μm.

The impact of device self-heating due to the low thermal conductivity of SiGe was investigated by measuring I_d/W for devices with a range of gate widths (W) while maintaining a constant field parallel to the device channel. The results for 0.3-μm (L) devices at $V_d = 1.0$ V are shown in Fig. 16. The greater deviation from ideal saturation characteristics observed for larger gate width devices is due to the generation of higher currents in these devices, verifying that the degraded performance enhancement in devices producing high current densities is due to self-heating. Thus, the reduced enhancements in g_m^{max} observed at higher bias voltages and smaller L (Fig. 15) are due to SiGe self-heating effects dominating the gain available in strained Si devices producing high current levels rather than a result of earlier velocity saturation in strained Si compared with unstrained Si [35].

The degradation in mobility at high vertical fields is dominated by surface roughness scattering. However, high values of fixed oxide charge Q_f may also degrade mobility over a wide range of E_{eff} [33]. The Si control device exhibits a slightly slower decrease of mobility with E_{eff} than observed for the strained Si device (Fig. 12). The greater dependence of μ_{fe} on E_{eff} for the strained Si device may be indicative of slightly higher gate oxide interface roughness than that of the control device. This may arise, for example, from Ge segregation from the SiGe layers into the Si channel leading to nonuniform oxidation rates [12] and consequently gate oxide interface roughness. Interference of Ge during gate oxidation additionally causes de-

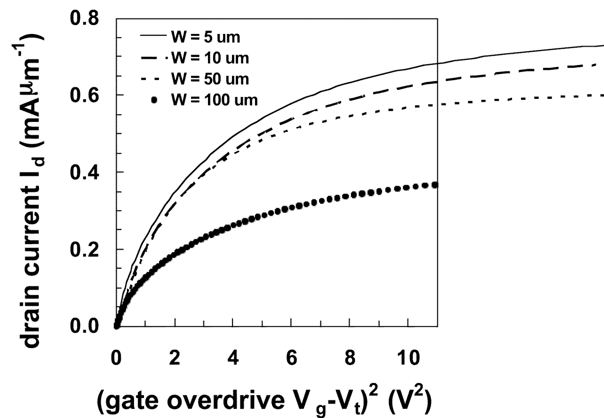

Fig. 16. Dependence of I_d on $(V_g–V_t)^2$ for 0.3-μm strained Si/SiGe devices as a function of W at $V_d = 1.0$ V. The deviation from ideal device behavior increases for larger W devices due to the increased impact of self-heating.

graded electrical properties of oxides. However, *C–V* measurements indicated that D_{it} for the strained Si devices was similar to that of the control device (Fig. 5) and therefore it is anticipated that Q_f for both devices is also similar. Consequently the impact of Ge segregation on the electrical characteristics of devices in the current study is believed to be minor. Furthermore, little difference in the gate oxide/Si interface roughness between strained and unstrained Si is expected from Si/SiGe material with such low values of cross-hatching roughness [36]. The slightly larger decrease in μ_{fe} for the strained Si device at higher fields is therefore attributed to μ_{fe} being derived from I_d, which has been shown to decrease due to self-heating at higher current levels and thus higher E_{eff}. At $V_d = 0.1$ V the effects are small (Fig. 15), in agreement with mobility data. However, at higher V_d the reduced performance advantages due to self-heating are significant (see Figs. 15 and Fig. 16). Consequently, minimizing self-heating, for example by using pulsed a.c. measurements or reducing the VS thickness will result in even greater performance gains over a wider range of operating conditions.

IV. Conclusion

High-performance nMOSFETs have been fabricated with an optimized strained Si/SiGe channel. The layer structure incorporated a high Ge content strain compensation layer, which minimized the overall strain within the device. Electrical performance in terms of transconductance, field-effect mobility and on-state drain current was found to be enhanced by up to 170% compared with conventional MOSFETs, some of the highest gains reported to date, while excellent off-state leakage currents and subthreshold characteristics were maintained. The high performance has been attained without the use of CMP or pulsed measurements. No modifications to standard processing were necessary and the gain in silicided strained Si/SiGe device performance was as great as in their unsilicided counterparts. The work suggests that pulsed measurements should be used for device measurements in order to assess the full potential of strained Si/SiGe MOSFETs, since this is a more realistic reflection of device performance in switching circuits.

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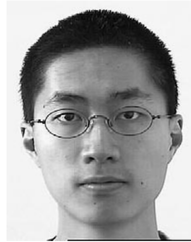

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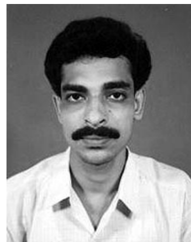

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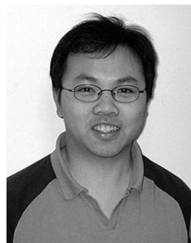

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David J. Norris photograph and biography not available at the time of publication.

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