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High performance organic transistor active-matrix driver developed on paper substrate

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The fabrication of electronic circuits on unconventional substrates largely broadens their application areas. For example, green electronics achieved through utilization of biodegradable or recyclable substrates, can mitigate the solid waste problems that arise at the end of their lifespan. Here, we combine screen-printing, high precision laser drilling and thermal evaporation, to fabricate organic field effect transistor (OFET) active-matrix (AM) arrays onto standard printer paper. The devices show a mobility and on/off ratio as high as 0.56 $cm^2V^{-1}s^{-1}$ and 10^9 respectively. Small electrode overlap gives rise to a cut-off frequency of 39 kHz, which supports that our AM array is suitable for novel practical applications. We demonstrate an 8 × 8 AM light emitting diode (LED) driver with programmable scanning and information display functions. The AM array structure has excellent potential for scaling up.

The development of new electronic devices has been made successful by integrating them onto unconventional substrates or objects, which enhances their functionalities and thus broadens their potential applications. For example, pressure and temperature sensors integrated with the clothing of athletes or medical patients, allow for real-time health monitoring and data recording[1–3]. For anti-counterfeiting and security purposes, flexible circuits and programmable non-volatile memory are deposited onto banknotes, enabling users to easily write, erase, and read the stored information by applying different gate bias levels[4–8]. As these novel devices utilize the flexible or bendable properties of organic materials, they are relatively difficult to achieve using typical rigid inorganic semiconductors. Among the different electronic components, the transistor, one of the cornerstones of the modern electronics industry, plays a crucial role in the further development of the flexible electronics. In particular, the ability of fabricating high performance flexible transistors on unconventional substrates, will enable innovative applications[9–11]. However, conventional microfabrication approaches such as spin coating or thermal evaporation may not be suitable for high roughness substrates. As a result, there is an imminent need to develop alternative microfabrication methods that can be applied suitably on rough substrates, and can scale up for large-area applications. Moreover, it is also important to investigate the growth mechanisms of organic semiconductors on rough surfaces, in order to achieve performance that is comparable to devices on smooth substrates.

Although some organic field effect transistors (OFETs) have shown comparable mobility with amorphous silicon transistors, they are usually limited to substrates with smooth surfaces such as silicon, glass and plastic films. To reduce leakage current and enhance field effect mobility, different approaches such as the substrate buffering process[8,11,12], self-assembled monolayers[5,13–20] and charge injection layers[17,21–23] have been developed to fabricate high performance OFETs on these conventional substrates. However, these approaches are usually designed for specific bulk substrate or thin-film dielectric materials with smooth surfaces, making them unsuitable for substrates with a high roughness of several micrometers (μm). Previously, in pentacene OFETs, it has been found that the carrier mobility decreases significantly from 0.31 $cm^2V^{-1}s^{-1}$ to 0.02 $cm^2V^{-1}s^{-1}$ when the silicon dioxide dielectric surface roughness increases from 0.2 nm to 1.5 nm[24,25]. A similar effect has also been reported in polymer dielectric devices where the pentacene grain size is largely influenced by the roughness variation induced by dielectric polymer chain movement[25,26]. In fact, aside from dielectric surfaces, the substrate itself can also cause the roughness effect. This is especially true for unconventional substrate materials where the substrates dominates the overall roughness. The rough surface will interrupt the lateral diffusion of the deposited organic molecules, resulting in the poor stacking of molecules and a smaller grain size, thus leading to lower carrier mobility[27].

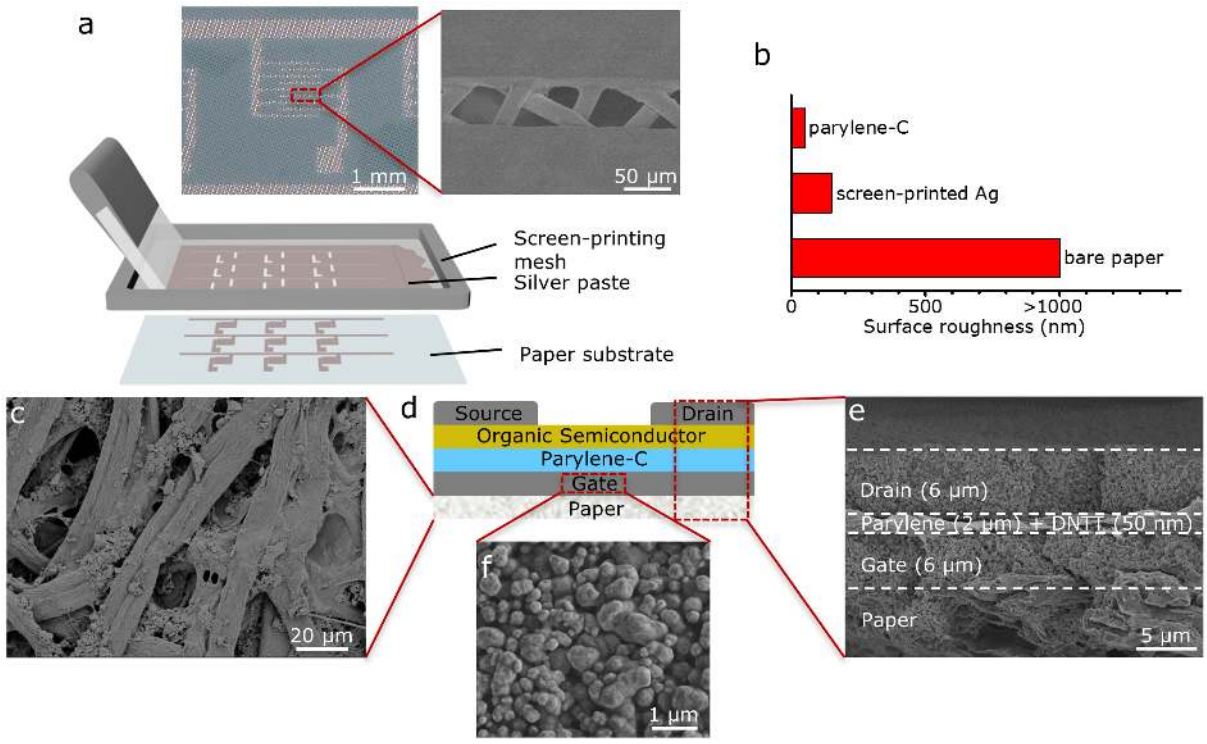

Figure 1 | Transistor structures on printer paper. (a) Schematic process of the screen-printing approach. Top middle inset shows an optical image of the enlarged source/drain pattern, where the light blue part is covered by emulsion. Top right inset is an SEM image of channel area defined between two fingers. (b) Surface roughness (root mean square) after different fabrication processes. (c) SEM surface image of the paper substrate. (d) Schematic cross sectional structure of the transistor. (e) SEM cross sectional image of the transistor under the drain electrode area. (f) SEM surface image of the screen-printed gate electrode on paper.

When selecting the substrates for flexible OFETs, polymeric materials are usually used due to their mechanical flexibility, ductility, and no lattice matching requirements[1,2,12,15,28–31]. When compared with commonly used flexible substrates such as poly(ethylene naphthalate) (PEN) or poly(ethylene terephthalate) (PET), paper substrates based on cellulose fiber are widely used in our daily life. They also have a number of advantages including a promising low cost, foldablility, and biodegradable properties. These unique assets open up new research directions for fabricating electronic devices on paper directly, and thus enable the further development of novel paper-based electronics applications. Devices like digital micro-fluidic chips[32–34], solar cells[35–37], batteries[38], and memory transistors[8,39] have been previously demonstrated. Nevertheless, the major drawback of paper substrates is the surface morphology. In typical commercial-grade printer paper made from plant fibers with diameters larger than 10 μm, the surface roughness can be up to a few micrometers (around 1,000 to 10,000 times larger than that of Si/SiO_2). As a result, obtaining high performance OFETs, let alone more complicated organic circuits, could be very challenging on such a rough surface.

Here we combine screen-printing, high resolution via-hole laser drilling, and thermal evaporation to fabricate an OFET active-matrix (AM) array (8 × 8) onto standard 80 g m^{-2} printer paper (Fuji-Xerox) without any substrate pretreatment. A statistical study of the transistor array shows uniform performance across the substrate and that device-to-device variation is insignificant. The maximum mobility and on/off ratio of the devices are 0.56 $cm^2V^{-1}s^{-1}$ and 10^9, respectively. By measuring the variation of the source-drain current under different gate bias frequency conditions, we evaluated the average cut-off frequency of the current OFETs on paper substrate to be around 39 kHz. This suggests that simple portable circuits are ready to be developed on paper substrates using the process. The 8 × 8 transistor array is further applied as an active-matrix LED driver by integrating with white color LEDs for point scanning, line scanning, and direct image display on the printer paper. Further, the presented fabrication method is suitable for scaling up to large-area devices and mass production. Our findings also shed light on new research areas of biodegradable green electronics that would have extremely low cost. The conventional printer paper can be electrically functionalized for advanced applications such as smart chips, bio-sensors, or anti-counterfeiting devices.

Results

Large-area screen-printed electrodes. To address the substrate roughness effects, we employed a screen-printing method to deposit the bottom silver (Ag) gate electrodes (Fig. 1a). The specially designed paste contains a silver nanoparticles (diameter ~300 nm) content of ~85% in carrier solvent, resulting a high viscosity of 200 Pa·s (Toyo Ink Asia, Supplementary Fig. S1a). Such a high viscosity helps prevent the paste from spreading or being absorbed into the cellulose fiber. It is also worth noting that the paste used in the current work does not require a post-deposition sintering process, and was used directly after simply drying it in an ambient air environment for 2 hours. To print the desired silver electrode patterns, a stainless steel mesh (wire diameter 18 μm) is first selectively covered by an emulsion, which fills the mesh in unused regions to create the desired gate electrode patterns. Both optical and scanning electron microscopy (SEM) images of a mesh are shown in Fig. 1a. The silver paste and different mesh patterns are then used to screen-print the source/drain electrodes and electrical interconnects using a homemade screen-printer. By optimizing both the screen printer settings and the mesh parameters, the printed electrodes can define a highly repeatable 60 μm channel length with nine source/drain fingers on each device. From the SEM images of the paper substrate (Fig. 1c) and subsequent screen-printed silver electrodes (Fig. 1f), a single layer of screen-printed

silver (~6 μm thick, Fig. 1e) is observed to significantly planarize the paper substrate and reduce the surface roughness from several micrometers down to around 150 nm (Fig. 1b). The electrical conductivity of the single layer screen-printed silver electrode on the paper substrate is measured to be 10^4 S cm^{-1}, which is comparable to other commonly used metal or indium tin oxide (ITO) electrodes. Such a large conductivity on high roughness surface is difficult to achieve by conventional thermal evaporation or magnetron sputtering of a metal thin film. Furthermore, the screen-printed gate electrode can eliminate the need for thick underlying dielectric buffer layers such as PDMS and Cytop on the paper surface[8,11]. Next, the screen-printed silver gate electrode layer is coated with a parylene-C dielectric layer via chemical vapor deposition (CVD) to a thickness of 2-μm-thick (areal capacitance $C_i \approx 1.4$ nF cm^{-2}, Supplementary Fig. S2). This process further reduces the surface roughness to 50 nm (Fig. 1b and Supplementary Fig. S3) and renders it ready for semiconductor deposition.

Semiconductor performance on a rough dielectric surface. Here we employ two different small molecular organic semiconductors, dinaphtho[2,3-b:2',3'-f] thieno[3,2-b] thiophene (DNTT) and pentacene, deposited by thermal evaporation as the device active layer and compare their performance on the paper substrate. Control samples are fabricated on ITO coated glass substrates for comparison. The schematic cross sectional structure of a single transistor device is shown in Fig. 1d. The channel width (W) and length (L) of all these single devices are 4 mm and 100 μm, respectively. In order to provide a fair comparison, a constant parylene-C layer thickness (2 μm) was used for all devices including the control samples, and the semiconductor active layers on both substrates are deposited together. The 2 μm thick parylene-C deposited onto ITO glass and screen-printed silver on printer paper had a resulting root-mean-square roughness (R_q) of 5 nm and 50 nm respectively (Supplementary Fig. S3). The device performance of all four device structures (2 substrates, 2 semiconductors) is summarized in Table 1. The DNTT and pentacene on ITO glass/parylene-C (Structures **I** and **II**) show average mobilities of 0.36 $cm^2V^{-1}s^{-1}$ and 0.074 $cm^2V^{-1}s^{-1}$. While equivalent devices on a paper substrate (Structure **III** and **IV**), exhibited carrier mobilities which decreased to 0.33 $cm^2V^{-1}s^{-1}$ and 0.038 $cm^2V^{-1}s^{-1}$, respectively. These findings suggest that the DNTT semiconductor has a higher tolerance towards substrate roughness than pentacene. From the atomic force microscope (AFM) imagery of the 50 nm thick DNTT and pentacene thin films deposited on ITO glass/parylene-C, shown in Fig. 2a and 2b, it can be observed that the pentacene grain size is smaller and more grain boundaries are apparent, while the DNTT thin film exhibits a stronger layer stacking structure with fewer grain boundaries. The large roughness of the underlying screen-printed silver nanoparticles on the paper substrate makes measuring the exact surface morphology of the organic active layer difficult (Fig. 2c and 2d). To characterize the active layer growth for the first few monolayers, we performed AFM measurements on the first 5 nm of both DNTT and pentacene (Fig. 2e and 2f). From the insets of Fig. 2e and 2f, it can be clearly noted that the first 5 nm of DNTT prefers to form taller island structures rather than covering a larger area of parylene-C. On the other hand, no significant individual islands are observed for the first few monolayers of pentacene and they tend to cover a larger area of parylene-C dielectric (Frank-van der Merwe mode)[40]. It is believed that the observed distinct behavior of DNTT and pentacene on the high-roughness substrate is correlated to different growth modes of the organic semiconductors. Our findings provide direct evidence that although the surface roughness is commonly believed to be one of the key limiting factors on the performance of OFETs, it can still be counterbalanced by the growth mode of the organic semiconductor materials.

Table 1 | Transistor performance comparison of the four designed structures

Structure	I	II	III	IV
Semiconductor	DNTT	Pentacene	DNTT	Pentacene
Substrate	Glass	Glass	Paper	Paper
Gate	ITO	ITO	SP Ag	SP Ag
$\mu(cm^2V^{-1}s^{-1})$	0.36	0.074	0.33	0.038
$V_{TH}(V)$	−15.4	−27.9	−1.22	−30.7

"SP Ag" stands for screen-printed silver;
Gate dielectric is 2-μm-thick parylene-C.

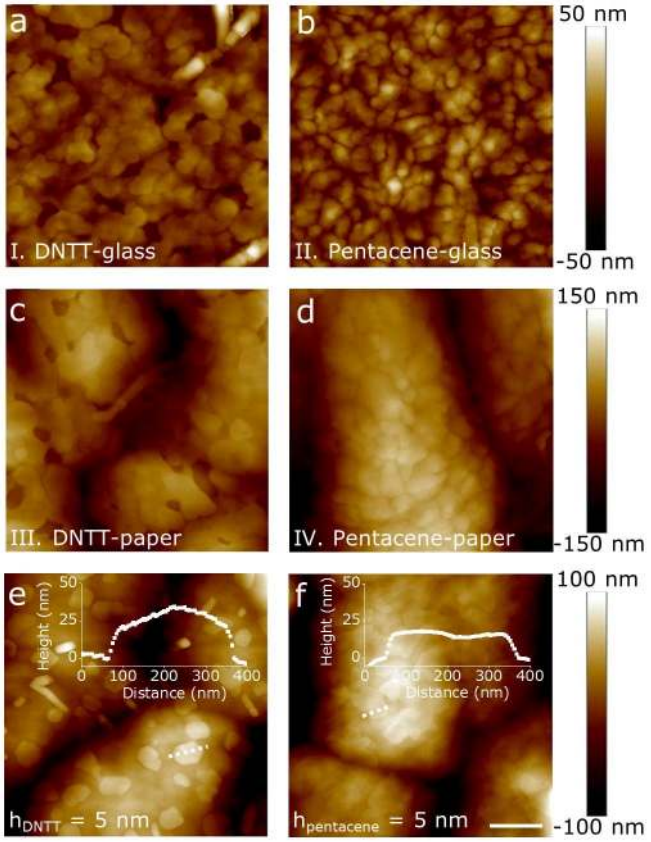

Figure 2 | AFM investigation on semiconductors growth on different surfaces. (a–d) AFM images of semiconductor surface morphology (50-nm-thick) of structures I, II, III and IV of Table 1. AFM images of the semiconductor surface morphology of 5-nm-thick (e) DNTT and (f) pentacene grown on a parylene-C surface on screen-printed Ag electrodes and paper substrate. Scale bar is 500 nm. Inset of (e) and (f) are the height profiles of the sample grains (white dotted lines).

Active-matrix transistor array on paper. Based on these highly reproducible OFETs, we further develop a more complex active-matrix OFET array onto the paper substrate (see Supplementary Fig. S4 for the schematic fabrication steps). The active-matrix (AM) transistor array is widely used as the driver in displays[41–45] and is dominated by silicon-based technology. Unlike discrete devices, where each transistor has its own three terminals (source, drain and gate), an AM array uses the crossing points of orthogonal row and column electrodes to locate each pixel, resulting in far fewer control electrodes. This configuration greatly reduces the space occupied by electrode lines to allow a much higher device density. However, the performance requirement for each transistor in the AM array is also higher, as one short or open circuited transistor may result in the breakdown of an entire row or column of the array.

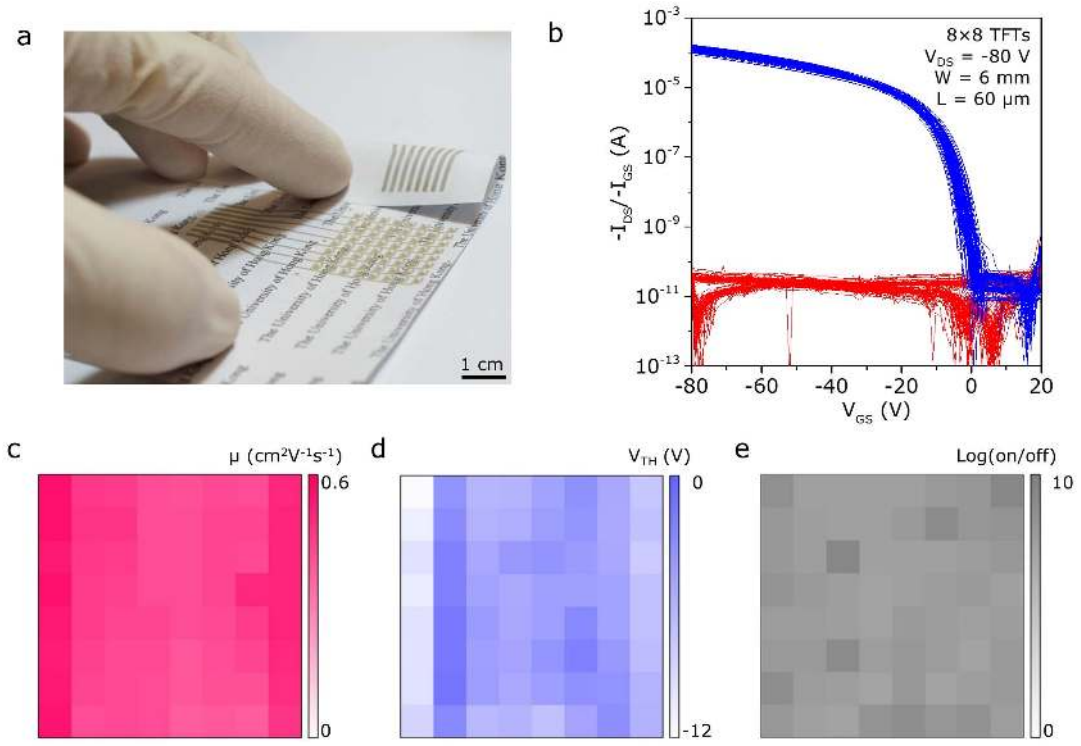

Figure 3 | Uniformity test of 8 × 8 active matrix (AM) transistor array. (a) AM transistor array on printer paper with pre-printed information. (b) 64 transfer curves of one AM array automatically acquired using LabVIEW™. (c–e) Mobility, threshold voltage (V_{TH}), and on/off ratio (log value) colormaps of the 64 transistors in the AM. Mobility mean value is 0.45 $cm^2V^{-1}s^{-1}$ with a standard deviation of 0.05 $cm^2V^{-1}s^{-1}$; V_{TH} mean value is −4.7 V with a standard deviation of 1.5 V; On/off ratio has a mean value of 1.5×10^8 and standard deviation of 3.7×10^8.

The challenge of realizing an AM array with a large device density, good large-area uniformity, and a high yield rate is further heightened when fabricating on high-roughness paper substrates. Here we realize an 8 × 8 AM OFET array with a pixel size of 3 mm × 3 mm corresponding to a resolution of 8.4 dots per inch (DPI). The completed array on a printer paper substrate, with laser pre-printed information, is shown in Fig. 3a. Unlike the single device geometry, the gate lines of the array are placed on the backside of the paper substrate to eliminate an extra crossing between electrodes to help suppress the leakage current. The backside gate lines are connected to the gate electrodes through two via-holes drilled through the substrate via a CO_2 laser. The through-paper via-holes are filled with Ag paste using the doctor blading technique and a laser-cut mask. Setting the via-hole diameter to 60 μm results in a 100% yield of electrical connections between the gate lines and gate electrodes (see Methods for experimental details). Fig. 3b shows the transfer curves of all 64 OFETs in a single 8 × 8 array. It should be noted that all the transistors exhibit uniform transfer characteristics, on/off ratios larger than 10^7, and leakage currents lower than 100 pA. The mobility, threshold voltage, and on/off ratio of the 64 devices are plotted as colormaps in Fig. 3c, 3d and 3e. The average mobility, threshold voltage and on/off ratio are 0.45 $cm^2V^{-1}s^{-1}$, −4.7 V and 1.5×10^8, respectively. The standard deviations of the mobility and the threshold voltage are as small as 0.05 $cm^2V^{-1}s^{-1}$ and 1.5 V. The slight mobility increase from the discrete transistor (Table 1) to the AM array structure (from 0.33 $cm^2V^{-1}s^{-1}$ to 0.45 $cm^2V^{-1}s^{-1}$) is attributed to the decrease of channel length from 100 μm to 60 μm, resulting in a decrease of the total grain boundary effects that dominate the overall mobility. It is also worth mentioning that the measured threshold voltages have a higher magnitude for the transistors with gate electrodes at the array edge. As the currents in the on state of edge devices are similar to other devices located elsewhere, the measured mobilities of these devices at the edge are relatively higher.

LED integration to AM array. To further demonstrate the application potential of the current OFET AM array on paper, we integrate light emitting diodes (LEDs) onto the individual source contacts of the array and use the array as the driver for a graphical display. A cross sectional schematic diagram of a single array pixel is shown in Fig. 4a, and optical image of the fabricated array is shown in Fig. 4c. It should be noted from Fig. 4a that on top of the AM array we deposit an additional parylene-C layer to prevent the overlap between drain lines and source lines at their intersection (red dotted box in the inset of Fig. 4c). After deposition of the top parylene-C layer, an additional laser drilling process is applied to create two via-holes to expose source electrodes through the parylene-C and allow screen-printing of the source lines directly. Contact pads for the discrete LEDs are co-fabricated with source lines in a single printing step, and are followed by LED mounting. From the inset of Fig. 4c detailing a single array pixel, the 60 μm channel gap can be clearly observed between the source and the drain electrodes. The 60 μm channel length with nine source/drain fingers can provide sufficient current for the LEDs and, at the same time, maintain the high device yield rate. The terminations of the source, drain and gate lines are designed to mate with commercial flexible flat cables (FFCs) for a direct plug-in connection. Three multiplexers are connected to the gate, source, and drain lines respectively to control array via device bias. These bias signals from the sourcemeters, and the three multiplexers, are synchronized by a custom LabVIEW™ (National Instruments) program on a control computer as shown in the driving circuit diagram in Fig. 4b. In order to visualize individual device currents and demonstrate the array capabilities, we control the switching methods of the different multiplexers to achieve both single point scanning (Fig. 4d) and line scanning (Fig. 4e). Figure 4f further demonstrates the image display application of the paper-based AM LED array by using the programmable scanning process and to pattern and clearly display the letters "HKU."

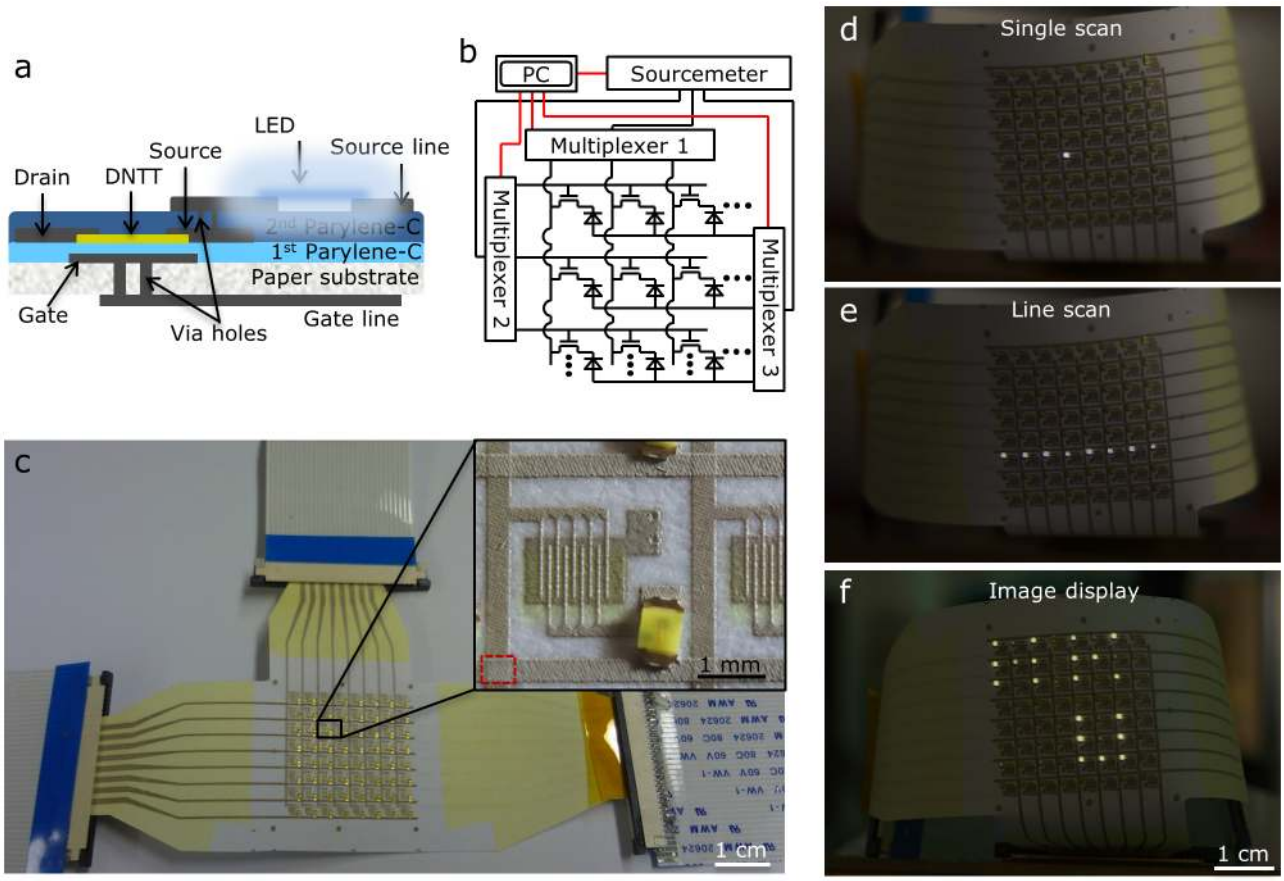

Figure 4 | OFET AM driver scanning and information display. (a) Schematic of OFET AM driver. (b) Array driving circuit, red lines correspond to digital signals and black lines to analog signals. (c) Optical image of OFET AM LED driver, standard connector interfaces to FFCs (flat flexible cables) are formed by screen-printing. Inset is an enlarged single pixel of the array, where the red dotted box indicates the insulation layer (2nd parylene-C) between drain (vertical) and source (horizontal) electrodes. $V_{GS} = -40$ V and $V_{DS} = -15$ V are used to operate the OFET AM LED driver. Different operating conditions of the driver are shown. (d) Single scan, one by one operation of each pixel. (e) Line scan, row by row operation of pixels. (f) Image display using programmed fast scanning to display "HKU" in capital letters.

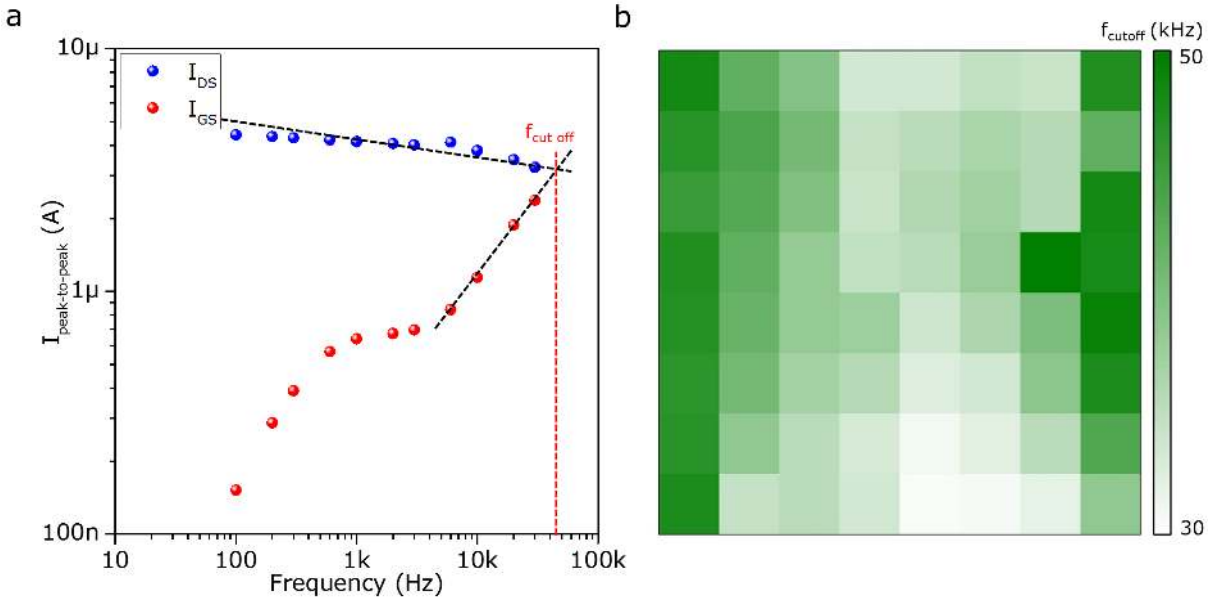

Figure 5 | Cut-off frequency of the AM array (a) $V_{DS} = -80$ V, V_{GS} (DC) $= -60$ V, V_{GS} (AC, peak to peak) $= 2$ V. Cut-off frequency is determined as the frequency where $I_{DS,\ pk\text{-}pk}$ equals to $I_{GS,\ pk\text{-}pk}$. (b) Cut-off frequency colormap of the AM array.

Cut-off frequency. The short channel length and little overlap between the source/drain and gate electrodes can enable a high operating frequency of the realized AM array[17]. A high operating frequency of the transistor array structure is extremely important for large-scale applications where a large number of devices are interconnected. To test the cut-off frequency of the fabricated structures, we measured the peak-to-peak source/drain current ($I_{DS,\ peak\text{-}peak}$) and gate current ($I_{GS,\ peak\text{-}peak}$) variations induced by a modulated gate bias under different frequencies. The cut-off frequency is defined as the operating frequency when $I_{DS,\ peak\text{-}peak}$ equals, $I_{GS,\ peak\text{-}peak}$. The measured values of the $I_{DS,\ pk\text{-}pk}$ and $I_{GS,\ pk\text{-}pk}$ of a typical device under different frequencies are shown in Fig. 5a, and the cut-off frequency can be obtained through a linear fitting of the log-log plot. The average cut-off frequency is of all 64 devices in an 8 × 8 array is around 39 kHz. This value compares favorably to a value of 41.3 kHz calculated using transistor parameters in the equation below:[17]

$$f = \frac{\mu |V - V_{TH}|}{2\pi L(L + 2\Delta L)} \quad (1)$$

where L is the channel length and ΔL is the overlapping length between the gate and source/drain electrodes which induce parasitic capacitance. A cut-off frequency colormap of all transistors in an array is shown in Fig. 5b, where the lowest frequency and highest frequency are ca. 30 kHz and 50 kHz, respectively. It suggests the number of devices in the array can be higher than the current demonstration of 64 devices.

Discussion

In summary, we developed a methodology combining screen-printing, laser drilling, and thermal evaporation to fabricate OFET active-matrix arrays on standard printer paper without pre-treatment. All electrode patterning is performed by a high-resolution screen-printing method with a fast speed and high potential for large-area production. Fine patterning of the electrodes allow for a remarkable channel length (60 μm) on the standard printer paper with an extremely high yield rate. Although rough surfaces are generally believed to be unsuitable for organic electronics, especially small molecule semiconductors, the realized DNTT OFETs on printer paper show comparable performance to those on conventional flat substrates. An 8 × 8 active-matrix array with 8.4 DPI resolution is successfully demonstrated and employed as an AM LED driver. Fully programmable scanning and information display functionality of the OFET AM LED array demonstrated the great potential of realizing new functionalities to standard printer paper. The presented technique can also be applied to memory, sensor and/or photovoltaic fabrication onto paper substrates, which can greatly broaden the application areas of paper-based green electronics.

Methods

AM array fabrication. The fabrication process started using 99.99% nitrogen to blow the surfaces of the paper substrate to dislodge particulates. Through-substrate via-holes were created with a CO_2 laser system (Universal, VLS 2.30) with 1.8% power, 1% speed and 1000 DPI. Due to the flammability of paper, no thermal expansion and local surface roughness changes were caused at laser focal points. The via-hole diameter was fixed to be around 60 μm with sharp well-defined edges. Relatively low viscosity Ag paste (diluted paste, Supplementary Fig. S1b) was filled into the via-holes to serve as the electrical conductor. The backside gate bus lines were then formed by screen-printing on a homemade printing stage. The optimized distance between the screen frame and substrate was set to be 0.9 mm. The printing speed was controlled to lower than 10 cm/s to ensure well-defined metal patterns. For all printing processes, if not specified, the printer paper was held by a vacuum suction stage to guarantee a uniformly printed pattern. Gate electrodes were next formed by screen-printing on the top side of the via-holes. The thickness of a single layer screen-printed electrode was 6 μm. Parylene-C was adopted as the gate dielectric layer because of its large-area capability, uniformity, and cost-efficiency. In order to ensure a uniform coating over all the gate electrodes and prevent leakage, the parylene-C layer thickness was set to be 2 μm at a deposition pressure of 25 mTorr (PDS 2010, SCS). After gate dielectric formation, 50-nm-thick DNTT or pentacene film was deposited by thermal evaporation at a base pressure lower than 1×10^{-6} Torr (Moorfield). Silver source and drain electrodes were also printed by the screen-printing process. The entire AM array was then held in a glove box for 2 hours to allow all solvents to dry. This corresponds to steps 1–6 of Supplementary Fig. S4.

OFET AM LED driver fabrication. After AM array fabrication, 5-μm-thick parylene-C layer was then deposited to act as the cross point insulator. To expose the source electrodes underneath the second parylene-C layer, another CO_2 laser drilling process was performed (0.3% power, 1% speed). Contact pads for the discrete micro-LEDs and the source bus lines were screen-printed together. For the final fabrication step, 64 micro-LEDs were mounted manually under an optical microscope. The completed OFET AM LED array was then plugged into a standard flexible flat cable (FFC) interface (1 mm pitch) to connect it to the electrical testing system. This corresponds to steps 7–9 of Supplementary Fig. S4.

Measurements. Transfer curves were obtained by a Keithley 2636B dual-channel source-meter under darkness in a glove box (water and oxygen content lower than 1 ppm). Cut-off frequency data was measured using a signal generator (Agilent 33210A), voltage amplifier (Thorlabs HVA200), and lock-in amplifier (Stanford SR 850). AC voltage signals were generated by the signal generator and linearly amplified. This amplified AC signal was then used as the gate-source voltage (Supplementary Fig. S6). A constant DC drain-source voltage of −80 V was applied to ensure transistor operation in the saturation regime. Peak to peak values of the drain-source and gate-source currents were acquired using a resistor (12 kΩ) combined with the lock-in amplifier.

The OFET AM driver was demonstrated by applying a $V_{GS} = -40$ V and $V_{DS} = -15$ V. A custom LabVIEW™ (National Instruments) program was employed to control the AM drivers by selectively opening or closing specific channels through a Keithley 7011 multiplexer. For point scanning, row scanning and information display, each step of the device scanning was pre-defined in the LabVIEW™ program to complete an entire image frame. Each from was then frame looped and changed over multiple refresh cycles to display the desired scanning functions. The electromechanical switching mechanism of the multiplexer limited the frame refresh rate of information display mode to 3 Hz. However, from the cut-off frequency measurements, the AM driver is capable of frame refresh rates of several hundred Hertz.

AFM characterization was completed via a Bruker Multimode 8 scanning probe microscope, and SEM imaging was performed with a Hitachi S-4800 field emission scanning electron microscope. XRD measurements made use of a Rigaku SmartLab X-ray Diffractometer. An Agilent 4294A Precision Impedance Analyzer was utilized for capacitance measurements.

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Author contributions

P.K.L.C conceptualized the work. B.P. carried out most of the experimental work including device fabrication and characterization. P.K.L.C and B.P. wrote the manuscript. X.R. offered ideas and helped in electrical circuit design. Z.W. carried out capacitance measurements and SEM. X.W. helped with thermal evaporation of the materials. R. C. R. offered ideas and helped in editing the manuscript. All authors discussed the results and commented on the manuscript.

Additional information

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