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COMMUNICATION

# High-performance Si microwire photovoltaics†

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**Crystalline Si wires, grown by the vapor–liquid–solid (VLS) process, have emerged as promising candidate materials for low-cost, thin-film photovoltaics. Here, we demonstrate VLS-grown Si microwires that have suitable electrical properties for high-performance photovoltaic applications, including long minority-carrier diffusion lengths ($L_n \gg 30$ μm) and low surface recombination velocities ($S \ll 70$ cm·s$^{-1}$). Single-wire radial p–n junction solar cells were fabricated with amorphous silicon and silicon nitride surface coatings, achieving up to 9.0% apparent photovoltaic efficiency, and exhibiting up to ~600 mV open-circuit voltage with over 80% fill factor. Projective single-wire measurements and optoelectronic simulations suggest that large-area Si wire-array solar cells have the potential to exceed 17% energy-conversion efficiency, offering a promising route toward cost-effective crystalline Si photovoltaics.**

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The favorable band gap and natural abundance of Si, combined with the large expertise base for semiconductor wafer processing, have led to the use of wafer-based crystalline Si in the vast majority of photovoltaic cells and modules produced worldwide. However, the high cost of purifying, crystallizing, and sawing Si wafers has inhibited these photovoltaic energy sources from approaching cost parity with fossil fuels, thus motivating the development of thin-film solar cells that can be deposited onto inexpensive or reusable substrates.[1,2] Crystalline Si wires, grown by the catalytic vapor–liquid–solid (VLS) chemical vapor deposition (CVD) process,[3] have recently emerged as promising candidate materials for thin-film photovoltaics that seek to combine low-cost Si deposition techniques with mechanically flexible, high-performance solar cell geometries.[4–20] Unlike conventional planar CVD techniques, VLS growth enables the precise control of the crystal grain size (*i.e.*, the wire dimensions)[16] as well as the physical access to modify or passivate the crystal surfaces, allowing the fabrication of novel solar cell geometries that optimally balance optical absorption with charge-carrier collection, such as radial p–n junctions.[4] Furthermore, arrays of VLS-grown wires afford numerous advantages for thin-film photovoltaic processes, including high absorption and effective optical concentration,[8,9] ease of layer-transfer by polymer encapsulation and mechanical peel-off,[17] and compatibility with either re-usable[18] or low-cost (*e.g.*, glass or foil) growth substrates.[7,8,19] For these reasons, VLS-grown Si-wire solar cells have attracted substantial interest, resulting in up to ~8% efficient wire-array devices,[5–8] ~3.5% efficient single-wire devices;[10–12] and ~3% efficient photoelectrochemical devices.[13–15] Reaching the >17% efficiency and >600 mV open-circuit voltage predicted for VLS-grown Si-wire solar cells,[20] however,

## Broader context

Throughout decades of double-digit growth of the photovoltaics (PV) industry, crystalline Si wafer-based solar cells have remained the predominant worldwide PV technology due in part to high module efficiencies (15–21%) and the tremendous scale at which they are manufactured. However, producing Si wafers is a costly and energy-intensive process, which has enabled lower-cost, less-efficient (8–12%) *thin-film* PV technologies such as CdTe to gain significant market share in recent years. Technologies that combine the high efficiency, abundance, and non-toxicity of crystalline Si with the low cost and light weight of thin-film PV have the potential to significantly accelerate the adoption of PV energy. In this report, we investigate crystalline Si microwires grown by the vapor–liquid–solid (VLS) process, a thin-film vapor deposition technique. By fabricating and measuring single-wire test structures, we find that these wires possess remarkably high material quality, potentially enabling Si microwire-array solar cells to reach efficiencies that rival those of many wafer-based crystalline Si technologies (>17%). These results suggest that VLS-grown microwires may offer a viable alternative to wafers for the production of cost-effective crystalline Si photovoltaics.

requires substantial improvements in junction quality, surface passivation, and minority-carrier diffusion length (which thus far has been reported as high as ~10 μm).[21,22] Herein, we present VLS-grown Si single-microwire solar cells that combine these properties to realize high photovoltaic performance.

The steps used to fabricate the Si wire solar cells are depicted in Fig. 1, and are described in detail in the ESI†. Ordered arrays of p-type crystalline Si microwires (1.2–1.8 μm diameter) were grown from gaseous $SiCl_4/BCl_3$ on Si(111) wafers using a patterned VLS CVD process (Fig. 1a).[16] Whereas most prior reports of VLS-grown Si-wire solar cells have employed Au as the growth-catalyst metal,[6–8,10–14] the growth of our wires was catalyzed by Cu, which requires higher temperatures for VLS growth, but which is less deleterious to the performance of crystalline Si photovoltaics as an impurity.[23] Deposition was performed at 1000 °C at 1 atm total pressure, yielding growth rates of ~5 μm $min^{-1}$. After growth, the Cu catalyst was chemically removed. Radial p–n junctions were then selectively formed within the upper portion of each wire by thermal phosphorus diffusion at 850 °C, using a polymer-infill (PDMS) etch-mask to define a $SiO_2$ diffusion barrier over the lower portion of each wire (Fig. 1b–e).[5] Single-wire devices were fabricated from wires that were removed from the growth wafer, deposited onto transparent (sapphire) or reflective ($SiN_x$-coated Ag) insulating substrates, and then patterned with Ag-capped Al contacts.[12] Typical devices had

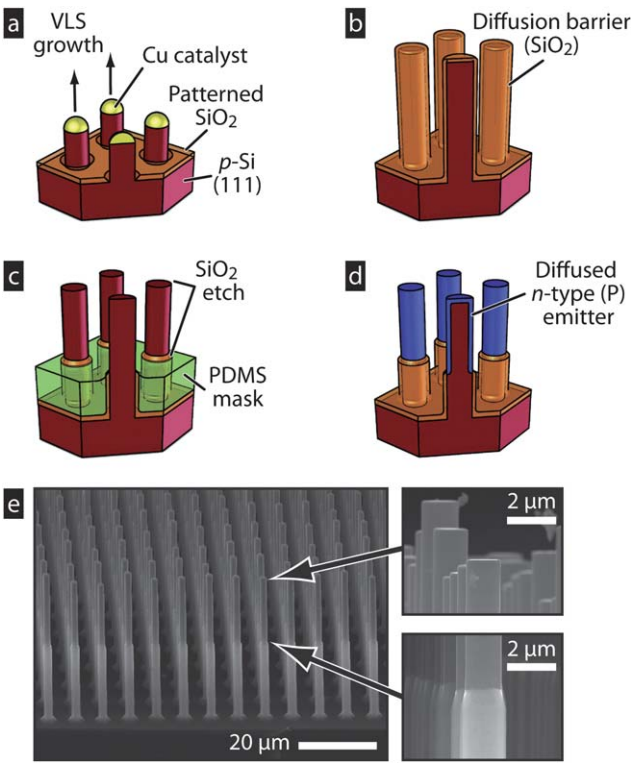


**Fig. 1** Fabrication of radial p–n junction Si microwire arrays. Schematic diagrams depict: (a) VLS-growth of p-type Si microwire arrays; (b) catalyst removal and growth of a thermal-oxide diffusion-barrier; (c) selective removal of the oxide barrier using a polymer-infill etch mask; and (d) thermal diffusion of radial p–n junctions. (e) SEM images of a microwire array following the fabrication step depicted in (d), viewed at ~45° tilt (left) and ~90° tilt (right).

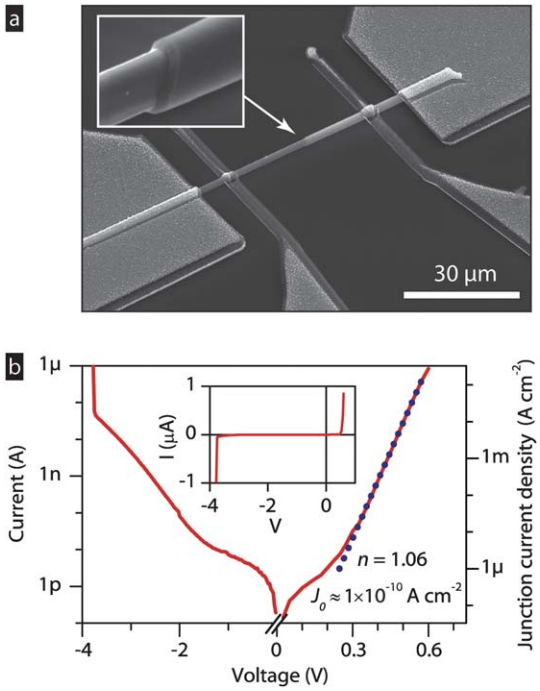


**Fig. 2** Single-Si-microwire device. (a) SEM image, and (b) dark *I–V* behavior of a typical single-wire device. The arrow indicates the start of the radial p–n junction, which extends to the left. Nearly identical *I–V* behavior was observed between the inner *vs.* the outer contacts. The junction current density and the dark saturation current density ($J_0$) were both normalized to the estimated surface area (~3 × $10^{-6}$ $cm^2$) of the radial p–n junction, which was calculated assuming a 100 nm junction depth.

a single contact to either end of the wire, however, four (Fig. 2a) or eight contacts were patterned to some wires, to allow full characterization of the effective base doping (~1 × $10^{17}$ $cm^{-3}$) and the sheet resistance of the emitter (~6 kΩ □$^{-1}$), as well as to confirm that the contacts to both regions were ohmic and low-resistance (<5% of device resistance). Fig. 2b shows the dark current–voltage (*I–V*) characteristics of a typical single-wire device. Ideality factors, *n*, of 1.0–1.2 were observed for most devices, indicative of high-quality, low-recombination p–n junctions.

Due to the high surface-area-to-volume ratio, Si wire solar cells are very sensitive to surface recombination, particularly within the bottom segment of each wire where no radial p–n junction is present (henceforth referred to as the *axial* region of the device). In this region, minority carriers must diffuse axially to reach the junction in order to be collected (Fig. 3a, top). The effective distance that carriers can travel before recombining, $L_{eff}$, can be greatly reduced by surface recombination, and surface-limited values of $L_{eff}$ as low as ~20 nm have been reported for VLS-grown Si nanowires.[22] To determine the $L_{eff}$ of our Si microwires, scanning photocurrent microscopy (SPCM) was performed to obtain spatially resolved maps of minority-carrier collection within the single-wire solar cells.[12,21] As shown in Fig. 3a (bottom), relatively uniform carrier collection was observed throughout the radial portion of the wires, but no carrier collection was observed from the axial portion. In fact, the abrupt spatial transition between the two collection regimes could not be resolved by the ~0.5 μm diameter beam spot of the $\lambda = 650$ nm illumination

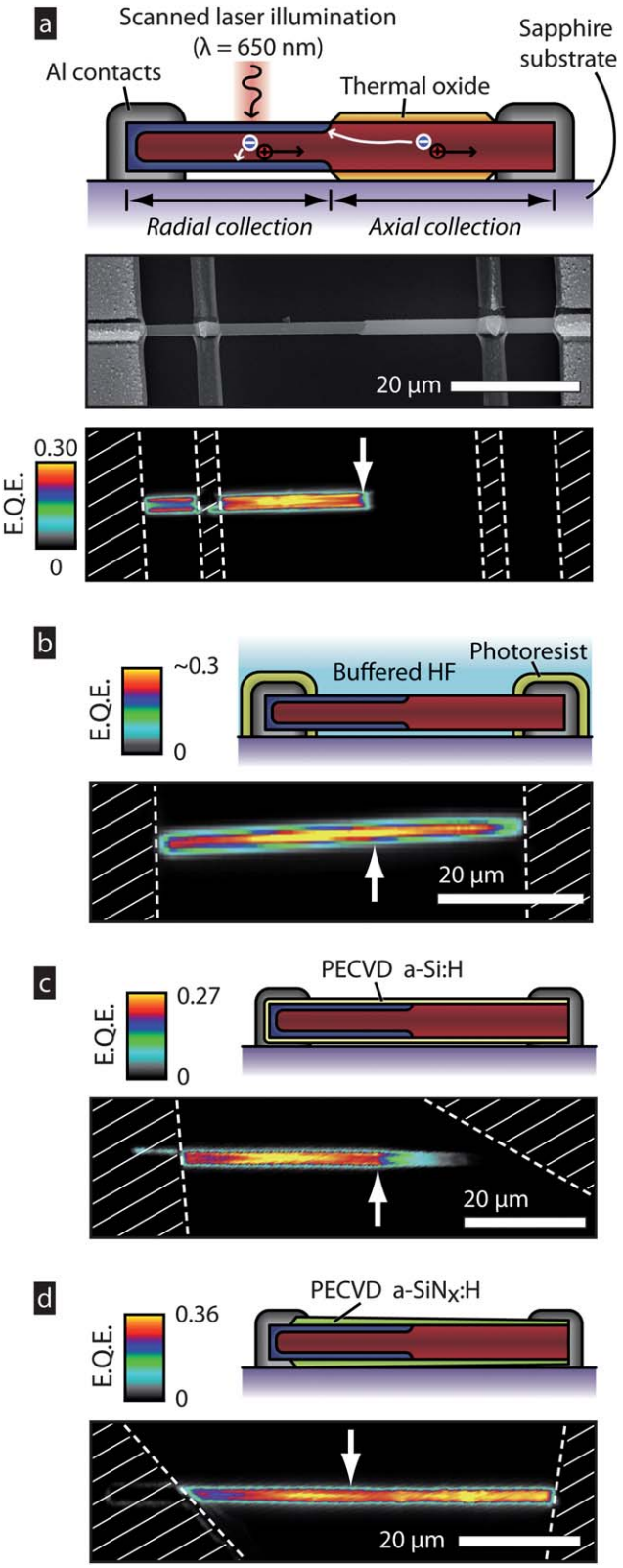


**Fig. 3** SPCM characterization of minority-carrier recombination in Si microwire radial p–n junction solar cells. (a) Top: schematic diagram of SPCM measurements performed on the single-wire test structures of the type depicted in Fig. 2b, which had $SiO_2$-coated axial-region sidewalls and bare (native-oxide-coated) radial-region sidewalls. Below: SEM image (center) and SPCM image (bottom) of a typical device. Schematic diagrams (top) and SPCM images (bottom) for wires with surfaces passivated by buffered HF (b), a-Si:H (c), and a-$SiN_x$:H (d). All SPCM measurements were normalized to the incident beam photocurrent and are reported in terms of external quantum efficiency (EQE). In all SPCM images, the white arrow indicates the start of the radial p–n junction (which extends to the left) and the hashed white areas indicate the location of the metal contacts.

source, indicating that the effective axial minority-carrier collection length, $L_{eff}$, was ≤0.5 μm for the as-fabricated Si wires.

To determine whether $L_{eff}$ was limited by bulk or surface recombination, the SPCM measurements were repeated on single-wire devices that were fully immersed in pH = 5.0 buffered hydrofluoric acid (BHF). Hydrofluoric acid removes oxides from crystalline Si surfaces and provides hydrogen-termination of dangling bonds, resulting in unusually low surface recombination velocities ($S$ < 1 cm $s^{-1}$).[24] With the single-wire devices immersed in BHF (waiting ~3 min for the $SiO_2$ diffusion-barrier to be removed), uniform carrier collection was observed from both the axial and the radial portions of the wire (Fig. 3b), with no apparent spatial decay throughout the ~20 μm length of the axial wire segment ($L_{eff} \gg$ 20 μm). This behavior implies that the bulk minority-carrier diffusion length, $L_n$, was ≫20 μm, and that the relatively short $L_{eff}$ observed prior to BHF immersion was thus due to a high surface recombination velocity of $S > 4 \times 10^5$ cm $s^{-1}$ (see ESI† for details of SPCM measurements and determination of $L_{eff}$ and $S$).

To effect passivation of the Si microwire solar cells with an air-stable solid-state surface termination, we used plasma-enhanced CVD (PECVD) to coat the wires with amorphous hydrogenated thin films of either Si (a-Si:H) or silicon nitride (a-$SiN_x$:H). PECVD a-Si:H and a-$SiN_x$:H coatings are commonly used in solar cell fabrication due to their stability and ease of growth ($T$ < 400 °C).[25,26] Low surface recombination velocities ($S$ < 10 cm $s^{-1}$) have been reported for Si surfaces coated with either material, and each offers additional beneficial properties for photovoltaic applications: a-$SiN_x$:H also functions as a versatile anti-reflective (AR) coating for crystalline Si,[27] while a-Si:H forms a heterojunction to crystalline Si, enabling extremely high open-circuit voltages (up to 743 mV) for wafer-based Si solar cells.[28] After diffusing p–n junctions into a Si wire-array as described above, we removed the remaining surface oxide, performed a standard clean, and then split the array into several pieces. One array was coated with ~10 nm of undoped PECVD a-Si:H that was grown from $SiH_4$ (5% in Ar) at 240 °C. Another was coated with low-stress PECVD a-$SiN_x$:H that was grown from $SiH_4$ (5% in $N_2$) and $NH_3$ at 350 °C, the thickness of which tapered from ~120 nm at the wire tips to ~60 nm at the wire bases (see ESI, Fig. S3†). Both PECVD films were also deposited onto planar p-type control wafers (400 μm float-zone Si, double-side-polished, $\rho$ > 4 kΩ cm) to enable optical characterization by spectroscopic ellipsometry (see ESI, Fig. S1 and S2†), as well as microwave-frequency photoconductivity decay measurements[29] which indicated $S$ < 20 cm $s^{-1}$ for a-Si:H passivation and $S$ < 10 cm $s^{-1}$ for a-$SiN_x$:H passivation. The a-Si:H-coated single-wire devices were annealed at 275 °C for 30 min in forming gas (5% $H_2$ in $N_2$) to produce ohmic contacts through the a-Si:H (Fig. 3c). To enable electrical contact to the a-$SiN_x$:H-coated wires, prior to removal from the growth substrate, the nitride was removed from the wire tips using an infill-masked chemical etch (Fig. 3d).

 

Shown in Fig. 3c, the SPCM profile of a typical a-Si:H-coated single-wire solar cell indicated axial-region carrier collection with a characteristic decay length of $L_{eff} \approx 10$ μm, indicating a surface recombination velocity of $S \approx 450$ cm s$^{-1}$ (see ESI, Fig. S7†). In contrast, the SPCM profile of a typical a-$SiN_x$:H-coated single-wire solar cell (Fig. 3d) exhibited high carrier collection efficiency throughout the entire axial portion of the wire, with no apparent decay length ($L_{eff} \gg 30$ μm). Furthermore, the EQE of the a-$SiN_x$:H-coated devices was markedly higher than that of the non-coated devices, due to the anti-reflective nature of the nitride coating. In fact, the EQE was usually greatest within the axial portion of these wires, because the tapering thickness of the a-$SiN_x$:H in this region yielded a nearly optimal antireflective coating at the excitation wavelength (see ESI, Fig. S9–S11†). These observations imply a low surface recombination velocity ($S \ll 70$ cm s$^{-1}$) as well as the longest minority-carrier diffusion length reported to date for VLS-grown Si wires ($L_n \gg 30$ μm, $\tau_n \gg 500$ ns). Because our observation of $L_n$ was limited by the ~30 μm axial length of the longest a-$SiN_x$:H-coated single-wire devices, the uniform SPCM profiles suggest not only that $L_n$ was many times this value, but also indicate an extremely low effective surface recombination velocity at the Al:p–Si interface. We attribute this behavior, observed under both a-$SiN_x$:H and BHF passivation, to the presence of a $p^+$ layer beneath the contact (*i.e.*, a back surface field) diffused from the degenerately doped growth wafer during growth and oxidation.

The above measurements reveal that, although the growth of the Si wires was catalyzed by Cu (one of the more soluble, mobile, and prevalent impurities in Si microelectronics fabrication),[30] it was nonetheless possible to synthesize long-diffusion-length material with well-passivated surfaces. These achievements enabled us to fabricate single-wire solar cell test structures that exhibited the highest open-circuit voltages ($V_{OC}$), fill factors (*FF*), and apparent photovoltaic efficiencies ($\eta$) reported to date for VLS-grown Si wire solar cells, as summarized in Table 1. To improve the absorption of incident sunlight, all devices were fabricated on reflective substrates consisting of Si wafers that had been coated with 100 nm of evaporated Ag (to provide high reflectivity) and ~300 nm of PECVD $SiN_x$ (to prevent shorting the contacts). Simulations suggest that using reflective Ag substrates enabled 17–22% greater $J_{SC}$ than would be possible using the $Si_3N_4$-coated Si substrates of prior studies[12] (see ESI†). Fig. 4 plots the current–density *vs.* voltage (*J–V*) behavior of the most-efficient device of each surface coating type.

Following the convention of prior single-wire solar cell studies,[10–12] current density was determined by normalizing the device current by the total non-shaded physical area of each wire (including both the axial and radial regions and the surface coating thickness). We note, however, that the wave nature of light and the photonic dimensions of micro- and nanowires enable them to interact with (and potentially absorb) more sunlight than predicted by their physical area, from a classical ray-optics perspective. This ill-defined absorption area prevents a true definition of photovoltaic efficiency for single-wire devices, and resulted in apparent EQE exceeding 100% at certain wavelengths for some of our devices (see ESI, Fig. S13†). Thus, it is understood that the apparent photovoltaic efficiency of single-wire solar cells does not necessarily represent that which could be achieved over macroscopic device areas, for example, by densely tiling the horizontal wires to occupy the optical plane. Nonetheless, for microwires of the diameter range studied herein (1.2–1.8 μm), numerical simulations suggest that minimal systematic error (<4% relative overstatement of $J_{SC}$) is introduced by normalizing the photovoltaic performance of our champion devices to their physical area (see ESI†).

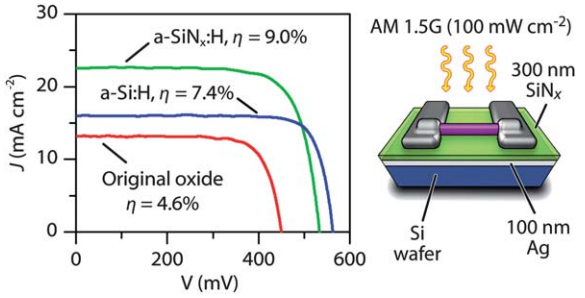


**Fig. 4** Photovoltaic *J–V* characteristics of the champion single-wire test structures of each surface passivation type (left) and a schematic diagram of the illumination configuration (right). The current density of each device was normalized to the total non-shaded wire area (determined by SEM) to determine apparent photovoltaic efficiency.

Comparing the PECVD coatings, we see that the long collection length and reduced reflectivity of the a-$SiN_x$:H-coated devices consistently yielded the highest short-circuit current densities (up to 26 mA cm$^{-2}$), and resulted in the device with the greatest apparent photovoltaic efficiency ($\eta = 9.0\%$). Interestingly, the a-Si:H-coated devices consistently produced the highest open-circuit voltages (up to 595 mV), despite having many times greater *S* within the axial region. This behavior indicates that, although the a-$SiN_x$:H provided the best passivation of the p-type (base) surfaces, the a-Si:H provided superior passivation of the n-type (emitter) surfaces or the Al:n-Si contacts, and that the latter recombination sources are more detrimental to the $V_{OC}$ of the Si microwire solar cells. It is well known that the wide

**Table 1** Measured properties of single-wire solar cell test structures, including the observed minority-carrier collection lengths ($L_{eff}$), inferred axial-region surface recombination velocities (*S*), and measured photovoltaic properties (AM 1.5G, 100 mW cm$^{-2}$) for each surface coating type. Upper values (bold) represent the champion cell of each group; lower values represent the measurement range within each group (*N* denotes number of samples)

| Wire coating | $L_{eff}$/μm | *S*/cm s$^{-1}$ | $\eta$ (%) | $V_{OC}$/mV | $J_{SC}$/mA cm$^{-2}$ | *FF* (%) |
|---|---|---|---|---|---|---|
| Original[a] ($N = 12$) | <0.5 | >4 × 10$^5$ | **4.6** | **451** | **13** | **77** |
| | | | 1.5–4.6 | 390–496 | 6.9–16 | 58–81 |
| a-Si:H ($N = 20$) | 5–10 | 450–600 | **7.4** | **564** | **16** | **81** |
| | | | 3.6–7.4 | 561–595 | 7.8–17 | 77–82 |
| a-$SiN_x$:H ($N = 13$) | ≫30 | ≪70 | **9.0** | **535** | **23** | **75** |
| | | | 4.8–9.0 | 462–543 | 17–26 | 56–78 |

[a] "Original" wires had a native oxide coating over the radial portion and a thermal oxide coating over the axial portion, as depicted in Fig. 3a.

band gap of a-Si:H provides effective passivation of metallic contacts to crystalline Si surfaces (forming a minority-carrier mirror).[31] Furthermore, studies have shown that a-$SiN_x$:H provides less-effective passivation on phosphorus-diffused (n-type) emitters than on mildly doped p-type Si surfaces.[26] These observations thus suggest that efficiency gains for Si microwire photovoltaics could result from improving the axial-region surface-passivation efficacy of the a-Si:H coating (noting that we observed $S < 20$ cm $s^{-1}$ for our planar control wafers), then coating this layer with an antireflective a-$SiN_x$:H film. A device combining the highest $V_{OC}$, *FF*, and $J_{SC}$ values reported herein would achieve apparent efficiencies in excess of 12%.

In seeking to further improve the efficiency of Si microwire photovoltaics, however, the performance of our horizontally oriented microwire devices may ultimately be limited by incomplete optical absorption, as evidenced by the low $J_{SC}$ and poor infrared spectral response (see ESI, Fig. S13†) of even our best test structures despite our use of back-reflecting substrates and antireflective coatings. The optimal thickness of planar crystalline Si solar cells is theoretically much thicker (~100 μm) even with ideal light trapping.[32] Thus, solar cells based on horizontally oriented crystalline Si microwires would likely benefit from the use of larger-diameter wires than studied herein, or advanced absorption enhancement techniques such as dielectric resonance engineering[33] or integrated optical micro-concentrators (*e.g.*, those demonstrated on Si microcells).[34]

Alternatively, recent optical absorption studies have shown that large-area solar cells made from mechanically flexible arrays of *vertically oriented*, polymer-embedded Si microwires, utilizing the light-trapping elements depicted in Fig. 5a, can absorb up to 85% of above-band gap sunlight, and thus offer a high photovoltaic performance potential for microwires of the dimensions studied herein.[9] This absorption study was performed on wire arrays of nearly identical dimensions as those produced here (Fig. 1e), and recently, such solar cells have demonstrated photovoltaic efficiencies approaching 8% over ~0.1 $mm^2$ areas.[5] Here, we present single-wire measurements and simulations to predict the efficiency potential of this three-dimensional photovoltaic microstructure.

Prior optical absorption measurements indicate that square-tiled vertical Si microwire arrays could produce up to $J_{SC} = 35.9$ mA $cm^{-2}$ under normal-incidence, one-sun (AM 1.5G) illumination (assuming that all absorbed photons result in charge-carrier collection). Considering the 7 × 7 μm unit cell of the wire array (Fig. 5b, left), this value corresponds to $I_{SC} = 17.6$ nA per wire. To emulate these optical excitation conditions, we measured the *I–V* behavior of the champion a-Si:H-coated single-wire test structure (oriented horizontally) under ~2.3 sun illumination intensity, which produced the desired $I_{SC}$ = 17.6 nA (Fig. 5b). If each wire within a vertical array exhibited this identical *I–V* behavior, the device would have an open-circuit voltage of 614 mV, a fill factor of 80%, and photovoltaic efficiency exceeding 17%.

Three-dimensional optoelectronic simulations were also performed to predict the behavior of the wire-array solar cell proposed in Fig. 5a, taking into account the experimentally observed wire dimensions, doping profiles, and recombination parameters presented herein, and also considering the optical effects of a 60 nm indium tin oxide (ITO) transparent top contact on the cell performance. Adapted from our prior modeling work,[20] these simulations combined full-field optical absorption simulations (Lumerical FDTD) with finite-element device-physics simulations (Synopsys Sentaurus Device) to simulate one unit cell of a periodic wire-array solar cell under one-sun normal-incidence illumination (see ESI† for simulation details). The results (Fig. 5b, blue) predict that, although the reflection and absorption losses of an ITO top contact produce a lower $J_{SC}$ (32.4 mA $cm^{-2}$), the reduced area of the electrical contacts to vertically oriented Si wires produces a higher $V_{OC}$ (649 mV), yielding similar overall efficiency ($\eta$ = 17.4%) as predicted by measurements on single-wire test structures. Although these projective measurements and simulations do not account for many challenges facing real wire-array solar cells (such as contact-grid shading, resistive losses, or variations in wire size or quality), the calculations are based on experimentally measured quantities, and use a physically meaningful device area for the definition of photovoltaic efficiency (rather than the ill-defined effective area of the single-wire devices). The results suggest the potential of VLS-grown Si wire-array solar cells to compete, on an efficiency basis, with commercial polycrystalline wafer-based Si technology.

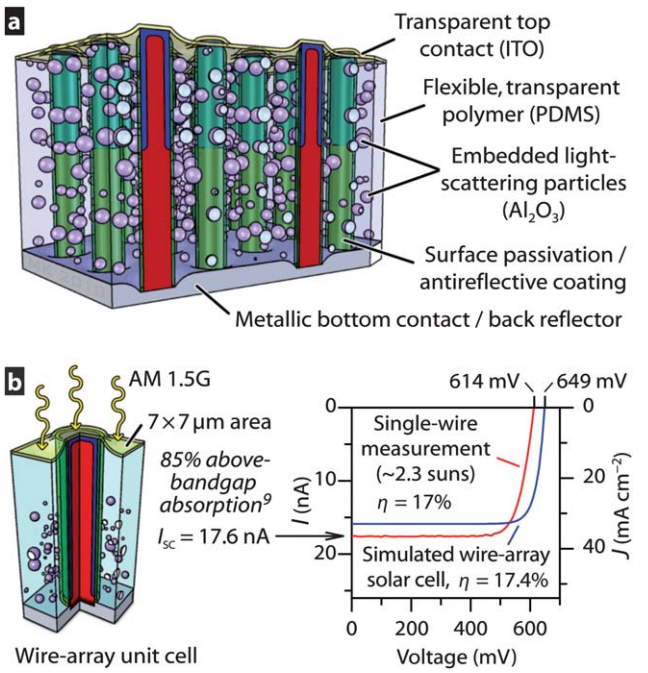


**Fig. 5** Projected Si wire-array solar cell performance. (a) Proposed large-area solar cell geometry consisting of vertically aligned Si wires embedded within a transparent polymer, employing light-scattering particles and a transparent top contact. (b) Predicted efficiency and *J–V* characteristics of the wire-array solar cell of configuration (a). Shown in red: the *I–V* behavior of a horizontal single-wire test structure (left axis) was measured under ~2.3 sun illumination to achieve $I_{SC}$ = 17.6 nA, the per-wire photocurrent corresponding to prior optical absorption measurements on vertical Si microwire arrays.[9] The *J–V* curve (right axis) has been normalized to the 49 $\mu m^2$ area of the wire-array unit cell. Shown in blue: an optoelectronic device-physics model[20] was employed to simulate the *J–V* behavior of the depicted wire-array unit cell based on measured values of $L_n$ = 30 μm and $S$ = 70 cm·$s^{-1}$.

The dramatic improvements in the bulk, surface, and junction properties of the Si microwire devices reported above have enabled us to overcome a fundamental challenge facing the development of efficient thin-film solar cells from VLS-grown Si wires: achieving high operating voltage. Despite the inherent contamination of VLS-grown Si by catalyst metal impurities, our best single-wire test structures exhibited reasonably high open-circuit voltages (~600 mV) and fill

 

factors (~80%). Furthermore, simulations indicate that even higher open-circuit voltages should be possible by improving the device structure. The surprising material quality of VLS-grown Si wires, combined with the advantageous optical and mechanical properties of wire arrays, offers a promising route for the development of efficient, thin-film crystalline Si solar cells.

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