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High-Performance Slow-Wave Transmission Lines With Optimized Slot-Type Floating Shields

Hsiu-Ying Cho, Tzu-Jin Yeh, Sally Liu, and Chung-Yu Wu, *Fellow, IEEE*

***Abstract*—A novel slow-wave transmission line with optimized slot-type floating shields in advanced CMOS technology is presented. Periodical slot-type floating shields are inserted beneath the transmission line to provide substrate shielding and to shorten the electromagnetic (EM) propagation wavelength. This is the first study that demonstrates how the wavelength, attenuation loss, and characteristic impedance can be adjusted by changing the strip length (SL), strip spacing (SS), and metal layer position of the slot-type floating shields. Wavelength shortening needs to be achieved with a tradeoff between slow-wave effect and attenuation loss. The slot-type floating shields with different SLs, SSs and metal layer positions are analyzed. It is concluded that minimum SL provides the most optimal result. A design guideline can be established to enable circuit designers to reach the most appropriate slot-type floating shields for optimal circuit performance. Transmission line test structures were fabricated by using 45-nm CMOS process technology. Both measurement and EM waves simulation were performed up to 50 GHz. Transmission lines are frequently used at a length of half- or quarter-wavelength. With a shortened wavelength, a saving in silicon area of more than 67% can be achieved by using optimized slot-type floating shields. Experimental results demonstrated a higher effective relative permittivity value, which is improved by a factor of more than 9, and a better quality factor, which is improved by a factor of more than 6, as compared to conventional transmission lines.**

***Index Terms*—Floating shields, grounded shields, slow wave, transmission lines.**

I. Introduction

IT IS KNOWN that conventional transmission lines suffer from their own unique type of loss as a result of structural limitations. Coplanar waveguide (CPW) transmission lines are often used in millimeter-wave integrated circuits (MMICs) [1] with an inherent disadvantage in having no shield between signal lines and the underlying substrate. Low-loss CPW structures on a silicon substrate have been designed and optimized by using either a thick dielectric layer [2] or a micromachining process [3]–[5]. However, the CPW structures mentioned above are not fully compatible with advanced CMOS processes. Microstrip (MS) line structures are composed of a signal line and a ground plane underneath such that there is no dependency on substrate properties due to the shielding by a ground plane [6].

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Several substrate shielding methods for passive devices, such as transmission lines, inductors, and transformers, have been developed to minimize the amount of lost radio-frequency (RF) energy that are coupled to the substrate. Substrate shielding can be either a patterned ground shield (PGS) [7]–[17] or a floating shield [18]. The PGS must be well designed; otherwise, they may not at all be able to improve the quality factor [7], [8]. According to Faraday's and Lenz's laws, an electric field is magnetically induced for every electrical-current-carrying segment, resulting in both substrate and conductor eddy-current loss [19]–[21]. The interactions and correlations of conductor eddy-current loss on slot-type floating shields [18] have not been investigated previously. The eddy-current loss plays a major role at high frequencies, and it is worth mentioning that the eddy-current loss in conductors is roughly proportional to the square of the frequency [21]. The majority of earlier research [9]–[12] covers frequencies less than 20 GHz at which there is not enough eddy-current loss on these PGS to significantly degrade the quality factor of devices. At frequency of 20 GHz or above, the quality factor of devices with PGS can be degraded further to be even lower than that of unshielded devices. As can be observed from the experimental results, the attenuation loss of PGS devices is much higher than that of devices with floating shields above 20 GHz. In practice, it is also difficult to implement an on-chip ground reference that does not suffer from some level of voltage variation due to the parasitic inductance and capacitance coupled with the neighboring interconnections of both circuits and packages. When an ac variation exists on the grounded shields, energy is again lost to the silicon, thereby degrading the shielding ability. However, floating shields do not suffer from voltage variations since no source is connected to the isolated floating shields.

In conventional transmission lines, the phase velocity V_p is controlled only by the dielectric material and can be expressed as

$$V_p = f \cdot \lambda = \frac{c_0}{\sqrt{\mu_r \cdot \epsilon_r}} \tag{1}$$

where c_0 is the velocity of light, μ_r is the effective relative permeability, and ϵ_r is the effective relative permittivity. Generally, a reduction in phase velocity results in a corresponding reduction in wavelength and an increase in the effective relative permittivity of dielectric material at a given operating frequency. Thus, the wavelength is not adjustable. However, a reduced wavelength in the transmission line can be achieved by adding periodical shields that decelerate the propagation electromagnetic (EM) waves in a guided medium. This is called the slow-wave phenomenon. The slow-wave theory in the microwave range has been investigated with most grounded slow-wave structures [22]–[31].

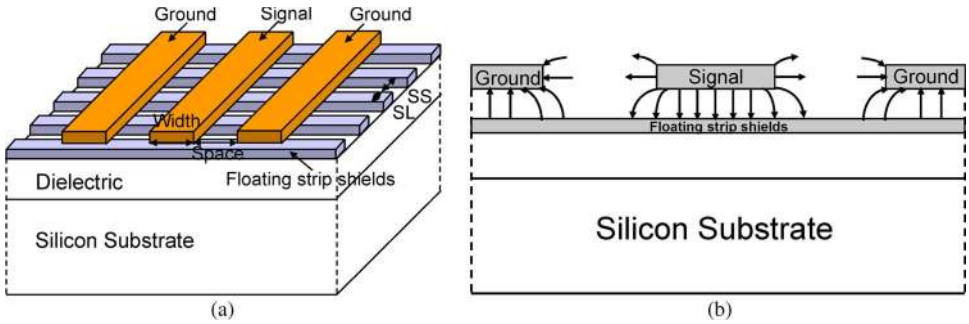

Fig. 1. Slow-wave CPW transmission line structure with slot-type floating shields. (a) Schematic view. (b) Electric field distribution from 3-D EM simulation.

In this paper, a slow-wave CPW transmission line, combining the advantages of both CPW transmission lines and MS lines, is proposed to create high-performance passive components for MMIC chips. Periodical slot-type floating shields are used to achieve a slow-wave phenomenon enabling a reduction in chip area while still maintaining high performance. Slot-type floating shields can also enhance the immunity of slow-wave CPW transmission lines from ac noise. The optimization of slot-type floating shields plays a key role in creating a high-performance slow-wave CPW. Investigations on floating metal coverage density and floating metal layer positions for substrate shielding and wavelength reduction, which has not yet been conducted before, are performed in this work. It is found from the experimental results that the currently prevalent concept that highest-density shields are the best choice [8] is simply not always true. Instead, the lower density coverage and the lower metal layer position of the slot-type floating shields exhibit a higher quality factor as frequencies increase. Moreover, the wavelength and attenuation loss can be adjusted by changing the strip length (SL), strip spacing (SS), and metal layer position of the slot-type floating shields while keeping the same area. As compared with conventional transmission lines, the proposed slow-wave CPW has a higher effective relative permittivity value up to 51 at 50 GHz, which is an improvement by a factor of more than 9, and a better quality factor of 17 at 33 GHz has been obtained, which is an improvement by a factor of more than 6. Moreover, a wavelength as short as 0.85 mm at 50 GHz has been obtained, which is a reduction by a factor of more than 3 and results in a saving in silicon area of more than 67%.

In Section II, the optimization of slot-type floating shields, including changing the SL, the SS, and the metal layer position of the slot-type floating shields, is proposed to create a high-performance slow-wave CPW. Section III contains the experimental results of the optimized slot-type floating shield design. The analysis and comparison on a floating and a grounded slow-wave CPW is also included. Finally, a conclusion is given in Section IV.

II. Optimization of Slot-Type Floating Shields in Transmission Lines

A slow-wave CPW transmission line structure with slot-type floating shields is shown in Fig. 1(a). The advantage of using slot-type floating shields is that slow-wave transmission lines have a lower electric field leakage to the substrate and a lower conductor eddy-current loss, particularly at high frequencies.

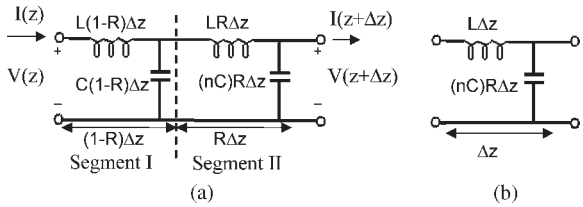

Fig. 2. Equivalent circuits for a slow-wave CPW transmission line. (a) Inductance and capacitance lumped-element equivalent circuit. (b) Cascaded equivalent circuit.

Fig. 1(b) shows the electric field distributions from a 3-D EM simulation of slot-type floating shields. The electric field starts from the signal line, couples to the floating shields, and finally terminates on the coplanar ground conductors. Therefore, the effective dielectric thickness of devices with floating shields is larger than that of devices with grounded shields. Thus, both capacitance and electric field intensity of devices with floating shields are smaller than those of devices with grounded shields. This leads to lower conductor eddy-current loss. Consequently, we propose to incorporate floating shields into transmission lines to replace the ground shields for better performance at high frequencies.

The performance of a transmission line can be characterized by attenuation loss per unit length α in (nepers per meter) and effective relative permittivity ϵ_r, which can be expressed as

$$\alpha = \text{real}(\gamma)$$
$$\epsilon_r = 9 \cdot 10^{16} \cdot \left(\frac{\beta}{\omega}\right)^2$$

respectively, where ω is the angular frequency, $\beta = 2\pi/\lambda$ is the phase constant, and λ is the propagation constant [32]. Generally, lower attenuation loss and higher effective relative permittivity are required to achieve a high-performance transmission line, and a compact size is desired.

If the length of the periodical structure is short compared to the wavelength, each segment of signal line can be modeled by an inductance and capacitance lumped-element equivalent circuit, as shown in Fig. 2(a), where L and C are the series inductance and the shunt capacitance per unit length, respectively. The density R of the slot-type floating shields is defined as

$$R = \frac{\text{SL}}{\text{SL} + \text{SS}}. \tag{2}$$

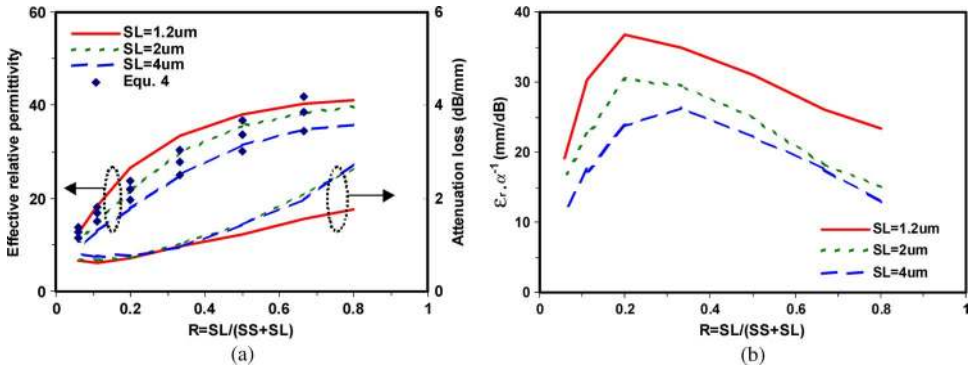

Fig. 3. Simulated slow-wave CPW transmission line performance versus parameter R with different SL values at a signal frequency of 50 GHz. (a) Effective relative permittivity and attenuation loss. (b) Optimization index value of $\epsilon_r \cdot \alpha^{-1}$.

Segment I, on top of the open slot, can be modeled by a series inductance $L(1-R)(\Delta z)$ and a shunt capacitance $C(1-R)(\Delta z)$. While Segment II, on top of the shield metal line, can be modeled by a series inductance $L(R\Delta z)$ and an increased shunt capacitance $(nC)(R\Delta z)$, where n represents the increased ratio in capacitance as a result of coupling to the slot-type shields, and Δz denotes the differential unit length. When two segments are cascaded together, the combined equivalent circuit can be condensed as shown in Fig. 2(b). Please note that the equivalent circuit in Fig. 2(b) is valid only when n is $\gg 1$. Consequently, the phase velocity V_p with the slow-wave effect can be expressed as

$$V_p = \frac{c_0}{\sqrt{\mu_r \cdot \epsilon_r}} = \frac{1}{\sqrt{LC^*(nR)}}. \tag{3}$$

The slow-wave phenomenon can be explained in (3), which shows that the phase velocity is decelerated by a factor of $\sqrt{nR}$.

The optimization of slot-type floating shields to reduce the attenuation loss and also increase the slow-wave features is performed. Both wavelength and attenuation loss can be adjusted by changing both the SL and SS of the slot-type floating shields while keeping the same area. Optimization analyses on SL and SS are conducted by analyzing the EM simulation results of structures with a variety of SL and SS while keeping the same area (using Ansoft HFSS). An empirical equation is derived to relate the effective relative permittivity ϵ_r to R and SL as follows:

$$\epsilon_r = 52 \cdot (R^{0.47} \cdot \mathrm{SL}^{-0.167}) + 0582. \tag{4}$$

The calculated values approximate well the simulation results at 50 GHz, as illustrated in Fig. 3(a). It exemplifies the slow-wave equation [see (3)] that predicts a higher density of slot-type floating shields, resulting in a higher effective relative permittivity. Furthermore, Fig. 3(a) indicates a higher effective relative permittivity at smaller SL. The parameter SL has been explicitly introduced in (4). When the performance of the attenuation loss is taken into consideration, it becomes even more obvious that a minimized SL is the best choice for slot-type floating shield design, as illustrated in Fig. 3(a). Though the high-density shields minimize the exposure of the signal line to the substrate, field leakage to the substrate can be reduced. However, the consequence of using high-density shields is that the conductor eddy-current loss is high, and this, in turn, increases the attenuation loss. In contrast, the opposite is true when the density of slot-type floating shields is low. There is a tradeoff between the slow-wave effect and the attenuation loss in slow-wave CPW transmission lines; namely, that while the wavelength is reduced to facilitate implementation of smaller devices, greater attenuation loss may be induced by the eddy-current loss on the slot-type floating shields. The optimization index of the slot-type floating shields is defined as $\epsilon_r \cdot \alpha^{-1}$ (in millimeters per decibel), and Fig. 3(b) shows the optimized performance is achieved when SL $= 1.2$ μm and SS $= 4.8$ μm. If the specification requirement for the attenuation loss is first determined, then the density of the slot-type floating shields can be calculated. Consequently, the effective relative permittivity can be predicated from the minimized SL and the density of the slot-type floating shields.

III. Experimental Results

Three types of transmission lines were fabricated by using 45-nm CMOS technology as listed in Table I, including the following: 1) a CPW transmission line without shields (CPW); 2) five slow-wave CPW transmission lines with slot-type floating shields (FSCPW1, FSCPW2, FSCPW3, FSCPW4, and FSCPW5); and 3) a slow-wave CPW transmission line with slot-type grounded shields (GSCPW1). A slow-wave CPW transmission line with slot-type floating shields was designed with periodically slot-type floating shields located beneath the CPW structure and the slot-type floating shields are oriented transversely to the CPW structure. For all transmission lines in Table I, the signal line is formed on the tenth (M10) metal layer and the slot-type shields are created on either the ninth (M9) or eighth (M8) metal layer. The CPW part of the structure has a signal/ground line width of 30 μm/10 μm, with a 30 μm space between signal and ground lines. In the slot-type floating shields, the SL is at the minimum length allowed by design rules to achieve high performance with minimized eddy-current loss. The minimum length on M8 is 0.07 μm and on M9 is 0.4 μm for the 45-nm CMOS technology. The slot-type floating shields are designed with the following dimension splits: 1) the SL on M8 is 0.07 μm, and the accompanying SS is 0.07 μm, and 2) the SL on M9 and M8 is 0.4 μm, and the accompanying SS varies between 0.4, 1.6, and 3.2 μm. For the grounded

TABLE I
TRANSMISSION LINE STRUCTURES

Name	Transmission Line Type	Metal Shield Layer	Strip Width (SL)	Strip Space (SS)	Shield Type
CPW	CPW	No strip shields			
FSCPW1	Floating slow-wave CPW	M9	0.4 um	0.4 um	floating
FSCPW2	Floating slow-wave CPW	M9	0.4 um	1.6 um	floating
FSCPW3	Floating slow-wave CPW	M9	0.4 um	3.2 um	floating
FSCPW4	Floating slow-wave CPW	M8	0.4 um	0.4 um	floating
FSCPW5	Floating slow-wave CPW	M8	0.07 um	0.07 um	floating
GSCPW1	Grounded slow-wave CPW	M8	0.07 um	0.07 um	grounded

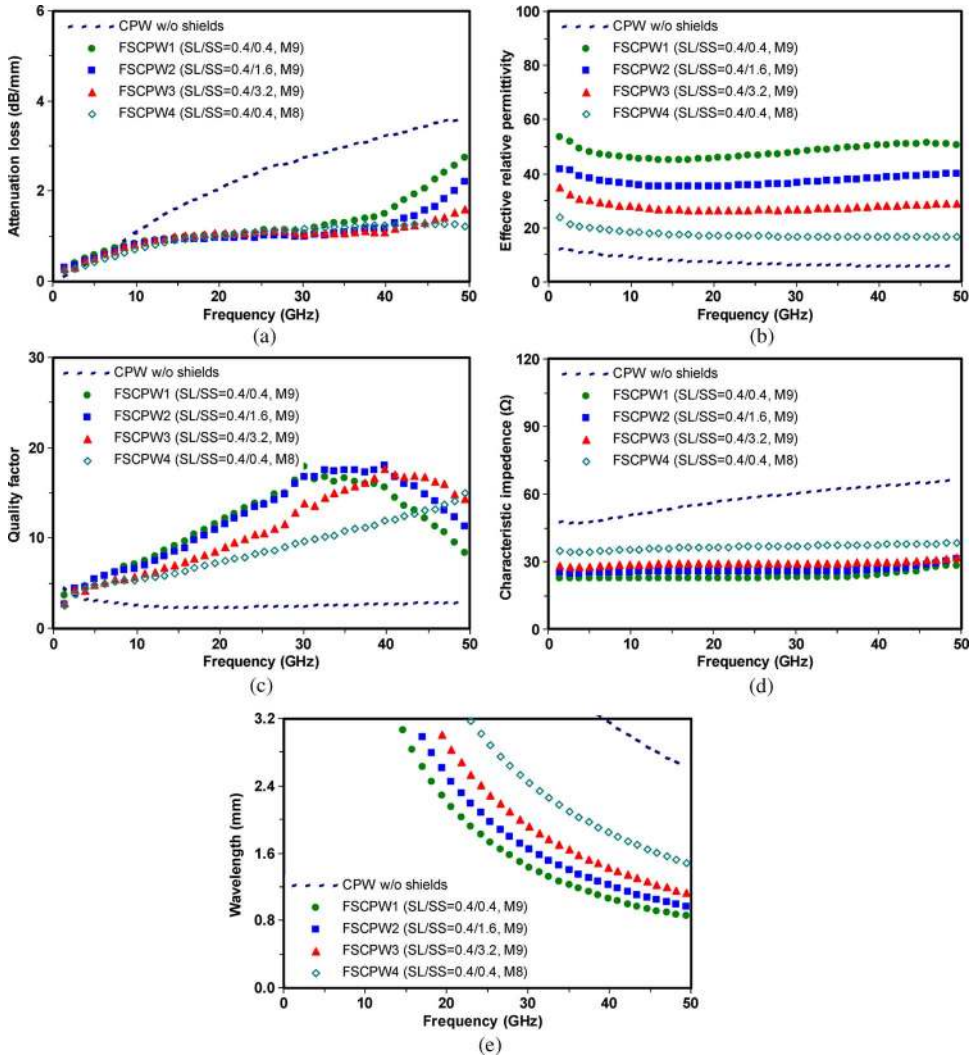

Fig. 4. Comparison of the measured transmission line performance for different floating shields. (a) Attenuation loss. (b) Effective relative permittivity. (c) Quality factor. (d) Characteristic impedance. (e) Wavelength.

slow-wave CPW transmission line, it is designed with the similar structure as that of the slow-wave CPW transmission line with floating shields as described above, but with the slot-type shields connected to the ground. This grounded slow-wave CPW is included for the purpose of comparison. Similarly, a CPW with the same signal/ground line structure but without shields is also included for comparison.

The backend metal scheme is a dual-damascene copper process with dielectric SiO_2 material for insulator layers that has an effective relative dielectric constant of around 5.4. All test structures have the same length of 400 μm and a width of 120 μm to ensure a fair comparison among different designs. The S-parameters of the transmission line test structures were measured up to 50 GHz using an Agilent 8510C network analyzer.

Fig. 4(a) shows that the attenuation loss of a CPW with slot-type floating shields is lower than the CPW without shields. It also shows that at frequencies above 50 GHz, slot-type floating shields on M8 is needed as it has the least amount of eddy-current loss on the floating shields. Among CPW with slot-type floating shields, in the 30–50 GHz frequency range, the attenuation loss of an SL of 0.4 μm and an SS of 0.4 μm on

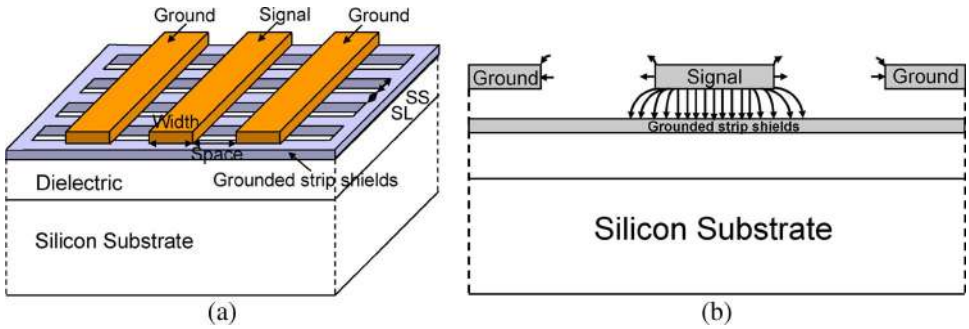

Fig. 5. Slow-wave CPW transmission line structure with slot-type grounded shields. (a) Schematic view. (b) Electric field distribution from 3-D EM simulation.

M8 is smaller than that on M9 because the dielectric thickness between the signal line on M10 and the floating shields on M8 is 3.2 μm, which is thicker than the dielectric thickness between the signal line on M10 and the floating shields on M9 (0.74 μm). By now, we can conclude that the smaller the SL, the wider the SS, and the greater the thickness between the signal line and the floating shields, the lower the attenuation loss will be induced.

Fig. 4(b) compares the effective relative permittivity constants of different CPW designs, with and without shields that are floating. In slow-wave CPW transmission lines with slot-type floating shields, a reduction in wavelength results in a corresponding increase in both the phase constant and the effective relative permittivity, pursuant to the relationship $\beta = 2\pi/\lambda$ and $\epsilon_r = 52 \cdot (R^{0.47} \cdot \mathrm{SL}^{-0.167}) + 0.582$. The effective relative permittivity increases to 51 at 50 GHz, for the CPW with shields on M9, SL $= 0.4$ μm and SS $= 0.4$ μm. This is an improvement by a factor of more than 9 compared to a conventional CPW transmission line. As expected, the wider the SS and the thicker the dielectric thickness between the signal line and the floating shields, the lower the effective relative permittivity will be obtained. Conventional passive devices in RF circuit design do not gain as much benefit from CMOS scaling as active devices. Passive devices play the role of a bottleneck in area reduction and performance improvement. Since the SL and the SS can be adjusted along technology scaling, a scaled slow-wave CPW can continue to offer lower attenuation loss and higher effective relative permittivity—a significant advantage for future technology scaling—which is a great breakthrough for RF circuit design.

An optimized design requires a good quality factor $Q = \beta/2\alpha$, where β is the phase constant, and α is the attenuation loss. Therefore, the quality factor should be used to judge an overall tradeoff between attenuation loss and effective relative permittivity. Guidelines for designing a transmission line with a high quality factor are illustrated in Fig. 4(c). The crossover of the quality factor is around 30 GHz, so the appropriate choice for designs operating at frequencies below 30 GHz is to create floating shields on M9 with an SL of 0.4 μm and an SS of 0.4 μm. At frequencies in the range of 30–50 GHz, floating shields on M9 with an SL of 0.4 μm and a variety of SS values is preferred. As a result, a quality factor of 18 can be achieved at 40 GHz, which is more than six times that of a conventional CPW transmission line, whose value is around 2.8. At significantly higher frequencies above 50 GHz, floating shields on M8 are strongly recommended. The wider the SS, the lower the attenuation loss will be obtained, but the corresponding effective relative permittivity will also be lower. As discussed above and as demonstrated in the experiments, the designers must weigh among SL and SS dimensions, as well as metal layer positions, to design a proper slow-wave CPW with slot-type floating shields with a good quality factor to achieve a functional circuit at the operating frequency.

Fig. 4(d) shows that the characteristic impedance can be tuned by changing the SL, the SS, and the metal layer position of the slot-type floating shields. A low characteristic impedance can be achieved by increasing the slot-type floating shield density or higher metal layer position. Characteristic impedance tuning by changing the metal density and metal layer position in the slot-type floating shields is also a new design approach.

Furthermore, the wavelength of a transmission line indicates if the transmission line design is compact in size. The wavelengths of transmission lines with a variety of slot-type floating shield design are compared in Fig. 4(e), which indicates that the best choice is FSCPW1 with floating shields on M9, SL $= 0.4$ μm and SS $= 0.4$ μm. The wavelength of FSCPW1 is reduced to 0.85 mm, i.e., by a factor of more than 3 as compared to a conventional CPW transmission line whose wavelength is 2.63 mm. A saving in silicon area of more than 67% can be achieved for FSCPW1, which demonstrates that this approach could have an extremely high potential for MMIC applications.

A slow-wave CPW transmission line with slot-type grounded shields is shown in Fig. 5(a). The slot-type shields are connected to ground by two parallel conductors added at the two ends of the slot-type shields. When the shields are grounded, the electric field starts from the signal line and terminates directly on the grounded shields, as illustrated in Fig. 5(b). In Fig. 6(a), the measured capacitance of the devices with grounded shields is higher than that of the devices with floating shields, which implies that the effective dielectric thickness of the devices with grounded shields is smaller than that of the devices with floating shields. Consequently, the electric field intensity of the devices with grounded shields is larger than that of the devices with floating shields. Fig. 6(b) indicates that the devices with grounded shields suffer an extremely rapid increase in attenuation loss when the frequency increases above 20 GHz. This is due to the eddy-current loss induced by increased voltage variation at extreme high frequency. As the signal frequencies increase, the number of voltage variations between the positive and the negative potential in unit time increases, resulting in an

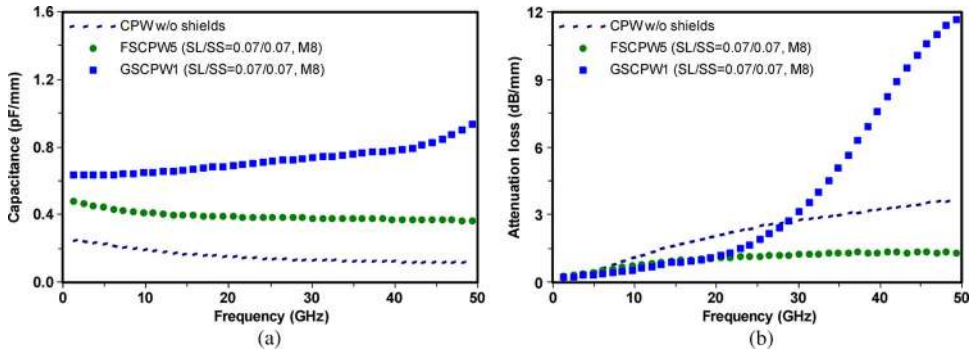

Fig. 6. Comparison of the measured transmission line performance for floating shields and grounded shields. (a) Capacitance. (b) Attenuation loss.

increase in eddy-current loss on the grounded shields, and the eddy-current loss in the conductors is proportional to the square of the frequency. Although the presence of the grounded shields increases the slow-wave feature as compared to floating shields, it is revealed that for frequencies above 20 GHz, the attenuation loss of a slow-wave CPW transmission line incorporating grounded shields is much higher as compared to that of a slow-wave CPW transmission line with floating shields. From the above analysis, it can be seen that grounded shields are a good choice at frequencies below 20 GHz, whereas floating shields are a better choice for frequencies above 20 GHz.

IV. Conclusion

High-performance slow-wave transmission lines with optimized slot-type floating shields have been analyzed. It has been shown that the wavelength, attenuation loss, and characteristic impedance can be adjusted by changing the SL, SS, and metal layer position of the slot-type floating shields while keeping the same area. An empirical equation that can predict a rough value for the effective relative permittivity has been presented. An optimization index of the floating slow-wave CPW transmission lines has been developed to enable circuit designers to expediently determine the most appropriate slot-type floating shields to meet design specifications. The designers must weigh among SL and SS dimensions, as well as metal layer positions, to design a proper slow-wave CPW with slot-type floating shields with a good quality factor to achieve a functional circuit at the operating frequency. The proposed floating slow-wave CPW transmission line has a higher effective relative permittivity value up to 51 at 50 GHz and a better quality factor of 17 at 33 GHz as compared to conventional CPW transmission lines. Moreover, a wavelength as short as 0.85 mm at 50 GHz has been obtained, which results in a saving in silicon area of more than 67%. It has also been proved that grounded shields are a good choice for frequencies below 20 GHz, whereas floating shields are a better choice for frequencies above 20 GHz.

References

[1] R. L. Peterson and R. F. Drayton, "A CPW T-resonator technique for electrical characterization of microwave substrates," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 3, pp. 90–92, Mar. 2002.

[2] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "A patterned dielectric support process for high performance passive fabrication," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 82–84, Feb. 2008.

[3] H. T. Kim, S. H. Jung, J. H. Park, C. W. Baek, Y. K. Kim, and Y. G. Kwon, "A new micromachined overlay CPW structure with low attenuation over wide impedance ranges and its application to low-pass filters," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 9, pp. 1634–1639, Sep. 2001.

[4] T. M. Weller, L. P. B. Katehi, and G. M. Rebeiz, "High performance microshield line components," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 3, pp. 534–543, Mar. 1995.

[5] L. L. W. Chow, Z. Wang, B. D. Jensen, K. Saitou, J. L. Volakis, and K. Kurabayashi, "Skin-effect self-heating in air-suspended RF MEMS transmission-line structures," *J. Microelectromech. Syst.*, vol. 15, no. 6, pp. 1622–1631, Dec. 2006.

[6] W. H. Haydl, "Conductive substrate losses in coplanar and microstrip transmission lines," in *Proc. IEEE Eur. Microw. Conf.*, Oct. 1997, vol. 1, pp. 532–537.

[7] O. El-Gharniti, E. Kerherve, and J.-B. Begueret, "Characterization of Si-based monolithic transformers with patterned ground shield," in *Proc. IEEE RFIC Symp.*, Jun. 11–13, 2006. 4 pp.

[8] X. Sun, G. Carchon, Y. Kita, K. Chiba, T. Tani, and W. De Raedt, "Experimental analysis of above-IC inductor performance with different patterned ground shield configurations and dummy metals," in *Proc. IEEE 36th Eur. Microw. Conf.*, Sep. 2006, pp. 40–43.

[9] R. Svitek, C. A. S. Klein, M. Clifford, S. Raman, L. H. Chang, K. M. Chen, and W. L. Chen, "Development of scalable models for patterned-ground-shield inductors in SiGe BiCMOS technology," in *Proc. Top. Meeting Silicon Monolithic Integr. Circuits RF Syst. Dig. Papers*, Sep. 8–10, 2004, pp. 211–214.

[10] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[11] R. D. Lutz, V. K. Tripathi, and A. Weisshaar, "Enhanced transmission characteristics of on-chip interconnects with orthogonal gridded shield," *IEEE Trans. Adv. Packag.*, vol. 24, no. 3, pp. 288–293, Aug. 2001.

[12] R. Lowther and S. G. Lee, "On-chip interconnect lines with patterned ground shields," *IEEE Microw. Guided Wave Lett.*, vol. 10, no. 2, pp. 49–51, Feb. 2000.

[13] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "Parameter characterization of silicon-based patterned shield and patterned ground shield coplanar waveguides," in *Proc. GSMM*, Apr. 21–24, 2008, pp. 142–145.

[14] L. F. Tiemeijer, R. J. Havens, N. Pavlovic, and D. M. W. Leenaerts, "Record Q symmetrical inductors for 10-GHz LC-VCOs in 0.18μm gate-length CMOS," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 713–715, Dec. 2002.

[15] Y. S. Lin, C. Z. Chen, H. B. Liang, and C. C. Chen, "High-performance on-chip transformers with partial polysilicon patterned ground shields (PGS)," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 157–160, Jan. 2007.

[16] Y. S. Lin, C. C. Chen, H. B. Liang, P. K. Tsai, C. Z. Chen, J. F. Chang, H. B. Liang, T. Wang, and S. S. Lu, "A high-performance micromachined RF monolithic transformer with optimized pattern ground shields (OPGS) for UWB RFIC applications," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 609–613, Mar. 2007.

[17] J. Shi, Z. Xiong, J. Brinkhoff, A. Issaoun, and F. Lin, "Resistive coupling efficiency criterion for evaluating substrate shielding structures of transformers," *IEEE Trans. Electron Devices*, vol. 29, no. 1, pp. 114–117, Jan. 2008.

[18] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "Shielded passive devices for silicon-based monolithic microwave and

millimeter-wave integrated circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, May 2006.
[19] C. B. Sia, B. H. Ong, K. W. Chan, K. S. Yeo, J. G. Ma, and M. A. Do, "Physical layout design optimization of integrated spiral inductors for silicon-based RFIC applications," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2559–2567, Dec. 2005.
[20] J. C. Guo and T. Y. Tan, "A broadband and scalable on-chip inductor model appropriate for operation modes of varying substrate resistivities," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 3018–3029, Nov. 2007.
[21] K. Y. Tong and C. Tsui, "A physical analytical model of multilayer on-chip inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1143–1149, Oct. 2005.
[22] I. C. H. Lai and M. Fujishima, "High-Q slow-wave transmission line for chip area reduction on advanced CMOS processes," in *Proc. IEEE ICMTS*, Mar. 19–22, 2007, pp. 192–195.
[23] Z. Lei, "Guided-wave characteristics of periodic coplanar waveguides with inductive loading—Unit-length transmission parameters," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 10, pp. 2133–2138, Oct. 2003.
[24] T. S. D. Cheung, J. R. Long, K. Vaed, R. Volant, A. Chinthakindi, C. M. Schnabel, J. Florkey, and K. Stein, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *Proc. ISSC Dig. Tech. Papers*, Feb. 2003, vol. 46, pp. 396–397.
[25] A. Komijani, A. Natarajan, and A. Hajimiri, "A 24-GHz, +14.5-dBm fully integrated power amplifier in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1091–1098, Sep. 2005.
[26] I. C. H. Lai, Y. Kambayashi, and M. Fujishima, "60-GHz CMOS down-conversion mixer with slow-wave matching transmission lines," in *Proc. IEEE ASSCC*, Nov. 2006, pp. 195–198.
[27] W. Kim and M. Swaminathan, "Characterization of co-planar silicon transmission lines with and without slow-wave effect," *IEEE Trans. Adv. Packag.*, vol. 30, no. 3, pp. 526–532, Aug. 2007.
[28] M. H. Cho, G. W. Huang, K. M. Chen, H. C. Tseng, and T. L. Hsu, "Slow-wave characteristics of interconnects on silicon substrates," in *Proc. Int. Semicond. Device Res. Symp.*, Dec. 2003, pp. 188–189.
[29] G. Wang, W. Woods, H. Ding, and E. Mina, "Novel low-cost on-chip CPW slow-wave structure for compact RF components and mm-wave applications," in *Proc. 58th ECTC*, May 27–30, 2008, pp. 186–190.
[30] D. B. Lin, "Signal integrity of bent differential transmission lines," *Electron. Lett.*, vol. 40, no. 19, pp. 1191–1192, Sep. 16, 2004.
[31] T. K. Ghosh, R. G. Carter, A. J. Challis, K. Rushbrook, and D. Bowler, "Optimization of coaxial couplers," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1753–1759, Jul. 2007.
[32] D. M. Pozar, *Microwave Engineering*, 2nd ed. Hoboken, NJ: Wiley, 1998, pp. 58–59. 308.

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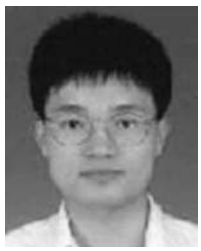

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