High-performance transparent inorganic–organic hybrid thin-film n-type transistors

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High-performance thin-film transistors (TFTs) that can be fabricated at low temperature and are mechanically flexible, optically transparent and compatible with diverse substrate materials are of great current interest. To function at low biases to minimize power consumption, such devices must also contain a high-mobility semiconductor and/or a high-capacitance gate dielectric. Here we report transparent inorganic–organic hybrid n-type TFTs fabricated at room temperature by combining In_2O_3 thin films grown by ion-assisted deposition, with nanoscale organic dielectrics self-assembled in a solution-phase process. Such TFTs combine the advantages of a high-mobility transparent inorganic semiconductor with an ultrathin high-capacitance/low-leakage organic gate dielectric. The resulting, completely transparent TFTs exhibit excellent operating characteristics near 1.0 V with large field-effect mobilities of $>120\,cm^2\,V^{-1}\,s^{-1}$, drain–source current on/off modulation ratio (I_{on}/I_{off}) $\sim 10^5$, near-zero threshold voltages and sub-threshold gate voltage swings of 90 mV per decade. The results suggest new strategies for achieving 'invisible' optoelectronics.

Thin-film transistors (TFTs) pervade our daily lives as indispensable elements in a myriad of electronic/photonic products, such as computers, cell phones, displays, household appliances and sensors[1]. Furthermore, the future demand for next-generation mobile computing, communication and identification devices is expected to increase markedly. For diverse multiple functionalities, the electronics of ideal mobile devices must achieve light weight, low power consumption, low operating voltages (powered by household batteries) and compatibility with diverse substrates[2–4]. Additional desirable features include optical transparency ('invisible electronics'), mechanical ruggedness, environmental stability and inexpensive room-temperature/large-area fabrication. TFTs meeting all the aforementioned requirements have proved elusive and will doubtless require unconventional materials and processing strategies. Conventional inorganic TFTs based on silicon and compound semiconductors have attractions such as high carrier mobilities, but also limitations, which include marginal mechanical flexibility and/or mandatory high-temperature processing (frequently $>400\,°C$ for II/VI and III/V compound semiconductors[5–9] and $>250\,°C$ for Si TFTs[10,11]). Although amorphous silicon TFTs have been fabricated on plastic at temperatures as low as 75–150 °C, reported carrier mobilities are modest (~ 0.03–$1\,cm^2\,V^{-1}\,s^{-1}$ on inorganic insulators) and the material is optically opaque[12–16]. Organic TFTs are promising and benefit from tailorable molecular functionality, low-temperature processability and compatibility with plastics[2,17–22]. Nevertheless, the low mobilities and modest environmental stabilities significantly constrain their applicability. For all of these reasons, unconventional 'hybrid' approaches combining the favourable characteristics of both inorganic and organic materials deposited at room temperature would be of great interest. Here we report fully transparent inorganic–organic hybrid TFTs with excellent performance, fabricated at room temperature using the highly unconventional combination of In_2O_3 semiconducting thin films, high-k nanoscopic organic self-assembled dielectrics and a precision, scalable growth technique, ion-assisted deposition (IAD).

The two essential TFT materials components are the semiconductor and the gate dielectric, with the field-effect mobility (μ_{FE}), drain–source current on/off modulation ratio (I_{on}/I_{off}),

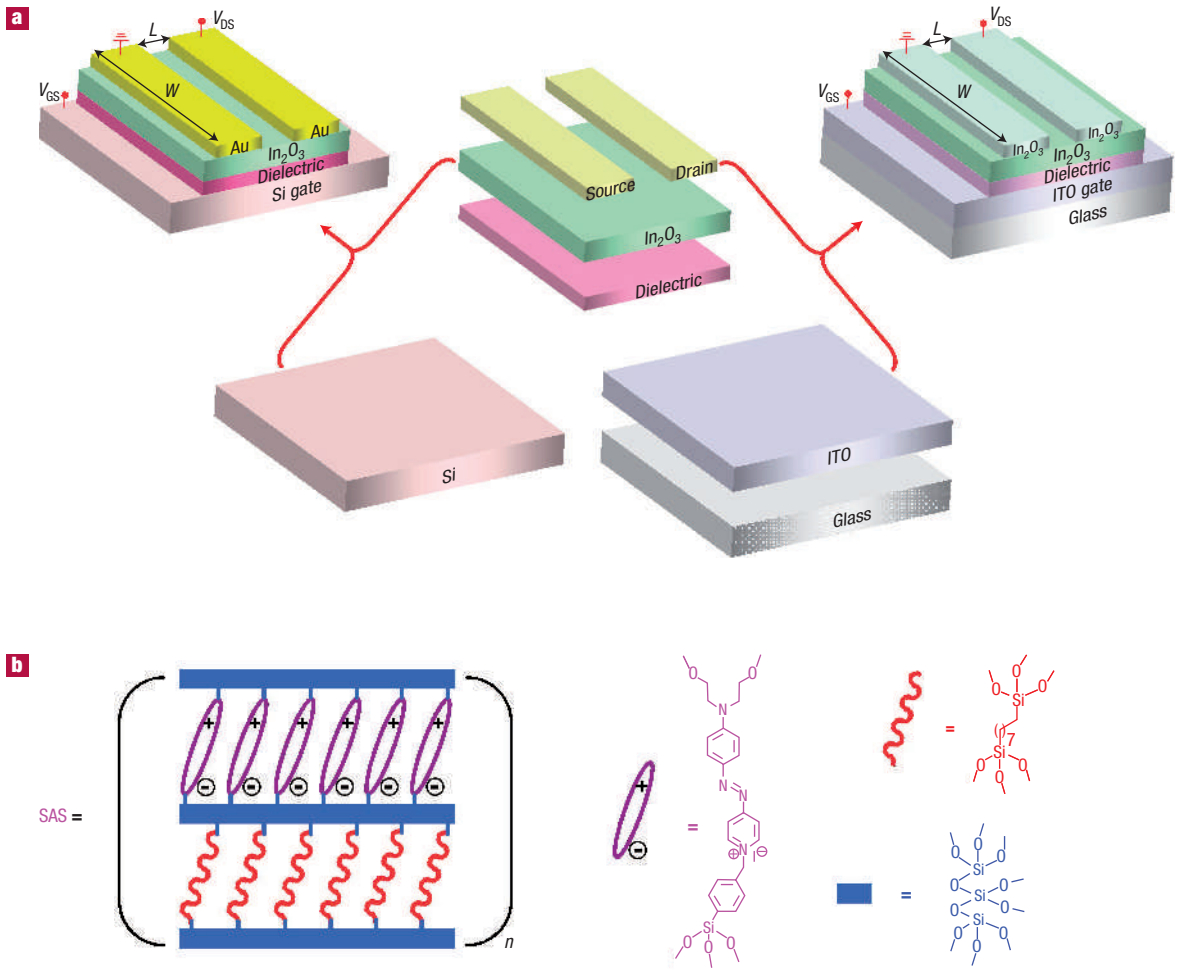

Figure 1 Inorganic-only and inorganic–organic hybrid TFTs fabricated using In_2O_3 thin films as the n-channel semiconductor; *L* (channel length) = 50/100 μm, *W* (channel width) = 5 mm. a, TFTs on doped Si gate substrates (left): the dielectrics are 300 nm thermally grown SiO_2, a 16.5 nm self-assembled SAS dielectric or a 20 nm CPB dielectric, and drain/source electrodes are Au thin films; fully transparent TFTs on glass/ITO substrates (right): the dielectric is a 16.5 nm self-assembled SAS dielectric, and drain/source electrodes are high-conductivity In_2O_3 thin films. **b**, Molecular structure of the nanoscopic SAS dielectric and its constituents.

threshold voltage (V_T) and sub-threshold gate voltage swing (S) being key performance metrics. High mobility values provide useful device currents, rapidly charged/discharged capacitive loads and high operating speeds, and thus enable numerous applications. I_{on} and I_{off} describe the gate-controlled drain–source current (I_{DS}) flow, and I_{DS} in the saturation regime is given by equation (1) according to the conventional metal–oxide–semiconductor field-effect transistor model[1], where W and L are the channel width and length, respectively, V_G is the gate voltage and is usually referenced to the source electrode, V_T is the threshold voltage and C_i is the areal dielectric capacitance. The threshold voltage V_T is defined as the V_G at which the device switches from the off state to the on state and vice versa. Ideally, V_T should be minimal (0.0 V) and is critical to minimizing power consumption.

$$I_{DS} = \frac{W C_i \mu_{FE}}{2L}(V_G - V_T)^2. \qquad (1)$$

Note that for fixed geometry, the required operating bias to achieve a given I_{DS} can be lowered by increasing either the semiconductor μ_{FE} or the gate dielectric C_i. To simultaneously achieve large μ_{FE} and large C_i, suitable semiconductor and dielectric materials are required, and compatibility between them must be established. Although metal oxides are potentially attractive for transparent, flexible TFTs, so far metal-oxide-based TFTs have typically required high temperatures for either semiconductor growth or post-annealing (usually >500 °C) to optimize crystallinity and μ_{FE} (refs 23–28). Such high temperatures are undesirable, and so far the performance of metal oxide TFTs fabricated near room temperature has been modest—low mobilities, low I_{on}/I_{off} ratios, unacceptably large operating voltages and/or using growth techniques incompatible with practical large-area/scale depositions[3,29].

In_2O_3 is a wide-bandgap (3.6–3.75 eV) n-type semiconductor[30,31], with appreciable single-crystal mobility (160 $cm^2 V^{-1} s^{-1}$) (ref. 32) and high film transparency in the visible region (>90%) (ref. 33); however, these attractive characteristics have not been exploited in TFTs, nor is it *a priori* obvious that room-temperature film growth and proper carrier densities for useful I_{on}/I_{off} ratios are achievable. Regarding potential gate dielectrics, nanoscopic organic dielectrics—self-assembled superlattice (SAS)[34] and spin-coatable cross-linked polymer blend (CPB)[35] dielectrics—have proved to be remarkably effective in organic TFTs and show

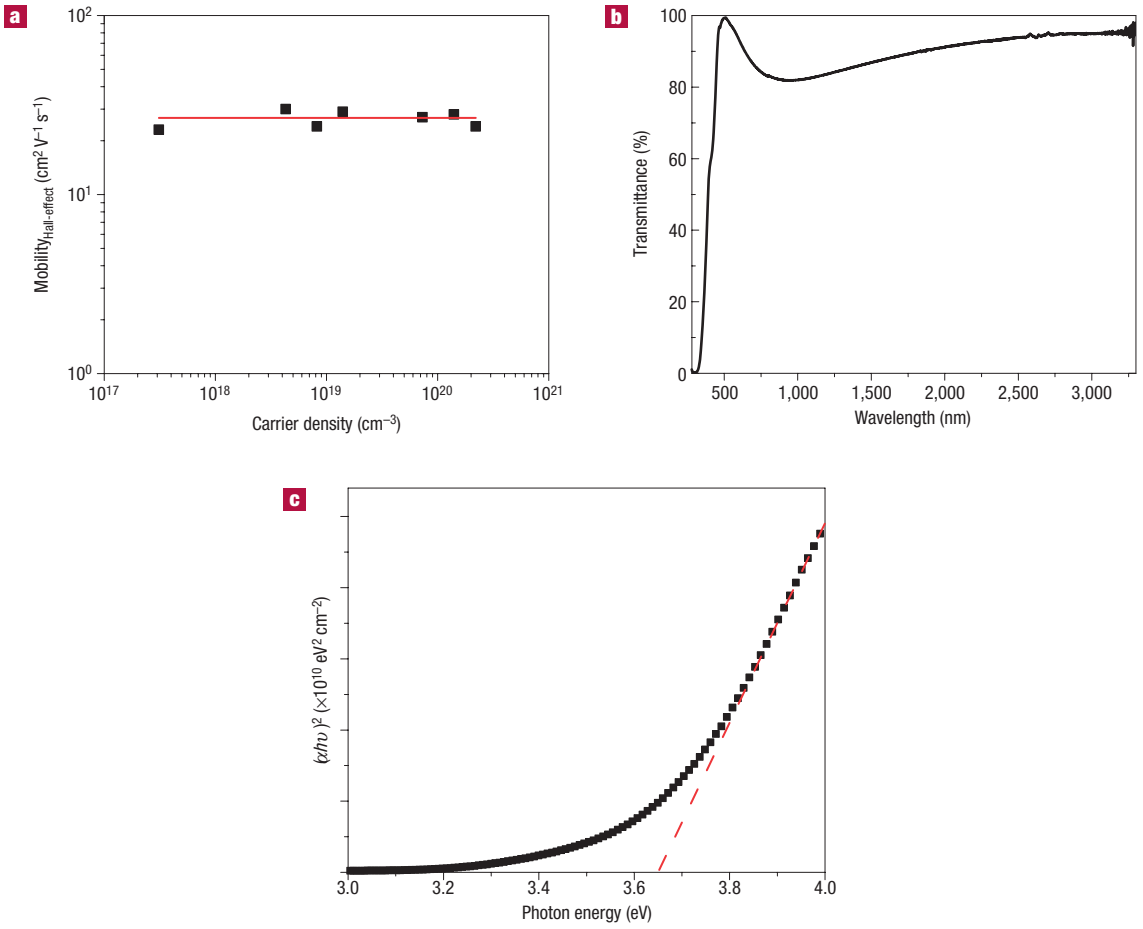

Figure 2 Electrical and optical properties of 120 nm as-deposited In_2O_3 thin films on Corning 1737F glass substrates. a, Hall-effect mobility versus carrier density. **b**, Optical transmittance spectrum. **c**, Derivation of the optical bandgap.

good optical transparency. Here we report that the combination of semiconducting In_2O_3 and nanoscopic organic dielectrics, both deposited at room temperature using readily scalable growth processes, achieves completely transparent and durable inorganic–organic hybrid TFTs on glass substrates with excellent operating characteristics.

The structures and components of the hybrid TFTs are illustrated in Fig. 1 and in Supplementary Information, Fig. S1, with all components deposited at room temperature. For comparison, In_2O_3 TFTs were also fabricated in combination with a conventional 300 nm SiO_2 dielectric layer. The semiconducting In_2O_3 thin films, thin nanoscopic dielectrics, TFT device structures and electrical properties were characterized as described below. These hybrid TFTs have exceptionally large field-effect mobilities of 140 cm^2 V^{-1} s^{-1} at low operating voltages ($\sim$1 V) with good I_{on}/I_{off} ratios. Furthermore, this fabrication approach is applicable to glass substrates to realize 'invisible' TFTs.

In_2O_3 thin films were deposited at room temperature by IAD, a large-area process, which applies two ion beams to simultaneously effect film growth, oxidation and crystallization, yielding smooth, dense and coherent films on a wide variety of substrates[33,36,37]. One ion beam effects a pre- and *in situ* cleaning/activation process, enhancing interfacial adhesion, and achieving full film oxidation stoichiometry. Moreover, IAD allows fine tuning of oxide film properties via manipulation of O_2 partial pressure and ion beam power during growth. The room-temperature Hall mobilities of the IAD-derived In_2O_3 films (Fig. 2a) are substantial and nearly constant as carrier concentration is varied over the broad range of 10^{17}–10^{20} cm^{-3}. For useful semiconduction (low I_{off}), In_2O_3 thin films for TFT channels were deliberately grown here using conditions to suppress carrier concentrations. The Hall mobility in this case is immeasurable by conventional techniques because of the low carrier density. The conductivity of these films is $\sim 10^{-4}$–10^{-5} S cm^{-1}, and the carrier concentration is estimated to be $\sim 10^{13}$–10^{14} cm^{-3} from the field-effect mobility (vide infra). All as-grown In_2O_3 films are colourless and optically transparent, with films on glass exhibiting an average transmittance of $\sim$90% in the visible region (Fig. 2b). The direct IAD In_2O_3 optical bandgap was estimated from transmittance data by extrapolating the linear part of the $(\alpha h\upsilon)^2$ versus $h\upsilon$ plot to $\alpha = 0$ (Fig. 2c), yielding 3.65 eV. Taken together, the electrical and optical results suggest that such In_2O_3 thin films are an excellent n-channel material for transparent TFT fabrication.

X-ray diffraction (XRD) θ–2θ scans of the present hybrid In_2O_3 TFTs reveal the characteristic cubic bixbyite structure with substantial crystallinity/texture when grown on SiO_2 at 25 °C, and that films grown on n^+-Si/SAS exhibit even greater texture, judging from the widths of the dominant reflections (Fig. 3a,b). All other factors being equal, crystallinity should enhance μ_{FE}. Contact-mode atomic force microscope (AFM)

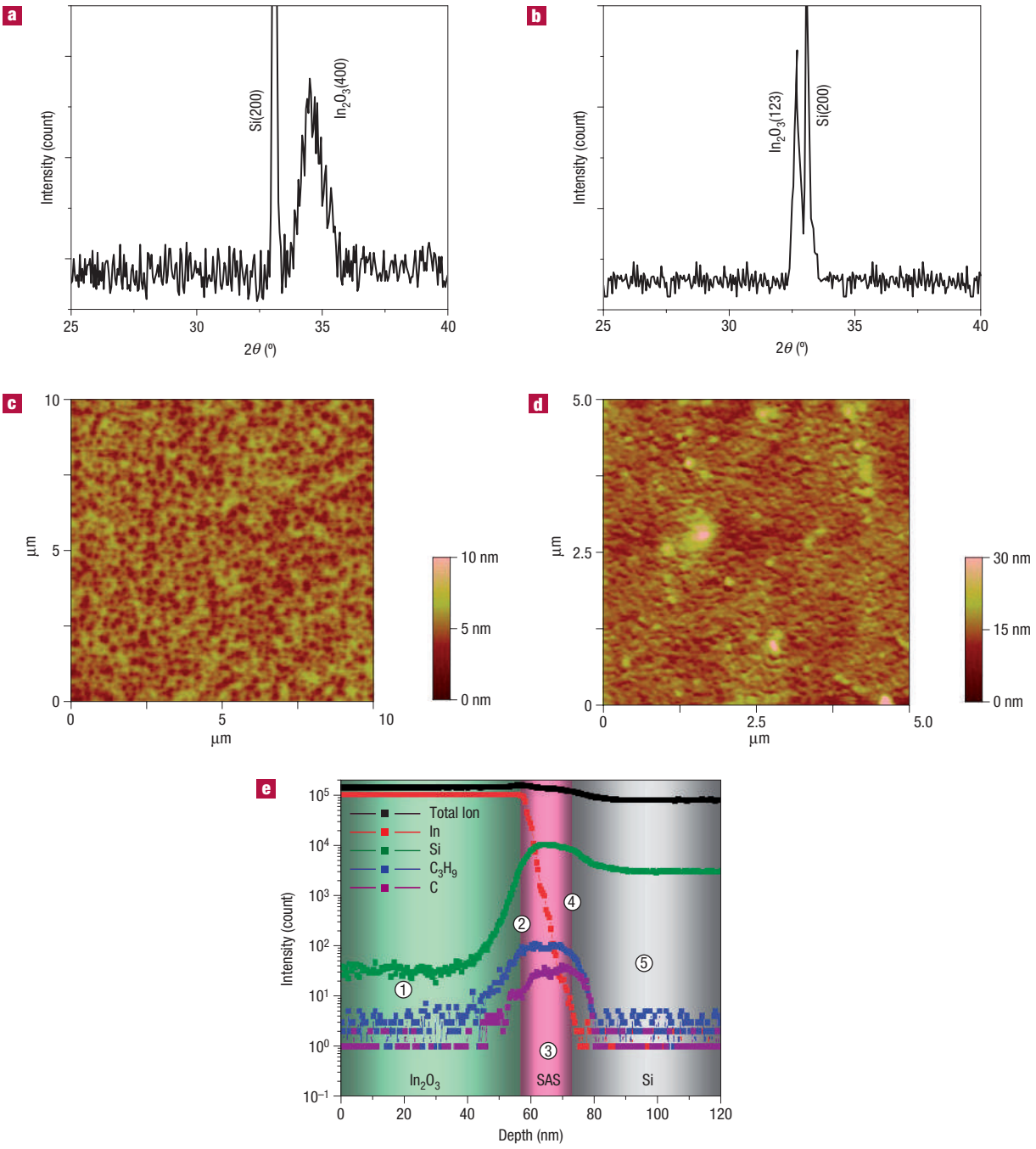

Figure 3 XRD, AFM and SIMS of IAD-derived In_2O_3 thin films in inorganic-only and inorganic–organic hybrid TFTs. a,**b**, XRD θ–2θ scans of IAD-derived In_2O_3 thin films in inorganic-only and inorganic–organic hybrid TFTs: p^+-Si/SiO_2/In_2O_3 structure (**a**); n^+-Si/SAS/In_2O_3 structure (**b**). **c**,**d**, AFM images of IAD-derived In_2O_3 thin films in inorganic-only and inorganic–organic hybrid TFTs: p^+-Si/SiO_2/In_2O_3 structure (**c**); n^+-Si/SAS/In_2O_3 structure (**d**). **e**, SIMS depth profile analysis of an n^+-Si/SAS/In_2O_3 structure. The numbers 1–5 correspond to regions analysed in the sample; full SIMS spectra of each of these regions are given in Fig. S3 of the Supplementary Information.

images show the In_2O_3 thin films grown on the dielectrics to be compact, dense, uniform and smooth, with small r.m.s. roughnesses of 0.7–0.8 nm on Si/SiO_2, 1.6–1.8 nm on Si/SAS, 2.7–3.1 nm on Si/CPB and 1.9–2.1 nm on glass/ITO/SAS (Fig. 3c,d, Supplementary Information, Fig. S2). The small roughnesses are attributed to: (1) the smooth underlying inorganic and organic dielectrics, supported by the AFM data; (2) the intrinsic efficacy of IAD in depositing smooth films[33,37].

The organic gate dielectrics were self-assembled or spin-coated by solution-phase techniques, leading to smooth, conformal, pin-hole-free, thermally stable films, having excellent cohesion and insulating characteristics (Fig. 1b, Supplementary Information, Fig. S1)[34,35]. Dielectric parameters are summarized in Table 1. Note that careful control of the IAD growth processes ensures that the organic dielectric materials survive the ion/plasma exposure during In_2O_3 deposition[33].

Table 1 Materials and device parameters for TFTs fabricated from In_2O_3 thin films + SiO_2 or nanoscopic organic SAS*/CPB† dielectrics on Si and glass/ITO gates using Au or In_2O_3 drain and source electrodes.

Gate	In_2O_3 thickness (nm)	Dielectric/thickness (nm)/C_i (nF cm^{-2})	D & S electrodes	μ_{FE} (cm^2 V^{-1}s^{-1})	μ_{GB}‡ (cm^2 V^{-1}s^{-1})	I_{on}/I_{off}	V_T (V)	N_t§ (cm^{-2})	S (V per decade)
p^+-Si	120	SiO_2/300/10	Au	10	24	10^5	23	1.73×10^{12}	5.6
n^+-Si	60	SAS*/16.5/180	Au	140	178	10^5	0.33	2.33×10^{11}	0.15
n^+-Si	60	CPB†/20/250	Au	80	94	10^3	0	2.79×10^{11}	0.41
Glass/ITO	60	SAS*/16.5/180	Au	140	181	10^5	0.17	2.44×10^{11}	0.08
Glass/ITO	60	SAS*/16.5/180	In_2O_3	120	154	10^5	0.19	2.51×10^{11}	0.09

* SAS = Self-assembled superlattice dielectric.

† CPB = Poly-4-vinylphenol + 1,6-bis(trichlorosilyl)hexane dielectric.

‡ μ_{GB} = Grain–boundary mobility.

§ N_t = Trap density.

The multilayer structures and compositions of the present hybrid TFTs having n^+-Si/SAS/In_2O_3 structures were first characterized by secondary ion mass spectrometric (SIMS) depth profiling (Fig. 3e, Supplementary Information, Fig. S3). These results show that these devices have abrupt In_2O_3–dielectric interfaces, minimal interfacial cross-diffusion, and phase purity. Clean interfaces in principle minimize electron traps and hysteresis, and should thereby enhance μ_{FE}. Generally, weak adhesion between inorganic and organic interfaces is a significant factor degrading organic field-effect transistor performance and stability[2,38]. For the present devices, the conventional 'Scotch tape' adhesion test[39–41] reveals no detectable change in multilayer thickness, optical microscopic images or optical transparency before and after the test, indicating that IAD-grown In_2O_3 films on the organic dielectrics exhibit strong interfacial adhesion.

In_2O_3-based TFTs were first characterized on p^+-Si substrates having a conventional SiO_2 dielectric, next on n^+-Si substrates with the SAS and CPB dielectrics (Fig. 4, Supplementary Information, Fig. S4), and then on glass/indium tin oxide (ITO) substrates with the SAS dielectric (Figs 4e,f, 5). TFT device response parameters are summarized in Table 1. The In_2O_3 devices using SiO_2 gate dielectrics show reasonable field-effect responses ($\mu_{FE} = 10$ cm^2 V^{-1}s^{-1}; $I_{on}/I_{off} = 10^5$) with operating voltages in the 100 V range (Fig. 4a,b, Table 1). In contrast, inorganic–organic hybrid TFTs fabricated on n^+-Si/SAS substrates exhibit excellent I–V characteristics (Fig. 4c,d, Table 1) with classical/crisp pinch-off linear curves and saturation lines at very low operating voltages. Low operating voltages (~1 V) are essential for mobile electronics powered by simple household batteries. Analysis of the n^+-Si/SAS/In_2O_3 device electrical response reveals large saturation-regime field-effect mobilities of ~140 cm^2 V^{-1}s^{-1}, encouraging for high-speed applications. Such mobilities are ~10× greater than previously reported for metal oxide TFTs fabricated at room temperature[3,29], and are attributed to the following: (1) substantial crystallinity of the IAD-derived In_2O_3 semiconductor, verified by the XRD results and grain-boundary trapping model analysis (vide infra), and the resulting suppressed neutral impurity scattering[42,43], (2) very small values of the interfacial trap density ($N_t \sim 10^{11}$ cm^{-2}, Table 1), (3) minimal ionized-impurity scattering (the carrier concentration is ~10^{13}–10^{14} cm^{-3}) (refs 42,44), (4) strong adhesion and smooth, abrupt semiconductor/dielectric interfaces to minimize electron traps and (5) advantageous characteristics of the high-capacitance organic nanoscopic dielectrics[34,35]. The threshold voltage V_T of the present devices is close to 0.0 V, with nearly hysteresis-free response and minimal trapped charge. That electrons are generated by a positive gate bias V_G, verifies that In_2O_3 shows n-channel behaviour. Furthermore, I_{on}/I_{off} ratios of ~10^5 are achieved, and the maximum drain–source current reaches the mA level, sufficient for most portable circuit applications. Small sub-threshold gate voltage swings of 150 mV per decade (Table 1) are achieved at the maximum slope for devices fabricated with the SAS dielectric (Fig. 4d). To correct for the differences in the different dielectric layers (for example capacitance, thickness and applied bias), the TFT transfer current characteristics are plotted versus accumulated charge carrier density (Fig. 4g). It can be seen that the n^+-Si/SAS/In_2O_3/Au hybrid devices switch on at much lower accumulated charge carrier densities than the inorganic-only p^+-Si/SiO_2/In_2O_3/Au devices, revealing that electron mobilities and charge-injection efficiency between the In_2O_3 channel and drain/source electrodes are markedly greater in the hybrid TFT case.

To further investigate the generality and applicability of the present inorganic–organic hybrid TFT strategy, In_2O_3 TFTs were next fabricated on n^+-Si/(20 nm CPB dielectric) with Au source and drain electrodes (see Supplementary Information, Fig. S4, Table 1). These n^+-Si/CPB/In_2O_3 devices also have good field-effect electrical response with field-effect mobilities of ~80 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} ratios of 10^3, and low $V_T \sim 0.0$ V. Next, using the same fabrication techniques, hybrid TFTs were grown at room temperature on glass/IAD-ITO/SAS gate structures with Au drain/source electrodes (Fig. 4e,f, Table 1). These TFTs also have excellent field-effect I–V characteristics with large field-effect mobilities of 140 cm^2 V^{-1} s^{-1}, high I_{on}/I_{off} ratio of 10^5, near 1.0 V operation with non-hysteretic characteristics, and small gate voltage swings of only 80 mV per decade. Finally, using high-conductivity IAD-derived In_2O_3 as drain and source electrodes affords completely transparent TFTs (Fig. 5), having field-effect mobilities of 120 cm^2 V^{-1} s^{-1}, large on/off ratios of 10^5, ~1.0 V operation, essentially hysteresis-free characteristics and very small sub-threshold gate voltage swings of 90 mV per decade. Note that such small gate voltage swings (benefiting from both the high-quality In_2O_3 semiconductor and the high-capacitance organic nanoscopic dielectric) are only slightly larger than the theoretical limit for Si-based TFTs (~60 mV per decade) (refs 22,45). Estimation of the grain-boundary mobilities μ_{GB}, using a grain-boundary trapping model[46], provides important information on intrinsic carrier transport characteristics within a single semiconductor grain (Table 1). It can be seen that μ_{GB} trends are in good agreement with the crystallinity results provided by XRD (Fig. 3a,b) and that the values of μ_{GB} are slightly larger than values of μ_{FE}, suggesting that grain-boundary scattering/trapping in these In_2O_3 films may limit μ_{FE}. That these hybrid TFTs on glass substrates are colourless and highly transparent is shown by transmission optical spectra and a photographic image (Fig. 5c,d), where the transmittance of an entire 70-device TFT array (glass/ITO/SAS/In_2O_3/In_2O_3 drain and

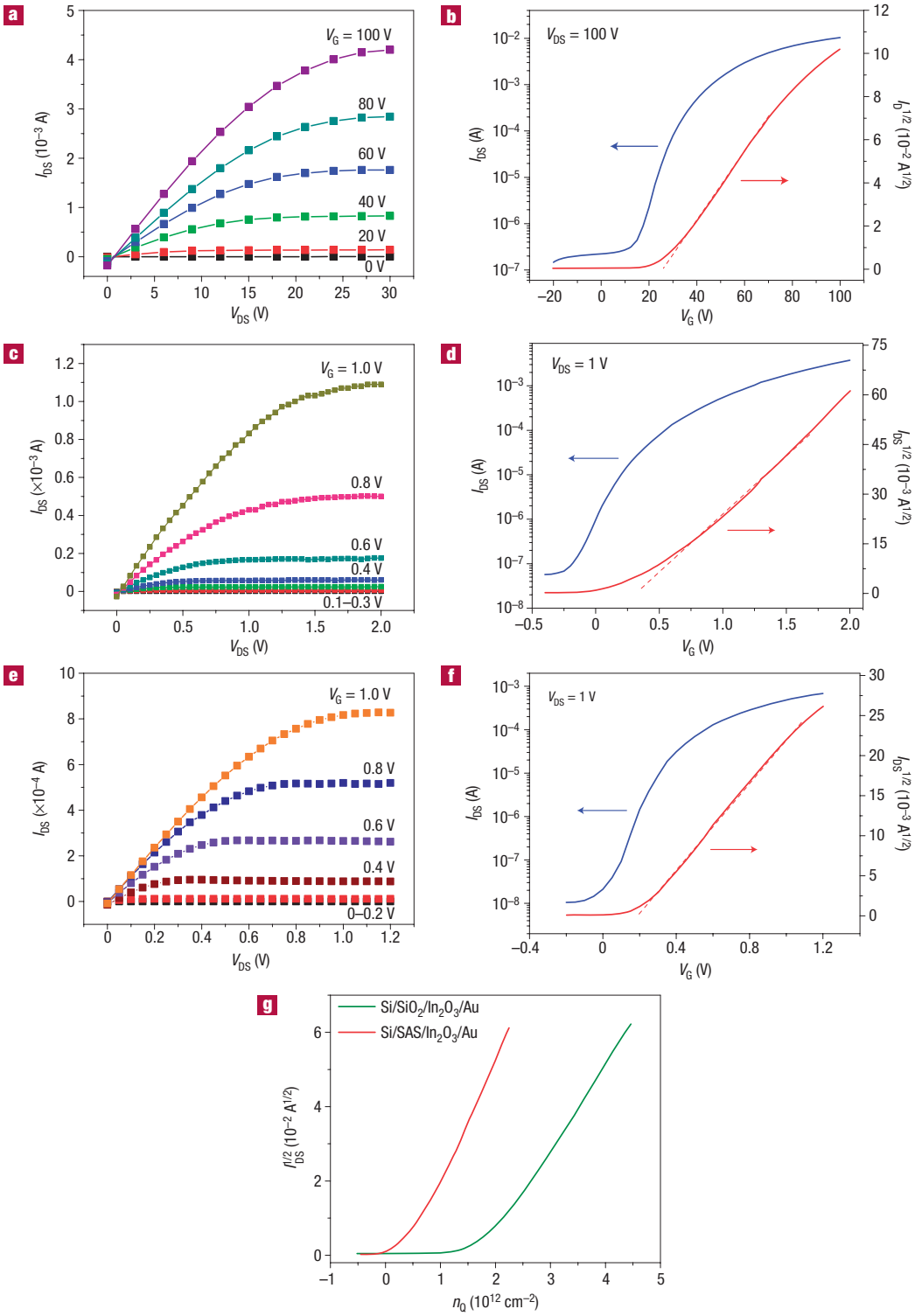

Figure 4 Field-effect device characteristics of inorganic-only TFTs on p$^+$-Si substrates and inorganic–organic hybrid TFTs on n$^+$-Si substrates and Corning 1737F glass substrates. a,**b**, Field-effect device characteristics of inorganic-only TFTs on p$^+$-Si substrates: current–voltage output characteristics as a function of gate voltage (**a**); TFT transfer characteristics of current versus gate voltage (**b**) (thin-film In_2O_3 as the semiconductor (100 μm (L) × 5 mm (W)) and 300 nm SiO_2 as the gate dielectric, with Au drain/source electrodes). **c**,**d**, Field-effect device characteristics of inorganic–organic hybrid TFTs on n$^+$-Si substrates: current–voltage output characteristics as a function of gate voltage (**c**); TFT transfer characteristics of current versus gate voltage (**d**) (thin-film In_2O_3 as the semiconductor (100 μm (L) × 5 mm (W)) and a 16.5 nm SAS dielectric with Au drain/source electrodes). **e**,**f**, Field-effect device characteristics of inorganic–organic hybrid TFTs on Corning 1737F glass substrates: current–voltage output characteristics as a function of gate voltage (**e**) ; TFT transfer characteristics of current versus gate voltage (**f**) (thin-film In_2O_3 as the semiconductor (100 μm (L) × 5 mm (W)) and a 16.5 nm SAS dielectric with Au drain/source electrodes). **g**, Comparison of TFT transfer current as a function of accumulated charge-carrier density: p$^+$-Si/SiO_2/In_2O_3/Au (green) and n$^+$-Si/SAS/In_2O_3/Au (red). Note that inspection of the plots reveals possible contact resistance effects, indicating that performance might be enhanced by contact optimization.

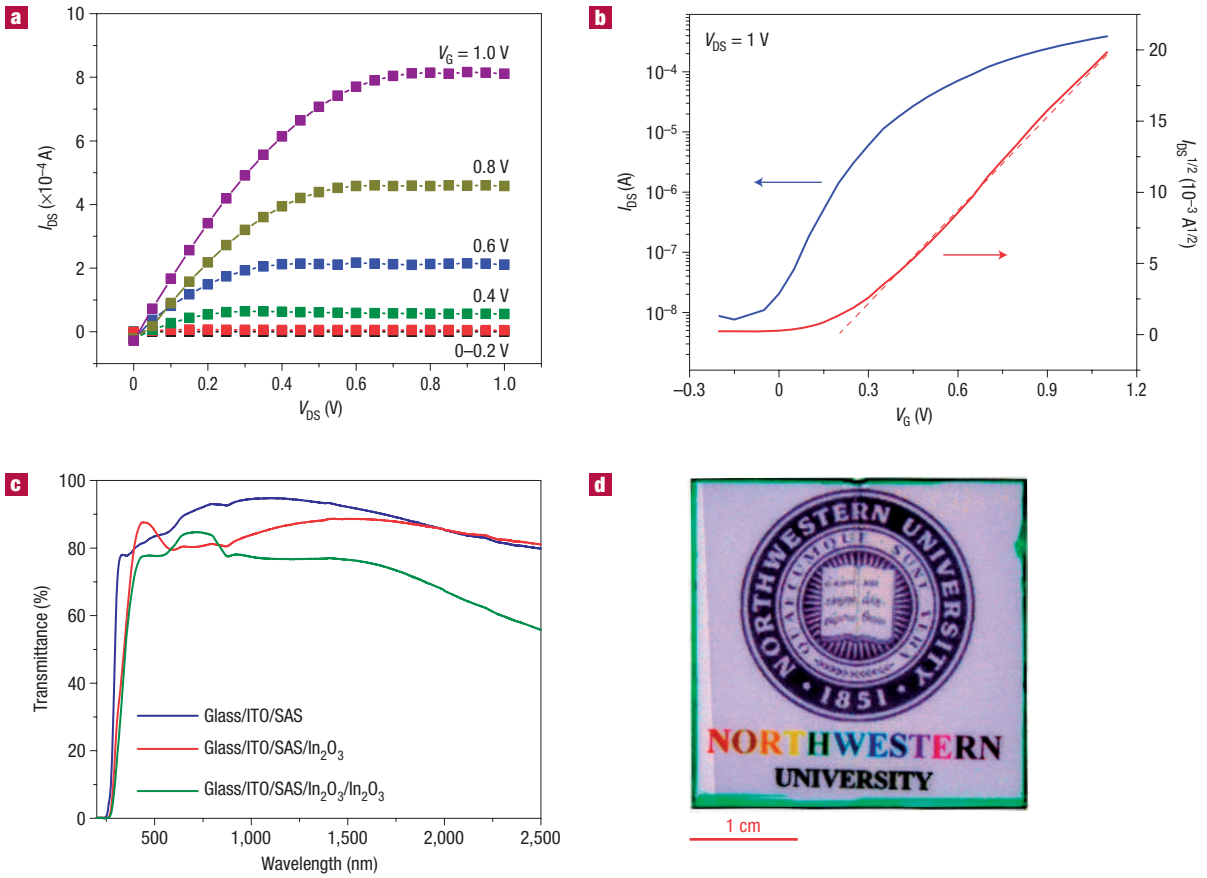

Figure 5 Typical field-effect device characteristics of fully transparent inorganic–organic hybrid TFTs on Corning 1737F glass substrates. a, Current–voltage output characteristics as a function of gate voltage. **b**, TFT transfer characteristics of current versus gate voltage (thin-film In_2O_3 as the semiconductor (100 μm (*L*) × 5 mm (*W*)) and a 16.5 nm SAS gate dielectric on glass/ITO substrates with high-conductivity In_2O_3 drain/source electrodes). **c**, Transmission optical spectrum of an array of 70 transparent inorganic–organic hybrid TFTs (glass/ITO/SAS/In_2O_3/In_2O_3 drain and source electrodes) taken through the In_2O_3 drain/source region; transmission optical spectra of glass/ITO/SAS and glass/ITO/SAS/In_2O_3 structures are also shown for comparison. **d**, Photo of a 70-device array of fully transparent inorganic–organic hybrid In_2O_3 TFTs: Northwestern University logo under TFTs fabricated on 0.7-mm-thick Corning 1737F glass. The edges of the glass substrate are marked in green for clarity.

source electrodes) is >80% in the visible region, and a colourful pattern beneath the aforementioned TFT array can easily be seen. These results demonstrate that hybrid integration of the oxide semiconductor In_2O_3 and nanoscopic organic dielectrics realizes room-temperature fabricated transparent TFTs with performance unobtainable via conventional approaches. In principle, this hybrid TFT strategy should be applicable to other In_2O_3-based TFT structures (bottom source–drain contacts, top gate and so on), as well as to other wide-bandgap metal oxide semiconductors and to other transparent ultrathin organic dielectrics. Furthermore, these hybrid devices are compatible with large-scale/large-area deposition techniques and simple dielectric growth processes, and are transparent—a promising approach to high-performance, transparent electronics.

METHODS

TFT FABRICATION

In_2O_3 thin films were deposited on p^+-Si/SiO_2 (Process Specialties; thermally grown SiO_2 are 300 nm thick), n^+-Si/SAS (n^+-Si from Process Specialties) and IAD-derived glass/ITO (Corning 1737F glass substrates from Precision Glass & Optics; the ITO gate was deposited by IAD at room temperature; sheet resistance = 60 Ω/□) as the back gate. The nanoscopic organic gate dielectrics (SAS, three 5.5 nm layers of type III; CPB, 20 nm prepared from poly-4-vinylphenol + 1,6-bis(trichlorosilyl)hexane) were grown via layer-by-layer self-assembly or spin-coating described elsewhere (Figs 1b, Supplementary Information, Fig. S1)[34,35]. Poly-4-vinylphenol and 1,6-bis(trichlorosilyl)hexane were purchased from Aldrich and Gelest, respectively. In_2O_3films were grown with a Veeco horizontal dual-gun IAD system at room temperature. The In_2O_3 target (99.99%) was purchased from Plasmaterials. During the semiconducting In_2O_3 deposition process, the growth system pressure and O_2 partial pressure were optimized at 4.0×10^{-4}–4.4×10^{-4} torr and 2.2×10^{-4}–2.6×10^{-4} torr, respectively. The growth rate of the In_2O_3 thin films was 3.3 ± 0.2 nm min^{-1}. During the In_2O_3 drain- and source-electrode deposition, the growth-system pressure and O_2 partial pressure were at 2.7×10^{-4} torr and 0.4×10^{-4} torr, respectively. The conductivity of the In_2O_3 drain and source electrodes was measured to be 1,400 S cm^{-1} by a four-probe technique. The ITO films were deposited using the same IAD growth system at room temperature. The ITO target (In_2O_3/SnO_2 = 9 : 1) was purchased from Sputtering Materials, and the ITO growth-process details have been reported elsewhere[37]. A top-contact electrode architecture was used in TFT device fabrication. The 50 nm Au source and drain electrodes were deposited by thermal evaporation (pressure ~10^{-6} torr) through shadow masks, affording channel dimensions of 50/100 μm (*L*) × 5 mm (*W*). Alternatively, 150 nm In_2O_3 source and drain electrodes were deposited by IAD through the same shadow masks for completely transparent TFTs. The top-contact Si/SiO_2/In_2O_3/Au, Si/SAS/In_2O_3/Au and

glass/ITO/SAS/In_2O_3/(Au or In_2O_3) TFT device structures are shown in Fig. 1 and Supplementary Information, Fig. S4.

CHARACTERIZATION METHODOLOGY

In_2O_3 film thicknesses were verified using a Tencor P-10 step profilometer by etching a step following film growth. XRD θ–2θ scans of In_2O_3 were acquired with a Rigaku DMAX-A diffractometer using Ni-filtered Cu Kα radiation. Optical transmittance spectra were acquired with a Cary 500 ultraviolet–visible–near-infrared spectrophotometer and were referenced to the spectrum of uncoated Corning 1737F glass. Film surface morphologies were imaged on a Digital Instruments Nanoscope III AFM. Quantitative SIMS analysis was carried out on a MATS quadrupole SIMS instrument using a 15 keV Ga^+ ion source. Conductivities of the semiconducting In_2O_3 thin films were measured with a Keithley 2182A nanovoltmeter and 6221 current source. The electrical properties of highly conductive ITO and In_2O_3 films were characterized on a Bio-Rad HL5500 van der Pauw Hall-effect measurement system. TFT device characterization was carried out on a customized probe station in air with a Keithley 6430 subfemtometer and a Keithley 2400 source meter, operated by a locally written Labview program and GPIB communication. The parameters u_{GB} and N_t (Table 1) were computed by plotting $\ln(I_{DS}/V_G)$ at a given drain–source voltage using the grain-boundary trapping model and the following equation[46]:

$$I_{DS} = \frac{W\mu_{GB}V_D C_i V_G}{L}\exp\left(\frac{-q^3 N_t t}{8\varepsilon kTC_i V_G}\right),$$

where W and L are the channel width and length, respectively, μ_{GB} is the grain-boundary mobility, V_D is the applied bias between the drain and source electrodes, C_i is the dielectric capacitance, V_G is the gate bias, q is the electron charge, N_t is the interfacial trap density between the semiconductor and dielectric, t is the channel thickness, ε is the In_2O_3 permittivity, k is the Boltzmann constant and T is the absolute temperature at room temperature.

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Competing financial interests

The authors declare that they have no competing financial interests.