High Performance Tri-gate GaN Power MOSHEMTs on Silicon Substrate

Jun Ma and Elison Matioli

***Abstract*—We demonstrate high-performance GaN power metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) on silicon substrate based on a nanowire tri-gate architecture. The common issue of partial removal of carriers by nanowire etching in GaN tri-gate transistors was resolved mainly by optimized tri-gate geometry including filling factor and trench width. The tri-gate reduced the OFF-state leakage current (I_{OFF}) and the subthreshold slope (*SS*), increased the on/off ratio, and improved the breakdown voltage (V_{BR}) of the device. With a gate-to-drain separation (L_{GD}) of 5 μm, the tri-gate MOSHEMTs exhibited V_{BR} of 792 V at I_{OFF} of 0.3 μA/mm, along with a small specific on-resistance ($R_{ON,SP}$) of 0.91 ± 0.08 mΩ·cm^2. With L_{GD} of 15 μm, hard V_{BR} of 1755 V at I_{OFF} of 45 μA/mm with high soft V_{BR} of 1370 V at I_{OFF} = 1 μA/mm was achieved, rendering excellent high-power figure of merits (FOMs) up to 1.25 GW/cm^2. These results unveil the significant potential of nanostructured GaN transistors for future power applications.**

***Index Terms*—GaN, HEMT, tri-gate, breakdown.**

I. Introduction

Nanowire tri-gate architectures have recently attracted large attention for GaN HEMTs. Compared with conventional planar gates, the tri-gate offers additional electrostatic control from sidewall gates, which reduces I_{OFF} and *SS* [1],[2]. Furthermore, the larger surface area of the tri-gate enhances heat dissipation of the device [3],[4]. Considering the superior Baliga FOM of GaN, tri-gate GaN HEMTs are very promising for future efficient power conversion. However, an important drawback of this approach is the degraded on-resistance (R_{ON}) and drain current (I_D) due to the partial removal of the two-dimensional electron gas (2DEG) when etching nanowires in the tri-gate region. Such degradation is detrimental for power devices, and has not been resolved up to now in the few reports on tri-gate GaN HEMTs [1]-[6]. More importantly, the full potential of tri-gates for power applications has not yet been understood nor demonstrated.

In this work we present high voltage GaN tri-gate power MOSHEMTs on silicon presenting smaller *SS* of 93 ± 7 mV/dec and I_{OFF} of 0.28 ± 0.12 nA/mm, and a larger on/off ratio beyond 10^9, compared to planar devices. The issue of partial removal of the 2DEG in the tri-gate region was mainly resolved by optimizing the tri-gate geometry. With L_{GD} of 5 μm, the tri-gate MOSHEMTs exhibited V_{BR} of 792 V at I_{OFF} of 0.3 μA/mm, with low $R_{ON,SP}$ of 0.91 ± 0.08 mΩ·cm^2. With L_{GD} of 15 μm, hard V_{BR} of 1755 V at I_{OFF} of 45 μA/mm with high soft V_{BR} of 1370 V at I_{OFF} = 1 μA/mm was achieved.

This work was supported in part by the European Research Council (ERC) under the European Union's H2020 programme/ERC Grant Agreement 679425 and in part by the Swiss National Science Foundation under Assistant Professor (AP) Energy Grant PYAPP2_166901. The authors are with the Power and Wide-band-gap Electronics Research Laboratory (POWERlab), École polytechnique fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland (e-mail: jun.ma@epfl.ch; elison.matioli@epfl.ch).

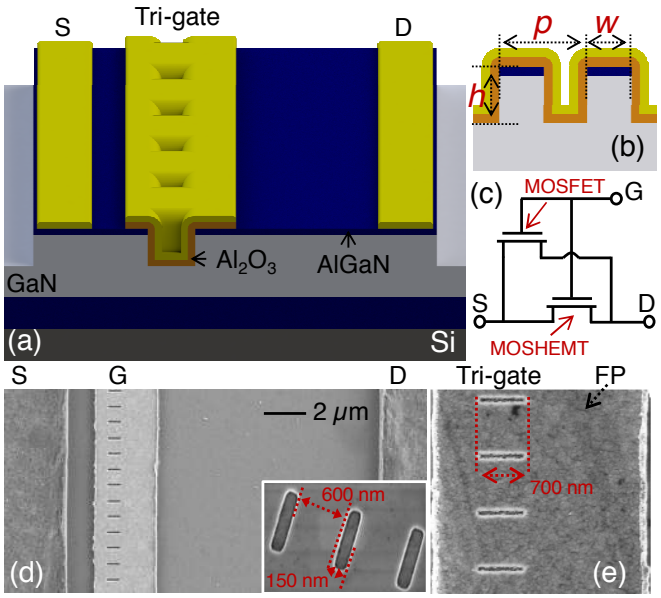

Fig. 1. (a) Schematic of the fabricated tri-gate MOSHEMTs. (b) Cross-sectional schematic of the tri-gate region. (c) Equivalent circuit of the tri-gate MOSHEMTs. (d)-(e) Top-view SEM images of the tri-gate MOSHEMTs. The inset shows SEM image of nanowires without dielectric and gate metal.

II. Device Structure

The AlGaN/GaN epitaxy in this work consisted of 3.75 µm of buffer, 0.3 µm of un-doped GaN (u-GaN) channel, 23.5 nm of AlGaN barrier and 2 nm of u-GaN cap layers. The schematics, an equivalent circuit and scanning electron microscopy (SEM) images of the tri-gate MOSHEMTs are shown in Fig. 1. The device fabrication started with e-beam lithography to define the mesa and nanowires, which were then etched by Cl_2-based inductively coupled plasma and followed by ohmic metal deposition and rapid thermal annealing. The height (*h*) of the nanowires was about 166 nm. The nanowire width (*w*) was 600 nm and period (*p*) was 750 nm, corresponding to a filling factor (*FF* = *w*/*p*) of ~0.8. Then 20 nm of Al_2O_3 was deposited by atomic layer deposition as the gate dielectric. Finally the gate was formed using Ni/Au, which was later used as the mask for removal of the Al_2O_3 in access/ohmic regions. AlGaN/GaN MOSHEMTs with similar dimensions but planar gates fabricated on the same chip were taken as reference, for which the Al_2O_3 was also removed in

their access regions. Device characteristics such as R_{ON}, I_D, I_{OFF} and transconductance (g_m) were normalized by device width (60 μm) in both planar and tri-gate devices, and their error bars were determined from measurements on up to 10 separate devices of the same kind.

III. Results and Discussion

As shown in Fig. 2(a), the planar (Planar) and tri-gate (Tri-gate) MOSHEMTs presented similar g_m of 66.1 ± 2 and 68.5 ± 3 mS/mm, respectively, and similar I_D at V_G = 5 V but different threshold voltages (V_{th}). The reduced V_{th} is mainly due to strain relaxation of the AlGaN/GaN nanowires [7]-[9] in addition to sidewall gate modulation, on which a physics-based model and detailed analysis will be reported elsewhere. I_{OFF} was reduced from 1.4 ± 0.7 to 0.28 ± 0.12 nA/mm and *SS* was improved from 98 ± 14 to 93 ± 7 mV/dec due to the better gate control of the tri-gate. The Planar and Tri-gate showed similar maximum I_D of 565 ± 24.5 and 535 ± 23.4 mA/mm at V_G = 5 V (Fig. 2(b)), which is a small difference considering the error bars. Furthermore, considering the difference of 1.5 V in V_{th}, the Tri-gate actually exhibited the same I_D as the Planar at the same gate driving voltage (V_G - V_{TH}). R_{ON} of the Planar and Tri-gate was 9.08 ± 0.16 and 9.01 ± 0.07 Ω·mm, respectively, extracted from I_D-V_D sweeps in linear region.

The similar on-state performances presented by the Tri-gate compared to the Planar suggests that the degradation due to the partial removal of 2DEG by nanowire etching was resolved, which is mainly due to the optimized tri-gate geometry. Figure 3 compares I_D-V_D characteristics of tri-gate MOSHEMTs with different *FFs*, which reveals an increase in I_D and reduction in R_{ON} with larger *FF*. This is firstly attributed to the wider effective channel with increased *FF* due to the larger total width of unetched areas, as shown in the insets of Fig. 3. Secondly, the smaller width of each trench (etched area of the tri-gate structure) with increasing *FF* reduced the spreading resistance in the tri-gate region [10]-[12]. Furthermore, the small length of the tri-gate relative to the source-to-drain distance is also important. The estimated increase in resistance between the source and drain due to the etching of the tri-gate length of 700 nm with *FF* of 80% is only 1.25%, which is within the measurement error bars and supports the observation of similar on-resistances (Fig. 4) (this estimation considers only the degradation in resistance due to etching of the trenches, and neglects other effects such as spreading resistance and strain relaxation). In addition to the geometry, two other factors compensate the effect of 2DEG etching in the recessed regions: reduced self heating [4],[13] and additional conduction channels at the trenches, which functions as a MOSFET (accumulation mode) in parallel with the tri-gate transistor (Fig. 1(c)) [3].

Three-terminal breakdown voltages of the MOSHEMTs were measured with floating substrate (Fig. 4), where two types of breakdown are discussed: hard (when device breaks) and soft (when I_{OFF} reaches 1 μA/mm) breakdowns. As shown in Fig. 4(a), the hard V_{BR} of the Tri-gate with L_{GD} of 5, 10 and 15 μm were 792, 1100 and 1755 V at I_{OFF} of 0.3, 0.3 and 45 μA/mm, respectively. Compared with the Planar, the tri-gate presented

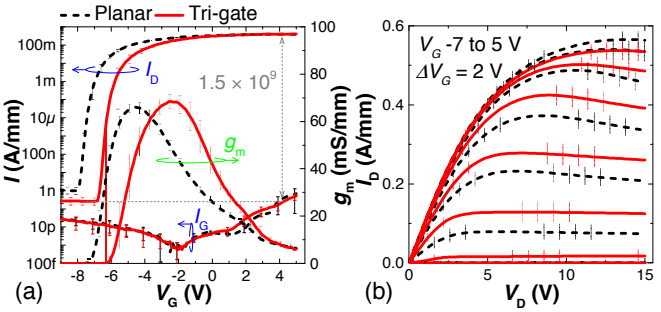

Fig. 2. (a) Transfer (at V_D = 5 V) and (b) output characteristics of the MOSHEMTs normalized by device width of 60 μm. The L_{GS}, L_G and L_{GD} were 1.5, 2.5 and 10 μm, respectively, and the *FF* for the Tri-gate was 0.8.

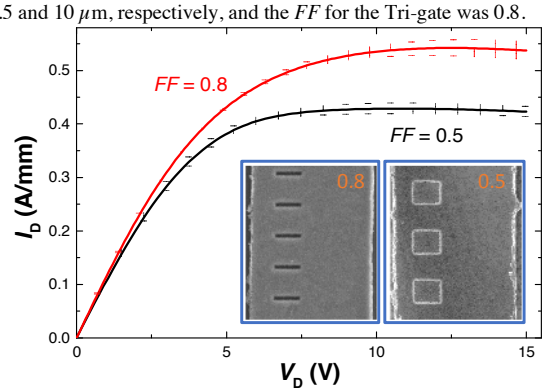

Fig. 3. Output characteristics at V_G = 5 V of tri-gate MOSHEMTs with the same *w* of 600 nm but different *FFs*. The insets show top-view SEM images of tri-gate MOSHEMTs with *FF* of 0.5 and 0.8. The L_{GS}, L_G and L_{GD} were 1.5, 2.5 and 10 μm, respectively.

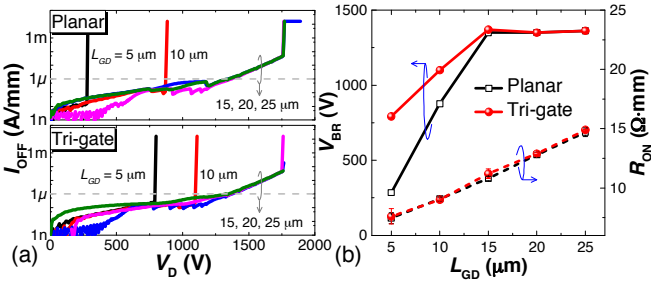

Fig. 4. (a) OFF-state breakdown characteristics of the planar and tri-gate (FF = 0.8) MOSHEMTs with different L_{GD}, measured with floating substrate. (b) Extracted L_{GD}-dependent R_{ON} and V_{BR} of the MOSHEMTs. The breakdown was defined at $I_{OFF} \leq 1$ μA/mm.

larger V_{BR} when L_{GD} < 10 μm, which is mainly due to the increased effective L_{GD} and the integrated plate (FP) in the Tri-gate (Fig. 1(e)). The effective gate control (or pinch off of channel by V_G) in the Tri-gate happens mainly within the nanowires. This shifts the gate edge from the drain-side edge of the gate metal to the drain-side edge of the nanowires, which increases the effective L_{GD} by 1.3 μm. The critical field strength, extracted from the V_{BR}-L_{GD} curve of the Planar, was about 107 V/μm, thus the increase in effective L_{GD} led to an increase of 140 V in V_{BR}. In addition, the planar portion of the MOS structure close to the drain side of the gate functioned as a gate-connected FP due to its more negative pinch-off voltage as compared to the tri-gate region (Fig. 2(a)). With increasing V_D, the heterostructure under the FP is depleted, reducing the electric field in the tri-gate region and leading to the enhanced V_{BR} [14]-[16]. Although other factors in the Tri-gate may also improve the V_{BR} due to 3-D geometry of the tri-gate, we consider these effects to be minor, since tri-gate transistors

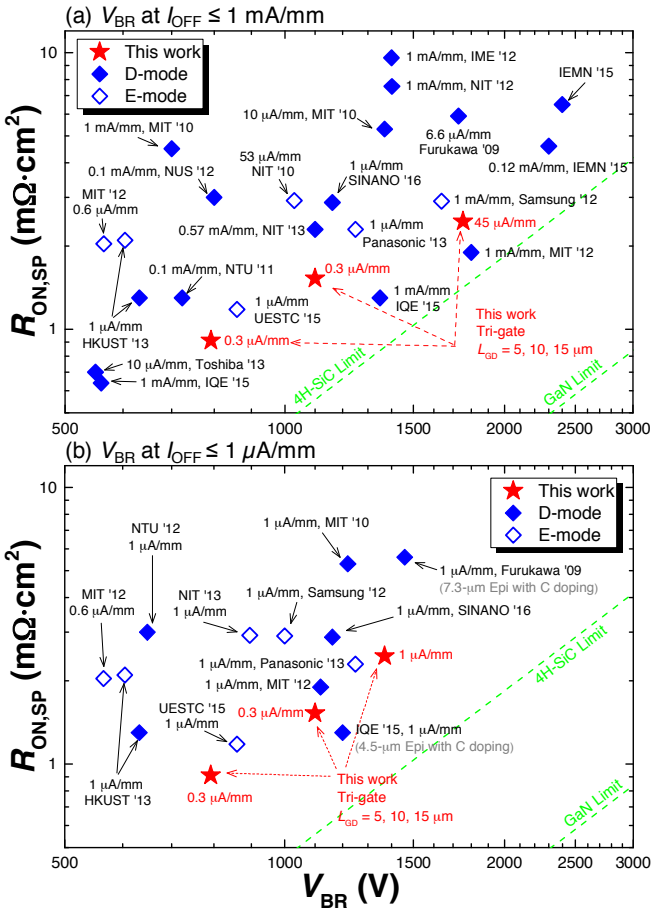

Fig. 5. $R_{ON,SP}$ versus V_{BR} benchmarks of the tri-gate MOSHEMTs with state-of-the-art GaN E/D-mode (MOS)HEMTs on silicon by defining V_{BR} at I_{OFF} (a) ≤ 1 mA/mm and (b) ≤ 1 μA/mm. For fair comparison, literature results with unspecified R_{ON} or I_R were not included.

without the integrated FP in the literature exhibited similar V_{BR} to their counterpart planar transistors (Ref. [17] and [18]). For L_{GD} ≥ 15 μm, hard V_{BR} of all devices saturated at ~1760 V, indicating that V_{BR} was limited by the buffer and silicon substrate, in agreement with Refs. [19]-[21]. Figure 4(b) shows the R_{ON} and soft V_{BR} of the devices versus L_{GD}. The Planar and Tri-gate exhibited similar R_{ON}, which were linearly dependent on L_{GD}. For L_{GD} ≤ 10 μm, there was no difference between soft and hard breakdown since I_{OFF} was always below 1 μA/mm. With L_{GD} ≥ 15 μm, the soft V_{BR} also saturated, which was limited again by the buffer layers.

The Tri-gate was benchmarked against state-of-the-art GaN (MOS)HEMTs on silicon using two commonly-used definitions of V_{BR} (I_{OFF} ≤ 1 mA/mm and ≤ 1 μA/mm). For calculation of the specific R_{ON} ($R_{ON,SP}$), 1.5 μm of transfer length for each ohmic contact was taken into account. Benchmark for V_{BR} at I_{OFF} ≤ 1 mA/mm is shown in Fig. 5(a). The Tri-gate with L_{GD} of 5, 10 and 15 μm exhibited high power FOM of 688, 791 and 1252 MW/cm², respectively, indicating their excellent performance as power transistors. However, 1 mA/mm is a large leakage level to determine V_{BR} for power devices, as devices with V_{BR} > 1000 V would present prohibitively large off-state dissipated power over 1 W/mm. 1 μA/mm is now becoming more common in the literature as it represents a fairer comparison of voltage blocking performance of power devices. Figure 5(b) presents the benchmark with V_{BR} at I_{OFF} ≤ 1 μA/mm. The V_{BR} for all reference devices was re-calculated based on the reported data following the definition of V_{BR} at I_{OFF} of 1 μA/mm. The 5-μm- L_{GD} Tri-gate exhibited high V_{BR} of 792 V at small I_{OFF} of 0.3 μA/mm, along with small $R_{ON,SP}$ of 0.91 ± 0.08 mΩ·cm², which is, to the best of our knowledge, the smallest $R_{ON,SP}$ among GaN (MOS)HEMTs on silicon with V_{BR} > 700 V. The 15-μm- L_{GD} Tri-gate presented high V_{BR} of 1370 V at 1 μA/mm, very close to the best value obtained by 7.3 μm of carbon-doped buffer layers [22], despite its much thinner buffer of 3.75 μm. These results indicate the outstanding potential of GaN tri-gate power MOSHEMTs.

IV. Conclusion

In this work we demonstrated high performance GaN nanowire tri-gate MOSHEMTs on silicon. The tri-gate reduced the *SS* and I_{OFF} with an enhanced on/off ratio. The issue on partial removal of the 2DEG by nanowire etching was overcome by optimized tri-gate geometries. The tri-gate also improved the V_{BR} of the devices, resulting in excellent high power FOMs among the state-of-the-art results of GaN (MOS)HEMTs on silicon, demonstrating the enormous potential of nanostructured GaN transistors for the future power conversion.

Acknowledgment

The authors would like to thank the staff in CMi and ICMP cleanrooms at EPFL for technical support.

References

[1] K. Ohi, J. T. Asubar, K. Nishiguchi, and T. Hashizume, "Current stability in Multi-mesa-channel AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, pp. 2997-3004, Oct. 2013. doi: 10.1109/TED.2013.2266663.

[2] B. Lu, E. Matioli, and T. Palacios, "Tri-gate normally-off GaN power MISFET," *IEEE Electron Device Lett.*, vol. 33, pp. 360-362, Mar. 2012. doi: 10.1109/LED.2011.2179971.

[3] J. Ma, G. Santoruvo, P. Tandon, and E. Matioli, "Enhanced electrical performance and heat dissipation in AlGaN/GaN Schottky barrier diodes using hybrid tri-anode structure," *IEEE Trans. Electron Devices*, vol. 63, pp. 3614-3619, Sept. 2016. doi: 10.1109/TED.2016.2587801.

[4] J. T. Asubar, Z. Yatabe, and T. Hashizume, "Reduced thermal resistance in AlGaN/GaN multi-mesa-channel high electron mobility transistors," *Appl. Phys. Lett.*, vol. 105, pp. 053510, Aug. 2014. doi: 10.1063/1.4892538.

[5] K. Ohi and T. Hashizume, "Drain current and controllability of threshold voltage and subthreshold current in a multi-measa-channel AlGaN/GaN high electron mobility trnasistor," *Jpn. J. Appl. Phys.*, vol. 48, pp. 081002, Aug. 2009. doi: 10.1143/JJAP.48.081002.

[6] T. Tamura, J. Kotani, S. Kasai, and T. Hashizume, "Nearly temperature-independent saturation drain current in a multi-mesa-channel AlGaN/GaN high electron mobility transistor," *Appl. Phys. Express*, vol. 1, pp. 023001, Feb. 2008. doi: 10.1143/APEX.1.023001.

[7] M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN nanoribbons," *Appl. Phys. Lett.*, vol. 98, pp. 042103, Jan. 2011. doi: 10.1063/1.3544048.

[8] O. Landré, D. Camacho, C. Bougerol, Y. M. Niquet, V. Favre-Nicolin, G. Renaud, H. Renevier, and B. Daudin, "Elastic strain relaxation in GaN/AlN nanowire superlattice," *Phys. Rev. B*, vol. 81, pp. 153306, Apr. 2010. doi: 10.1103/PhysRevB.81.153306.

[9] S. Liu, Y. Cai, G. Gu, J. Wang, C. Zeng, W. Shi, Z. Feng, H. Qin, Z. Cheng, K. J. Cheng and B. Zhang, "Enhancement-mode operation of nanochannel array (NCA) AlGaN/GaN HEMTs," *IEEE Electron Device Lett.* vol. 33, pp. 354-356, Jan. 2012. doi: 10.1109/LED.2011.2179003.

[10] J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H. -S. P. Wong, "Extension and source/drain design for high-performance FinFet Devices," *IEEE Trans. Electron Devices*, vol. 50, pp. 952-958, Apr. 2003. doi: 10.1109/TED.2003.811412.

[11] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. D. Meyer, "Analysis of the parasitic S/D resistance in multiple-gate FETs," *IEEE Trans. Electron Devices*, vol. 52, pp. 1132-1140, Jun. 2005. doi: 10.1109/TED.2005.848098.

[12] G. Baccarani, and G. A. Sai-Halasz, "Spreading resistance in submicro MOSFETs," *IEEE Electron Device Lett*. vol. 4, pp. 27-29, Feb. 1983. doi: 10.1109/EDL.1983.25635.

[13] J. Ma and E. Matioli, "Improved electrical and thermal performances in nanostructured GaN devices," *2016 International Conference on IC Design and Technology (ICICDT)*, Ho Chi Minh City, 2016, pp. 1-4. doi: 10.1109/ICICDT.2016.7542061.

[14] R. Coffie, "Slant field plate model for field effect transistors," *IEEE Trans. Electron Devices*, vol. 61, pp. 2867-2872, Aug. 2014. doi: 10.1109/TED.2014.2329475.

[15] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Lett*., vol. 27, pp. 713-715, Sept. 2006. doi: 10.1109/LED.2006.881020.

[16] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally-off GaN-on-Si field-effect transistors with low dynamic on-resistance," *IEEE Electron Device Lett*. vol. 32, pp. 632-634, May 2011. doi: 10.1109/LED.2011.2118190.

[17] J. H. Seo, Y. -W. Jo, Y. J. Yoon, D. -H. Son, C. -H. Won, H. S. Jang, I. M. Kang, and J. -H. Lee, "Al(In)N/GaN Fin-type HEMT with very-low leakage current and enhanced I-V characteristic for switching applications," *IEEE Electron Device Lett*., vol. 37, pp. 855-858, Jul. 2016. doi: 10.1109/LED.2016.2575040.

[18] X. Tan, X. Y. Zhou, H. -Y. Guo, G. -D. Gu, Y. -G. Wang, X. -B. Song, J. -Y. Yin, Y. -J. Lv, and Z. -H. Feng, "Excellent-performance AlGaN/GaN Fin-MOSHEMTs with self-alighed Al_2O_3 gate dielectric," *Chin. Phys. Lett*., vol. 33, pp. 098501, Apr. 2016. doi: 10.1088/0256-307X/33/9/098501.

[19] B. Lu and T. Palacios, "High breakdown (> 1500 V) AlGaN/GaN HEMTs by substrate-transfer technology," *IEEE Electron Device Lett*. vol. 31, pp. 951-953, Sept. 2010. doi: 10.1109/LED.2010.2052587.

[20] Y. -W. Lian, Y. -S. Lin, H. -C. Lu, Y. -C. Huang, and S. S. H. Hsu, "AlGaN/GaN HEMTs on Silicon with hybrid Schottky-ohmic drain for high breakdown voltage and low leakage current," *IEEE Electron Device Lett*., vol. 33, pp. 973-975, Jul. 2012. doi: 10.1109/LED.2012.2197171.

[21] S. L. Selvaraj. A. Watanabe, A. Wakejima, and T. Egawa, "1.4-kV breakdown voltage for AlGaN/GaN high-electron-mobility transistor on silicon substrate," *IEEE Electron Device Lett*., vol. 33, pp. 1375-1377, Oct. 2012. doi: 10.1109/LED.2012.2207367.

[22] N. Ikeda, S. Kaya, J. Li, T. Kokawa, M. Masuda, and S. Katoh, "High-power AlGaN/GaN MIS-HFETs with field plates on Si substrates", *2009 21st International Symposium on Power Semiconductor Devices & IC's*, Barcelona, 2009, pp. 251-254. doi: 10.1109/ISPSD.2009.5158049.